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(54) **Buffer and organic light emitting display and a data driving circuit using the buffer**

Puffer und organische lichtemittierende Anzeige sowie Datentreiberschaltung mit dem Puffer

Mémoire tampon, affichage électroluminescent organique et circuit de commandes de données utilisant la mémoire tampon

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Description

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a buffer and organic light emitting display and a data driving circuit using the buffer, particularly to a buffer and organic light emitting display and a data driving circuit using the buffer that are able to provide an accurate output voltage regardless of the threshold voltage of a transistor.

2. Discussion of Related Technology

[0002] Various flat -panel displays have been developed so as to have less weight and bulk than that of a CRT (Cathode Ray Tube). Flat-panel displays include liquid crystal displays, electric field emission displays, plasma display panels, and organic light emitting displays, as well as others. An organic light emitting display presents an image using organic light emitting diodes that emit light from the recombination of electrons and holes. The organic light emitting display creates a data signal using input data from an outside source and displays an image having a desired brightness by supplying the generated data signal to pixels using at least a data driving circuit and data lines.

[0003] The data driving circuit converts the input data into a voltage corresponding to a gray scale value and supplies the converted voltage to data lines as a data signal via a buffer. Each respective pixel receives an electrical current corresponding to the voltage from the driving circuit. As a result, the organic light emitting diode within each pixel emits light according to the current it receives and a predetermined image is displayed.

[0004] In the above mentioned data driving circuit, the buffer should supply the data signal to a pixel without a voltage drop between its input and output. However, conventional buffers supply a data signal with a voltage drop corresponding to a threshold voltage of a transistor. Because of this, the voltage of the data signal is dropped by as much as a transistor threshold voltage and the result is that pixels are not able to display the image with a desired brightness.

[0005] US 6,498,596 discloses a buffer for driving a data line in a display device. The buffer comprises three stages consisting of an inverter and a feedback switch connecting the inverter's input and output nodes. The stages are coupled to each other via capacitors and a feedback loop is formed by means of two additional switches.

SUMMARY OF CERTAIN INVENTIVE EMBODIMENTS

[0006] Accordingly, an aspect of certain embodiments is to provide a buffer which does not produce an output with a transistor threshold drop.

According to one aspect of the invention a buffer is disclosed, the buffer comprising a first capacitor including first and second capacitor terminals, the first capacitor being configured to receive an analog voltage on the first capacitor terminal, where the analog voltage is an input to the buffer; a first inverter having a first input terminal and a first output terminal, the first input terminal being connected to the second capacitor terminal of the first capacitor; a second capacitor having a third capacitor terminal connected to the first output terminal of the first inverter, and a fourth capacitor terminal; a second inverter having a second input terminal and a second output terminal, the second input terminal being connected to the fourth capacitor terminal of the second capacitor; a third capacitor having a fifth capacitor terminal connected to the second output terminal of the second inverter, and a sixth capacitor terminal; a first transistor connected to the sixth capacitor terminal of the third capacitor, the first transistor being configured to control a flow of a current from a first power source to a data line such that a buffer voltage is supplied to the data line, where the first transistor is configured to control the current in response to a voltage supplied from the third capacitor; a second transistor connected to the first capacitor terminal of the first capacitor, the second transistor being configured to supply the analog voltage to the first capacitor terminal of the first capacitor when a first control signal is supplied to the second transistor; a third transistor connected to the data line and to the first terminal of the first capacitor; a fourth transistor connected to the first power source and the sixth capacitor terminal of the third capacitor, the fourth transistor being configured to supply a voltage equal to the voltage of the first power source to the third capacitor when the first control signal is supplied to the fourth transistor; and a fifth transistor connected to the data line and to a second power source, the fifth transistor being configured to supply the data line with the voltage of the second power source when a second control signal is supplied to the fifth transistor.

Preferably the first transistor is configured to be turned off when the value of the buffer voltage is substantially equal to the value of the analog voltage input. Preferably the absolute value of the voltage supplied from the third capacitor to the first transistor is larger than the absolute value of the analog voltage input. Preferably the voltage of the first power source is higher than the voltage of the second power source. Preferably The buffer further comprises: a sixth transistor connected to the first output of the first inverter and to the first input of the first inverter, the sixth transistor configured to be turned on when the first control signal is supplied to the sixth transistor.; and a seventh transistor connected to the second output of the second inverter and to the second input of the second inverter, the seventh transistor configured to be turned on when the first control signal is supplied to the seventh transistor. Preferably the third transistor is configured to be turned on when a third control signal is supplied. Pref-

erably the buffer is configured to receive the start of the first control signal and the second control signal substantially simultaneously, and to receive the end of the first control signal earlier than the end of the second control signal. Preferably the buffer is configured to receive the start of the third control signal after the end of the first control signal and before the end of the second control signal, and to receive the end of the third control signal after the end of the second control signal. Preferably the buffer further comprises: an eighth transistor connected between the first inverter and the first power source; and a ninth transistor connected between the second inverter and the second power source. Preferably the eighth transistor and the ninth transistor are of different conductivity. Preferably the eighth transistor is configured to be turned on when a fourth control signal is supplied to the eighth transistor, and wherein the ninth transistor is configured to be turned on when a fifth control signal is supplied to the ninth transistor. Preferably the buffer is configured to receive the start of the fourth and fifth control signals before or substantially simultaneously with the second control signal and to receive the end of the fourth and fifth control signals after the start of the third control signal. Preferably the buffer is configured to receive fourth and fifth control signals each comprising at least one of a voltage substantially equal to the voltage of the first power source, a voltage substantially equal to the voltage of the second power source, and a voltage configured to provide a limited non-zero current to the first or second inverter. Preferably the buffer is configured to receive the fourth and fifth control signals continuously and to provide a first limited non-zero current to the first inverter and a second limited non-zero current to the second inverter in response to the fourth and fifth control signals.

According to another aspect of the invention a data driving circuit is disclosed, the data driving circuit comprising a digital to analog converter configured to generate an analog voltage in response to a bit value of a data input, and a plurality of buffers according to the first aspect of the invention, wherein each buffer is configured to supply the analog voltage to a data linePreferably the data driving circuit further comprises: a shift register configured to sequentially generate a sampling signal; and a latch section configured to store the data corresponding to the sampling signal and to supply the stored data to the digital to analog converter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] These and/or other aspects and advantages of certain embodiments will become apparent and more readily appreciated from the following description, taken in conjunction with the accompanying drawings of which:

[0008] FIG. 1 is a schematic diagram illustrating an organic light emitting display according to one embodiment;

[0009] FIG. 2 is a block diagram illustrating an embodiment of a data driving circuit depicted in FIG. 1;

[0010] FIG. 3 is a block diagram illustrating another embodiment of a data driving circuit depicted in FIG. 1;

[0011] FIG. 4 is a schematic circuit diagram of a structure of a buffer according to an embodiment;

[0012] FIG. 5 is a timing diagram showing control signals supplied to the buffer depicted in FIG. 4;

[0013] FIG. 6 is a timing diagram showing voltage values of certain nodes of the buffer depicted in FIG. 4;

[0014] FIG. 7 is a schematic circuit diagram of a structure of a buffer according to another embodiment;

[0015] FIG. 8 is a timing diagram showing control signals supplied to the buffer depicted in FIG. 7; and

[0016] FIGs. 9a through 9c are timing diagrams showing control signals supplied to the buffer depicted in FIG. 7.

[0017] The following Examples are given for the purpose of illustration and are not intended to limit the scope of this invention.

DETAILED DESCRIPTION OF CERTAIN EMBODIMENTS

[0018] Hereinafter, certain embodiments will be described with reference to the accompanying drawings. When one element is connected to another element, the one element may be not only directly connected to the other element but may also be indirectly connected to the other element via a third element. Further, some elements are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0019] FIG. 1 illustrates an organic light emitting display according to the present invention. Referring to FIG. 1, an organic light emitting display in accordance with one embodiment includes a pixel portion 130 which has pixels 140 formed in an array with a plurality of scan lines S1 through Sn and a plurality of data lines D1 through Dm, a scan driver 110 configured to drive the scan lines S1 through Sn, a data driver 120 configured to drive the plurality of data lines D1 through Dm and a timing controller 150 configured to control the scan driver 110 and the data driver 120.

[0020] The scan driver 110 generates a scan signal in response to a scan drive control signal SCS from the timing controller 150 and sequentially supplies the generated scan signal to the scan lines S1 through Sn. The scan driver 110 also generates a light emission control signal in response to the scan drive control signal SCS and sequentially supplies the generated light emission control signal to light emitting control lines E1 through En.

[0021] The data driver 120 generates data signals in response to a data drive control signal DCS from the timing controller 150 and supplies the generated data signals to the data lines D1 through Dm. The data driver 200 has at least a first data driving circuit 129. The data driving circuit 129 converts input data into a data signal to be driven onto the data lines D1 through Dm. A detailed structure of the data driving circuit 129 will be explained below.

[0022] The timing controller 150 generates the data drive control signal DCS and the scan drive control signal SCS. The data drive control signal DCS is supplied to the data driver 120 and the scan drive control signal SCS is supplied to the scan driver 110. The timing controller 150 also supplies input data to the data driver 120.

[0023] The pixel portion 130 receives a first power source ELVDD and a second power source ELVSS. The first power source ELVDD and the second power source ELVSS are supplied to respective pixels 140. The pixels 140 receiving the first power source ELVDD and the second power source ELVSS display an image corresponding to the data signal supplied from the data driving circuit 129.

[0024] FIG. 2 illustrates a block diagram according to an example embodiment of a data driving circuit depicted in FIG. 1. The data driving circuit in this example includes j (j is a positive integer) data lines and J channels that are able to be connected. Referring to FIG. 2, the data driving circuit 129 comprises a shift register 121 for sequentially generating a sampling signal, a sampling latch section 122 for sequentially storing data in response to the sampling signal, a holding latch section 123 for storing data from the sampling latch section 122 and for supplying the stored data to a digital-analog converter 125 (referred to as a "DAC" hereafter), a DAC 125 for generating an analog voltage corresponding to the data and a buffer unit 126 for supplying the analog voltage to the data lines D.

[0025] The shift register 121 receives a source shift clock SSC and a source start pulse SSP from the timing controller 150. After receiving the source start pulse SSP, the shift register 121 generates j sampling signals, one at each period of the source shift clock SSC.

[0026] The sampling latch section 122 sequentially stores the data in response to a sampling signal. The sampling latch section 122 has j sampling latches so as to store the data, where each latch has bit-width corresponding to the number of bits in the data. For example, each latches is configured with a size of k bits in the case that the data has k bits.

[0027] The holding latch section 123 receives the data from the sampling latch section 122 when a source output enable signal SOE is received from the timing controller 150. After receiving the data, the holding latch section 123 supplies the data stored to DAC 125 when a next source output enable signal SOE is received from the timing controller 150. The holding latch section 123 includes j of holding latches each having a size of k bits.

[0028] The DAC 125 generates an analog voltage corresponding to a bit value of the data and supplies the generated voltage to a buffer unit 126.

[0029] The buffer unit 126 includes buffers 127 which buffer data signals from the DAC 125 and drive them to j data lines D1 through Dj. For advantageous system performance, the buffers 127 output data signals which are substantially not voltage-dropped to the data lines D1 through Dj regardless of the threshold voltage of the transistors included in the buffers 127.

[0030] The voltage level of the data before the level shifter 124 is low to reduce power in this digital portion of the circuit. In some embodiments the DAC 125 may be better driven with higher digital voltage levels. As shown in FIG. 3, the data driving circuit 129 may further comprises a level shifter 124 located between the holding latch section 123 and the DAC 125 to increase the voltage level of the data supplied from the holding latch section 123 to the DAC 125.

[0031] FIG. 4 illustrates a detailed schematic circuit diagram of a buffer according to an example embodiment. The buffer 127 comprises a first inverter 127a, a second inverter 127b, a first transistor M1 connected between the data line Dj and a third power source VVdd, a second transistor M2 and a first capacitor C1 connected between the DAC 125 and the first inverter 127a, a second capacitor C2 connected between the first inverter 127a and the second inverter 127b and a third capacitor C3 connected between the second inverter 127b and the first transistor M1.

[0032] The buffer 127 also comprises a transistor M3 connected between the data line Dj and a first node N1 which is a common terminal of the second transistor M2 and the first capacitor C1, a fourth transistor M4 connected between the third power source VVdd and a sixth node N6 which is a common terminal of the third capacitor C3 and the first transistor M1, a fifth transistor M5 connected between the fourth power source VVss and a seventh node N7 which is a common terminal of the first transistor M1 and the data line Dj, a sixth transistor M6 connected between an input terminal N2 and an output terminal N3 of the first inverter 127a and a seventh transistor connected between an input terminal N4 and an output terminal N5 of the second inverter 127b.

[0033] The first transistor M1 controls a current which flows into the seventh node N7 from the third power source VVdd in response to a voltage value supplied to a sixth node N6. The analog voltage at node N7 responds according to the current, and is supplied to a pixel 140 as a data signal. The second transistor M2 supplies an analog voltage from the DAC 125 to the first node N1 when a first control signal CS1 is supplied. The third transistor M3 is on when a third control signal CS3 is supplied, and the seventh node N7 and the first node N1 are electrically connected. This closes the feedback loop by which N7 is controlled. The fourth transistor M4 supplies a voltage of the third power source Wdd to the sixth node N6 when a first control signal CS1 is supplied, thereby turning off transistor M1. . The fifth transistor M5 supplies a voltage of the fourth power source VVss to the seventh node N7 (and therefore to data line Dj) when a second control signal CS2 is supplied. The first inverter 127a includes an eighth transistor M8 and a ninth transistor M9 which are connected between the third power source VVdd and the fourth power source VVss. From here, the eighth transistor M8 is adjusted by a P-MOS and the ninth transistor M9 is adjusted by an N-MOS.

[0034] The gate terminals of the eighth transistor M8 and the ninth transistor M9 and one terminal of the first capacitor C1 are each connected to the second node N2 which is driven in response to a voltage driven on the first node N1. The sixth transistor M6 electrically connects the second node N2 with the third node N3 when the first control signal CS1 is supplied. The second inverter 127b includes a tenth transistor M10 and an eleventh transistor M11 which are connected between the third power source VVdd and the fourth power source VVss. From here, the tenth transistor M10 is adjusted by a P-MOS and the eleventh transistor M11 is adjusted by an N-MOS.

[0035] The gate terminals of the tenth transistor M10 and the eleventh transistor M11 and one terminal of the second capacitor C2 are connected to the fourth node N4, and are driven in response to a voltage driven on the third node N3. The seventh transistor M7 electrically connects the fourth node N4 with the fifth node N5 when the first control signal CS1 is supplied.

[0036] FIG. 5 is a timing diagram showing the DAC signal Vga, and the control signals CS1, CS2, and CS3 for the buffer of FIG. 4 during drive periods T1, T2, T3, and T4. As shown, the first control signal CS1 and the second control signal CS2 are supplied during drive period T1. Accordingly, during drive period T1, the second transistor M2, the sixth transistor M6, the seventh transistor M7, the fourth transistor M4 and the fifth transistor M5 are each on. With transistor M6 on, the first inverter 127a will provide a voltage to the second node N2 and the third node N3. The voltage provided will be of a level between the level of the voltage of the fourth power source VVss and the level of the voltage of third power source VVdd. Likewise, with transistor M7 on, the second inverter 127b will similarly provide a voltage to the fourth node N4 and the fifth node N5, where the voltage provided will have a level between the level of the voltage on the fourth power source Wss and the level of the voltage on the third power source VVdd. With the second transistor M2 on, an analog voltage Vga is supplied from the DAC 125 to the first node N1. Accordingly, a voltage that corresponds to the difference between the analog voltage Vga and the voltage at the second node N2 is stored across the first capacitor C1.

[0037] Furthermore, because the voltage supplied to the second node N2 is always the same, the voltage stored across the first capacitor C1 is based on the analog voltage Vga. With the fourth transistor M4 on, the voltage of the third power source VVdd is supplied to the sixth node N6, and the first transistor M1 is off. Also, the difference between the voltage on the fifth node N5 and the voltage on the sixth node N6, is stored across the third capacitor C3.

[0038] Next, the first control signal CS1 is discontinued during the second drive period T2. Accordingly, the second transistor M2, the sixth transistor M6, the seventh transistor M7 and the fourth transistor M4 are off during the second drive period T2. Note that at the end of the second drive period T2, the voltages at the first through fifth nodes N1-N5 are such that the voltage at the sixth node N6 is the same as the third source voltage VVdd. Accordingly, at the end of the second drive period T2, the first transistor M1, is off.

[0039] During the third drive period T3, the third control signal CS3 is supplied. Accordingly, the third transistor M3 is on during the third drive period T3, and the seventh node N7 is electrically connected to the first node N1. As the seventh node N7 is driven to the fourth voltage source VVss by the fifth transistor M5, the first node N1 will be driven from the second drive period value of Vga to VVss during the third drive period T3. The value of the voltage at the second node N2 is likewise reduced because of the first capacitor C1 when the voltage of the first node N1 is reduced to VVss. Because the amount of voltage drop at the first node N1 is based on the analog voltage Vga, the voltage drop at the second node N2 will likewise be based on the analog voltage Vga.

[0040] As the second node N2 is the input of the first inverter 127a, when the voltage at the second node N2 is reduced, the output of the first inverter 127a, at the third node N3, will be increased. Because of the second capacitor C2, the voltage at the fourth node N4 will increase according to the increase at the third node N3. As the fourth node N4 is the input of the second inverter 127b, when the voltage at the fourth node N4 is increased, the output of the second inverter 127b, at the fifth node N5, will be reduced. As the sixth node N6 is capacitively coupled to the fifth node N5, when the fifth node N5 is reduced, the sixth node N6 will similarly be reduced.

[0041] Because the sixth node N6 is the gate voltage of the first transistor M1, when the voltage at the sixth node is reduced, the first node turns on and begins to conduct current to the seventh node N7. However, because the fifth transistor M5 is still on, the voltage at node N7 does not substantially change. Note that at the end of the third drive period T3, the voltages at the first through fifth nodes N1-N5 are such that the voltage at the sixth node N6 is lower than the third source voltage VVdd. Accordingly, at the end of the third drive period T3, the first transistor M1, is on.

[0042] Next, during the fourth driving period T4, the control signal CS2 is discontinued and the fifth transistor M5 turns off. The voltage at the seventh node N7 rises according to the current supplied from the first transistor M1. Because the voltage at the seventh node is fed back to the first and second inverters 127a and 127b through the third transistor M3 and the first capacitor C1, the voltage at the sixth node N6 at the input of the first transistor M1 is affected by the rising voltage at the seventh node N7. The voltage at the sixth node is affected in such a way that an increasing voltage at the seventh node N7 causes the voltage at the sixth node N6 to rise. The voltages at the seventh node N7 and at the sixth node N6 will continue to rise until the first transistor M1 turns off. This will occur when the voltage at the seventh node N7

has risen enough to bring the voltages at the first through sixth nodes N1-N6 back to the values these voltages had at the end of the second drive period T2. Recall that at the end of the second drive period T2, the voltage at the sixth node N6 was equal to the value of the power source VVdd, and the first transistor M1 was therefore off. This will again occur when the voltage at the seventh node N7, and therefore the voltage at the first node N1, has risen so as to be equal to the value of the voltage at the first node N1 at the end of the second driving period T2. Recall that the value of the voltage at the first node N1 at the end of the second driving period was the analog voltage Vga. Thus, during the fourth driving period, the buffer will drive the data line Dj with the analog voltage Vga without a transistor threshold voltage drop, and the associated pixel 140 will illuminate according to the accurate voltage.

[0043] FIG. 6 shows the transitions of the second, fourth, and sixth nodes N2, N4, and N6 during the second third and fourth driving periods. As described above, at the end of the second driving period, the voltage at the second node N2 has a value based on the first inverter 127a with its input and output shorted by the sixth transistor M6. Similarly, the voltage at the fourth node N4 has a value based on the second inverter 127b with its input and output shorted by the seventh transistor M7. The voltage at the sixth node N6 has a value equal to the power source Wdd because the sixth node N6 was shorted to the power source VVdd during the first drive period T1 by the fourth transistor M4.

[0044] During the third driving period T3, the voltages at the second, fourth, and sixth nodes N2, N4, and N6 transition according to the first set of transitions shown in FIG. 6. The voltage at the second node N2 is reduced by an amount V1, which is based on the analog voltage Vga. The voltage at the fourth node N4 increases based on the increase in the voltage at the third node N3, which is based on the reduction in the voltage at the second node N2 and the gain of the first inverter 127a. Note that the voltage at the fourth node N4 increases by more than the amount the voltage at the second node N2 reduces. This occurs because of the gain of the first inverter 127a. The voltage at the sixth node N6 decreases based on the decrease in the voltage at the fifth node N5, which is based on the increase in the voltage at the fourth node N4 and the gain of the second inverter 127b. Note that the voltage at the sixth node N6 decreases by more than the amount the voltage at the fourth node N4 increases. This occurs because of the gain of the second inverter 127b.

[0045] During the fourth period, as described above, the voltage at the seventh node N7 is fed back to the first node N1. The rising voltage at the seventh node N7 causes the voltage at the first node N1 to rise. Because of the coupling capacitor between the first and second nodes, the rising voltage at the first node N1 causes the voltage at the second node N2 to also rise. Because of the first inverter 127a, the rising voltage at the second node N2 causes the voltage at the third node N3 to reduce. Because of the coupling capacitor between the third and fourth nodes, the reduction in the voltage at the third node N3 causes the voltage at the fourth node N4 to also reduce. Because of the second inverter 127b, the reduction in the voltage at the fourth node N4 causes the voltage at the fifth node N5 to increase. Because of the coupling capacitor between the fourth and fifth nodes, the increasing voltage at the fifth node N5 causes the voltage at the sixth node N6 to increase. As described above, once the voltage at the sixth node N6 increases to VVdd, the first transistor will stop driving current to the seventh node N7, and accordingly the seventh node N7 will stop rising. As illustrated in FIG. 6, this occurs when the voltages at the second, fourth and sixth nodes each return to the value of the voltages these nodes had at the end of the second driving period.

[0046] Accordingly, an accurate analog voltage Vga from the DAC 125 can be supplied by the buffer 127 to the data line Dj regardless of the transistor threshold voltage. One advantageous aspect of the buffer is that in can be easily used in large displays with high resolution because of the accuracy of the output. Additionally, because of the gain of the two transistors, the voltage presented at the gate of the first transistor is an amplified version of the analog voltage Vga. This results in faster operation of the buffer. In some embodiments the gain may be realized with other circuitry configurations. On the other hand, in some embodiments the gain is not necessary, and the circuitry between the first node N1 and the fifth node N5 may be replaced with a wire or some other substantially unity gain circuit.

[0047] FIG. 7 illustrates a detailed schematic circuit diagram of a structure of a buffer according to another example embodiment. This embodiment differs from the embodiment shown in FIG. 4 by the addition of a twelfth transistor M12 connected with between the first inverter 127a and the third power source VVdd and the addition of a thirteenth transistor M13 connected between the second inverter 127b and the fourth power source VVss. The twelfth transistor M12 and the thirteenth transistor M13 are of different conductivity. That is, the twelfth transistor M12 is a PMOS transistor, and the thirteenth transistor M13, is an NMOS transistor. The first and second transistors operating with inputs and outputs between VVss and VVdd may consume excessive power. The twelfth and thirteenth transistors enable the first and second inverters only when the first and second inverters are used by the buffer to change the buffer output level, as described below.

The twelfth transistor M12 is turned-on when a fourth control signal CS4 is supplied. The result is that a voltage of the third voltage VVdd is supplied to the first inverter 127a, which is thereby enabled.

[0048] The thirteenth transistor M13 is turned-on when a fifth control signal CS5 is supplied. The result is that a voltage of the third voltage VVss is supplied to the second inverter 127b, which is thereby enabled.

[0049] Referring to FIGs. 7 and 8, the operation of the buffer will be explained. As shown in FIG. 8, prior to the first driving period T1, the first control signal CS1, the second control signal CS2, the third control signal CS3, the fourth control signal CS4 and the fifth control signal CS 5 are not active. Note that the first control signal CS1, the third control signal CS3, and the fourth control signal CS4 are active low as they are used to drive PMOS transistors, and, the second control signal CS2, and the fifth control signal CS5 are active high as they are used to drive NMOS transistors. From the first driving period T1 through the beginning fourth driving period T4, the fourth control signal CS4 and the fifth control signals CS5 are active. Therefore, the first inverter 127a and the second inverter 127b are each enabled from the first driving period T1 through the beginning fourth driving period T4. During these time periods the first through third control signals CS1-CS3 are driven in the same manner as the corresponding signals, which were discussed with reference to FIG. 4. Similarly, the operation of the buffer is the same as that which was discussed with reference to FIG. 4. Note, however, that during the fourth time period T4, once the voltage at the sixth node N6 is at VVdd, and the first transistor is off, the first and second inverters do not need to operate. The power they consume can be saved if they are disabled. Accordingly, after some time has passed in the fourth driving period T4, the fourth control signal CS4 is changed to a not active state, and the first inverter 127a is disabled. Similarly, the fifth control signal CS5 is changed to a not active state, and the second inverter 127b is disabled. Note that the circuit is configured to maintain the voltage at the sixth node N6 to be at least VVdd when the first and second inverters are disabled.

[0050] Other control signal driving schemes, such as those depicted in FIGs 9A through 9C, may also be used. FIG. 9A shows a timing diagram where the fourth and fifth control signals CS4 and CS5 enable the first and second inverters throughout the first through fourth driving periods. Similarly, FIG 9B shows a timing diagram where the fourth and fifth control signals CS4 and CS5 enable the first and second inverters throughout most of, but not all of the first through fourth driving periods.

[0051] FIG 9C shows another type of driving strategy. In this strategy, the fourth and fifth control signals CS4 and CS5 enable the first and second inverters continually. However, the voltages at the fourth and fifth control signals CS4 and CS5 are selected so as to allow a limited amount of current to flow to the inverters, rather than being substantially equal to one of the voltages of the third or fourth power sources. In this way, the inverters are always on and operational, but are operating with limited current so as to save power.

[0052] As described above, a buffer and organic light emitting display with data driving circuit using the same in accordance with an exemplary embodiment of the present invention are able to provide an accurate analog voltage regardless of a threshold voltage of a transistor. Because the buffer is able to provide an accurate gradation voltage regardless of a threshold voltage of a transistor, the buffer may advantageously drive a panel having a large area and a high resolution. Also, because an enable voltage is selectively supplied such that the inverters operate only when used to change the buffer output voltage, power consumption can be reduced.

Claims

1. A buffer (127) comprising:

a first capacitor (C1) comprising first (N1) and second capacitor (N2) terminals, the first capacitor being configured to receive an analogue voltage on the first capacitor terminal,
wherein the analogue voltage is an input to the buffer (127);
a first inverter (127a) having a first input terminal (N2) and a first output terminal (N3), the first input terminal being connected to the second capacitor terminal of the first capacitor (N2);
a second capacitor (C2) having a third capacitor terminal (N3) connected to the first output terminal of the first inverter, and a fourth capacitor terminal (N4);
a second inverter (127b) having a second input terminal (N4) and a second output terminal (N5), the second input terminal being connected to the fourth capacitor terminal of the second capacitor;
a third capacitor (C3) having a fifth capacitor terminal (N5) connected to the second output terminal of the second inverter, and a sixth capacitor terminal (N6);
a second transistor (M2) connected to the first capacitor terminal (N1) of the first capacitor, the second transistor being configured to supply the analogue voltage to the first capacitor terminal of the first capacitor when a first control signal (CS1) is supplied to the second transistor;
a third transistor (M3) connected to the data line (Dj) and to the first terminal (N1) of the first capacitor;

characterized in

a first transistor (M1) connected to the sixth capacitor terminal of the third capacitor (N6), the first transistor being configured to control a flow of a current from a first power source (VVdd) to a data line (Dj) such that a buffer voltage is supplied to the data line, wherein the first transistor is configured to control the current in response to a voltage supplied from the third capacitor;
a fourth transistor (M4) connected to the first power source (VVdd) and the sixth capacitor (N6) terminal of the third capacitor, the fourth transistor being con-

figured to supply a voltage equal to the voltage of the first power source to the third capacitor when the first control signal (CS1) is supplied to the fourth transistor; and
a fifth transistor (M5) connected to the data line (Dj) and to a second power source (VVss), the fifth transistor being configured to supply the data line with the voltage of the second power source when a second control signal (CS2) is supplied to the fifth transistor.

2. The buffer of claim 1, wherein the first transistor is configured to be turned off when the value of the buffer voltage is equal to the value of the analog voltage input.

3. The buffer of claim 1, wherein the absolute value of the voltage supplied from the third capacitor to the first transistor is larger than the absolute value of the analog voltage input.

4. The buffer of one of the preceding claims, wherein the voltage of the first power source is higher than the voltage of the second power source.

5. The buffer according to one of the preceding claims, further comprising:

a sixth transistor connected to the first output of the first inverter and to the first input of the first inverter, the sixth transistor configured to be turned on when the first control signal is supplied to the sixth transistor.; and
a seventh transistor connected to the second output of the second inverter and to the second input of the second inverter, the seventh transistor configured to be turned on when the first control signal is supplied to the seventh transistor.

6. The buffer of claim 5, wherein the third transistor is configured to be turned on when a third control signal is supplied.

7. The buffer of claim 6, wherein the buffer is configured to receive the start of the first control signal and the second control signal simultaneously , and to receive the end of the first control signal earlier than the end of the second control signal.

8. The buffer of claim 7, wherein the buffer is configured to receive the start of the third control signal after the end of the first control signal and before the end of the second control signal, and to receive the end of the third control signal after the end of the second control signal.

9. The buffer according to one of the claims 5 through 8, further comprising:

an eighth transistor connected between the first inverter and the first power source; and
a ninth transistor connected between the second inverter and the second power source.

10. The buffer of claim 9, wherein the eighth transistor and the ninth transistor are of different conductivity.

11. The buffer of claim 10, wherein the eighth transistor is configured to be turned on when a fourth control signal is supplied to the eighth transistor, and wherein the ninth transistor is configured to be turned on when a fifth control signal is supplied to the ninth transistor.

12. The buffer of claim 11, wherein the buffer is configured to receive the start of the fourth and fifth control signals before or simultaneously with the second control signal and to receive the end of the fourth and fifth control signals after the start of the third control signal.

13. The buffer of claim 11, wherein the buffer is configured to receive fourth and fifth control signals each comprising at least one of a voltage equal to the voltage of the first power source, a voltage equal to the voltage of the second power source, and a voltage configured to provide a limited non-zero current to the first or second inverter.

14. The buffer of claim 11, wherein the buffer is configured to receive the fourth and fifth control signals continuously and to provide a first limited non-zero current to the first inverter and a second limited non-zero current to the second inverter in response to the fourth and fifth control signals.

15. A data driving circuit comprising:

a digital to analog converter configured to generate an analog voltage in response to a bit value of a data input; and
a plurality of buffers according to one of the preceding claims, each buffer configured to supply the analog voltage to a data line.

16. The data driving circuit according to claim 15, further comprising:

a shift register configured to sequentially generate a sampling signal; and
a latch section configured to store the data corresponding to the sampling signal and to supply the stored data to the digital to analog converter.

Patentansprüche

1. Ein Puffer (127), umfassend:

einen ersten Kondensator (C1), umfassend erste (N1) und zweite (N2) Kondensatoranschlüsse, wobei der erste Kondensator zum Empfangen einer analogen Spannung an dem ersten Kondensatoranschluss konfiguriert ist,

wobei die analoge Spannung eine Eingabe an den Puffer (127) ist;
einen ersten Inverter (127a) mit einem ersten Eingangsanschluss (N2) und einem ersten Ausgangsanschluss (N3), wobei der erste Eingangsanschluss mit dem zweiten Kondensatoranschluss des ersten Kondensators (N2) verbunden ist;
einen zweiten Kondensator (C2) mit einem mit dem ersten Ausgangsanschluss des ersten Inverters verbundenen dritten Kondensatoranschluss (N3) sowie einem vierten Kondensatoranschluss (N4);
einen zweiten Inverter (127b) mit einem zweiten Eingangsanschluss (N4) und einem zweiten Ausgangsanschluss (N5), wobei der zweite Eingangsanschluss mit dem vierten Kondensatoranschluss des zweiten Kondensators verbunden ist;
einen dritten Kondensator (C3) mit einem mit dem zweiten Ausgangsanschluss des zweiten Inverters verbundenen fünften Kondensatoranschluss (N5) sowie einem sechsten Kondensatoranschluss (N6);
einen mit dem ersten Kondensatoranschluss (N1) des ersten Kondensators verbundenen zweiten Transistor (M2), der derart konfiguriert ist, dass er dem ersten Kondensatoranschluss des ersten Kondensators die analoge Spannung liefert, wenn dem zweiten Transistor ein erstes Steuersignal (CS1) geliefert wird;
einen mit der Datenleitung (Dj) und dem ersten Anschluss (N1) des ersten Kondensators verbundenen dritten Transistor (M3);
gekennzeichnet durch
einen mit dem sechsten Kondensatoranschluss des dritten Kondensators (N6) verbundenen ersten Transistor (M1), wobei der erste Transistor derart konfiguriert ist, dass er einen Fluss eines Stroms von einer ersten Stromquelle (VVdd) zu einer Datenleitung (Dj) derart steuert, dass der Datenleitung eine Pufferspannung geliefert wird, und der erste Transistor derart konfiguriert ist, dass er den Strom als Antwort auf eine von dem dritten Kondensator gelieferte Spannung steuert;
einen mit der ersten Stromquelle (VVdd) und dem sechsten Kondensatoranschluss (N6) des dritten Kondensators verbundenen vierten Transistor (M4), wobei der vierte Transistor derart konfiguriert ist, dass er dem dritten Kondensator eine Spannung gleich der Spannung der ersten Stromquelle liefert, wenn dem vierten Transistor das erste Steuersignal (CS1) geliefert wird; und
einen mit der Datenleitung (Dj) und einer zweiten Stromquelle (VVss) verbundenen fünften Transistor (M5), wobei der fünfte Transistor derart konfiguriert ist, dass er der Datenleitung die Spannung der zweiten Stromquelle liefert, wenn dem fünften Transistor ein zweites Steuersignal (CS2) geliefert wird.

2. Der Puffer nach Anspruch 1, wobei der erste Transistor derart konfiguriert ist, dass er abgeschaltet wird, wenn der Wert der Pufferspannung gleich dem Wert des analogen Spannungseingangs ist.

3. Der Puffer nach Anspruch 1, wobei der Absolutbetrag der von dem dritten Kondensator dem ersten Transistor gelieferten Spannung größer ist als der Absolutbetrag des analogen Spannungseingangs.

4. Der Puffer nach einem der vorangehenden Ansprüche, wobei die Spannung der ersten Stromquelle höher ist als die Spannung der zweiten Stromquelle.

5. Der Puffer gemäß einem der vorangehenden Ansprüche, ferner umfassend:

einen mit dem ersten Ausgang des ersten Inverters und dem ersten Eingang des ersten Inverters verbundenen sechsten Transistor, wobei der sechste Transistor derart konfiguriert ist, dass er angeschaltet wird, wenn dem sechsten Transistor das erste Steuersignal geliefert wird; und
einen mit dem zweiten Ausgang des zweiten Inverters und dem zweiten Eingang des zweiten Inverters verbundenen siebten Transistor, wobei der siebte Transistor derart konfiguriert ist, dass er angeschaltet wird, wenn dem siebten Transistor das erste Steuersignal geliefert wird.

6. Der Puffer nach Anspruch 5, wobei der dritte Transistor derart konfiguriert ist, dass er angeschaltet wird, wenn ein drittes Steuersignal geliefert wird.

7. Der Puffer nach Anspruch 6, wobei der Puffer derart konfiguriert ist, dass er den Beginn des ersten Steuersignals und des zweiten Steuersignals gleichzeitig empfängt und das Ende des ersten Steuersignals früher empfängt als das Ende des zweiten Steuersignals.

8. Der Puffer nach Anspruch 7, wobei der Puffer derart konfiguriert ist, dass er den Beginn des dritten Steuersignals nach dem Ende des ersten Steuersignals und vor dem Ende des zweiten Steuersignals empfängt und das Ende des dritten Steuersignals nach dem Ende des zweiten Steuersignals empfängt.

9. Der Puffer gemäß einem der Ansprüche 5 bis 8, fer-

ner umfassend:

einen zwischen dem ersten Inverter und der ersten Stromquelle angeschlossenen achten Transistor; und
einen zwischen dem zweiten Inverter und der zweiten Stromquelle angeschlossenen neunten Transistor.

10. Der Puffer nach Anspruch 9, wobei der achte Transistor und der neunte Transistor unterschiedliche Leitfähigkeit aufweisen.

11. Der Puffer nach Anspruch 10, wobei der achte Transistor derart konfiguriert ist, dass er angeschaltet wird, wenn dem achten Transistor ein viertes Steuersignal geliefert wird, und wobei der neunte Transistor derart konfiguriert ist, dass er angeschaltet wird, wenn dem neunten Transistor ein fünftes Steuersignal geliefert wird.

12. Der Puffer nach Anspruch 11, wobei der Puffer derart konfiguriert ist, dass er den Beginn der vierten und fünften Steuersignale vor oder gleichzeitig mit dem zweiten Steuersignal empfängt und das Ende der vierten und fünften Steuersignale nach dem Beginn des dritten Steuersignals empfängt.

13. Der Puffer nach Anspruch 11, wobei der Puffer derart konfiguriert ist, dass er vierte und fünfte Steuersignale empfängt, deren jedes mindestens eine aus einer Spannung gleich der Spannung der ersten Stromquelle, einer Spannung gleich der Spannung der zweiten Stromquelle und einer Spannung, die derart konfiguriert ist, dass sie dem ersten oder zweiten Inverter einen begrenzten, von null verschiedenen Strom liefert, umfasst.

14. Der Puffer nach Anspruch 11, wobei der Puffer derart konfiguriert ist, dass er die vierten und fünften Steuersignale kontinuierlich empfängt und als Antwort auf die vierten und fünften Steuersignale dem ersten Inverter einen ersten begrenzten, von null verschiedenen Strom und dem zweiten Inverter einen zweiten begrenzten, von null verschiedenen Strom liefert.

15. Eine Datentreiberschaltung, umfassend:

einen Digital-Analog-Wandler, der derart konfiguriert ist, dass er als Antwort auf einen Bitwert eines Dateneingangs eine analoge Spannung erzeugt; und
eine Vielzahl von Puffern gemäß einem der vorangehenden Ansprüche,

wobei jeder Puffer derart konfiguriert ist, dass er einer Datenleitung die analoge Spannung liefert.

16. Die Datentreiberschaltung gemäß Anspruch 15, ferner umfassend:

ein Schieberegister, das derart konfiguriert ist, dass es sequenziell ein Abtastsignal erzeugt; und
einen Signalspeicherabschnitt, der derart konfiguriert ist, dass er die dem Abtastsignal entsprechenden Daten speichert und die gespeicherten Daten dem Digital-Analog-Wandler liefert.

Revendications

1. Tampon (127) comprenant :

un premier condensateur (C1) comprenant des première (N1) et deuxième (N2) bornes de condensateur, le premier condensateur étant configuré pour recevoir une tension analogique sur la première borne de condensateur,

dans lequel la tension analogique est une entrée du tampon (127) ;
un premier inverseur (127a) ayant une première borne d'entrée (N2) et une première borne de sortie (N3), la première borne d'entrée étant connectée à la deuxième borne de condensateur (N2) du premier condensateur ;
un deuxième condensateur (C2) ayant une troisième borne de condensateur (N3) connectée à la première borne de sortie du premier inverseur, et une quatrième borne de condensateur (N4) ;
un deuxième inverseur (127b) ayant une deuxième borne d'entrée (N4) et une deuxième borne de sortie (N5), la deuxième borne d'entrée étant connectée à la quatrième borne de condensateur du deuxième condensateur ;
un troisième condensateur (C3) ayant une cinquième borne de condensateur (N5) connectée à la deuxième borne de sortie du deuxième inverseur, et une sixième borne de condensateur (N6) ;
un deuxième transistor (M2) connecté à la première borne de condensateur (N1) du premier condensateur, le deuxième transistor étant configuré pour délivrer la tension analogique à la première borne de condensateur du premier condensateur lorsqu'un premier signal de commande (CS1) est délivré au deuxième transistor ;
un troisième transistor (M3) connecté à la ligne de données (Dj) et à la première borne (N1) du premier condensateur ;
caractérisé par
un premier transistor (M1) connecté à la sixième borne de condensateur (N6) du troisième condensateur, le premier transistor étant configuré pour commander le passage d'un courant d'une première source d'alimentation (VVdd) à une ligne de données

(Dj) de façon qu'une tension de tampon soit délivrée à la ligne de données, dans lequel le premier transistor est configuré pour commander le courant en réponse à une tension délivrée par le troisième condensateur ;
un quatrième transistor (M4) connecté à la première source d'alimentation (VVdd) et à la sixième borne de condensateur (N6) du troisième condensateur, le quatrième transistor étant configuré pour délivrer une tension égale à la tension de la première source d'alimentation au troisième condensateur lorsque le premier signal de commande (CS1) est délivré au quatrième transistor ; et
un cinquième transistor (M5) connecté à la ligne de données (Dj) et à une deuxième source d'alimentation (VVss), le cinquième transistor étant configuré pour délivrer à la ligne de données la tension de la deuxième source d'alimentation lorsqu'un deuxième signal de commande (CS2) est délivré au cinquième transistor.

2. Tampon selon la revendication 1, dans lequel le premier transistor est configuré pour être rendu non passant lorsque la valeur de la tension du tampon est égale à la valeur de l'entrée de tension analogique.

3. Tampon selon la revendication 1, dans lequel la valeur absolue de la tension délivrée par le troisième condensateur au premier transistor est supérieure à la valeur absolue de l'entrée de tension analogique.

4. Tampon selon l'une des revendications précédentes, dans lequel la tension de la première source d'alimentation est supérieure à la tension de la deuxième source d'alimentation.

5. Tampon selon l'une des revendications précédentes, comprenant en outré :

un sixième transistor connecté à la première sortie du premier inverseur et à la première entrée du premier inverseur, le sixième transistor étant configuré pour être rendu passant lorsque le premier signal de commande est délivré au sixième transistor ; et
un septième transistor connecté à la deuxième sortie du deuxième inverseur et à la deuxième entrée du deuxième inverseur, le septième transistor étant configuré pour être rendu passant lorsque le premier signal de commande est délivré au septième transistor.

6. Tampon selon la revendication 5, dans lequel le troisième transistor est configuré pour être rendu passant lorsqu'un troisième signal de commande est délivré.

7. Tampon selon la revendication 6, dans lequel le tampon est configuré pour recevoir simultanément le début du premier signal de commande et du deuxième signal de commande, et pour recevoir la fin du premier signal de commande plus tôt que la fin du deuxième signal de commande.

8. Tampon selon la revendication 7, dans lequel le tampon est configuré pour recevoir le début du troisième signal de commande après la fin du premier signal de commande et avant la fin du deuxième signal de commande, et pour recevoir la fin du troisième signal de commande après la fin du deuxième signal de commande.

9. Tampon selon l'une des revendications 5 à 8, comprenant en outre :

un huitième transistor connecté entre le premier inverseur et la première source d'alimentation ; et
un neuvième transistor connecté entre le deuxième inverseur et la deuxième source d'alimentation.

10. Tampon selon la revendication 9, dans lequel le huitième transistor et le neuvième transistor ont des conductivités différentes.

11. Tampon selon la revendication 10, dans lequel le huitième transistor est configuré pour être rendu passant lorsqu'un quatrième signal de commande est délivré au huitième transistor, et dans lequel le neuvième transistor est configuré pour être rendu passant lorsqu'un cinquième signal de commande est délivré au neuvième transistor.

12. Tampon selon la revendication 11, dans lequel le tampon est configuré pour recevoir le début des quatrième et cinquième signaux de commande avant ou en même temps que le deuxième signal de commande et pour recevoir la fin des quatrième et cinquième signaux de commande après le début du troisième signal de commande.

13. Tampon selon la revendication 11, dans lequel le tampon est configuré pour recevoir des quatrième et cinquième signaux de commande comprenant chacun au moins une tension égale à la tension de la première source d'alimentation, une tension égale à la tension de la deuxième source d'alimentation et une tension configurée pour fournir un courant limité non nul au premier ou deuxième inverseur.

14. Tampon selon la revendication 11, dans lequel le tampon est configuré pour recevoir en continu les quatrième et cinquième signaux de commande et pour fournir un premier courant limité non nul au premier inverseur et un deuxième courant limité non nul

au deuxième inverseur en réponse aux quatrième et cinquième signaux de commande.

15. Circuit d'attaque de données comprenant :

un convertisseur numérique-analogique configuré pour générer une tension analogique en réponse à une valeur binaire d'une entrée de données ; et
une pluralité de tampons selon l'une des revendications précédentes, chaque tampon étant configuré pour délivrer la tension analogique à une ligne de données.

16. Circuit d'attaque de données selon la revendication 15, comprenant en outre :

un registre à décalage configuré pour générer séquentiellement un signal d'échantillonnage ; et
une section à verrouillage configurée pour stocker les données correspondant au signal d'échantillonnage et pour délivrer les données stockées au convertisseur numérique-analogique.

FIG. 1

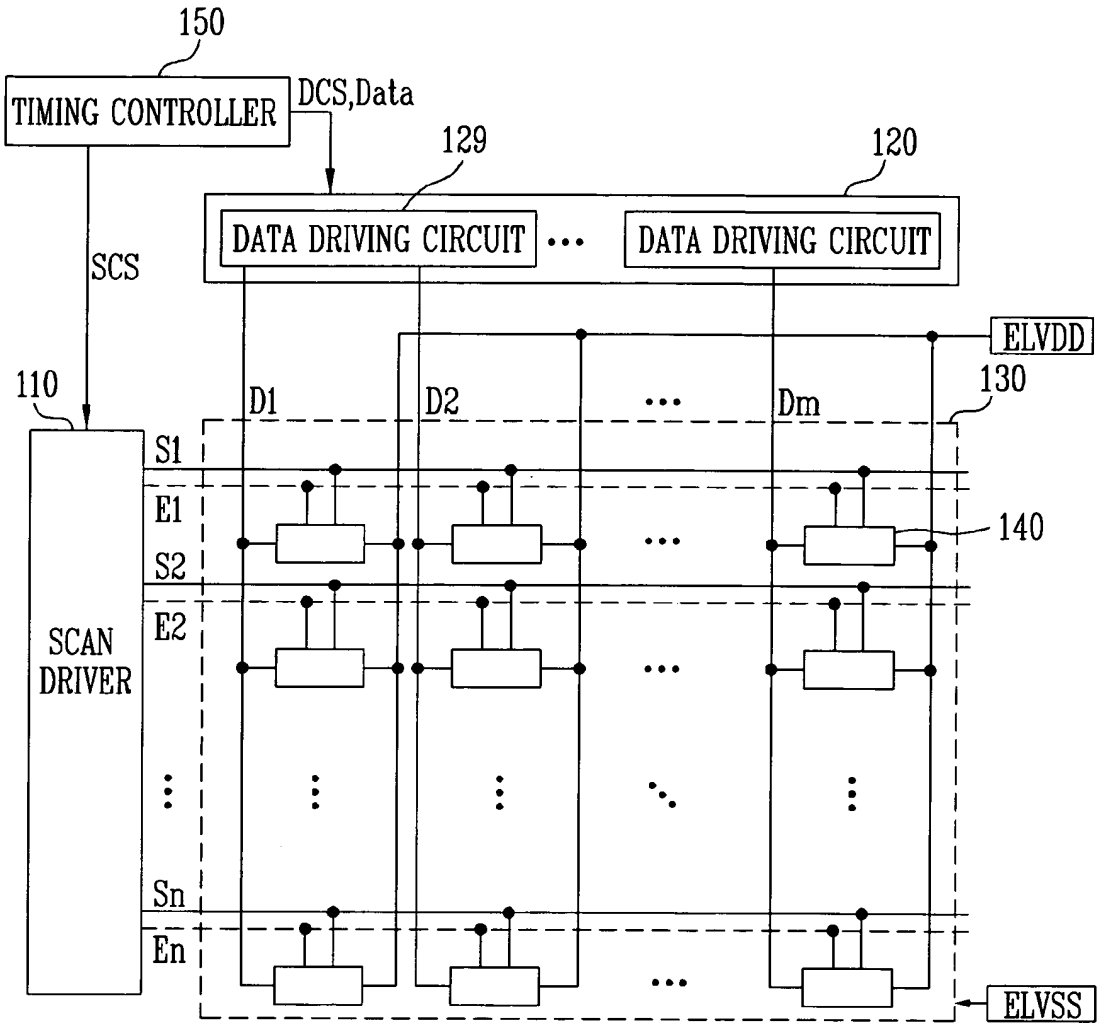

150
TIMING CONTROLLER
DCS,Data
129
120
DATA DRIVING CIRCUIT
DATA DRIVING CIRCUIT
SCS
ELVDD
110
D1
D2
Dm
130
S1
E1
140
S2
E2
SCAN DRIVER
Sn
En
ELVSS

FIG. 2

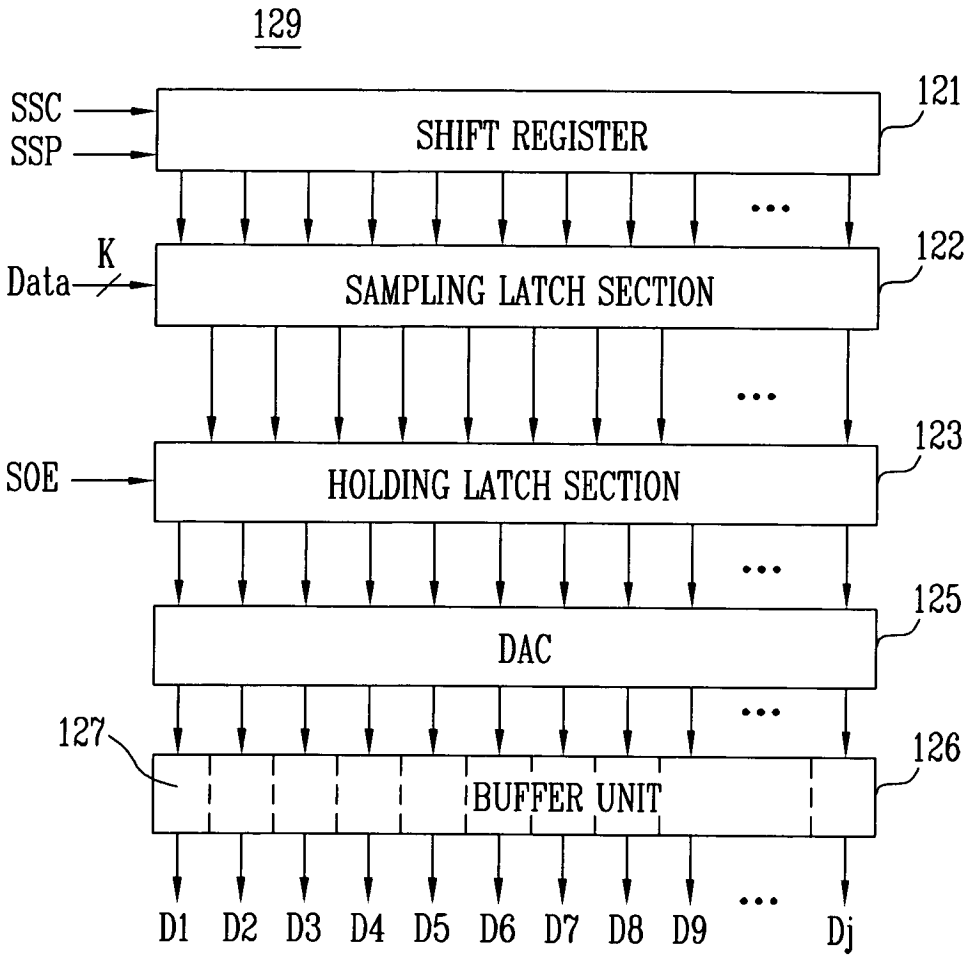

129
SSC
SSP
SHIFT REGISTER
121
Data
K
SAMPLING LATCH SECTION
122
SOE
HOLDING LATCH SECTION
123
DAC
125
127
BUFFER UNIT
126
D1
D2
D3
D4
D5
D6
D7
D8
D9
Dj

FIG. 3

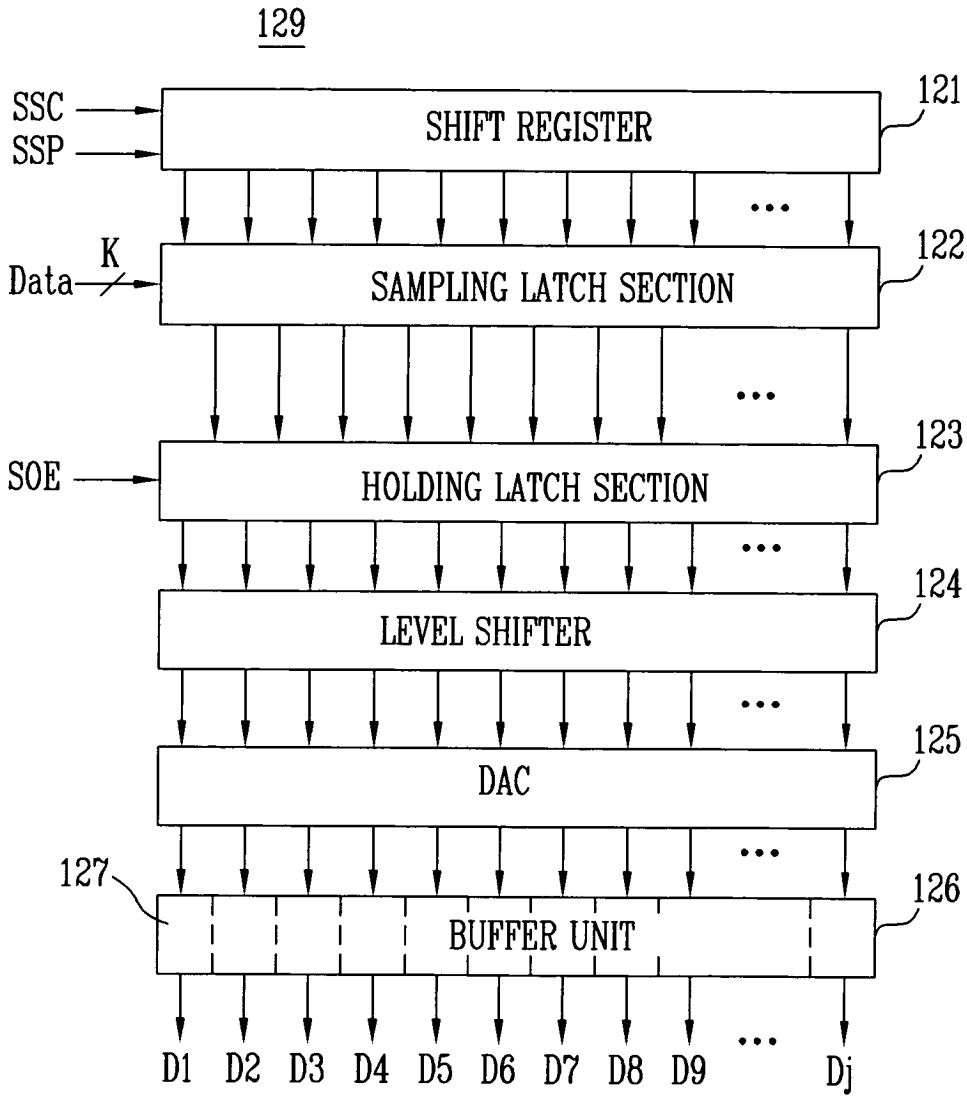

129
SSC
SSP
SHIFT REGISTER
121
Data
K
SAMPLING LATCH SECTION
122
SOE
HOLDING LATCH SECTION
123
LEVEL SHIFTER
124
DAC
125
127
BUFFER UNIT
126
D1 D2 D3 D4 D5 D6 D7 D8 D9 Dj

FIG. 4

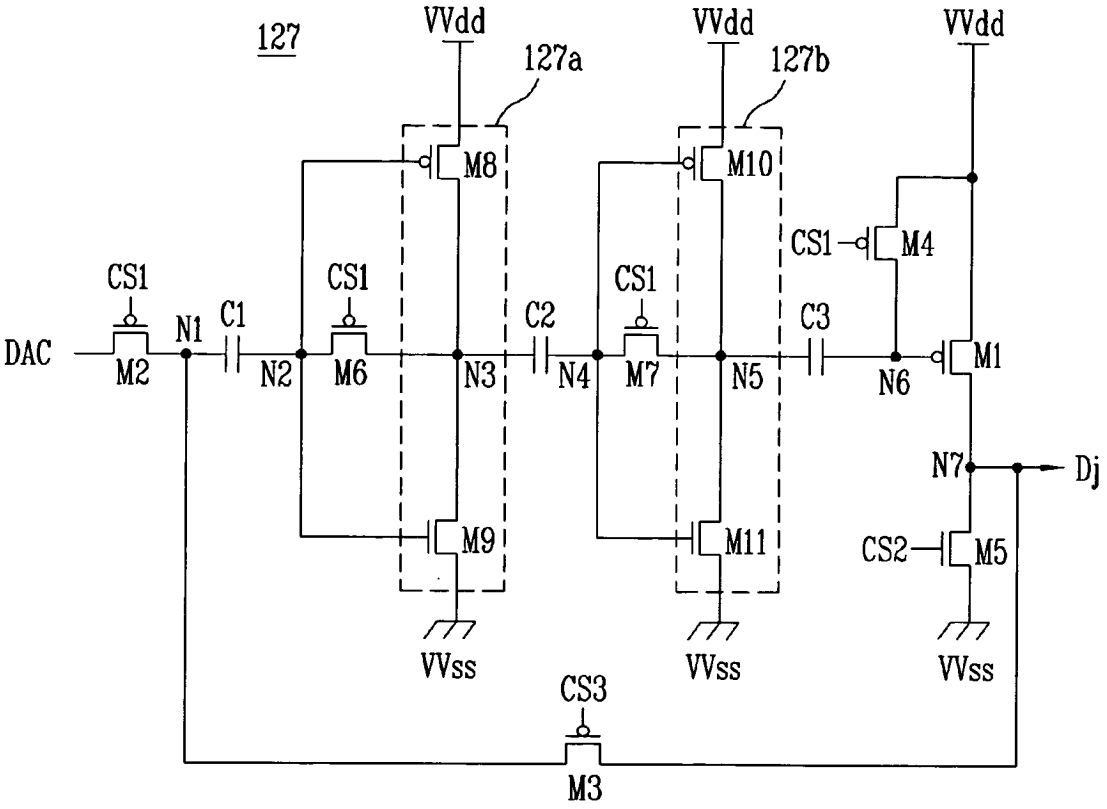

127
VVdd
127a
VVdd
127b
VVdd
M8
M10
CS1
M4
CS1
CS1
CS1
DAC
N1
C1
C2
C3
M2
N2
M6
N3
N4
M7
N5
N6
M1
N7
Dj
M9
M11
CS2
M5
VVss
VVss
VVss
CS3
M3

FIG. 5

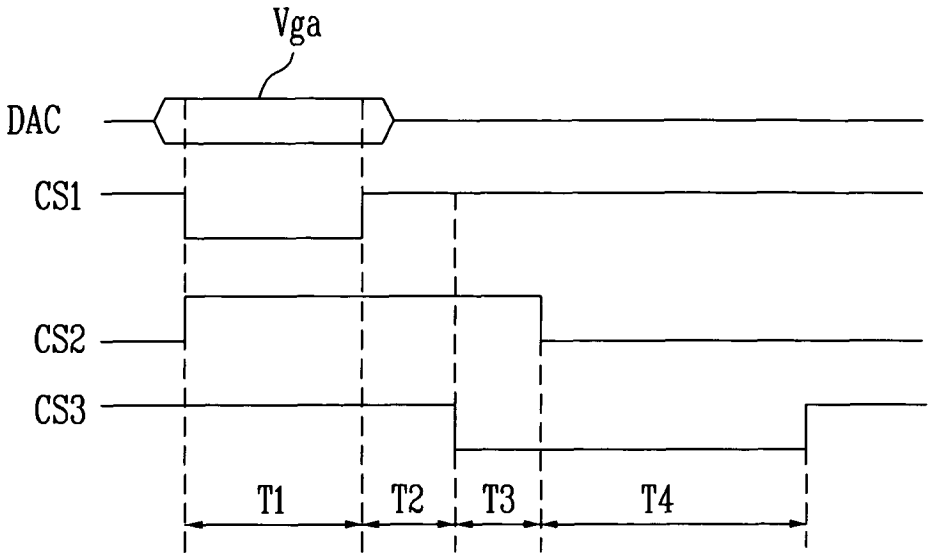


FIG. 6

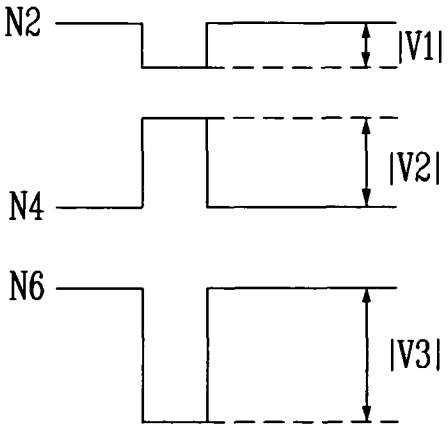


FIG. 7

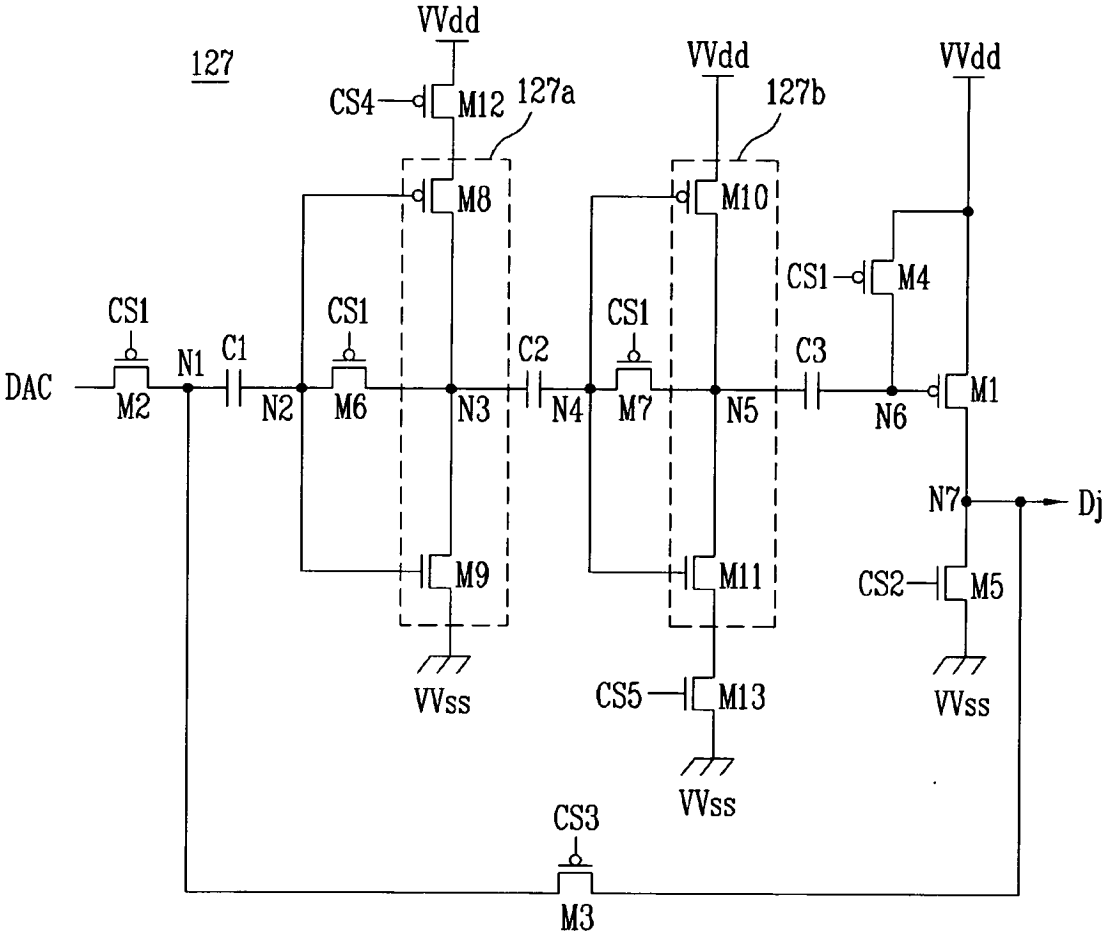

127
VVdd
CS4
M12
127a
M8
M10
127b
VVdd
VVdd
CS1
M4
CS1
CS1
CS1
DAC
M2
N1
C1
N2
M6
N3
C2
N4
M7
N5
C3
N6
M1
N7
Dj
M9
M11
CS2
M5
VVss
CS5
M13
VVss
VVss
CS3
M3

FIG. 8

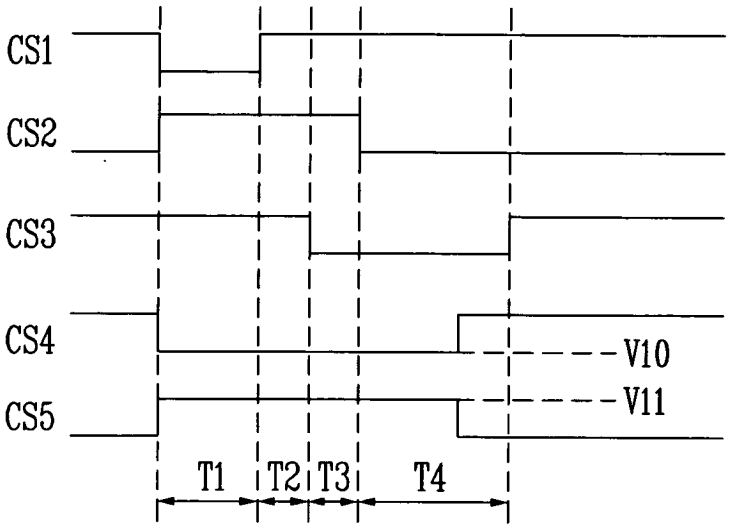


FIG. 9A

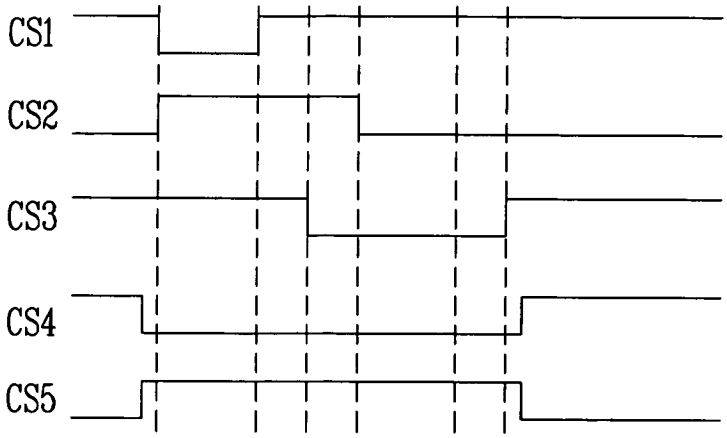


FIG. 9B

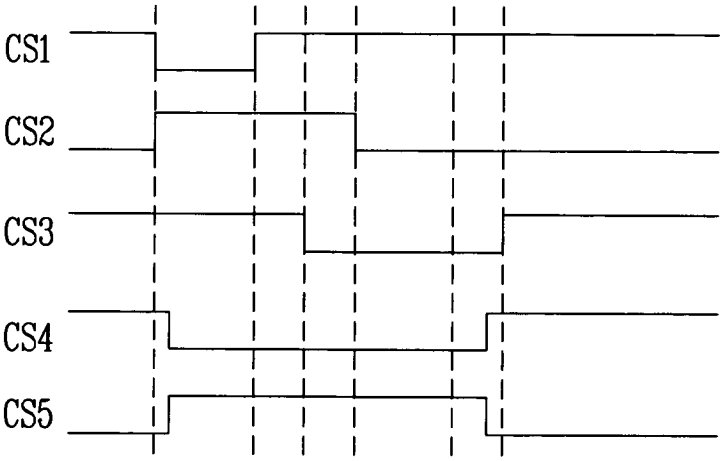
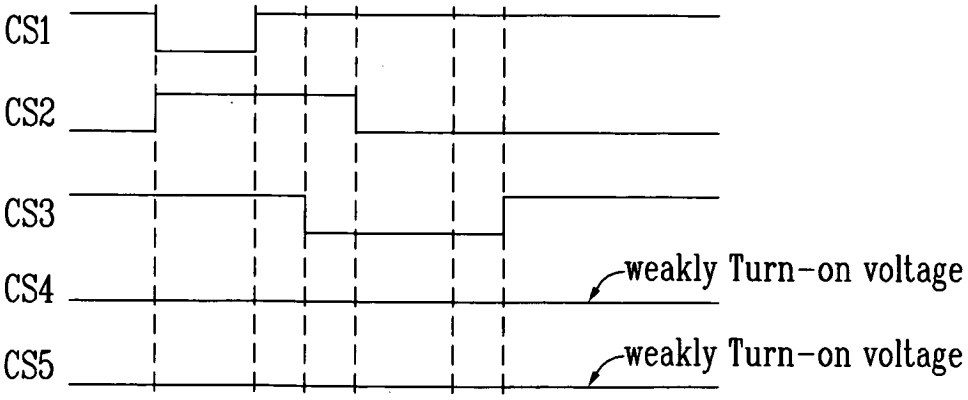


FIG. 9C



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 6498596 B **[0005]**

专利名称(译)	缓冲器和有机发光显示器以及使用该缓冲器的数据驱动电路		
公开(公告)号	EP1708163B1	公开(公告)日	2008-08-20
申请号	EP2006111883	申请日	2006-03-29
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摘要(译)

提供一种缓冲器和有机发光显示器，其具有使用缓冲器的数据驱动电路。缓冲器包括用于接收模拟电压的第一电容器;第一反相器，其输入端连接到第一电容器;第二反相器，其输入端通过第二电容器连接到第一反相器的输出端;第三电容器，连接到第二反相器的输出端;第一晶体管，用于控制从第一电源流到数据线的电流，以便响应于提供给连接在数据线和数据线之间的第三晶体管的控制信号，将缓冲器输出电压提供给数据线。第一个电容器

FIG. 1