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(54) Organic light emitting display device and method of fabricating the same

(57) An organic light emitting display (OLED) device and method of fabricating the same are disclosed. The device may include unit pixel regions arranged on a substrate. Each of the unit pixel regions may include an emission region and a non-emission region. A pixel electrode may be disposed at least in the emission region. A pillar (155) may be disposed between emission regions of adjacent unit pixel regions that emit same-colored light. The pillar may protrude upward further than the pixel electrode. An emission layer (145R) may be disposed on the pixel electrode. An opposite electrode may be disposed on the emission layer.

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Description

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Korean Patent Application No. 2004-37555, filed May 25, 2004, the disclosure of which is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to flat panel displays (FPDs) generally and, more particularly, to an organic light emitting display (OLED) device and method of fabricating the same.

Description of the Related Art

[0003] Flat panel displays (FPDs) incorporating light emitting diodes (LEDs) have garnered much attention as replacements for conventional cathode ray tube (CRT) displays. An LED is an electronic device fabricated by positioning a series of thin films between two conductors. The thin films emit bright light when current is applied to the conductors. Even with multiple layers, LEDs are very thin and can be used to produce thin FPDs that are self-luminous, *e.g.*, do not require backlighting. If the thin films sandwiched between the conductors are formed of organic materials, a flat panel organic electroluminescent display (OLED) device may be produced. Such OLED devices have wider viewing angles, faster video response speeds, and lower power consumption than CRT displays. Other advantages of OLED devices over CRT displays include increased brightness, lighter weight, improved durability, and expanded ranges of operating temperatures.

[0004] FIG. 1A and FIG. 1 B are plan views illustrating a method of fabricating a conventional OLED device, and FIG. 2A and FIG. 2B are cross-sectional views taken along lines I-I of FIG. 1A and FIG. 1 B, respectively.

[0005] Referring to FIG. 1A and FIG. 2A, anodes 3 are formed on an insulating substrate 1 including red (R), green (G), and blue (B) unit pixel regions R, G, and B. Each of the anodes 3 is located in one of the unit pixel regions R, G, and B. A pixel defining layer 2 is formed on the anode 3 such that it has an opening 2a exposing a portion of the surface of the anode 3. The opening 2a defines an emission region E. A hole injection/transport layer 4 is formed on the entire surface of the substrate 1 having the opening 2a.

[0006] Thereafter, a fine metal mask 9 is located on the substrate 1 where the hole injection/transport layer 4 is formed such that the mask has a slit exposing the red unit pixel region R. The fine metal mask 9 is adhered to the substrate 1 using a vacuum absorption process. Then, a red emission layer 5R is deposited using the fine metal mask 9 as a mask. Thus, the red emission layer 5R is formed on the hole injection/transport layer 4 in the red unit pixel region R.

[0007] Referring to FIG. 1 B and FIG. 2B, after the red emission layer 5R is formed, the fine metal mask 9 is removed. During this process, a crack C may form in a portion (S of FIG. 2A) of the hole injection/transport layer 4, which adheres to an edge of the slit of the fine metal mask 9. Generally, the edge of the slit of the fine metal mask 9 is rough, and this rough edge may make the crack C worse. The crack C may also form in the underlying pixel defining layer 2 through the hole injection/transport layer 4. Also, when the hole injection/transport layer 4 is not formed, the crack C may form directly in the pixel defining layer 2.

[0008] After the fine metal mask 9 is removed, a green emission layer 5G and a blue emission layer 5B are formed on the green and blue unit pixel regions G and B, respectively, in the same manner as when the red emission layer 5R is formed. Likewise, cracks may be formed in the hole injection/transport layer 4 or the pixel defining layer 2 on both sides of each of the green and blue emission layers 5G and 5B.

[0009] Subsequently, a cathode 6 is formed on the emission layers 5R, 5G, and 5B. However, if a crack C was formed, it may thin or sever the portion of the cathode 6that overlays the crack C. In either case, the cathode 6 is weakened. The weakened cathode regions may result in some disadvantages, such as a unit pixel reduction phenomenon that reduces the amount of light emitted from an edge portion of a unit pixel during the operation of the OLED device.

SUMMARY OF THE INVENTION

[0010] The present invention may solve the aforementioned problems and/or overcome the disadvantages associated with manufacturing and/or operating conventional OLED devices by providing an OLED device and method of fabricating the same that suppress and/or eliminate the unit pixel reduction phenomenon.

[0011] The present invention discloses an OLED device including unit pixel regions arranged on a substrate. Each of the unit pixel regions may include an emission region and a non-emission region. A pixel electrode may be disposed at least in the emission region. A pillar may be disposed between emission regions of adjacent unit pixel regions that emit a same-colored light. The pillar may protrude upward further than the pixel electrode. An emission layer may be disposed on the pixel electrode, and an opposite electrode may be disposed on the emission layer.

[0012] The present invention also discloses an OLED device including unit pixel regions arranged on a substrate, each of the unit pixel regions including an emission region and a non-emission region. A pixel electrode may be disposed at least in the emission region. A pillar may protrude upward further than the pixel electrode.

The pillar may have a length equal to or smaller than a distance between emission regions of adjacent unit pixel regions that emit same-colored lightthat emit the same colored light. The pillar may have a width smaller than that of each of the unit pixel regions. An emission layer may be disposed on the pixel electrode. An opposite electrode may be disposed on the emission layer.

[0013] The present invention also discloses a method of fabricating an OLED device including the following, which may be performed in any suitable order. Forming a pixel electrode on a substrate in an emission region of a unit pixel region, the unit pixel region also including a non-emission region. Forming a pillar between emission regions of adjacent unit pixel regions that emit the same-colored light. Adhering a fine metal mask to the substrate having the pillar, the fine metal mask having a slit that exposes the adjacent unit pixel regions that emit the same-colored light. Additionally, the method may include forming an emission layer on the exposed unit pixel regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The above and other features of the present invention will be described in reference to certain embodiments thereof with reference to the attached drawings.

[0015] FIG. 1A and FIG. 1 B are plan views illustrating a method of fabricating a conventional organic light emitting display device (OLED).

[0016] FIG. 2A and FIG. 2B are cross-sectional views taken along lines I-I of FIG. 1A and FIG. 1 B, respectively.

[0017] FIG. 3A and FIG. 3B are plan views illustrating a first method of fabricating an OLED device according to embodiments of the present invention.

[0018] FIG. 4A and FIG. 4B are cross-sectional views taken along lines II-II of FIG. 3A and FIG. 3B, respectively, which further illustrate the first method of fabricating an OLED device of the present invention.

[0019] FIG. 5A and FIG. 5B are cross-sectional views taken along lines III-III of FIG. 3A and FIG. 3B, respectively, which further illustrate the first method of fabricating an OLED device of the present invention.

[0020] FIG. 6A and FIG. 6B are cross-sectional views taken along lines IV-IV of FIG. 3A and FIG. 3B, respectively, which further illustrate the first method of fabricating an OLED device of the present invention.

[0021] FIG. 7A and FIG. 7B are cross-sectional views taken along lines V-V of FIG. 3A and FIG. 3B, respectively, which further illustrate the first method of fabricating an OLED device of the present invention.

[0022] FIG. 8A and FIG. 8B are cross-sectional views taken along lines II-II of FIG. 3A and FIG. 3B, respectively, which illustrate a second method of fabricating an OLED device of the present invention.

[0023] FIG. 9A and FIG. 9B are cross-sectional views taken along lines III-III of FIG. 3A and FIG. 3B, respectively, which further illustrate the method according to another embodiment of the present invention.

[0024] FIG. 10A and FIG. 10B are cross-sectional views taken along lines IV-IV of FIG. 3A and FIG. 3B, respectively, which further illustrate the second method of fabricating an OLED device of the present invention.

[0025] FIG. 11A and FIG. 11 B are cross-sectional views taken along lines V-V of FIG. 3A and FIG. 3B, respectively, which further illustrate the second method of fabricating an OLED device of the present invention.

DETAILED DESCRIPTION

[0026] The present invention is described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that the disclosure is thorough and complete and fully conveys the scope of the invention to those skilled in the art. The thicknesses of layers or regions shown in the drawings may be exaggerated for clarity, and the same reference numerals may be used to denote the same elements throughout the specification.

[0027] A first method of fabricating an organic light emitting display (OLED) according to an embodiment of the present invention is now described with reference to FIG. 3A, FIG. 3B, FIG. 4A, FIG. 4B, FIG. 5A, FIG. 5B, FIG. 6A, FIG. 6B, FIG. 7A and FIG. 7B. Specifically, FIG. 3A and FIG. 3B are plan views illustrating a method of fabricating an OLED device manufactured in accordance with the principles of the present invention. FIG. 4A and FIG. 4B are cross-sectional views taken along lines II-II of FIG. 3A and FIG. 3B, respectively. FIG. 5A and FIG. 5B are cross-sectional views taken along lines III-III of FIG. 3A and FIG. 3B, respectively. FIG. 6A and FIG. 6B are cross-sectional views taken along lines IV-IV of FIG. 3A and FIG. 3B, respectively. FIG. 7A and FIG. 7B are cross-sectional views taken along lines V-V of FIG. 3A and FIG. 3B, respectively.

[0028] Referring to FIG. 3A, FIG. 4A, FIG. 5A, FIG. 6A, and FIG. 7A, a substrate 100 on which red (R), green (G), and blue (B) unit pixel regions R, G, and B are arranged is provided. The unit pixel regions R, G, and B may be arranged in a stripe shape. That is, regions that emit same-colored light may be arranged in a column or row. Each of the unit pixel regions R, G, and B includes an emission region E and a non-emission region, which corresponds to a region excluding the emission region E.

[0029] The substrate 100 may be a glass substrate, a plastic substrate, or a quartz substrate. A buffer layer 105 may be formed on the substrate 100. A semiconductor layer 110 is formed on the buffer layer 105 in the non-emission region. The semiconductor layer 110 may be formed of amorphous silicon (a-Si) or poly crystalline

silicon (poly-Si). Preferably, the semiconductor layer 110 is formed of poly-Si. The poly-Si semiconductor layer 110 can be obtained by forming a-Si on the substrate 100 and crystallizing the same. The crystallization of the a-Si may be performed using a metal induced crystallization (MIC) process, a metal induced lateral crystallization (MILC) process, an excimer laser annealing (ELA) process, or a sequential lateral solidification (SLS) process.

[0030] A gate insulating layer 115 may be formed on the semiconductor layer 110, and a gate electrode 120 may be formed on the gate insulating layer 115. Impurity ions may be doped into the semiconductor layer 110 using the gate electrode 120 as a mask, thereby forming source and drain regions 110a and 110b in the semiconductor layer 110. A channel region 110c may be defined between the source region 110a and drain region 110b. An interlayer insulating layer 125 may be formed on the gate electrode 120. A source electrode 130a and drain electrode 130b may be formed on the interlayer insulating layer 125. The source electrode 130a may contact the source region 110a through a first contact hole. The drain electrode 130 may contact the drain region 110b through a second contact hole. In this manner, a thin film transistor (TFT) including the semiconductor layer 110, the gate insulating layer 115, the gate electrode 120, and the source and drain electrodes 130a and 130b may be formed. During the formation of the TFT, a capacitor (not shown) may be formed in the non-emission region.

[0031] A passivation insulating layer 135 may be formed on the source and drain electrodes 130a and 130b. The passivation insulating layer 135 may be an organic layer, an inorganic layer, or a combination thereof. A pixel electrode 140 may be formed on the passivation insulating layer 135 to contact either the source electrode 130a or the drain electrode 130b through a via hole. The pixel electrode 140 may be formed as an anode or a cathode. When the pixel electrode 140 is formed as the anode, it may be made of indium tin oxide (ITO) or indium zinc oxide (IZO). Before the pixel electrode 140 as the anode is formed, a reflective layer may be formed on the passivation insulating layer 135 using one selected from the group consisting of Al, Ag, MoW, AlNd, and Ti. On the other hand, when the pixel electrode 140 is formed as the cathode, it may be made of Mg, Ca, Al, Ag, Ba, or an alloy thereof.

[0032] A pixel defining layer 150 may be formed on the pixel electrode 140 such that it has an opening 150a exposing a portion of the surface of the pixel electrode 140. A region occupied by the opening 150a corresponds to the emission region E. That is, in one embodiment, the emission region E is defined by the opening 150a, and the pixel electrode 140 is located at least in the emission region E. Meanwhile, a pixel driving circuit, which is electrically connected to the pixel electrode 140, may be disposed in the non-emission region. The pixel driving circuit may include the above-described TFT and capacitor.

[0033] The pixel defining layer 150 may be formed of an organic or inorganic layer. When the pixel defining layer 150 is formed of an organic layer, it may be formed of one selected from the group consisting of benzocyclobutene (BCB), acrylic photoresist, phenolic photoresist, and polyimide photoresist. However, the present invention is not limited to the materials or configurations described above.

[0034] Referring briefly to FIG. 6A and FIG. 7A, a pillar 155 may be formed on the pixel defining layer 150 or at any other suitable location. The pillar 155 is formed between emission regions of adjacent unit pixel regions that emit the same-colored light. Also, a length 155L of the pillar 155 may be equal to or smaller than a distance Ed (FIG. 3A) between the emission regions of the adjacent unit pixel regions that emit the same-colored light. The pillar 155 may be formed of the same material as or a different material from the pixel defining layer 150. More specifically, the pillar 155 may be a photosensitive resin. Further, the pillar 155 may be formed of one selected from the group consisting of an acrylic-based organic material, a polyimide-based organic material, and a polyphenolic-based organic material.

[0035] The pillar 155 and the pixel defining layer 150 having the opening 150a may be formed at the same time using a halftone mask. More specifically, a single or double insulating layer for forming the pixel defining layer 150 and the pillar 155 is stacked on the pixel electrode 140. By using the halftone mask, while the opening 150a is being formed in the pixel defining layer 150, the pillar 155 is formed at the same time.

[0036] Thereafter, a first charge injection/transport layer 143 may be formed on the substrate 100 having the pillar 155. The first charge injection/transport layer 143 may be a single layer or a multilayer charge injection/ transport layer. When the pixel electrode 140 is an anode, the first charge injection/transport layer 143 is a hole injection/transport layer. When the pixel electrode 140 is a cathode, the first charge injection/transport layer 143 is an electron injection/transport layer.

[0037] Thereafter, a fine metal mask 900 may be adhered to the substrate 100 such that it has a slit exposing the red unit pixel region R. In one embodiment, the fine metal mask 900 may be adhered to the first charge injection/transport layer 143 formed on the pillar 155. Alternatively, if the first charge injection/transport layer 143 is not formed, the fine metal mask 900 may be adhered to the pillar 155. That is, the fine metal mask 900 may be supported by the pillar 155. Since the pillar 155 is formed between the emission regions of the adjacent unit pixel regions that emit the same-colored light, the pillar 155 is exposed by the slit or covered by the fine metal mask 900 so that it is not in contact with an edge 900s of the slit. Accordingly, the edge 900s of the slit is located a predetermined distance from the first charge injection/transport layer 143 above the substrate 100. Alternatively, if the first charge injection/transport layer

143 is not formed, the edge 900s of the slit is located a predetermined distance above the pixel defining layer 150.

[0038] Subsequently, a red emission layer 145R may be formed on the substrate 100 using the fine metal mask 900 as a mask. The red emission layer 145R may be formed on the first charge injection/transport layer 143 in the red unit pixel region R. After that, the fine metal mask 900 may be removed from the substrate 100. As described above, because the edge 900s of the slit is located a predetermined distance above the first charge injection/transport layer 143 or the pixel defining layer 150 due to the pillar 155, cracks may not form in the first charge injection/transport layer 143 or the pixel defining layer 150 during the removal of the fine metal mask 900.

[0039] The pillar 155 may be formed to a height of 1 μm or more such that the edge 900s of the slit can be spaced a sufficient distance apart from the first charge injection/transport layer 143 or the pixel defining layer 150. However, when the pillar 155 has an excessive height, a shadow effect may take place. Accordingly, the pillar 155 may be formed to a height of about 1 μm to about 5 μm. Also, the pillar 155 may have a width 155w smaller than a width Pw of the red unit pixel region R. More preferably, the width 155w of the pillar 155 is equal to or smaller than a width Ew of the emission region E. Hence, close adhesion of the edge 900s of the slit to the pillar 155 or the first charge injection/transport layer 143 formed on the pillar 155 can be effectively prevented.

[0040] Referring to FIG. 3B, FIG. 4B, FIG. 5B, FIG. 6B, and FIG. 7B, a green emission layer 145G and a blue emission layer 145B are formed in the green and blue unit pixel regions, respectively, in the same manner as when the red emission layer 145R is formed. As described above, the pillar 155 prevents edges of slits of fine metal masks used to form the green and blue emission layers 145G and 145B from being adhered to the first charge injection/transport layer 143 formed on the pixel defining layer 150 or the pixel defining layer 150. Thus, when the fine metal masks are removed, (a crack) or cracks may not form in the first charge injection/transport layer 143 formed on the pixel defining layer 150 or in the pixel defining layer 150.

[0041] A second charge injection/transport layer 147 may be formed on the red, green, and blue emission layers 145R, 145G, and 145B. The second charge injection/transport layer 147 may be formed using a spin coating process or a blanket deposition process. The second charge injection/transport layer 147 may be a single layer or a multiple layer of a second charge injection layer and a second charge transport layer. When the pixel electrode 140 is an anode, the second charge injection/transport layer 147 is an electron injection/transport layer. When the pixel electrode 140 is a cathode, the second charge injection/transport layer 147 is a hole injection/transport layer.

[0042] An opposite electrode 149 is formed on the second charge injection/transport layer 147. When the pixel electrode 140 is an anode, the opposite electrode 149 is formed as a cathode, whereas when the pixel electrode 140 is a cathode, the opposite electrode 149 is formed as an anode. As stated above, the present invention may prevent formation of cracks in an organic layer adjacent to the emission region E (*i.e.*, in the first charge injection/transport layer 143 formed on the pixel defining layer 150 or the pixel defining layer 150) that may be caused by removal of the fine metal mask 900. As a result, the cathode may be applied uniformly, without having portions thereof thinned or separated by a crack. The uniform application of the cathode suppresses and/or eliminates the pixel reduction phenomenon, and increases the amount of light emitted from an edge portion of the unit pixel region.

[0043] Hereinafter, a method of fabricating an OLED according to another embodiment of the present invention is described with reference to FIG. 3A, FIG. 3B, FIG. 8A, FIG. 8B, FIG. 9A, FIG. 9B, FIG. 10A, FIG. 10B, FIG. 11A, and FIG. 11 B. Specifically, FIG. 8A and FIG. 8B are cross-sectional views taken along lines II-II of FIG. 3A and FIG. 3B, respectively. FIG. 9A and FIG. 9B are cross-sectional views taken along lines III-III of FIG. 3A and FIG. 3B, respectively. FIG. 10A and FIG. 10B are cross-sectional views taken along lines IV-IV of FIG. 3A and FIG. 3B, respectively. FIG. 11A and FIG. 11 B are cross-sectional views taken along lines V-V of FIG. 3A and FIG. 3B, respectively.

[0044] Referring to FIG. 3A, FIG. 8A, FIG. 9A, FIG. 10A, and FIG. 11A, a substrate 100 on which red, green, and blue unit pixel regions R, G, and B are arranged is provided. The red, green, and blue unit pixel regions may be arranged in a stripe shape. That is, regions that emit same-colored light may be arranged in a column or row. Each of the unit pixel regions R, G, and B includes an emission region E and a non-emission region, which corresponds to a region excluding the emission region E.

[0045] The substrate 100 may be a glass substrate, a plastic substrate, or a quartz substrate. A buffer layer 105, a TFT, and an interlayer insulating layer 125 may be formed on the substrate 100 in the same manner TFT completed after 125 as described with reference to FIG. 4A, FIG. 5A, FIG. 6A, and FIG. 7A. The TFT may include a semiconductor layer 110, a gate insulating layer 115, a gate electrode 120, and source and drain electrodes 130a and 130b, and the semiconductor layer 110 includes source and drain regions 110a and 110b and a channel region 110c. As mentioned above, a capacitor (not shown) may be formed in the non-emission region during the formation of the TFT.

[0046] A passivation insulating layer 135 may be formed on the source and drain electrodes 130a and 130b. The passivation insulating layer 135 may be an organic layer, an inorganic layer, or a combination thereof. A pixel electrode 140 may be formed on the passivation insulating layer 135 to contact one of the source

and drain electrodes 130a and 130b through a via hole. Unlike the embodiments described above, a region occupied by the pixel electrode 140 may correspond to the emission region E. That is, the emission region E may be defined by the pixel electrode 140. Meanwhile, a pixel driving circuit, which is electrically connected to the pixel electrode 140, may be disposed in the non-emission region. The pixel driving circuit may include the above-described TFT and capacitor.

[0047] The pixel electrode 140 may be formed as an anode or a cathode. When the pixel electrode 140 is formed as the anode, it may be made of ITO or IZO. Before the pixel electrode 140 as the anode is formed, a reflective layer may be formed on the passivation insulating layer 135 using one selected from the group consisting of Al, Ag, MoW, AlNd, and Ti. On the other hand, the pixel electrode 140 as the cathode may be made of Mg, Ca, Al, Ag, Ba, or an alloy thereof.

[0048] A pillar 155 may be formed on the substrate 100 on which the pixel electrode 140 is formed such that it protrudes upward further than the pixel electrode 140. The pillar 155 may be formed between emission regions of adjacent unit pixel regions that emit same-colored light. Also, the pillar 155 may have a length 155L equal to or smaller than a distance Ed between the emission regions of the adjacent unit pixel regions that emit the same-colored light. The pillar 155 may be a photosensitive resin. Further, the pillar 155 may be formed of one selected from the group consisting of an acrylic-based organic material, a polyimide-based organic material, and a polyphenolic-based organic material.

[0049] Thereafter, a first charge injection/transport layer 143 may be formed on the substrate 100 having the pillar 155. The first charge injection/transport layer 143 may be a single layer or a multilayer charge injection/transport layer. When the pixel electrode 140 is an anode, the first charge injection/transport layer 143 is a hole injection/transport layer. When the pixel electrode 140 is a cathode, the first charge injection/transport layer 143 is an electron injection/transport layer.

[0050] Thereafter, a fine metal mask 900 may be adhered to the substrate 100 such that a slit in the mask exposes the red unit pixel region R. In such an embodiment,the fine metal mask 900 may be adhered to the first charge injection/transport layer 143 formed on the pillar 155. If the first charge injection/transport layer 143 is not formed, the fine metal mask 900 may be adhered to the pillar 155. That is, the fine metal mask 900 may be supported by the pillar 155. Since the pillar 155 is formed between the emission regions of the adjacent unit pixel regions that emit the same-colored light, the pillar 155 is exposed by the slit or covered by the fine metal mask 900 so that it is not in contact with an edge 900s of the slit. Accordingly, the edge 900s of the slit is located a predetermined distance from the first charge injection/transport layer 143 above the substrate 100.

[0051] Subsequently, a red emission layer 145R may be formed on the substrate 100 using the fine metal mask 900 as a mask. The red emission layer 145R may be formed on the first charge injection/transport layer 143 in the red emission region R. After that, the fine metal mask 900 is removed from the substrate 100. As stated above, because the edge 900s of the slit is located a predetermined distance from the first charge injection/transport layer 143 due to the pillar 155, cracks may not form in the first charge injection/transport layer 143 during the removal of the fine metal mask 900.

[0052] The pillar 155 may be formed to a height of 1 μm or more such that the edge 900s of the slit can be spaced a sufficient distance apart from the first charge injection/transport layer 143. However, when the pillar 155 has an excessive height, a shadow effect may take place. Accordingly, the pillar 155 may be formed to a height of about 1 μm to about 5 μm. Also, the pillar 155 may have a width 155w smaller than a width Pw of the red unit pixel region R. More preferably, the width 155w of the pillar 155 is equal to or smaller than a width Ew of the emission region E. Hence, close adhesion of the edge 900s of the slit to the pillar 155 or the first charge injection/transport layer 143 formed on the pillar 155 can be effectively prevented.

[0053] Referring to FIG. 3B, FIG. 8B, FIG. 9B, FIG. 10B, and FIG. 11 B, a green emission layer 145G and a blue emission layer 145B are formed in the green and blue unit pixel regions, respectively, in the same manner as when the red emission layer 145R is formed. As described above, the pillar 155 prevents edges of slits of fine metal masks used to form the green and blue emission layers 145G and 145B from adhering to the first charge injection/transport layer 143. Thus, when the fine metal masks are removed, cracks may not form in the first charge injection/transport layer 143.

[0054] A second charge injection/transport layer 147 may be formed on the red, green, and blue emission layers 145R, 145G, and 145B. The second charge injection/transport layer 147 may be formed using a spin coating process or a blanket deposition process. The second charge injection/transport layer 147 may be a single layer or multi-layer second charge injection/transport layer. When the pixel electrode 140 is an anode, the second charge injection/transport layer 147 is an electron injection/transport layer. When the pixel electrode 140 is a cathode, the second charge injection/transport layer 147 is a hole injection/transport layer.

[0055] An opposite electrode 149 is formed on the second charge injection/transport layer 147. When the pixel electrode 140 is an anode, the opposite electrode 149 is formed as a cathode, whereas when the pixel electrode 140 is a cathode, the opposite electrode 149 is formed as an anode. As stated above, the present invention may prevent formation of cracks in an organic layer adjacent to the emission region E (*i.e.*, in the first charge injection/transport layer 13) that may be caused by removal of the fine metal mask 900. Consequently, the cathode may be uniformly deposited. Uniform application of the cathode suppresses and/or eliminates the

pixel reduction phenomenon,and increases the amount of light emitted from an edge portion of the unit pixel region.

[0056] As explained thus above, the present invention may prevent formation of cracks in an organic layer adjacent to an emission region caused by removal of a fine metal mask, so that a cathode is not thinned or cut by the crack. Hence, an OLED device manufactured according to the principles of the invention can operate with improved viewing contrast and/or picture quality.

[0057] Although the present invention has been described with reference to certain embodiments thereof, it will be understood by those skilled in the art that a variety of modifications and variations may be made to the present invention without departing from the spirit or scope of the present invention defined in the appended claims, and their equivalents.

Claims

1. An organic light emitting display device, comprising:

unit pixel regions arranged on a substrate, each of the unit pixel regions including an emission region and a non-emission region;
a pixel electrode disposed at least in the emission region;
a pillar disposed between emission regions of adjacent unit pixel regions that emit same-colored light, the pillar protruding upward further than the pixel electrode;
an emission layer disposed on the pixel electrode; and
an opposite electrode disposed on the emission layer.

2. The device of claim 1, wherein the pillar has a width smaller than a width of each of the unit pixel regions.

3. The device of claim 2, wherein the width of the pillar is equal to or smaller than a width of the emission region.

4. The device of claim 1, wherein the pillar has a length equal to or smaller than a distance between the emission regions of the adjacent unit pixel regions that emit same-colored light.

5. The device of claim 1, wherein the pillar has a height of about 1 μm or more.

6. The device of claim 5, wherein the height of the pillar is about 1 μm to about 5 μm.

7. The device of claim 1, wherein the pillar is formed of a material selected from the group consisting of an acrylic-based organic material, a polyimide-based organic material, and a polyphenolic-based organic material.

8. The device of claim 1, wherein the emission region is defined by the pixel electrode.

9. The device of claim 1, further comprising a pixel defining layer disposed on the pixel electrode and having an opening that exposes a portion of the pixel electrode,
wherein the emission region is defined by the opening.

10. The device of claim 9, wherein the pillar is disposed on the pixel defining layer.

11. The device of claim 1, wherein the emission layer is formed using a fine metal mask.

12. The device of claim 1, wherein the unit pixel regions include red unit pixel regions, green unit pixel regions, and blue unit pixel regions.

13. The device of claim 1, wherein the unit pixel regions are arranged on the substrate in a stripe shape.

14. The device of claim 1, further comprising a pixel driving circuit disposed in the non-emission region and electrically connected to the pixel electrode.

15. The device of claim 14, wherein the pixel driving circuit includes a thin film transistor.

16. A method of fabricating an organic light emitting display device, comprising:

providing a substrate including unit pixel regions, each of the unit pixel regions including an emission region and a non-emission region;
forming a pixel electrode on the substrate in the emission region;
forming a pillar between emission regions of adjacent unit pixel regions that emit same-colored light;
closely adhering a fine metal mask to the substrate having the pillar, the fine metal mask having a slit that exposes the adjacent unit pixel regions that emit same-colored light; and
forming an emission layer on the exposed unit pixel regions.

17. The method of claim 16, wherein the pillar is formed to have a width smaller than a width of each of the unit pixel regions and a length equal to or smaller than a distance between the emission regions of the adjacent unit pixel regions that emit same-colored light.

18. The method of claim 16, wherein the pillar is formed to have a width equal to or smaller than a width of the emission region.

19. The method of claim 16, wherein a region where the pixel electrode is formed corresponds to the emission region.

20. The method of claim 16, further comprising forming a pixel defining layer on the pixel electrode, the pixel defining layer having an opening that exposes a portion of the pixel electrode,

wherein a region where the opening is formed corresponds to the emission region, and the pillar is formed on the pixel defining layer.

21. The method of claim 20, wherein the pillar and the pixel defining layer having the opening are formed simultaneously using a halftone mask.

FIG. 1A
(PRIOR ART)

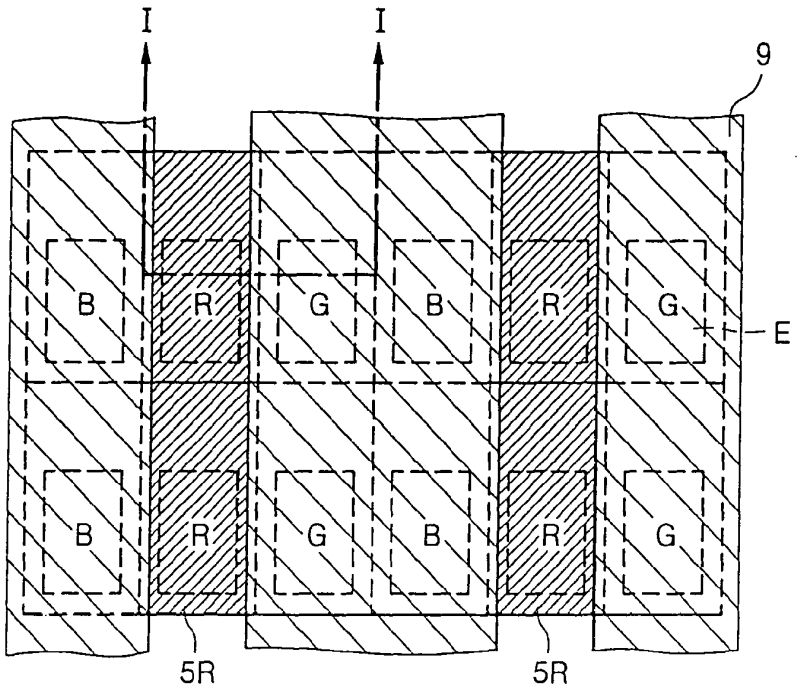


FIG. 1B
(PRIOR ART)

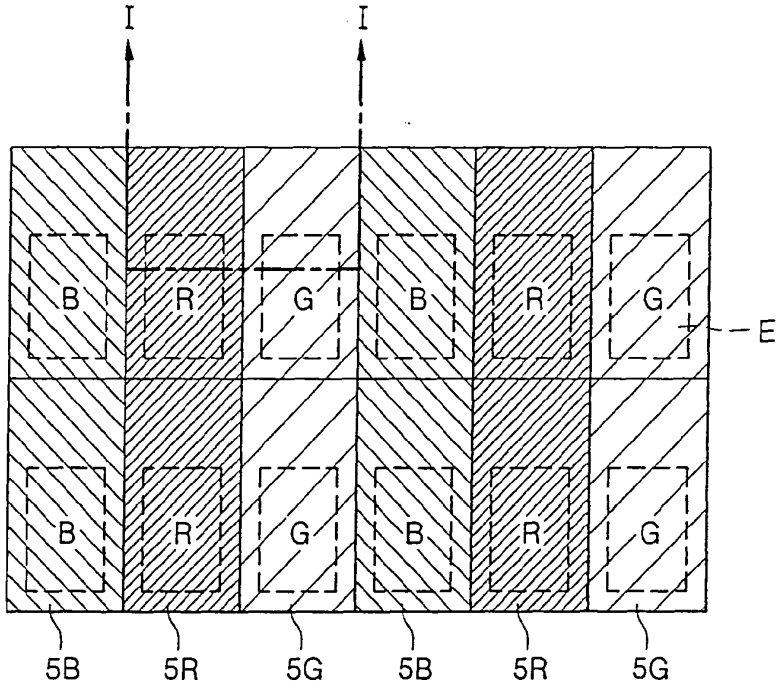


FIG. 2A
(PRIOR ART)

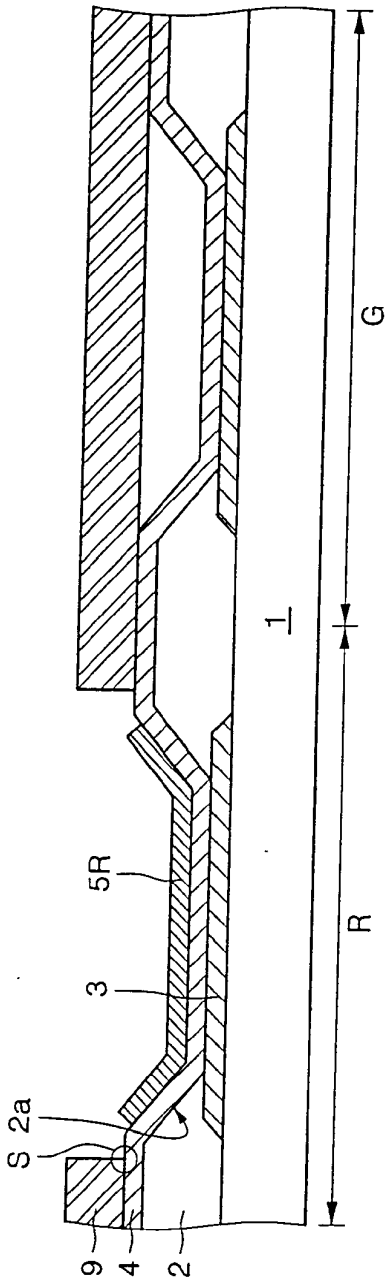


FIG. 2B
(PRIOR ART)

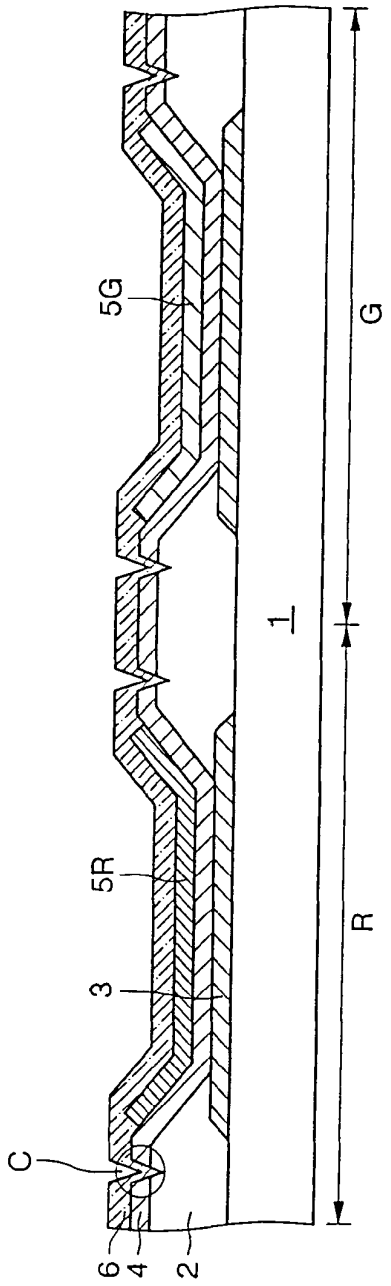
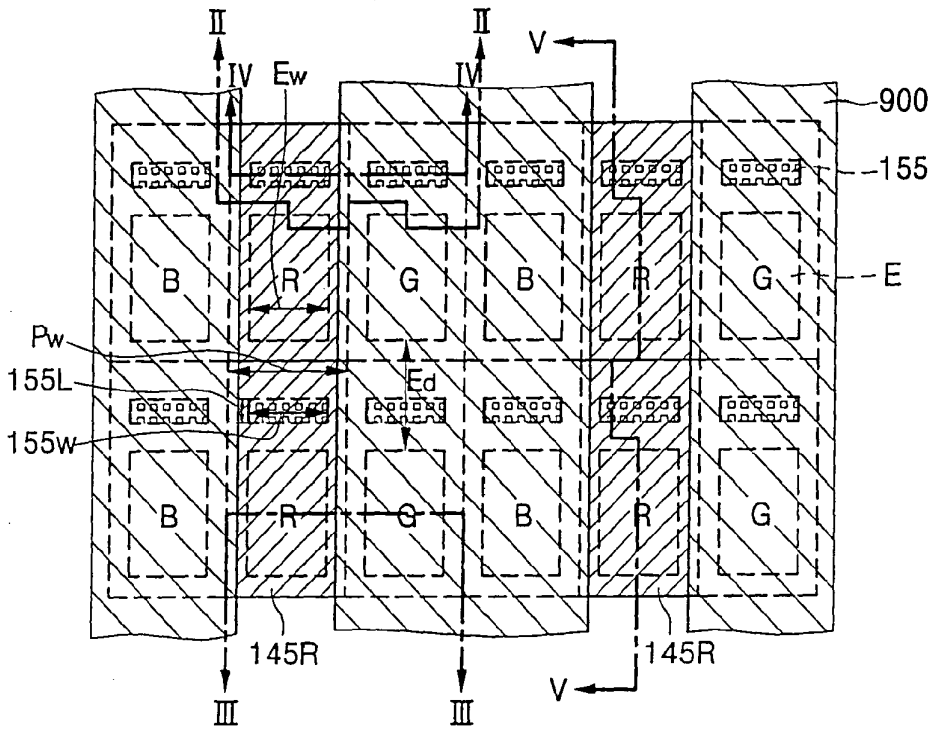


FIG. 3A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V
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IV
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G
B
R
G
E
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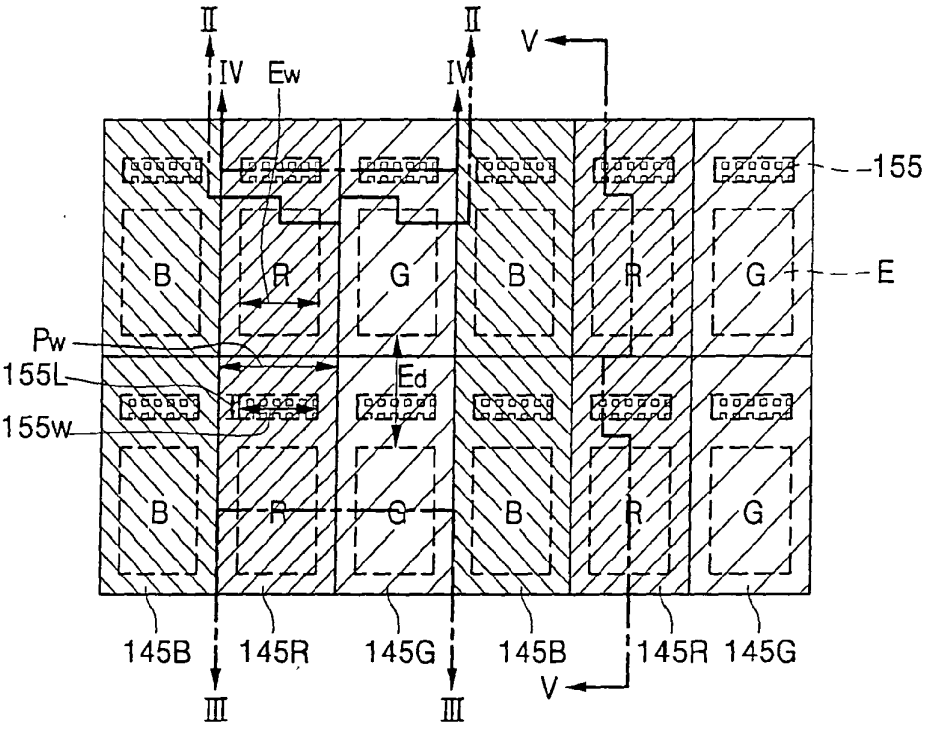
R
G
B
R
G
145R
145R
V
III
III

FIG. 3B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145G
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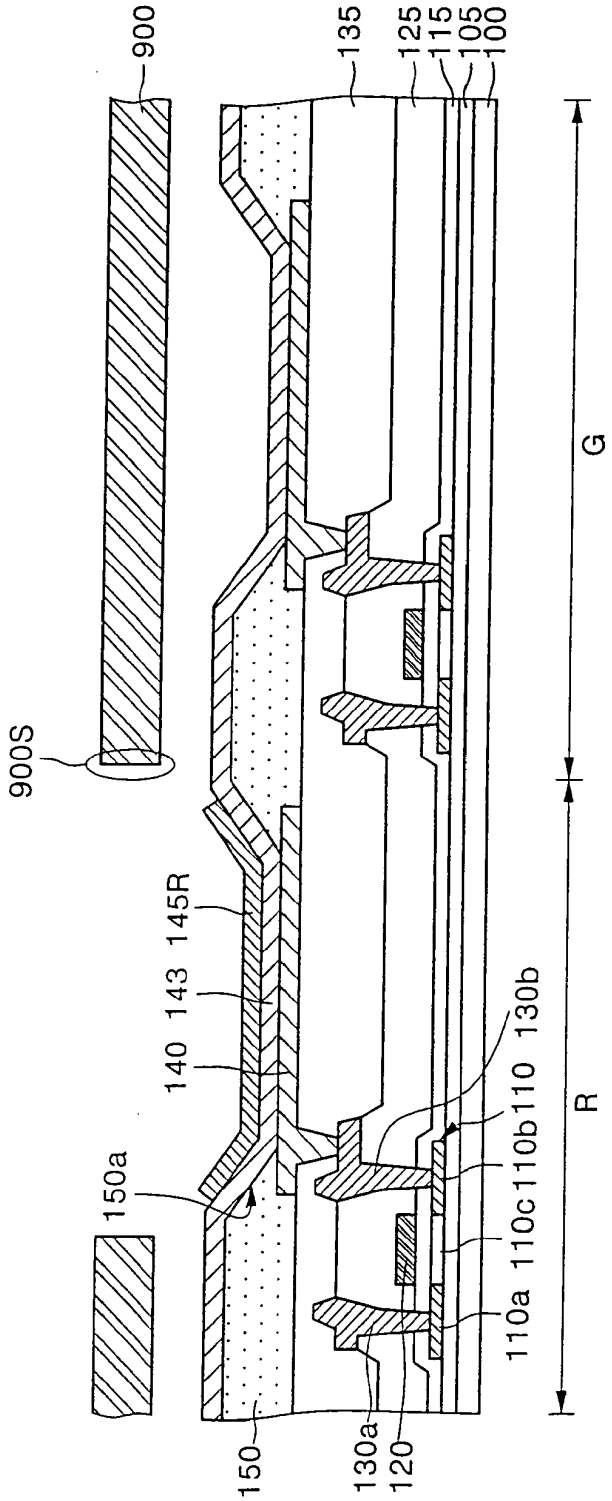
145R
145G
V
III
III

FIG. 4A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110b
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110a
R
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130a
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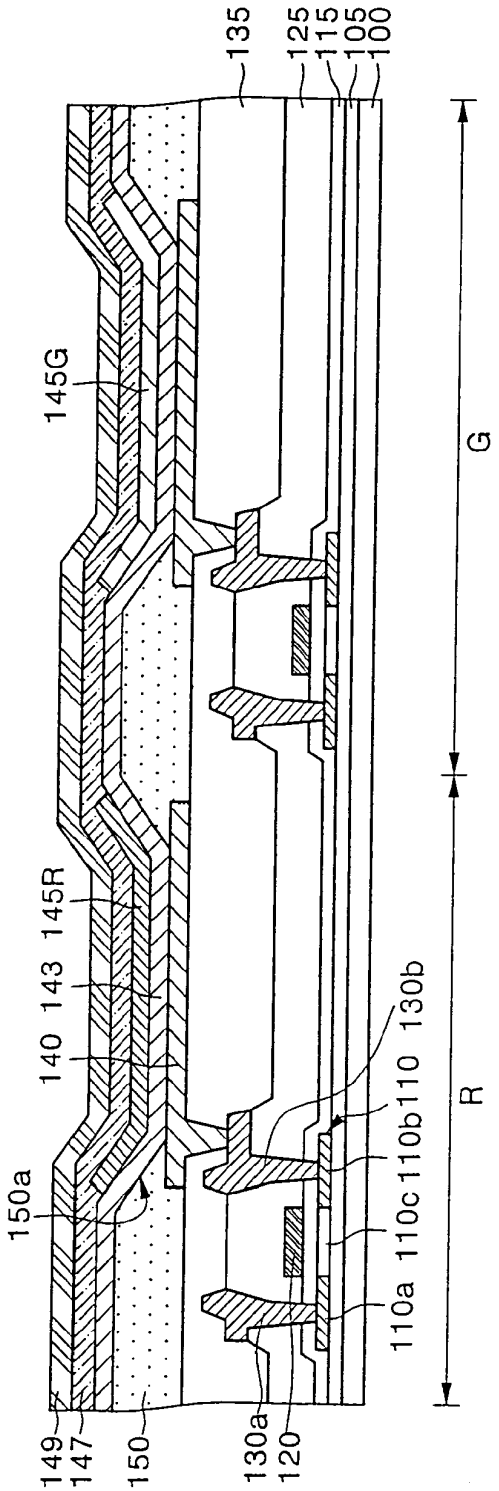
FIG. 4B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110c
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R
150a
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130a
120

FIG. 5A

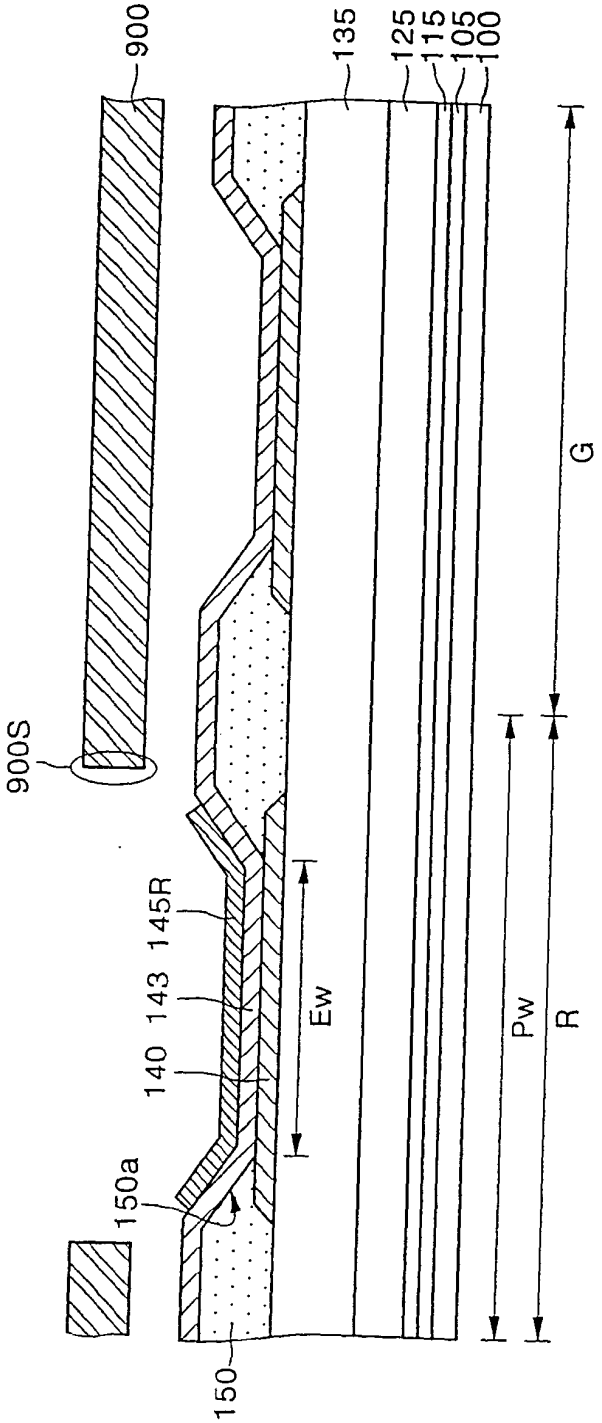


FIG. 5B

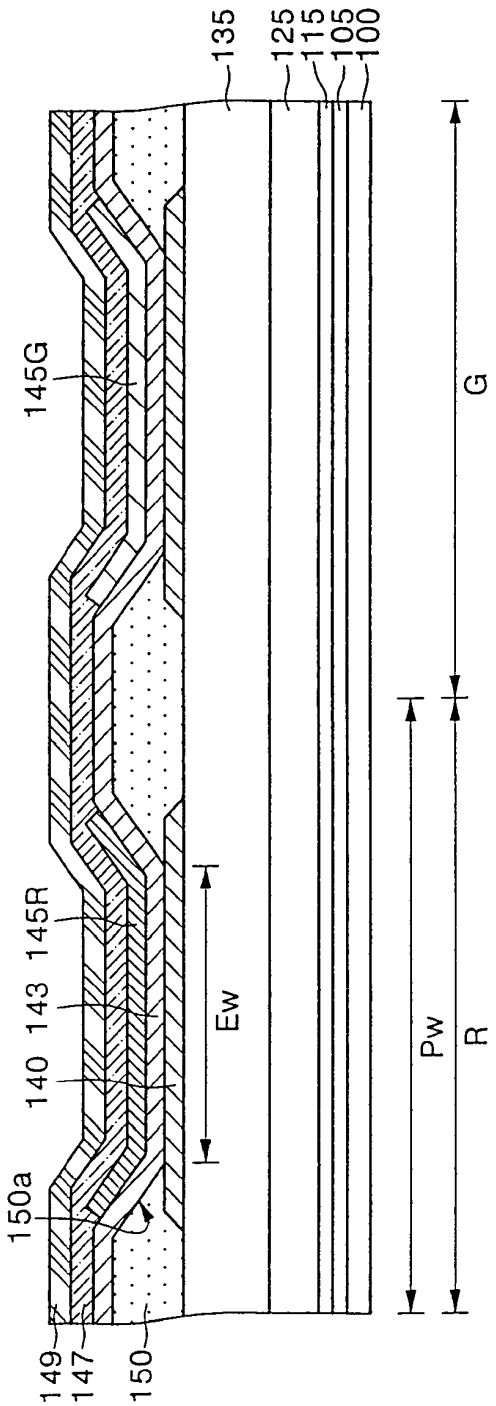


FIG. 6A

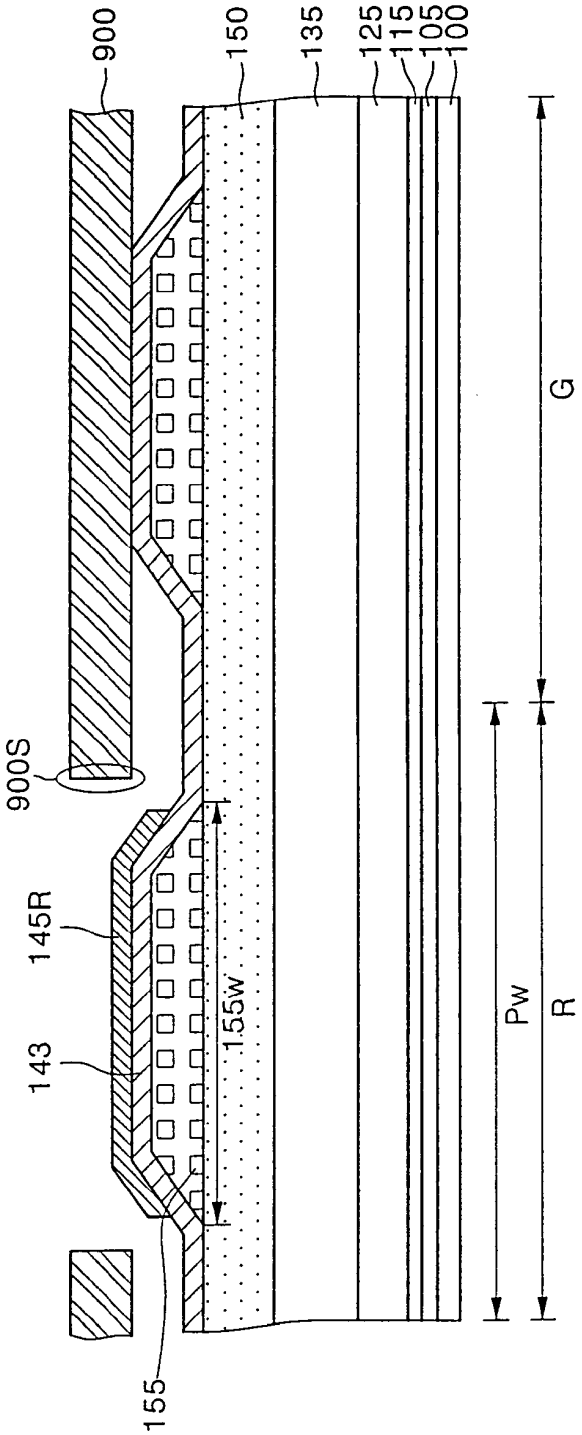


FIG. 6B

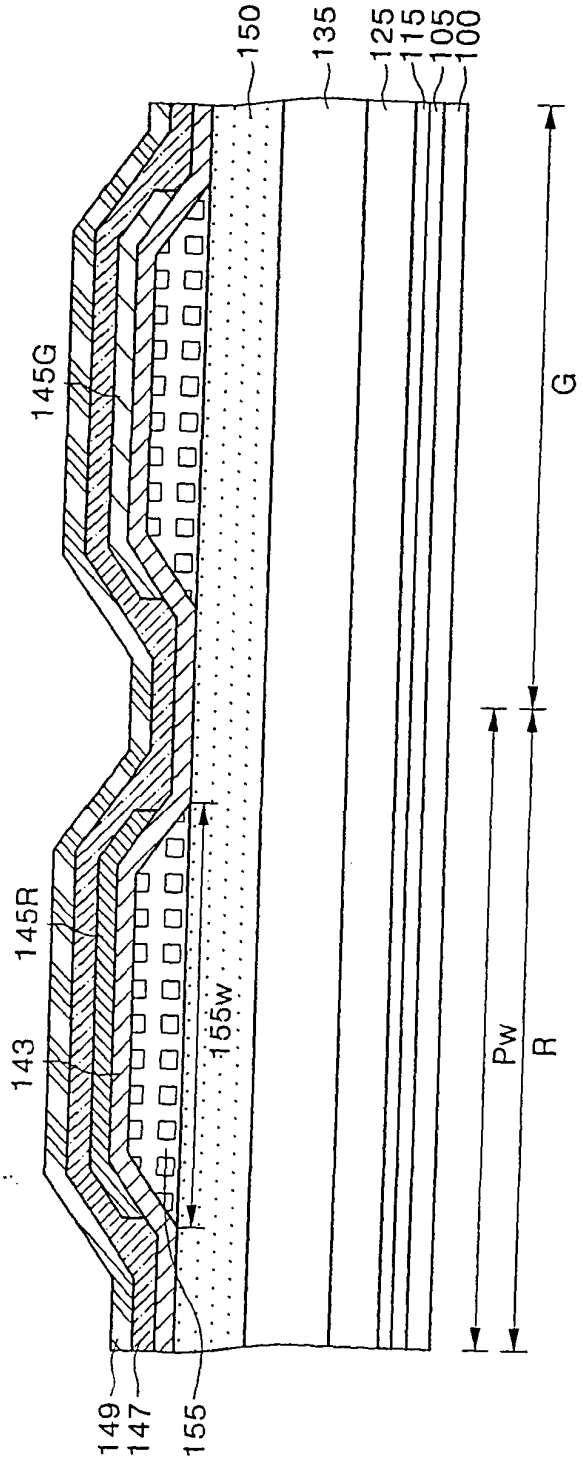
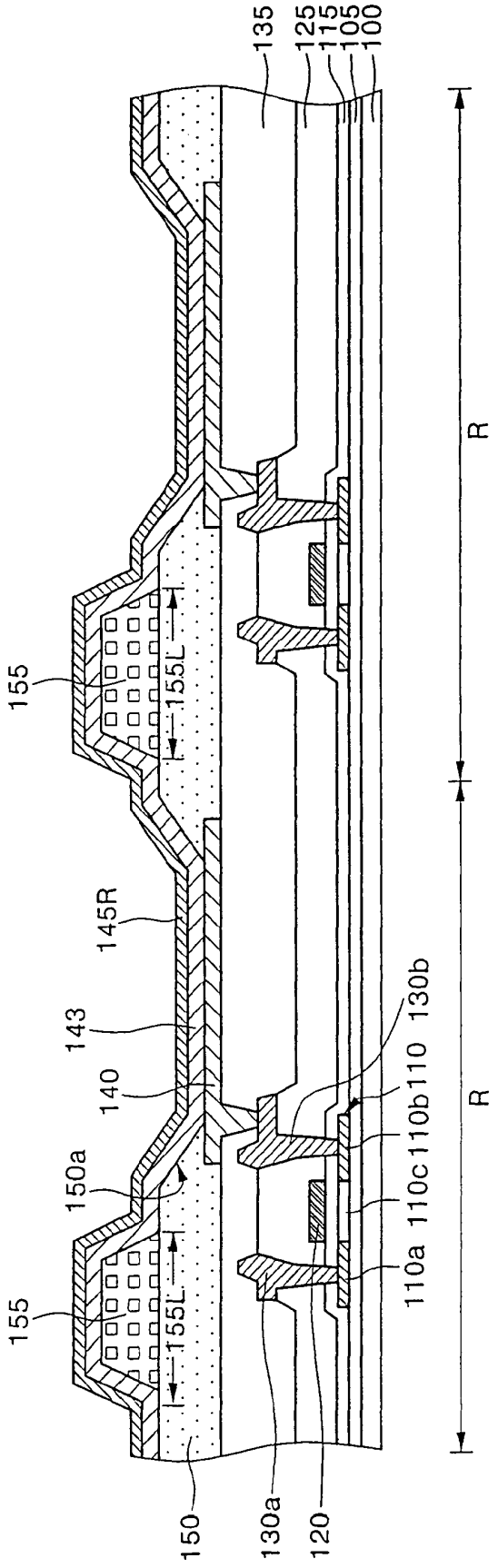


FIG. 7A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155L
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110b
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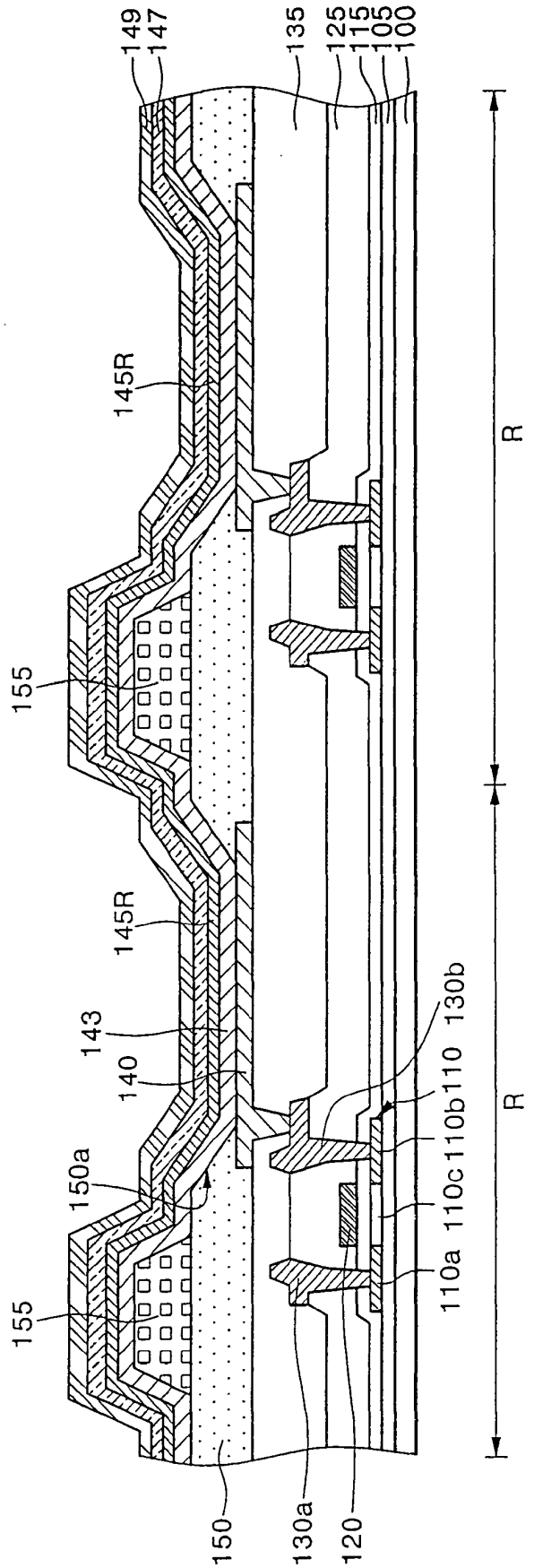
110a
R
155
155L
150
130a
120

FIG. 7B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130a
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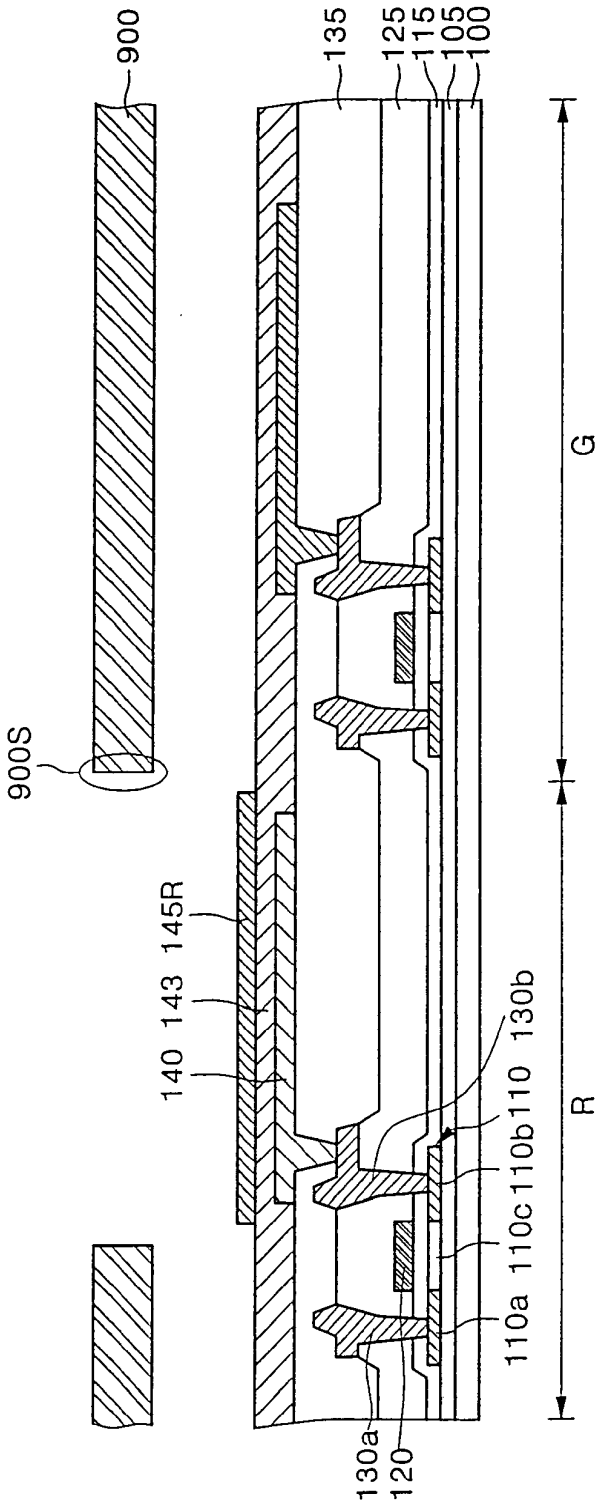
110c
110b
110
130b
R
R

FIG. 8A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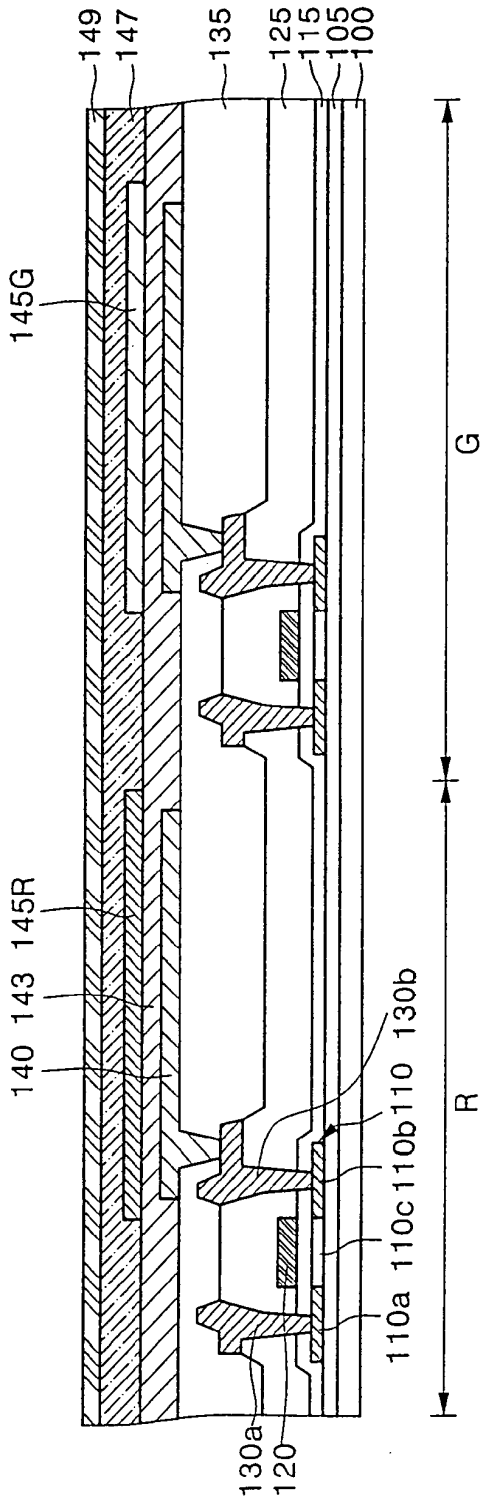
110b
110c
110a
R
130a
120

FIG. 8B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110b
110c
110a
R
130a
120

FIG. 9A

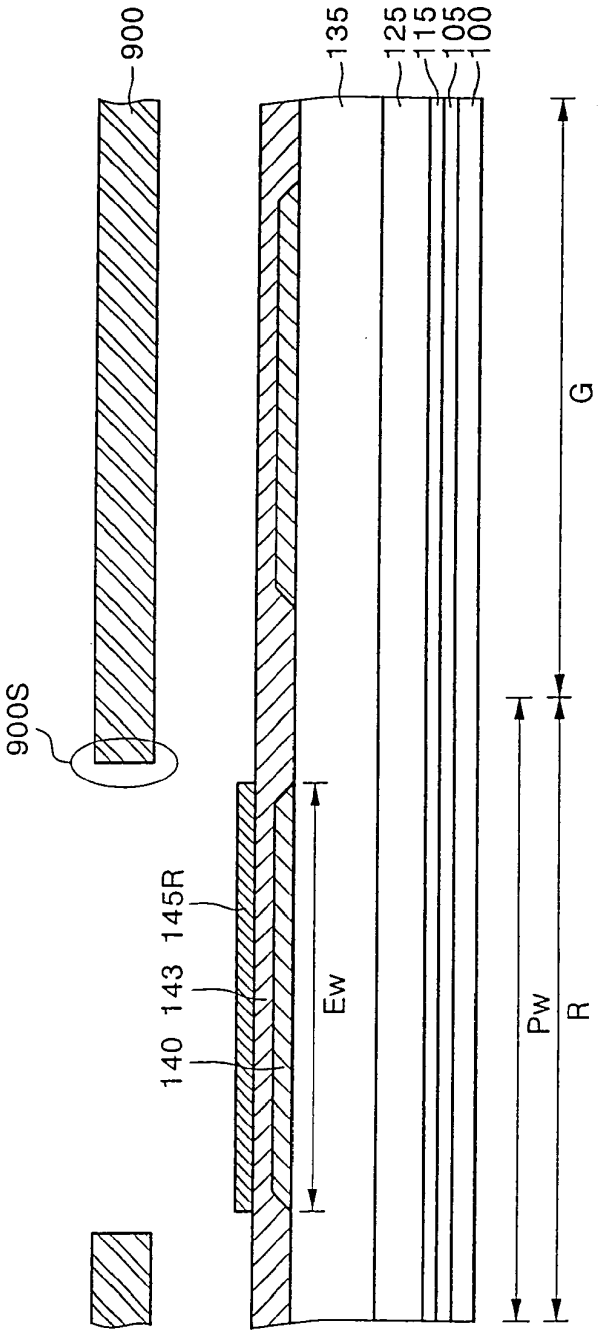


FIG. 9B

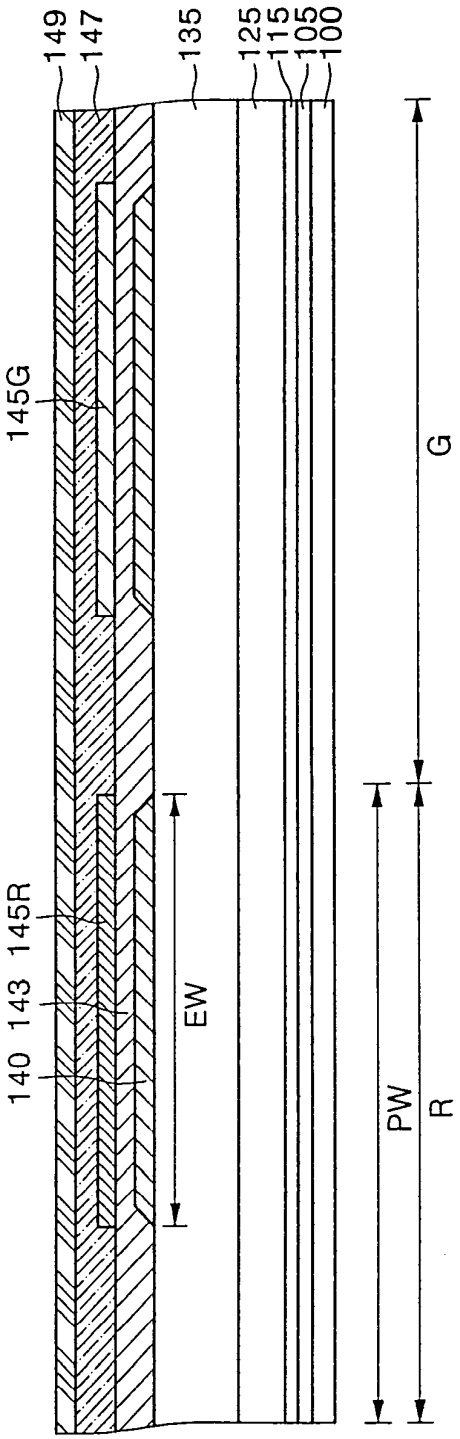


FIG. 10A

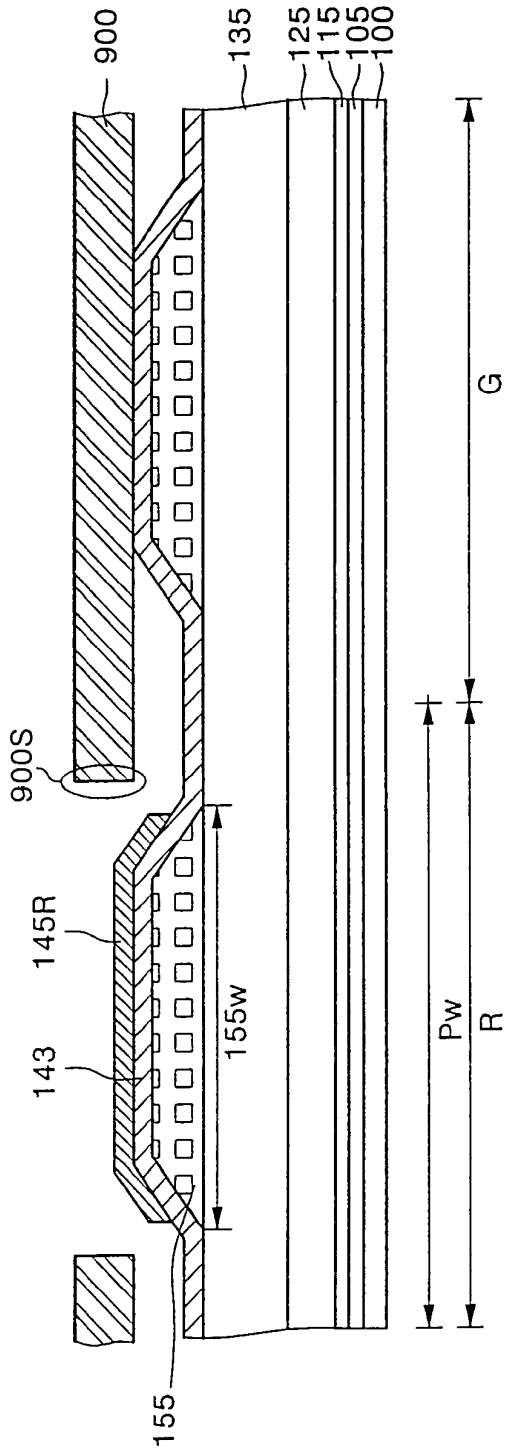


FIG. 10B

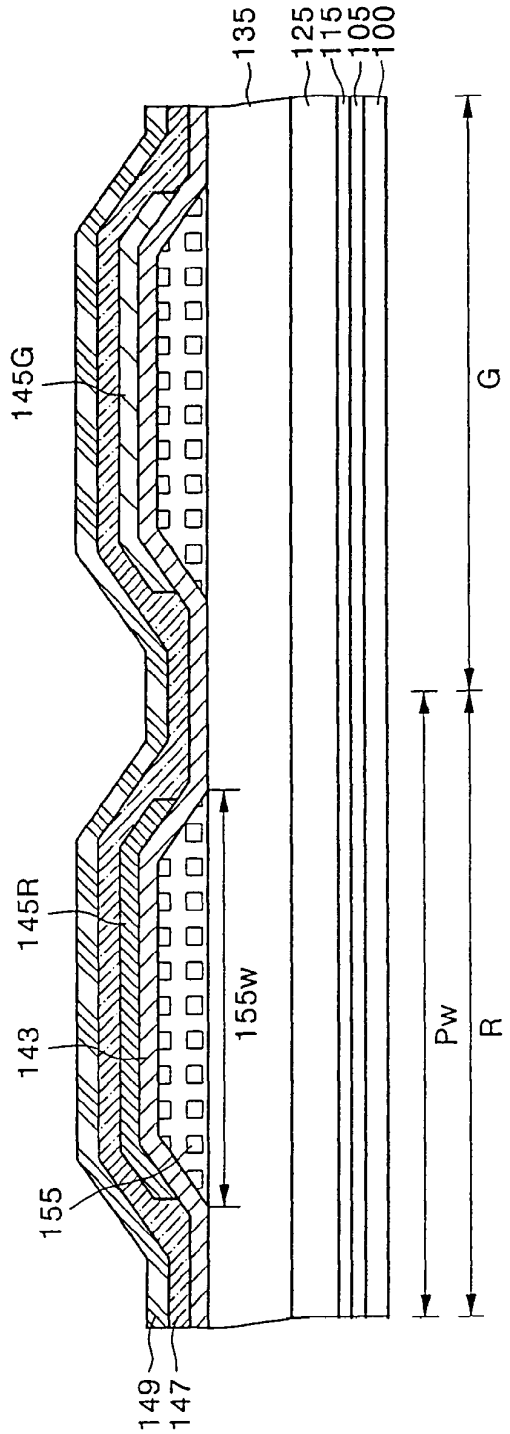
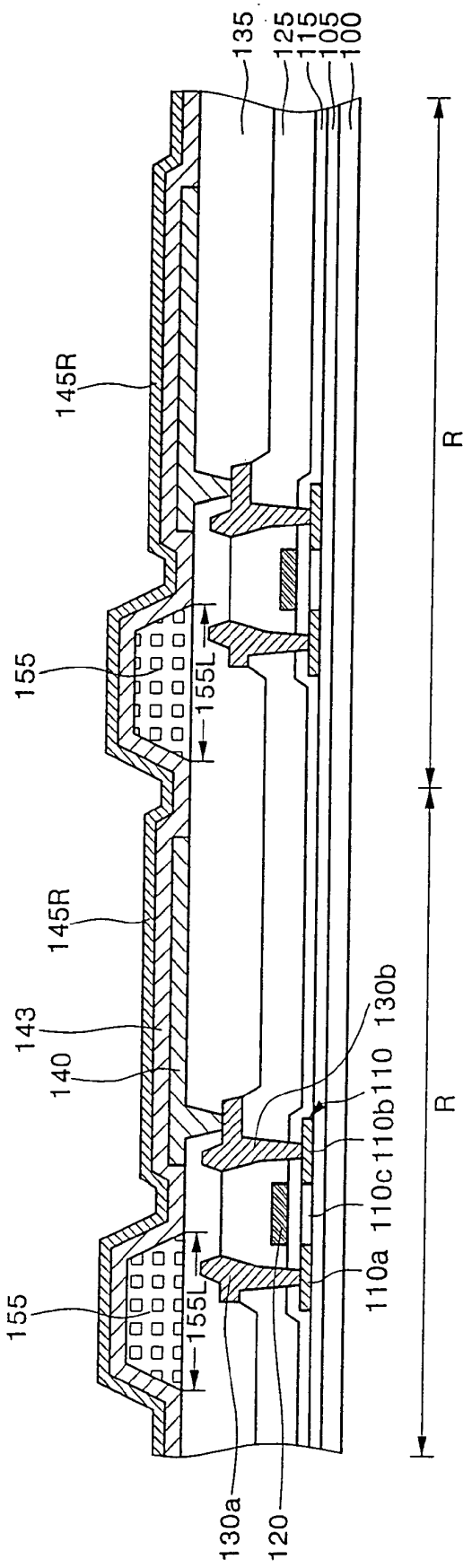


FIG. 11A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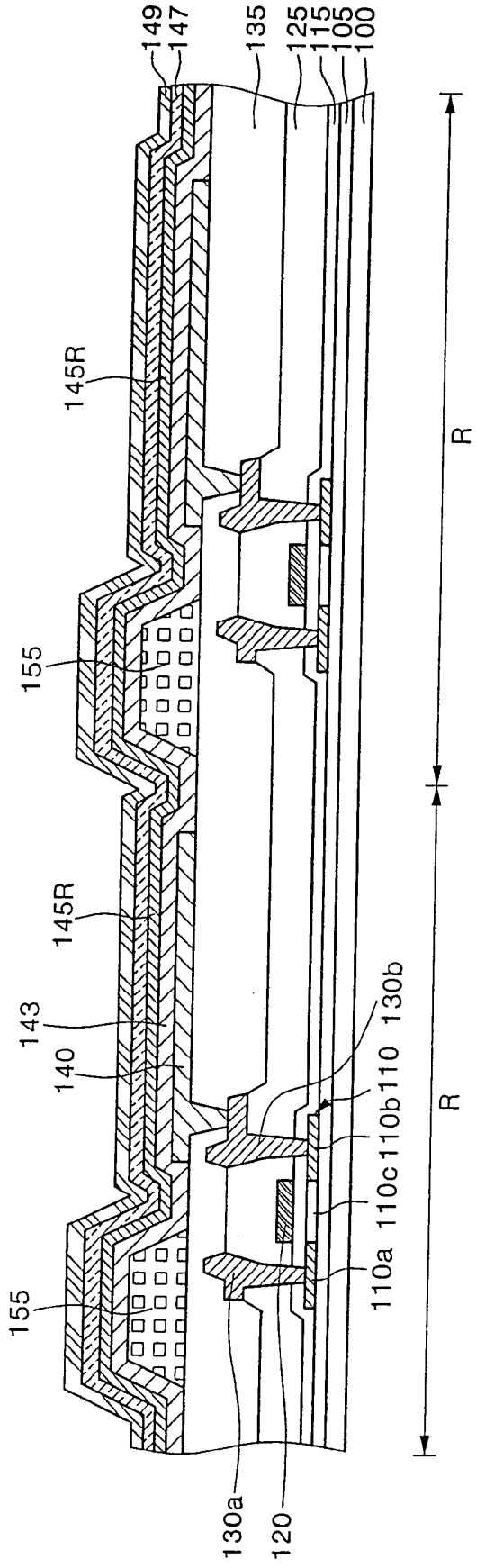
120
R
R

FIG. 11B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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 05 10 4331

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 2002/093286 A1 (OHSHITA ISAMU ET AL) 18 July 2002 (2002-07-18) * page 1, paragraph 12 - paragraph 14 * * page 2, paragraph 25 - page 3, paragraph 34 * * claims 5,6 * * figures 5A-5D * -----	1-11, 14-21	H01L51/40 H01L27/00
X	EP 1 102 317 A (SONY CORPORATION) 23 May 2001 (2001-05-23) * column 2, line 58 - column 3, line 49 * * column 4, line 33 - column 8, line 12 * * column 9, line 11 - line 32 * * figures 1,3 * -----	1,4-6, 9-16,20, 21	
X	US 2002/187265 A1 (MORI TAKAO ET AL) 12 December 2002 (2002-12-12) * page 3, paragraph 49 - paragraph 51 * * page 7, paragraph 109 - paragraph 112 * * figure 14 * -----	1,7, 9-12,16, 20,21	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
X	US 5 742 129 A (NAGAYAMA ET AL) 21 April 1998 (1998-04-21) * the whole document * -----	1,5-9, 11,12, 14-16,19	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	17 August 2005	Welter, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 05 10 4331

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17-08-2005

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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	有机发光显示装置及其制造方法		
公开(公告)号	EP1601033A1	公开(公告)日	2005-11-30
申请号	EP2005104331	申请日	2005-05-23
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星SDI CO.，LTD.		
[标]发明人	LEE KWAN HEE		
发明人	LEE, KWAN-HEE		
IPC分类号	H01L27/32 H05B33/22 H01L51/00 H01L51/50 H01L51/56 H05B33/12 H01L51/40 H01L27/00		
CPC分类号	H01L27/3211 H01L27/3246 H01L51/0011 C02F1/74 C02F3/02 Y02W10/15		
代理机构(译)	hengelhaupt，Jürgen		
优先权	1020040037555 2004-05-25 KR		
其他公开文献	EP1601033B1		
外部链接	Espacenet		

摘要(译)

公开了一种有机发光显示（OLED）器件及其制造方法。该器件可以包括布置在衬底上的单位像素区域。每个单位像素区域可以包括发射区域和非发射区域。像素电极可以至少设置在发射区域中。柱（155）可以设置在发射相同颜色的光的相邻单位像素区域的发射区域之间。柱可以比像素电极向上突出得更多。发射层（145R）可以设置在像素电极上。相对电极可以设置在发射层上。