(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 December 2017 (21.12.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/215229 A1

(51) International Patent Classification:
G09G 3/3225 (2016.01) *G09G 3/3275* (2016.01)

(21) International Application Number:
PCT/CN2016/111468

(22) International Filing Date:
22 December 2016 (22.12.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
201610440604.7 17 June 2016 (17.06.2016) CN

(71) Applicant: **BOE TECHNOLOGY GROUP CO., LTD.** [CN/CN]; No.10 Jiuxianqiao Rd., Chaoyang District, Beijing 100015 (CN).

(72) Inventor: **WU, Zhongyuan**; No.9 Dize Rd., BDA, Beijing 100176 (CN).

(74) Agent: **TEE & HOWE INTELLECTUAL PROPERTY ATTORNEYS**; Yuan CHEN, 10th Floor, Tower D, Minsheng Financial Center, 28 Jianguomennei Avenue, Dongcheng District, Beijing 100005 (CN).

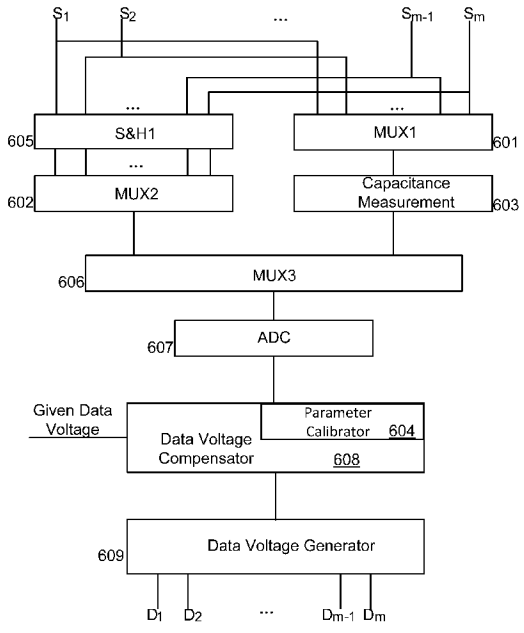
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: CALIBRATION APPARATUS FOR OLED SUB-PIXEL CIRCUIT, SOURCE ELECTRODE DRIVING CIRCUIT, AND DATA VOLTAGE COMPENSATION METHOD

FIG. 6B



(57) Abstract: Disclosed are a calibration apparatus (300) associated with a sub-pixel circuit, a source electrode driving circuit, and a method for compensating data voltage applied to the data line of the sub-pixel circuit associated with a data line and a sense line. The calibration apparatus (300) includes a capacitance measurement circuit (301,603) to output a capacitance measurement voltage (Vout) related to the sense line, a charge sensing circuit (302) to sense a charge voltage on the sense line when the data line is applied with a reference data voltage, and a parameter calibrator (303,604) to calculate parameters of driving transistor (DT) in the sub-pixel circuit based on the capacitance measurement voltage (Vout), the reference data voltage, and the charge voltage, and is configured to determine electrical parameter drifts of the driving transistor (DT) for the source electrode driving circuit to determine a compensation data voltage to compensate non-uniformity of luminance due to the electrical parameter drifts.

WO 2017/215229 A1

CALIBRATION APPARATUS FOR OLED SUB-PIXEL CIRCUIT, SOURCE ELECTRODE DRIVING CIRCUIT, AND DATA VOLTAGE COMPENSATION METHOD

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Chinese Patent Application No. 201610440604.7, filed June 17, 2016, the contents of which are incorporated by reference in the entirety.

TECHNICAL FIELD

[0002] The present invention relates to organic light emission display technology field, and particularly to a calibration apparatus associated with each sub-pixel circuit, a source electrode driving circuit, and a data voltage compensation method used in the organic light emission display equipment.

BACKGROUND

[0003] Organic light emission diode (OLED) has been widely used as a current-source-based light emitter for high performance display equipment. Specifically, in active matrix OLED display, each row of an array of pixels is sequentially turned on by progressively scanning through row-by-row for display. A data voltage is applied to every row of pixels that is turned on, based on which an OLED current is generated to cause the diodes in the row of pixels to emit light for displaying an image controlled by the data voltage.

SUMMARY

[0004] In one aspect, the present invention provides a calibration apparatus associated with a sub-pixel circuit, wherein the sub-pixel circuit comprises a driving transistor having a gate coupled to a data line and a drain coupled to a sense line to drive a light emitter; the calibration apparatus comprises a capacitance measurement circuit coupled to a pulse voltage source, configured to charge the parasitic capacitance based on a pulse voltage provided by the pulse voltage source and to output a capacitance measurement voltage associated with the parasitic capacitance and the pulse voltage; a charge sensing circuit, configured to sense a charge voltage on the sense line in response to a reference data voltage applied to the data line; and a parameter calibrator, configured to calculate electrical parameters of the driving

transistor based on the capacitance measurement voltage, the pulse voltage, the reference data voltage, and the charge voltage.

[0005] Optionally, the charge sensing circuit comprises a conductive wire and is configured to sense a first charge voltage on the sense line in response to a first reference data voltage applied to the data line, and to sense a second charge voltage on the sense line in response to a second reference data voltage applied to the data line; wherein the parameter calibrator calculates electrical parameters of the driving transistor based on the capacitance measurement voltage, the pulse voltage, the first reference data voltage, the first charge voltage, the second reference data voltage, and the second charge voltage.

[0006] Optionally, the electrical parameters include threshold voltage and carrier mobility rate.

[0007] Optionally, the capacitance measurement circuit comprises the pulse voltage source having a first terminal connected to the second power-supply terminal and a second terminal for outputting the pulse voltage; a voltage comparator having a non-inverting input terminal connected to the second terminal of the pulse voltage source, an inverting input terminal connected to the sense line, and an output terminal for outputting the capacitance measurement voltage; and a feedback circuit having a first terminal connected to the output terminal of the voltage comparator and a second terminal connected to the inverting input terminal of the voltage comparator.

[0008] Optionally, the feedback circuit comprises a first resistor and a first capacitor having a first common terminal connected to the inverting input terminal of the voltage comparator and a second common terminal connected to the output terminal of the voltage comparator; wherein a difference between the capacitance measurement voltage and the pulse voltage is proportional to the parasitic capacitance of the sense line, proportional to the pulse voltage, and inversely proportional to a capacitance of the first capacitor when a pulse rate of the pulse voltage is higher than a predetermined threshold frequency.

[0009] In another aspect, the present invention provides a source electrode driving circuit configured to generate a data voltage for each corresponding sub-pixel circuit in a pixel array, wherein the pixel array includes a plurality of sub-pixels, a plurality of first scan lines, a plurality of second scan lines, a plurality of data lines, and a plurality of sense lines, each sub-pixel comprises a sub-pixel circuit including a driving transistor, a first switching transistor, a second switching transistor, and a light emitter, wherein the sense line comprises a parasitic

capacitance; the source electrode driving circuit comprising a first multiplexer configured to select each sense line in the pixel array; a capacitance measurement circuit connected to an output terminal of the first multiplexer, the capacitance measurement circuit comprising a pulse voltage source, the capacitance measurement circuit configured to charge the sense line selected by the first multiplexer based on a pulse voltage generated by the pulse voltage source and configured to output a capacitance measurement voltage associated with the pulse voltage and the parasitic capacitance of the sense line selected by the first multiplexer; a second multiplexer comprises a plurality of input lines configured to select each sense line in the pixel array and an output line configured to output a charge voltage to charge the sense line selected by the second multiplexer; and a parameter calibrator coupled to the output line of the second multiplexer and configured to calculate electrical parameters of the driving transistor in a sub-pixel circuit corresponding to the sense line selected by the second multiplexer based on the capacitance measurement voltage corresponding to the sense line selected by the second multiplexer, and based on a reference data voltage applied to the data line and the charge voltage to charge the sense line selected by the second multiplexer.

[0010] Optionally, the pixel array includes M rows and N columns of pixels, each pixel includes at least one sub-pixel, each row of sub-pixels share a first scan line and a second scan line, and each column of sub-pixels share a data line and a sense line.

[0011] Optionally, the source electrode driving circuit further comprises a third multiplexer configured to select one of the capacitance measurement voltage received from the capacitance measurement circuit to control the source electrode driving circuit to operate in a capacitance measurement mode and the charge voltage received from the second multiplexer to control the source electrode driving circuit to operate in a charge sensing mode.

[0012] Optionally, the source electrode driving circuit further comprises an analog-to-digital convertor connected to an output terminal of the third multiplexer to convert an analog signal associated with either the capacitance measurement voltage or the charge voltage to a digital signal; a data voltage compensator configured to determine a compensation data voltage for each sub-pixel circuit in the pixel array based on a given data voltage applied to the data line of the sub-pixel circuit and the electrical parameters of the driving transistor of the sub-pixel circuit obtained by the parameter calibrator; and a data voltage generator configured to generate and apply the compensation data voltage to the data line connected to the sub-pixel circuit.

[0013] Optionally, the parameter calibrator and the data voltage compensator each comprises a digital signal processor for processing the electrical parameters and the compensation data voltage in digital format.

[0014] Optionally, the data voltage generator comprises a digital-to-analog convertor configured to convert the compensation data voltage in digital format determined by the data voltage compensator to an analog signal and apply the compensation data voltage in analog format to the data line connected to the sub-pixel circuit.

[0015] Optionally, the second multiplexer is configured to output a first charge voltage corresponding to a sense line selected in order by the second multiplexer from a row of sub-pixel circuits selected from the pixel array, each data line connected to the row of sub-pixel circuits being applied with a first reference data voltage; the second multiplexer is further configured to output a second charge voltage corresponding to a sense line selected in order by the second multiplexer from a row of sub-pixel circuits selected from the pixel array, each data line connected to the row of sub-pixel circuits being applied with a second reference data voltage; and the parameter calibrator is configured to determine the electrical parameters of the driving transistor of each sub-pixel circuit in the pixel array based on the capacitance measurement voltage on the sense line connected to the sub-pixel circuit measured by the capacitance measurement circuit, the first reference data voltage applied to the corresponding data line connected to the sub-pixel circuit, the first charge voltage on the corresponding sense line connected to the sub-pixel circuit, the second reference data voltage applied to the corresponding data line, and the second charge voltage on the corresponding sense line, wherein the first reference data voltage and the second reference data voltage are applied to the corresponding data line in different time periods.

[0016] Optionally, the electrical parameters comprise threshold voltage and carrier mobility rate associated with a driving transistor in the sub-pixel circuit.

[0017] Optionally, the capacitance measurement circuit comprises the pulse voltage source having a first terminal being grounded and a second terminal outputting the pulse voltage; a voltage comparator having a non-inverting input terminal connected to the second terminal of the pulse voltage source and an inverting input terminal connected to the sense line and an output terminal outputting the capacitance measurement voltage, and a feedback circuit having a first terminal connected to the output terminal of the voltage comparator and a second terminal connected to the inverting input terminal of the voltage comparator.

[0018] Optionally, the feedback circuit comprises a first resistor and a first capacitor having a first common terminal connected to the inverting input terminal of the voltage comparator and a second common terminal connected to the output terminal of the voltage comparator; and the parameter calibrator is configured to determine the electrical parameters of the driving transistor of the sub-pixel circuit corresponding to the sense line selected by the second multiplexer based on the capacitance measurement voltage measured for the sense line by the capacitance measurement circuit and associated pulse voltage, the capacitance of the first capacitor, the reference data voltage applied to the data line connected to the sub-pixel circuit, and the charge voltage to charge the sense line.

[0019] In another aspect, the present invention provides a method for compensating data voltage applied to each data line of a selected row of sub-pixel circuits driven by a source electrode driving circuit described herein, the method comprising selecting the capacitance measurement voltage received from the capacitance measurement circuit by the third multiplexer to control the source electrode driving circuit to operate in the capacitance measurement mode, , the capacitance measurement voltage being associated with the parasitic capacitance of the sense line selected by the first multiplexer; wherein the first multiplexer sequentially selects each sense line associated with the selected row of sub-pixel circuits; outputting a first reference data voltage in a first period from the digital voltage generator progressively to one data line after another and obtaining a first charge voltage for each sub-pixel circuit read from a currently charged voltage on the corresponding sense line sequentially selected by the second multiplexer for the selected row of sub-pixel circuits from the pixel array; outputting a second reference data voltage in a second period from the digital voltage generator progressively to one data line after another and obtaining a second charge voltage for each sub-pixel circuit read from a currently charged voltage on the corresponding sense line sequentially selected by the second multiplexer for the selected row of sub-pixel circuits from the pixel array; calculating electrical parameters of a driving transistor in each of the selected row of sub-pixel circuits from the pixel array by the parameter calibrator based on the capacitance measurement voltage measured for the corresponding sense line, the first charge voltage and the second charge voltage of each sub-pixel circuit associated with the corresponding sense line obtained respectively in the first time period and the second time period; and determining a compensation data voltage of the sub-pixel circuit by the data voltage compensator based on a given data voltage applied to the corresponding data line of the sub-pixel circuit and the electrical parameters of the driving transistor in the sub-pixel

circuit, generating and applying the compensation data voltage to the data line connected to the sub-pixel circuit.

[0020] Optionally, outputting a first reference data voltage to each data line and obtaining a first charge voltage from each corresponding sense line further comprise connecting the sense line in the pixel array to a reference voltage terminal as the first reference data voltage being progressively outputted to each corresponding data line; disconnecting the sense line being charged by the sub-pixel circuit from the reference voltage terminal; sequentially selecting each sense line by the second multiplexer and reading a charged voltage currently on the sense line as an output; and selecting the output by the third multiplexer during the charge sensing mode and outputting the output as the first charge voltage.

[0021] Optionally, outputting a second reference data voltage to each data line and obtaining a second charge voltage from each corresponding sense line further comprise connecting the sense line in the pixel array to a reference voltage terminal as the second reference data voltage is progressively outputted to each corresponding data line; disconnecting the sense line being charged by the sub-pixel circuit from the reference voltage terminal; sequentially selecting each sense line by the second multiplexer and reading a charged voltage currently on the sense line as an output; and selecting the output by the third multiplexer during the charge sensing mode and outputting the output as the second charge voltage.

[0022] Optionally, determining a compensation data voltage of the sub-pixel circuit comprises processing digital signals associated with the given data voltage applied to the data line of the sub-pixel circuit and corresponding electrical parameters of the driving transistor in the sub-pixel circuit to calculate a digital voltage signal, converting the digital voltage signal to an analog voltage signal by the data voltage generator, outputting the analog voltage signal as a compensation data voltage to the data line of the sub-pixel circuit.

[0023] Optionally, the electrical parameters of the driving transistor include threshold voltage and carrier mobility rate associated with the driving transistor in the sub-pixel circuit.

BRIEF DESCRIPTION OF THE FIGURES

[0024] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present invention.

[0025] FIG. 1 is a sub-pixel circuit associated with a calibration apparatus according to an embodiment of the present invention.

[0026] FIG. 2 is a schematic timing waveform associated with the sub-pixel circuit of FIG. 1 according to an embodiment of the present invention.

[0027] FIG. 3 is a block diagram of a calibration apparatus in a sub-pixel circuit according to an embodiment of the present invention.

[0028] FIG. 4A is a block diagram of a capacitance measurement circuit in the calibration apparatus according to an embodiment of the present invention.

[0029] FIG. 4B is a circuitry diagram of the capacitance measurement circuit according to an embodiment of the present invention.

[0030] FIG. 5 is a schematic diagram of an AMOLED display panel according to an embodiment of the present invention.

[0031] FIG. 6A is a schematic diagram of a source electrode driving circuit according to an embodiment of the present invention.

[0032] FIG. 6B is a schematic diagram of another source electrode driving circuit according to another embodiment of the present invention.

[0033] FIG. 7 is a schematic diagram of a data voltage generator according to an embodiment of the present invention.

[0034] FIG. 8 is a circuitry diagram of a sample-and-hold channel in a sample-and-hold circuit according to an embodiment of the present invention.

[0035] FIG. 9 is a flow chart showing a method for compensating a data voltage from a source electrode driving circuit according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0036] The disclosure will now be described more specifically with reference to the following embodiments. It is to be noted that the following descriptions of some embodiments are presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

[0037] Active matrix OLED display apparatus usually adopt low-temperature poly-silicon (LTPS) thin-film transistor (TFT) or oxide TFT to construct each sub-pixel circuit for providing the OLED current. Comparing to typical amorphous silicon TFT, the LTPS TFT or Oxide TFT is more suitable for the AMOLED display due to its characteristics on a higher carrier mobility rate and superior stability. Because of limitation in crystallization process for manufacturing a plurality of LTPS TFTs on a large glass substrate, several electrical parameters such as threshold voltage and carrier mobility rate are not uniform among the TFTs. If a same data voltage is applied, the non-uniformity in carrier mobility rates or threshold voltages can result in variances of OLED current and luminance which can be perceived by human eyes. Alternatively, for Oxide TFT, its threshold voltage will drift like the amorphous silicon TFT after the data voltage is applied for a substantial long time or during a high-temperature environment even though the manufacturing process for the Oxide TFTs is more uniform over a large area. For different display images, the threshold voltages of different Oxide TFTs in different portions of the AMOLED display panel also drift different amounts. Thus, as a same data voltage is applied, different drifts of threshold voltage in different Oxide TFTs will cause different OLED currents in different sub-pixels, resulting in non-uniform brightness at different parts of the AMOLED display.

[0038] Additionally, in large size AMOLED display application, because of different distances between different sub-pixel circuits relative to data voltage output port of a source electrode driving circuit and resistance of the data line that connects the sub-pixel circuits to the source electrode driving circuit, the actual data voltages at different sub-pixel circuits also vary and are different from the original data voltage provided by the source electrode driving circuit. Similarly, power supply voltages (ARVDD) applied to the different sub-pixel circuits also vary and are different from the original power supply voltage at an output of the power supply source. Given a same data voltage outputted from the source electrode driving circuit, different data voltages and power supply voltages at different sub-pixel circuits also cause different OLED current and luminance at different part of the large size display panel. Therefore, it is desirable to have a source electrode driving circuit including a calibration apparatus to compensate non-uniformity of OLED sub-pixel circuit currents caused by a variety of non-uniformity in AMOLED display devices.

[0039] Accordingly, the present invention provides, *inter alia*, a calibration apparatus associated with each sub-pixel circuit, a source electrode driving circuit, and a data voltage compensation method used in the organic light emission display equipment that substantially

obviate one or more of the problems due to limitations and disadvantages of the related art. In one aspect, the present disclosure provides a calibration apparatus associated with a sub-pixel circuit in an AMOLED display panel, wherein the sub-pixel circuit includes a driving transistor, a first switching transistor, a second switching transistor, and a light emitter, the first switching transistor having a gate connected to a first scan line, a first terminal and a second terminal respectively connected to a data line and a gate of the driving transistor, the second switching transistor having a gate connected to a second scan line, a first terminal and a second terminal respectively connected to a sense line and a second terminal of the driving transistor, the driving transistor also having a first terminal connected to a first power supply terminal, the light emitter having an anode and a cathode respectively connected to the second terminal of the driving transistor and a second power supply terminal, the sense line includes a parasitic capacitance. In some embodiments, the calibration apparatus includes a capacitance measurement circuit coupled to a pulse voltage source, configured to charge the parasitic capacitance based on a pulse voltage provided by the pulse voltage source and to output a capacitance measurement voltage associated with the parasitic capacitance and the pulse voltage; a charge sensing circuit, configured to sense a charge voltage on the sense line in response to a reference data voltage applied to the data line; and a parameter calibrator, configured to calculate electrical parameters of the driving transistor based on the capacitance measurement voltage, the pulse voltage, the reference data voltage, and the charge voltage.

[0040] FIG. 1 is a sub-pixel circuit associated with a calibration device according to an embodiment of the present invention. A calibration device for providing compensation data voltage for overcoming non-uniformity issue is configured to be associated with the sub-pixel circuit of FIG. 1 of an AMOLED display. As shown, the sub-pixel circuit is constructed using N-type TFT transistors, including a driving transistor DT, a first switching transistor T1, a second switching transistor T2, and a light emitter EL.

[0041] Referring to FIG. 1, the first switching transistor T1 has a first terminal connected to a data line DATA. The second switching transistor has a second terminal connected to a gate of the driving transistor DT. The gate of the first switching transistor T1 is connected to a first scan line G1. The driving transistor DT has a first terminal connected to a first power supply terminal ELVDD. Optionally, the ELVDD is a high voltage terminal. The driving transistor DT has a second terminal connected to an anode of the light emitter EL which has a cathode connected to a second power supply terminal ELVSS. Optionally, the ELVSS is a low voltage terminal. Optionally, the ELVSS is grounded. The second switching transistor

T2 has a first terminal connected to the second terminal of the driving transistor DT, and a second terminal connected to a sense line SENSE. The second switching transistor T2 has also a gate connected to a second scan line G2. Referring to FIG. 1, the sense line SENSE includes a parasitic capacitance C_{SENSE} forming a sense-line capacitor.

[0042] FIG. 2 is a schematic timing waveform associated with the sub-pixel circuit of FIG. 1 according to an embodiment of the present invention. The timing waveform shows how the sub-pixel circuit is operated as one unit of an AMOLED display. Referring to FIG. 2, in a first time period t1 (reset time-period), the first scan line G1 is provided with a high voltage level and the second scan line G2 also is provided with a high voltage level. The data line DATA is given by a data voltage V_g. The sense line SENSE is connected to a reference voltage terminal provided with V_{ref}. High voltage level allows the first switching transistor T1 in a conduction state to apply the data voltage V_g to the gate of the driving transistor DT and also allows the second switching transistor T2 in a conduction state to connect the second terminal of the driving transistor DT to the reference voltage terminal. During this first time period t1, a gate-to-source voltage of the driving transistor DT is V_g-V_{ref}. Optionally, the reference voltage terminal can be connected to ELVSS, or grounded, or any other low voltage terminal.

[0043] Referring to FIG. 2, in a second time period t2 (sense time-period), the first scan line G1 is at a low voltage level and the second scan line G2 is at a high voltage level. The sense line SENSE is disconnected from the reference voltage terminal. The first switching transistor T1 is in a blocking state due to low voltage level at G1 and the second switching transistor T2 remains in the conduction state due to high voltage level at G2. At the beginning of t2, gate-to-source voltage of the driving transistor is V_g-V_{ref}. A driving current i_{DT} that passes through the driving transistor DT can be represented by

$$i_{DT} = k(V_g - V_{ref} - V_{th})^2, \quad (1)$$

where V_{th} is threshold voltage of the driving transistor DT and k is coefficient proportional to a carrier mobility rate of the driving transistor. During the second time period t2, the sense-line capacitor is charged by the driving current i_{DT}, which makes the voltage on the sense line (i.e., the voltage at the second terminal of the driving transistor DT) to be $V_{ref} + i_{DT} \times \Delta t/C_{SENSE}$. Assuming that the voltage change on the sense line $i_{DT} \times \Delta t/C_{SENSE}$ is substantially smaller than the data voltage V_g so that the change of driving current i_{DT} is limited to a certain

range, e.g., 0 – 20%. Then, at the end of t2, the voltage on the sense line can be proximately represented by

$$V_{SENSE} = V_{ref} + i_{DT} \times \Delta t / C_{SENSE} = V_{ref} + k(V_g - V_{ref} - V_{th})^2 \times t2 / C_{SENSE}, \quad (2)$$

where t2 is a time span of the second time period.

[0044] Assuming that the parasitic capacitance C_{SENSE} is known, the formula (2) above can be used to determine the drifts of electrical parameters, such as threshold voltage V_{th} and a carrier mobility rate, of the driving transistor DT. However, due to process non-uniformity of the AMOLED display, the parasitic capacitance associated with each sense line is different and has to be determined individually.

[0045] In an embodiment, the parasitic capacitance of a sense line is firstly measured before the electrical parameter drift of the driving transistor in a corresponding sub-pixel circuit connected to the sense line. On the other hand, the measurement of the parasitic capacitance on the sense line does not have to be performed directly to obtain a capacitance value, instead, an alternative electrical parameter that reflects the capacitance value can be measured. For example, a voltage level on the sense-line capacitor can be measured.

[0046] FIG. 3 is a block diagram of a calibration apparatus in a sub-pixel circuit according to an embodiment of the present invention. The calibration apparatus is provided to be associated with the above sub-pixel circuit for providing data voltage compensation to at least partially compensate the e drifts of electrical parameters of the driving transistor in the sub-pixel circuit. Referring to FIG. 3, the calibration apparatus 300 associated with the sub-pixel circuit includes a capacitance measurement circuit 301, a charge sensing circuit 302, and a parameter calibrator 303.

[0047] The capacitance measurement circuit 301 is configured to charge the sense-line capacitor using a pulse voltage provided by a pulse voltage source and to output a capacitance measurement voltage associated with the capacitance of the sense-line capacitor and the pulse voltage.

[0048] The charge sensing circuit 302 is configured to sense a currently charged voltage on the sense-line capacitor under a condition that a reference data voltage is applied to the corresponding data line of a same sub-pixel circuit. Optionally, the charge sensing circuit 302 can be a conductive wire to directly pass the charged voltage from the sense-line capacitor to the parameter calibrator 303.

[0049] The parameter calibrator 303 is configured to calculate electrical parameters of the driving transistor of the sub-pixel circuit based on the capacitance measurement voltage, the pulse voltage, the reference data voltage, and the charge voltage mentioned all above. The electrical parameters of the driving transistor include threshold voltage and carrier mobility rate.

[0050] FIG. 4A is a block diagram of a capacitance measurement circuit in the calibration apparatus according to an embodiment of the present invention. Referring to the FIG. 4A, the capacitance measurement circuit 301 includes a pulse voltage source, a voltage comparator COMP, and a feedback circuit FB. The pulse voltage source has a first terminal connected to ground and a second terminal for outputting a pulse voltage Vin. The voltage comparator COMP has a non-inverting input terminal connected to the second terminal of the pulse voltage source and an inverting input terminal connected to the sense line SENSE. The feedback circuit FB has a first terminal connected to an output terminal of the voltage comparator COMP and a second terminal connected to the inverting input terminal of the voltage comparator COMP.

[0051] In a specific embodiment, as in a circuitry diagram shown in FIG. 4B, the feedback circuit FB includes a first resistor R_f and a first capacitor C_f connected in parallel. A first terminal of the first resistor R_f and a first terminal of the first capacitor C_f are commonly connected to the inverting input terminal of the voltage comparator COMP. A second terminal of the first resistor R_f and a second terminal of the second capacitor C_f are commonly connected to the output terminal of the voltage comparator COMP.

[0052] The configuration of circuitry connection associated with the first resistor R_f, the first capacitor C_f, and the voltage comparator COMP forms a high-pass filter for effectively filtering out low-frequency noise.

[0053] Referring to FIG. 4B, in the circuitry diagram no current passes through the inverting input terminal and the non-inverting input terminal. Thus, the current passing the sense-line capacitor C_{SENSE} is the same as the current passing the feedback circuit FB. The sense-line capacitor C_{SENSE} is charged to a voltage level equal to the pulse voltage Vin. A relationship between the pulse voltage Vin and an output voltage Vout of the voltage comparator COMP can be represented by following formula:

$$Vin \times (j\omega C_{SENSE}) = (Vout - Vin) \times (j\omega R_f C_f + 1) / R_f, \quad (3)$$

$$Vout = Vin(1 + j\omega R_f C_{SENSE} / (j\omega R_f C_f + 1)) \quad (4)$$

Where $j\omega C_{SENSE}$ is impedance of the sense-line capacitor, $\omega=2\pi f$, f is a base frequency of the pulse voltage Vin, and j is Imaginary unit.

[0054] When the base frequency f of the pulse voltage Vin is sufficiently high, for example, higher than a predetermined threshold frequency, the formula (4) can be proximately rewritten into:

$$Vout = Vin(1 + j\omega R_f C_{SENSE} / (j\omega R_f C_f)) = Vin(1 + C_{SENSE} / C_f) \quad (5)$$

This is simplified as:

$$Vout - Vin = Vin \times C_{SENSE} / C_f \quad (6)$$

$$C_{SENSE} = C_f (Vout / Cin - 1) \quad (7)$$

[0055] As seen in the formula (6), when the frequency of the pulse voltage is higher than the threshold frequency, the difference between the capacitance measurement voltage Vout outputted at the output terminal of the voltage comparator COMP and the pulse voltage Vin is proportional to the parasitic capacitance C_{SENSE} of the sense line, proportional to the pulse voltage Vin, and inversely proportional to the capacitance C_f of the first capacitor.

[0056] As seen in the formula (7), when the frequency of the pulse voltage is higher than the threshold frequency, the parasitic capacitance C_{SENSE} can be calculated based on the capacitance value C_f of the first capacitor and a ratio of the capacitance measurement voltage Vout at the output terminal of the voltage comparator COMP and the pulse voltage Vin.

[0057] In some embodiments, after determining the sense-line capacitance C_{SENSE}, the electrical parameters (with corresponding drifts) of the driving transistor DT can be determined using the following relationship as shown in FIG. 1 and FIG. 2:

$$V_{SENSE} = V_{ref} + k(V_g - V_{ref} - V_{th})^2 \times t2 / C_{SENSE} \quad (8)$$

[0058] In a specific embodiment, after determining the value of the sense-line capacitance C_{SENSE}, the charge sensing circuit 302 senses a first charge voltage V_{S1} on the sense line SENSE when the corresponding data line DATA is applied with a first reference data voltage V_{g1}. Further in a different time period, the charge sensing circuit 302 senses a second charge

voltage V_{S2} on the sense line SENSE when the corresponding data line DATA is applied with a second reference data voltage V_{g2}.

[0059] Particularly in the embodiment, referring to FIG. 1 and FIG. 2, in a first time period (a first rest period), the first scan line G1 is at a high voltage level and the second scan line G2 is also at a high voltage level. Data line DATA is applied with V_{g1}. Sense line SENSE is connected to a reference voltage terminal. The first switching transistor T1 in conduction state passes the data voltage V_{g1} to the gate of the driving transistor DT. The second switching transistor T2 in conduction state passes the reference voltage V_{ref} from the sense line SENSE to the second terminal of the driving transistor DT. Thus, the gate-source voltage of the driving transistor DT is V_{g1}-V_{ref}. In a second time period (a first sensing period), the first scan line G1 is at low voltage level and the second scan line G2 is at high voltage level. The sense line SENSE is disconnected from the reference voltage terminal. The first switching transistor T1 is in blocking state and the second switching transistor T2 is in conduction state so that the parasitic sense-line capacitor C_{SENSE} is charged by a voltage passed from the first power supply terminal ELVDD and the driving transistor DT. In a third time period (a first read-out period), the first scan line G1 is at low voltage level and the second scan line G2 is also at the low voltage level. The sense line remains disconnected from the reference voltage terminal. The charge sensing circuit 302 reads out a currently charged voltage (i.e., charge voltage on the sense-line capacitor) as a first charge voltage V_{S1}.

[0060] Referring to FIG. 1 and FIG. 2 again, in a fourth time period (a second reset period, which is substantially the same period of t1 shown in FIG. 2), the first scan line G1 is at high voltage level and the second scan line G2 is also at high voltage level. The data line DATA is given a data voltage V_{g2}. The sense line SENSE is connected to a reference voltage terminal V_{ref}. The first switching transistor T1 in conduction state allows the data voltage V_{g2} to be applied to the gate of the driving transistor DT. The second switching transistor T2 in conduction state allows the reference voltage V_{ref} to be applied to the second terminal of the driving transistor DT, making the gate-source voltage of DT to be V_{g2}-V_{ref}. In a fifth time period (a second sensing period), the first scan line G1 is at low voltage level and the second scan line G2 is at high voltage level. The sense line SENSE is disconnected from the reference voltage terminal. The first switching transistor T1 is in blocking state and the second switching transistor T2 is in conduction state. The sense-line capacitor C_{SENSE} is charged by a voltage passed from the first power supply voltage terminal ELVDD and the driving transistor DT. In a sixth time period (a second read-out period), both the first scan

line G1 and the second scan line G2 are at low voltage level. The sense line SENSE remains disconnected from the reference voltage terminal. The charge sensing circuit 302 reads out currently charged voltage (i.e., charge voltage on the sense-line capacitor) as a first charge voltage V_{S2}.

[0061] Accordingly, the parameter calibrator 303 is able to calculate the electrical parameters of the driving transistor DT based on the capacitance measurement voltage Vout, the pulse voltage Vin, the first reference data voltage V_{g1}, the first charge voltage V_{S1}, the second reference data voltage V_{g2}, the second charge voltage V_{S2}.

[0062] Optionally, the parameter calibrator 303 determines the capacitance value of the sense-line capacitor C_{SENSE} based on the capacitance measurement voltage outputted by the capacitance measurement circuit 301 and the pulse voltage Vin received by the capacitance measurement circuit 301. Then, the parameter calibrator 303 can calculate the electrical parameters of the driving transistor DT using the capacitance of the sense-line capacitor, the first reference data voltage V_{g1}, the first charge voltage V_{S1}, the second reference data voltage V_{g2}, and the second charge voltage V_{S2}. Particularly, electrical parameters like the threshold voltage and carrier mobility rate of the driving transistor DT are obtained.

[0063] Optionally, the fourth time period mentioned above can be set right after the third time period. Optionally, between the fourth time period and the third time period there can be at least one of other time periods mentioned above.

[0064] In an alternative embodiment, after the capacitance measurement voltage Vout is measured or after the sense line capacitance C_{SENSE} is determined, the charge sensing circuit 302 senses a first charge voltage V_{S1} on the sense line SENSE after a sensing time period of t2 under a condition that the corresponding data line DATA is applied with a first reference data voltage V_{g1}. Further, the charge sensing circuit 302 senses a second charge voltage V_{S2} on the sense line SENSE after a sensing time period of (t2+t4) under a condition that the corresponding data line DATA is applied with the first reference data voltage V_{g1}.

[0065] Particularly in the embodiment, referring to FIG. 1 and FIG. 2, in a first time period (a first rest period), the first scan line G1 is at a high voltage level and the second scan line G2 is also at a high voltage level. Data line DATA is applied with V_{g1}. Sense line SENSE is connected to a reference voltage terminal. The first switching transistor T1 in conduction state passes the data voltage V_{g1} to the gate of the driving transistor DT. The second switching transistor T2 in conduction state passes the reference voltage V_{ref} from the sense

line SENSE to the second terminal of the driving transistor DT. Thus, the gate-source voltage of the driving transistor DT is V_{g1}-V_{ref}. In a second time period (a first sensing period), the first scan line G1 is at low voltage level and the second scan line G2 is at high voltage level. The sense line SENSE is disconnected from the reference voltage terminal. The first switching transistor T1 is in blocking state and the second switching transistor T2 is in conduction state so that the parasitic sense-line capacitor C_{SENSE} is charged by a voltage passed from the first power supply terminal ELVDD and the driving transistor DT. In a third time period (a first read-out period), the first scan line G1 is at low voltage level and the second scan line G2 is also at the low voltage level. The sense line remains disconnected from the reference voltage terminal. The charge sensing circuit 302 reads out a currently charged voltage (i.e., charge voltage on the sense-line capacitor) as a first charge voltage V_{S1}.

[0066] Referring to FIG. 1 and FIG. 2 again, in a fourth time period (a second sensing period), the first scan line G1 is at low voltage level and the second scan line G2 is at high voltage level. The sense line SENSE is disconnected from the reference voltage terminal. The first switching transistor T1 is in blocking state and the second switching transistor T2 is in conduction state. Thus, the sense-line capacitor C_{SENSE} is charged by a voltage passed from the first power supply terminal ELVDD and the driving transistor DT. For example, the fourth time period includes a time span of t4 which can be equal to or different from a time span t2 associated the second time period (i.e., the first sensing period mentioned above). In a fifth time period (a second read-out period), the first scan line G1 is at low voltage level and the second scan line G2 is at low voltage level. The sense line SENSE remains disconnected from the reference voltage terminal. The charge sensing circuit 302 reads out a charged voltage on the sense-capacitor as a second charge voltage V_{S2}.

[0067] Accordingly, the parameter calibrator 303 is able to calculate the electrical parameters of the driving transistor DT based on the capacitance measurement voltage Vout (or the capacitance of the sense-line capacitor C_{SENSE}), the first reference data voltage V_{g1}, the time span t2 over the second time period, the first charge voltage V_{S1}, the time span t4 over the fourth time period, and the second charge voltage V_{S2}. For example, the threshold voltage and the carrier mobility rate of the driving transistor DT are obtained.

[0068] FIG. 5 is a schematic diagram of an AMOLED display panel according to an embodiment of the present invention. Referring to FIG. 5, the AMOLED display panel includes a pixel array having M rows and N columns of pixels. Each pixel includes at least

one sub-pixel. Each row of sub-pixels shares a first scan line and a second scan line. Each column of sub-pixels shares a data line and a sense line.

[0069] As an example, assuming each pixel includes three sub-pixels, there are *n* numbers of source electrode driving circuits for providing data voltages to the pixel array of the AMOLED display panel. Each source electrode driving circuit includes *m* data lines and *m* sense lines. Here $3N = m \times n$. *m* and *n* are integers greater than 1. In the following sections of the specification, only one source electrode driving circuit, i.e., $n=1$, is selected to provide data voltages for the pixel array of the display panel. Of course, the invention is not limited by this selection.

[0070] FIG. 6A is a schematic diagram of a source electrode driving circuit according to an embodiment of the present invention. Referring to FIG. 6A, the source electrode driving circuit includes a first multiplexer (MUX1) 601, a second multiplexer (MUX2) 602, a capacitance measurement circuit 603, and a parameter calibrator 604.

[0071] The first multiplexer 601 has *m* selective input ports respectively connected to *m* sense lines and is configured to progressively select each sense line in the pixel array, such as S1, S2, …, Sm-1, and Sm.

[0072] The capacitance measurement circuit 603 is connected to an output port of the first multiplexer 601 and connects a pulse voltage source to use a pulse voltage to charge any one sense line selected by the first multiplexer 601 and output a capacitance measurement voltage associated with the pulse voltage and the capacitance value of the sense line selected by the selected by the first multiplexer 601. The capacitance measurement circuit 603 can be substantially the same as the capacitance measurement circuit 301 as shown in FIG. 3.

[0073] For any sense line selected by the first multiplexer 601, the parameter calibrator 604 can determine a capacitance value of the sense-line capacitor associated with the selected sense line based on the capacitance measurement voltage and the pulse voltage. In particular, as ahown in FIG. 4B, the parameter calibrator 604 can determine the capacitance value of the sense-line capacitor based on the capacitance measurement voltage Vout on the selected sense line, the pulse voltage Vin, and the feedback capacitor C_f.

[0074] The second multiplexer (MUX2) 602 has *m* selective input ports respectively connected to *m* sense lines. MUX2 is configured to progressively select each sense line of S1, S2, …, Sm-1, and Sm in the pixel array and output a charge voltage on the selected sense line.

[0075] The parameter calibrator 604 also connects an output port of the MUX2. For each sense line selected by the MUX2, the parameter calibrator 604 can calculate electrical parameters of the driving transistor of a currently selected sub-pixel circuit associated with the currently selected sense line. The calculation is based on the capacitance measurement voltage (or the sense-line capacitance) of the selected sense line, a reference data voltage applied to the corresponding data line (associated with the same selected sub-pixel circuit), and the charge voltage on the selected sense line by MUX2. For example, electrical parameters like threshold voltage and carrier mobility rate of the driving transistor are obtained.

[0076] FIG. 6B is a schematic diagram of another source electrode driving circuit according to another embodiment of the present invention. The source electrode driving circuit also includes a third multiplexer (MUX3) 606, an analog-to-digital converter (ADC) 607, a data voltage compensator 608, and a data voltage generator 609. Two selective inputs of MUX3 606 respectively are connected to an output of the MUX2 602 and an output of the capacitance measurement circuit 603. The MUX3 606 is configured to select either a charge voltage outputted by the MUX2 602 to control the source electrode driving circuit to operate in a charge sensing mode or a capacitance measurement voltage outputted by the capacitance measurement circuit 603 to control the source electrode driving circuit to operate in a capacitance measurement mode. Two selective inputs of MUX3 606 respectively are connected to an output of the MUX2 602 and an output of the capacitance measurement circuit 603. During the capacitance measurement mode, an output of the MUX3 606 outputs the capacitance measurement voltage outputted by the capacitance measurement circuit 603. During the charge sensing mode, the output of MUX3 606 outputs the charge voltage outputted by the MUX2 602.

[0077] The analog-to-digital converter 607 has an input terminal connected to the output of the MUX3 to convert analog signals received at the output of MUX3 606 into digital signals. Particularly, when the MUX3 606 selects the capacitance measurement voltage from the output of the capacitance measurement circuit with the source electrode driving circuit in a capacitance measurement mode, the analog-to-digital converter 607 receives a capacitance measurement voltage from the MUX 606 which is outputted from the capacitance measurement circuit 603 and converts this capacitance measurement voltage into a signal in digital format. When the MUX3 606 selects the charge voltage from the output of the second multiplexer with the source electrode driving circuit in a charge sensing mode, the ADC 607

receives a charge voltage from the MUX 606 which is outputted from the MUX2 602 and converts this charge voltage into a digital signal.

[0078] For each sub-pixel circuit in the pixel array of the AMOLED display panel, the data voltage compensator 608 is configured to calculate a compensation data voltage associated with the sub-pixel circuit based on a given data voltage on the data line and relevant electrical parameters of the corresponding driving transistor of the sub-pixel circuit determined by the parameter calibrator 604. The parameter calibrator 604 and the data voltage compensator 608 are respectively configured using digital signal processors. Thus, the data voltage compensator 608 is able to output a compensation data voltage as an output signal in digital format.

[0079] Referring to FIG. 6B, the data voltage generator 609 has *m* output terminals respectively connected to m data lines D1, D2, …, Dm-1, and Dm to output corresponding data voltages. For each sub-pixel circuit in the pixel array, the data voltage generator 609 is configured to generate a compensation data voltage based on the compensation data voltage calculated by the data voltage compensator 608, and further apply the compensation data voltage to the corresponding data line connected to the sub-pixel circuit.

[0080] Next, a single sub-pixel circuit is used as an example to describe operations of the parameter calibrator 604 for handling digital signal format. The ADC 607 converts an input analog voltage into an n-bit digital signal. Particularly, the ADC 607 has a conversion base voltage Vbase. When the input analog voltage equals to the Vbase, the n-bits of the digital signal outputted by the ADC 607 are all 1. For a capacitance measurement voltage Vout, the ADC 607 converts the inputted capacitance measurement voltage Vout into an n-bit digital signal Evc. Thus, a relationship between the capacitance measurement voltage Vout and the digital signal Evc can be represented by the following formula:

$$Vout = Vbase \times Evc / 2^n \tag{9}$$

Correspondingly, formula (7) can rewritten as:

$$C_{SENSE} = C_f (Vbase / Vin \times Evc / 2^n - 1) \tag{10}$$

On the other hand, for the charge voltage V_{SENSE} on the sense-line capacitor, the ADC 607 converts the inputted charge voltage V_{SENSE} to an n-bit digital signal Evs. Thus, a

relationship between the charge voltage V_{SENSE} and the digital signal Evs can be represented by the following formula:

$$V_{SENSE} = Vbase \times Evs / 2^n \tag{11}$$

Combining the formulas (11) and (2),

$$Vbase \times Evs / 2^n = V_{ref} + k(V_g - V_{ref} - V_{th})^2 \times t2 / C_{SENSE}$$

$$Evs = (V_{ref} + k(V_g - V_{ref} - V_{th})^2 \times t2 / C_{SENSE}) / Vbase \times 2^n \tag{12}$$

For simplifying the equation above, the reference voltage V_{ref} is assumed to be 0, the following formula is obtained:

$$Evs = 2^n \times k(V_g - V_{th})^2 \times t2 / (C_{SENSE} \times Vbase) \tag{13}$$

Substituting the formula (10) into the formula (13),

$$\begin{aligned} k(V_g - V_{th})^2 &= ((Evs \times Vbase) / (2^n \times t2)) \times (C_f \times Vbase / Vin \times Evc / 2^n - 1)) \\ &= Evs \times (Vbase / (2^n \times t2)) \times (C_f \times Vbase / (Vin \times 2^n) \times Evc - 1)) \\ &= Evs \times k1 \times (k2 \times Evc - 1) \end{aligned} \tag{14}$$

where $k1 = Vbase / (2^n \times t2)$, $k2 = C_f \times Vbase / (Vin \times 2^n)$. For a specific capacitance measurement circuit 603, a sub-pixel circuit, and an ADC 607, *k1* and *k2* are constants.

[0081] As describe in earlier sections of the specification, under a condition that the first reference data voltage V_{g1} is applied to the data line, the charge sensing circuit 302 senses a first charge voltage V_{SESNE1} on the corresponding sense line. Similarly, under another condition that the first reference data voltage V_{g2} is applied to the data line, the charge sensing circuit 302 senses a first charge voltage V_{SESNE2} on the corresponding sense line. Therefore, one can deduce the following equations:

$$\begin{aligned} k(V_{g1} - V_{th})^2 &= Evs1 \times k1 \times (k2 \times Evc - 1) \\ k(V_{g2} - V_{th})^2 &= Evs2 \times k1 \times (k2 \times Evc - 1) \end{aligned} \tag{15}$$

For each sense line in the pixel array, after the ADC 607 converts the capacitance measurement voltage generated by the capacitance measurement circuit 603 into a digital signal Evc, it can store the digital signal Evc only and no need to calculate the capacitance associated with the sense line based on the digital signal Evc. Additionally, for each sub-

pixel circuit, after obtaining digital signals Evs1 and Evs2 respectively corresponding to a first charge voltage and a second charge voltage, the parameter calibrator 604 can directly calculate relevant electrical parameters of the corresponding driving transistor of the sub-pixel circuit based on the digital signal Evc associated with the sense line corresponding to the sub-pixel circuit, and the digital signals Evs1 and Evs2. For example, threshold voltage and carrier mobility rate of the driving transistor can be calculated using the above method.

[0082] Further referring to FIG. 6B, the source electrode driving circuit also includes a first sample-and-hold circuit (S&H1) 605 having *m* sample-&-hold channels. Each sample-&-hold channel has an input and an output. The S&H1 605 has *m* inputs respectively connected to *m* sense lines S1, S2,..., Sm-1, and Sm, and *m* outputs respectively connected to *m* selective input ports of the second multiplexer MUX2.

[0083] In some embodiments, the parameter calibrator 303 in FIG. 3 can include the analog-to-digital converter 607 and parameter calibrator 604 in FIG. 6B. In some embodiments, the charge sensing circuit 302 in FIG. 3 can include one channel of the sample-and-hold circuit 605, one selective channel of the second multiplexer MUX2 602, and one selective channel of the third multiplexer MUX3 606 in FIG. 6B.

[0084] FIG. 7 is a schematic diagram of a data voltage generator according to an embodiment of the present invention. Referring to FIG. 7, the data voltage generator 609 includes a digital-to-analog converter (DAC) 701, a fourth multiplexer (MUX4) 702, and a second sample-and-hold circuit (S&H2) 703. For each sub-pixel circuit in the pixel array, the DAC 701 is configured to convert the compensation data voltage outputted from the data voltage compensator 608 for the sub-pixel circuit from a digital signal into an analog signal. The fourth multiplexer MUX4 702 has an input connected to an output of the DAC 701 and *m* selective output ports. The MUX4 702 selects one of *m* output ports to output the analog signal received from the DAC 701. The S&H2 circuit 703 includes *m* sample-and-hold channels. Each sample-and-hold channel has an input and an output. The *m* inputs of the S&H2 circuit 703 respectively connect to *m* selective output ports of the MUX4 702. The *m* outputs of the S&H2 circuit 703 respectively connect to *m* data lines of the pixel array.

[0085] For each sample-and-hold channel of the S&H2 circuit 702, when a selective output port of the MUX4 702 connected to the input of the sample-and-hold channel is selected, the input of the sample-and-hold channel receives a compensation data voltage in an analog

signal format outputted from the DAC 701 and performs a sampling process to maintain the sampled compensation data voltage thereof.

[0086] FIG. 8 is a circuitry diagram of a sample-and-hold channel in a sample-and-hold circuit according to an embodiment of the present invention. Referring to FIG. 8, a sample-and-hold channel includes an input terminal *in*, a sampling switch SW1, a maintaining capacitor C, an output switch SW2, and an output terminal *out*. FIG 8 is just a simplified example of the sample-and-hold channel though the present invention is not limited thereof.

[0087] FIG. 9 is a flow chart showing a method for compensating a data voltage from a source electrode driving circuit according to an embodiment of the present invention. In some embodiments, the method is implemented based on the source electrode driving circuit as shown in FIG. 6A and FIG. 6B. Optionally, in a capacitance measurement period, the MUX3 606 (of FIG. 6B) select an output from the capacitance measurement circuit as the source electrode driving circuit is set in a capacitance measurement mode. The MUX1 601 progressively selects each sense line in the pixel array. For each sense line selected by the MUX1 601, the capacitance measurement circuit 603 outputs a capacitance measurement voltage associated with the sense-line capacitance and a pulse voltage provided by a pulse voltage source thereof. Therefore, in this period, a corresponding capacitance measurement voltage associated with respective sense line in the pixel array is obtained. A specific operation can be referred to FIG 4B, in which each sense line is disconnected from the reference voltage terminal and the second switching transistor in each sub-pixel circuit is in blocking state.

[0088] Referring to FIG. 9, in a first charge voltage sensing period, each row of sub-pixel circuits in the pixel array is selected one-after-another. For each currently selected row of sub-pixel circuits, in a first time period, the MUX3 606 is not operated so that all sense lines in the pixel array are connected to respective reference voltage terminals. The data voltage generator 609 progressively outputs a first reference data voltage to each data line of the pixel array. Then in a second time period, the MUX3 606 is not operated as each sense line is disconnected from respective reference voltage terminals. Accordingly, each sense line (with a parasitic capacitor) is charged by the corresponding sub-pixel circuit within the selected row of the sub-pixel circuits. Subsequently in a third time period, the MUX3 606 is operated to select a charge voltage from the output of the MUX2 602 as the source electrode driving circuit is set in a charge sensing mode. The MUX2 602 progressively selects each sense line

in the pixel array so that a first charge voltage corresponding to each sub-pixel circuit of the currently selected row of sub-pixel circuits can be read out. A specific operation of the second time period can be referred to FIG. 2 above. Optionally, in the first charge voltage sensing period, the method including progressively select each row of sub-pixel circuits in the pixel array, and performing operations as mentioned above respectively in the first time period, the second time period, and the third time period for each selected row of sub-pixel circuits.

[0089] In an example, the operation includes, in the first time period, setting the first scan line G1 to high voltage level, setting the second scan line G2 to high voltage level; in the second time period, setting the first scan line G1 to low voltage level and the second scan line G2 to high voltage level; and in the third time period, setting both the first scan line G1 and the second scan line G2 to low voltage level.

[0090] Referring to FIG. 9, in a second charge voltage sensing period, each row of sub-pixel circuits in the pixel array is sequentially selected. For a currently selected row of sub-pixel circuits, the method includes performing operations in a first time period, a second time period, and a third time periods substantially the same as that in the first charge voltage sensing period, except that some different operations are done. The different operation includes, in the first time period, outputting a second reference data voltage by the data voltage generator 609 progressively to each data line; and in the third time period, sequentially reading out a second charge voltage corresponding to each sub-pixel circuit in the selected row of sub-pixel circuits. Specific operations during the second charge voltage sensing period can be referred to FIG. 2.

[0091] Referring to FIG. 9 again, in a parameter calibration period, the parameter calibrator 604 is operated to calculate electrical parameters of driving transistor in each sub-pixel circuit (or the selected row) based on the capacitance measurement voltage for each corresponding sense line obtained in the capacitance measurement period, the first charge voltage of each sub-pixel circuit obtained in the first charge voltage sensing period, and the second charge voltage of each sub-pixel circuit obtained in the second charge voltage sensing period. For example, threshold voltage and carrier mobility rate of driving transistor are calculated. Specific operations in this period can be referred to FIG. 6B.

[0092] In some embodiments, the method includes executing all the operations in the capacitance measurement period, in the first charge voltage sensing period, in the second

charge voltage sensing period, and in the parameter calibration period on a regular basis on the pixel array of the AMOLED display. For example, the method includes executing the operations once every half year, or once every year, or every time when the AMOLED display is starting its operation.

[0093] In some embodiments, the method includes storing the electrical parameters of driving transistor for each sub-pixel circuit in the pixel array. In some embodiments, the capacitance measurement period is not necessary before the first charge voltage sensing period and the second charge voltage sensing period, but can be between the first charge voltage sensing period and the second charge voltage sensing period, or can be after the first charge voltage sensing period and the second charge voltage sensing period.

[0094] Referring to FIG. 9, in a data voltage compensation period, each row of sub-pixel circuits in the pixel array is sequentially selected. For each sub-pixel circuit in a selected row of sub-pixel circuits, the data voltage compensator 608 is operated to calculate a compensation data voltage of the sub-pixel circuit based on a given data voltage to the sub-pixel circuit and the corresponding electrical parameters of the sub-pixel circuit obtained in the parameter calibration period. Further, the compensation data voltage in analog signal format is generated and outputted to the corresponding data line of the sub-pixel circuit. Specific operations associated with the data voltage compensation period can be referred to FIG. 7.

[0095] Based on the calibration apparatus associated with each sub-pixel circuit, the source electrode driving circuit, and the data voltage compensation method provided by the present invention, by measuring the capacitance voltage of the sense line and sensing the charge voltage on the sense-line capacitor under a condition that a reference data voltage is applied to the corresponding data line, relevant electrical parameters and their drifts of driving transistor of each selected sub-pixel circuit can be determined. Further, the data voltage applied to the data line can be adjusted based on the as-determined drifts of the electrical parameters of the driving transistor to make a compensation to the non-uniformity in pixel luminance due to the drifts of the electrical parameters among different sub-pixel circuits.

[0096] The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously,

many modifications and variations will be apparent to practitioners skilled in this art. The embodiments are chosen and described in order to explain the principles of the invention and its best mode practical application, thereby to enable persons skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. Therefore, the term "the invention", "the present invention" or the like does not necessarily limit the claim scope to a specific embodiment, and the reference to exemplary embodiments of the invention does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is limited only by the spirit and scope of the appended claims. Moreover, these claims may refer to use "first", "second", etc. following with noun or element. Such terms should be understood as a nomenclature and should not be construed as giving the limitation on the number of the elements modified by such nomenclature unless specific number has been given. Any advantages and benefits described may not apply to all embodiments of the invention. It should be appreciated that variations may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element and component in the present disclosure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.

WHAT IS CLAIMED IS:

1. A calibration apparatus associated with a sub-pixel circuit, wherein the sub-pixel circuit comprises a driving transistor having a gate coupled to a data line and a drain coupled to a sense line to drive a light emitter; the calibration apparatus comprises:

a capacitance measurement circuit coupled to a pulse voltage source, configured to charge the parasitic capacitance based on a pulse voltage provided by the pulse voltage source and to output a capacitance measurement voltage associated with the parasitic capacitance and the pulse voltage;

a charge sensing circuit, configured to sense a charge voltage on the sense line in response to a reference data voltage applied to the data line; and

a parameter calibrator, configured to calculate electrical parameters of the driving transistor based on the capacitance measurement voltage, the pulse voltage, the reference data voltage, and the charge voltage.

2. The calibration apparatus of claim 1, wherein the charge sensing circuit comprises a conductive wire and is configured to sense a first charge voltage on the sense line in response to a first reference data voltage applied to the data line, and to sense a second charge voltage on the sense line in response to a second reference data voltage applied to the data line; wherein the parameter calibrator calculates electrical parameters of the driving transistor based on the capacitance measurement voltage, the pulse voltage, the first reference data voltage, the first charge voltage, the second reference data voltage, and the second charge voltage.

3. The calibration apparatus of claim 1, wherein the electrical parameters include threshold voltage and carrier mobility rate.

4. The calibration apparatus of claim 2, wherein the capacitance measurement circuit comprises:

the pulse voltage source having a first terminal connected to the second power-supply terminal and a second terminal for outputting the pulse voltage;

a voltage comparator having a non-inverting input terminal connected to the second terminal of the pulse voltage source, an inverting input terminal connected to the sense line, and an output terminal for outputting the capacitance measurement voltage; and

a feedback circuit having a first terminal connected to the output terminal of the voltage comparator and a second terminal connected to the inverting input terminal of the voltage comparator.

5. The calibration apparatus of claim 4, wherein the feedback circuit comprises a first resistor and a first capacitor having a first common terminal connected to the inverting input terminal of the voltage comparator and a second common terminal connected to the output terminal of the voltage comparator;

wherein a difference between the capacitance measurement voltage and the pulse voltage is proportional to the parasitic capacitance of the sense line, proportional to the pulse voltage, and inversely proportional to a capacitance of the first capacitor when a pulse rate of the pulse voltage is higher than a predetermined threshold frequency.

6. A source electrode driving circuit configured to generate a data voltage for each corresponding sub-pixel circuit in a pixel array, wherein the pixel array includes a plurality of sub-pixels, a plurality of first scan lines, a plurality of second scan lines, a plurality of data lines, and a plurality of sense lines, each sub-pixel comprises a sub-pixel circuit including a driving transistor, a first switching transistor, a second switching transistor, and a light emitter, wherein the sense line comprises a parasitic capacitance; the source electrode driving circuit comprising:

a first multiplexer configured to select each sense line in the pixel array;

a capacitance measurement circuit connected to an output terminal of the first multiplexer, the capacitance measurement circuit comprising a pulse voltage source, the capacitance measurement circuit configured to charge the sense line selected by the first multiplexer based on a pulse voltage generated by the pulse voltage source and configured to output a capacitance measurement voltage associated with the pulse voltage and the parasitic capacitance of the sense line selected by the first multiplexer;

a second multiplexer comprises a plurality of input lines configured to select each sense line in the pixel array and an output line configured to output a charge voltage to charge the sense line selected by the second multiplexer; and

a parameter calibrator coupled to the output line of the second multiplexer and configured to calculate electrical parameters of the driving transistor in a sub-pixel circuit corresponding to the sense line selected by the second multiplexer based on the capacitance measurement voltage corresponding to the sense line selected by the second multiplexer, and

based on a reference data voltage applied to the data line and the charge voltage to charge the sense line selected by the second multiplexer.

7. The source electrode driving circuit of claim 6, wherein the pixel array includes M rows and N columns of pixels, each pixel includes at least one sub-pixel, each row of sub-pixels share a first scan line and a second scan line, and each column of sub-pixels share a data line and a sense line.

8. The source electrode driving circuit of claim 6, further comprising a third multiplexer configured to select one of the capacitance measurement voltage received from the capacitance measurement circuit to control the source electrode driving circuit to operate in a capacitance measurement mode and the charge voltage received from the second multiplexer to control the source electrode driving circuit to operate in a charge sensing mode.

9. The source electrode driving circuit of claim 8, further comprising:

an analog-to-digital convertor connected to an output terminal of the third multiplexer to convert an analog signal associated with either the capacitance measurement voltage or the charge voltage to a digital signal;

a data voltage compensator configured to determine a compensation data voltage for each sub-pixel circuit in the pixel array based on a given data voltage applied to the data line of the sub-pixel circuit and the electrical parameters of the driving transistor of the sub-pixel circuit obtained by the parameter calibrator; and

a data voltage generator configured to generate and apply the compensation data voltage to the data line connected to the sub-pixel circuit.

10. The source electrode driving circuit of claim 9, wherein the parameter calibrator and the data voltage compensator each comprises a digital signal processor for processing the electrical parameters and the compensation data voltage in digital format.

11. The source electrode driving circuit of claim 9, wherein the data voltage generator comprises a digital-to-analog convertor configured to convert the compensation data voltage in digital format determined by the data voltage compensator to an analog signal and apply the compensation data voltage in analog format to the data line connected to the sub-pixel circuit.

12. The source electrode driving circuit of claim 11, wherein the second multiplexer is configured to output a first charge voltage corresponding to a sense line selected in order by the second multiplexer from a row of sub-pixel circuits selected from the pixel array, each data line connected to the row of sub-pixel circuits being applied with a first reference data voltage;

the second multiplexer is further configured to output a second charge voltage corresponding to a sense line selected in order by the second multiplexer from a row of sub-pixel circuits selected from the pixel array, each data line connected to the row of sub-pixel circuits being applied with a second reference data voltage; and

the parameter calibrator is configured to determine the electrical parameters of the driving transistor of each sub-pixel circuit in the pixel array based on the capacitance measurement voltage on the sense line connected to the sub-pixel circuit measured by the capacitance measurement circuit, the first reference data voltage applied to the corresponding data line connected to the sub-pixel circuit, the first charge voltage on the corresponding sense line connected to the sub-pixel circuit, the second reference data voltage applied to the corresponding data line, and the second charge voltage on the corresponding sense line, wherein the first reference data voltage and the second reference data voltage are applied to the corresponding data line in different time periods.

13. The source electrode driving circuit of claim 6, wherein the electrical parameters comprise threshold voltage and carrier mobility rate associated with a driving transistor in the sub-pixel circuit.

14. The source electrode driving circuit of claim 6, wherein the capacitance measurement circuit comprises:

the pulse voltage source having a first terminal being grounded and a second terminal outputting the pulse voltage;

a voltage comparator having a non-inverting input terminal connected to the second terminal of the pulse voltage source and an inverting input terminal connected to the sense line and an output terminal outputting the capacitance measurement voltage, and

a feedback circuit having a first terminal connected to the output terminal of the voltage comparator and a second terminal connected to the inverting input terminal of the voltage comparator.

15. The source electrode driving circuit of claim 14, wherein the feedback circuit comprises a first resistor and a first capacitor having a first common terminal connected to the inverting input terminal of the voltage comparator and a second common terminal connected to the output terminal of the voltage comparator; and

the parameter calibrator is configured to determine the electrical parameters of the driving transistor of the sub-pixel circuit corresponding to the sense line selected by the second multiplexer based on the capacitance measurement voltage measured for the sense line by the capacitance measurement circuit and associated pulse voltage, the capacitance of the first capacitor, the reference data voltage applied to the data line connected to the sub-pixel circuit, and the charge voltage to charge the sense line.

16. A method for compensating data voltage applied to each data line of a selected row of sub-pixel circuits driven by a source electrode driving circuit of claim 9, the method comprising:

selecting the capacitance measurement voltage received from the capacitance measurement circuit by the third multiplexer to control the source electrode driving circuit to operate in the capacitance measurement mode, , the capacitance measurement voltage being associated with the parasitic capacitance of the sense line selected by the first multiplexer; wherein the first multiplexer sequentially selects each sense line associated with the selected row of sub-pixel circuits;

outputting a first reference data voltage in a first period from the digital voltage generator progressively to one data line after another and obtaining a first charge voltage for each sub-pixel circuit read from a currently charged voltage on the corresponding sense line sequentially selected by the second multiplexer for the selected row of sub-pixel circuits from the pixel array;

outputting a second reference data voltage in a second period from the digital voltage generator progressively to one data line after another and obtaining a second charge voltage for each sub-pixel circuit read from a currently charged voltage on the corresponding sense line sequentially selected by the second multiplexer for the selected row of sub-pixel circuits from the pixel array;

calculating electrical parameters of a driving transistor in each of the selected row of sub-pixel circuits from the pixel array by the parameter calibrator based on the capacitance measurement voltage measured for the corresponding sense line, the first charge voltage and the second charge voltage of each sub-pixel circuit associated with the

corresponding sense line obtained respectively in the first time period and the second time period; and

determining a compensation data voltage of the sub-pixel circuit by the data voltage compensator based on a given data voltage applied to the corresponding data line of the sub-pixel circuit and the electrical parameters of the driving transistor in the sub-pixel circuit, generating and applying the compensation data voltage to the data line connected to the sub-pixel circuit.

17. The method of claim 16, wherein outputting a first reference data voltage to each data line and obtaining a first charge voltage from each corresponding sense line further comprise:

connecting the sense line in the pixel array to a reference voltage terminal as the first reference data voltage being progressively outputted to each corresponding data line;

disconnecting the sense line being charged by the sub-pixel circuit from the reference voltage terminal;

sequentially selecting each sense line by the second multiplexer and reading a charged voltage currently on the sense line as an output; and

selecting the output by the third multiplexer during the charge sensing mode and outputting the output as the first charge voltage.

18. The method of claim 16, wherein outputting a second reference data voltage to each data line and obtaining a second charge voltage from each corresponding sense line further comprise:

connecting the sense line in the pixel array to a reference voltage terminal as the second reference data voltage is progressively outputted to each corresponding data line;

disconnecting the sense line being charged by the sub-pixel circuit from the reference voltage terminal;

sequentially selecting each sense line by the second multiplexer and reading a charged voltage currently on the sense line as an output; and

selecting the output by the third multiplexer during the charge sensing mode and outputting the output as the second charge voltage.

19. The method of claim 16, wherein determining a compensation data voltage of the sub-pixel circuit comprises processing digital signals associated with the given data voltage applied to the data line of the sub-pixel circuit and corresponding electrical

parameters of the driving transistor in the sub-pixel circuit to calculate a digital voltage signal, converting the digital voltage signal to an analog voltage signal by the data voltage generator, outputting the analog voltage signal as a compensation data voltage to the data line of the sub-pixel circuit.

20. The method of claim 16, wherein the electrical parameters of the driving transistor include threshold voltage and carrier mobility rate associated with the driving transistor in the sub-pixel circuit.

FIG. 1

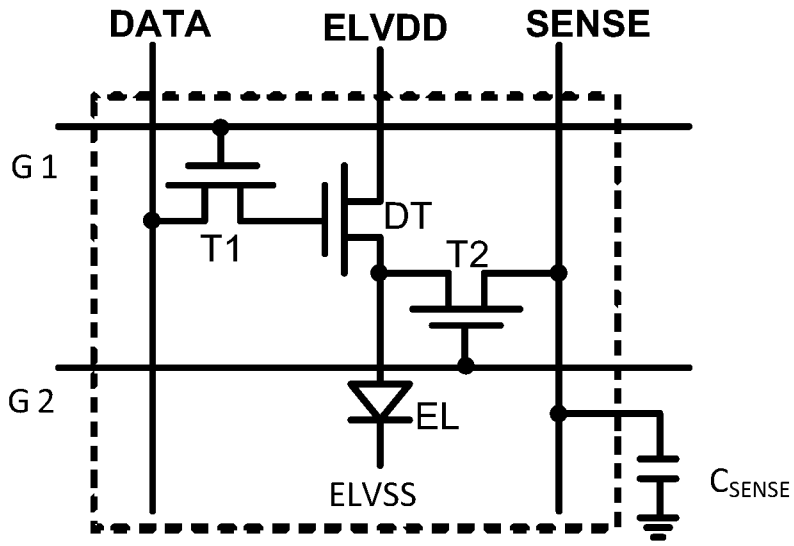

DATA
ELVDD
SENSE
G 1
T1
DT
T2
G 2
EL
ELVSS
C_{SENSE}

FIG. 2

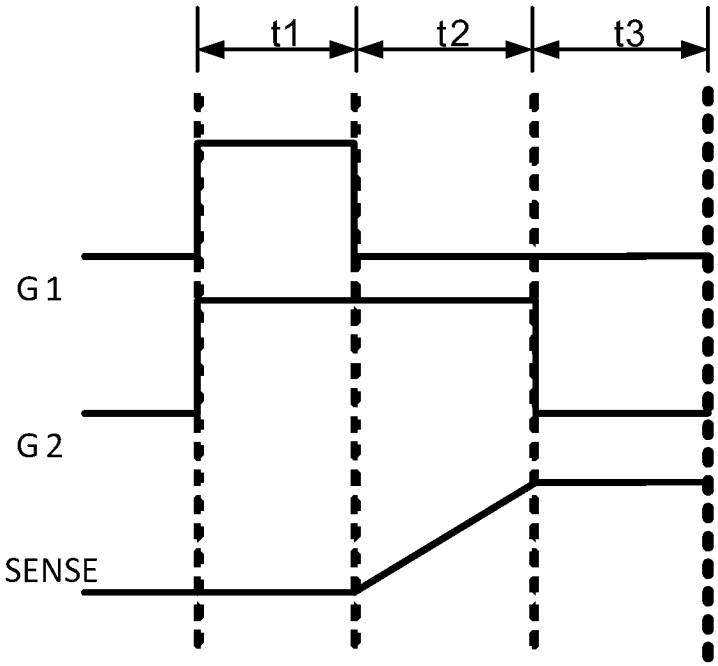

t1
t2
t3
G 1
G 2
SENSE

FIG. 3

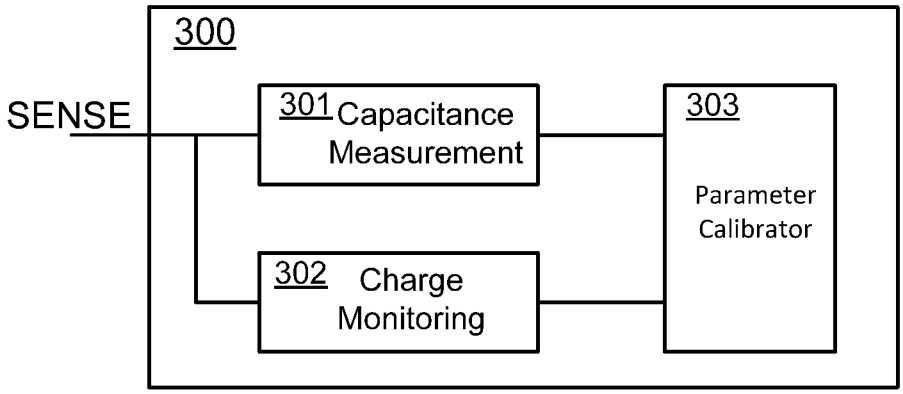

300
SENSE
301 Capacitance Measurement
303
Parameter Calibrator
302 Charge Monitoring

FIG. 4A

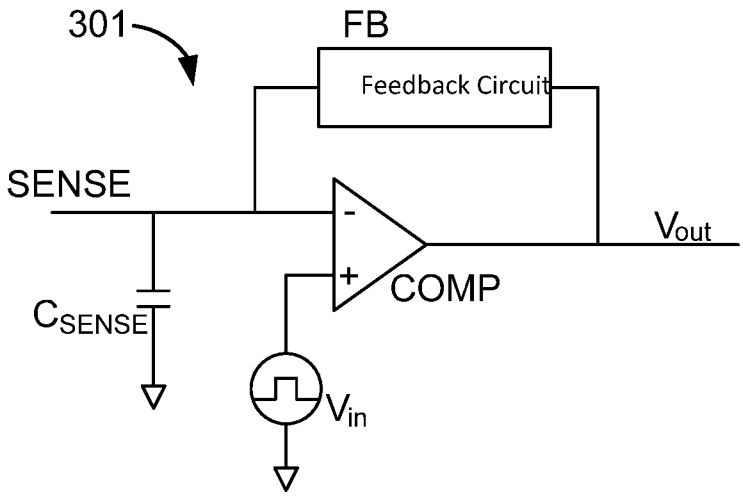

301
FB
Feedback Circuit
SENSE
-
+
COMP
Vout
CSENSE
Vin

FIG. 4B

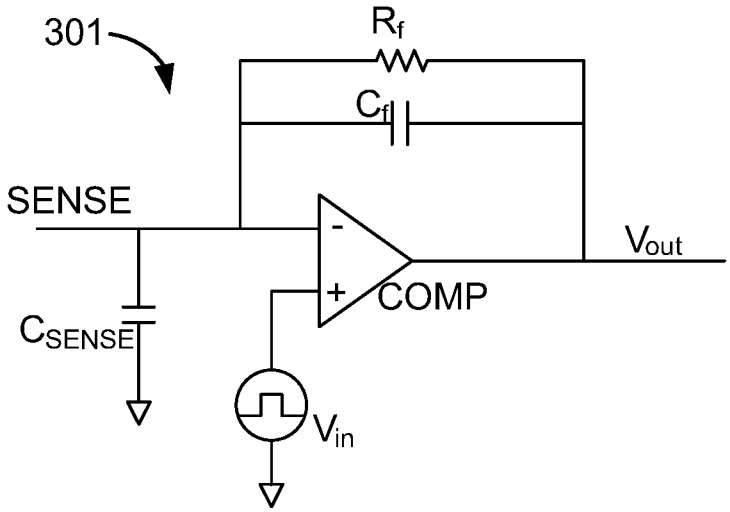

301
R_f
C_f
SENSE
-
+
COMP
V_{out}
C_{SENSE}
V_{in}

FIG. 5

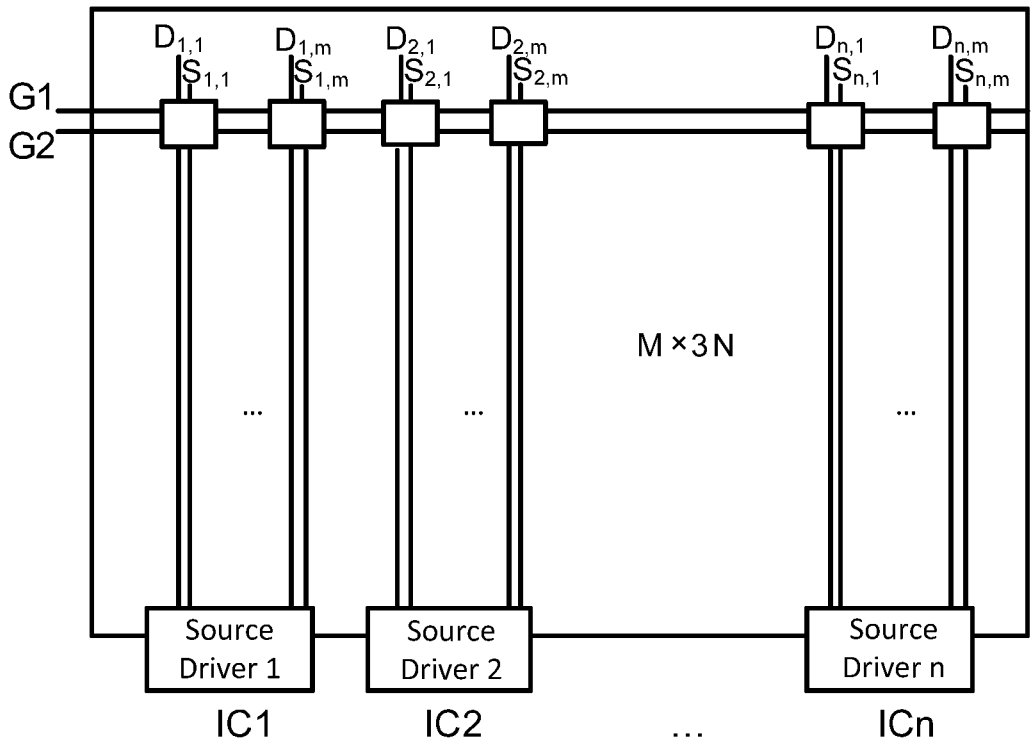

$D_{1,1}$ $S_{1,1}$
$D_{1,m}$ $S_{1,m}$
$D_{2,1}$ $S_{2,1}$
$D_{2,m}$ $S_{2,m}$
$D_{n,1}$ $S_{n,1}$
$D_{n,m}$ $S_{n,m}$
G1
G2
M×3N
Source Driver 1
Source Driver 2
Source Driver n
IC1
IC2
…
ICn

FIG. 6A

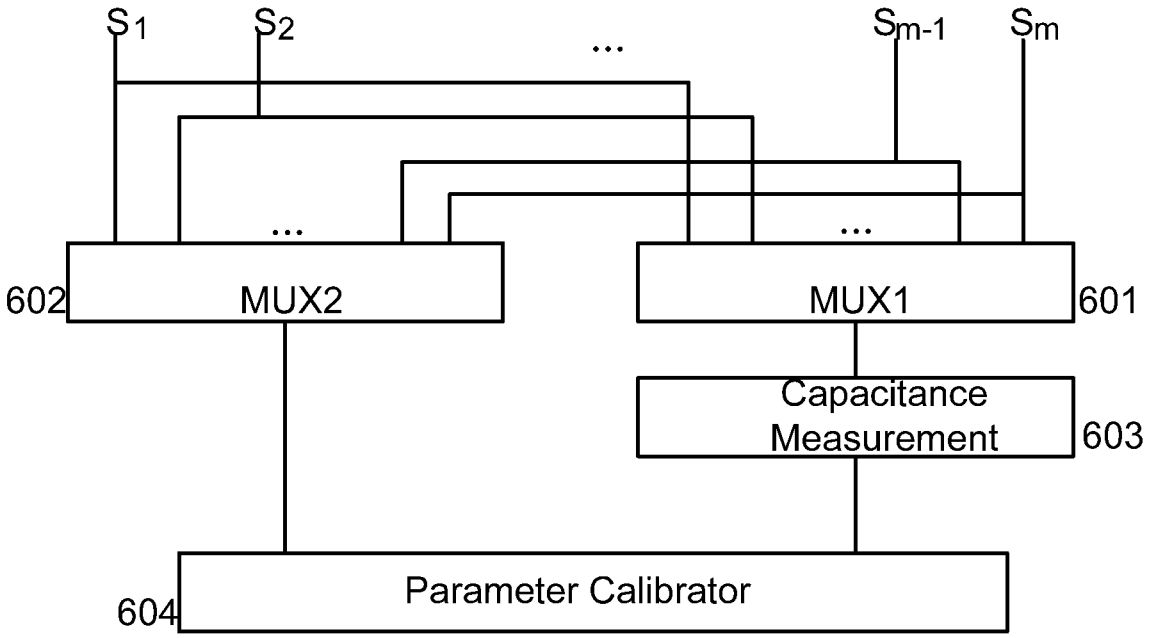

S1
S2
...
Sm-1
Sm
...
...
602
MUX2
MUX1
601
Capacitance Measurement
603
604
Parameter Calibrator

FIG. 6B

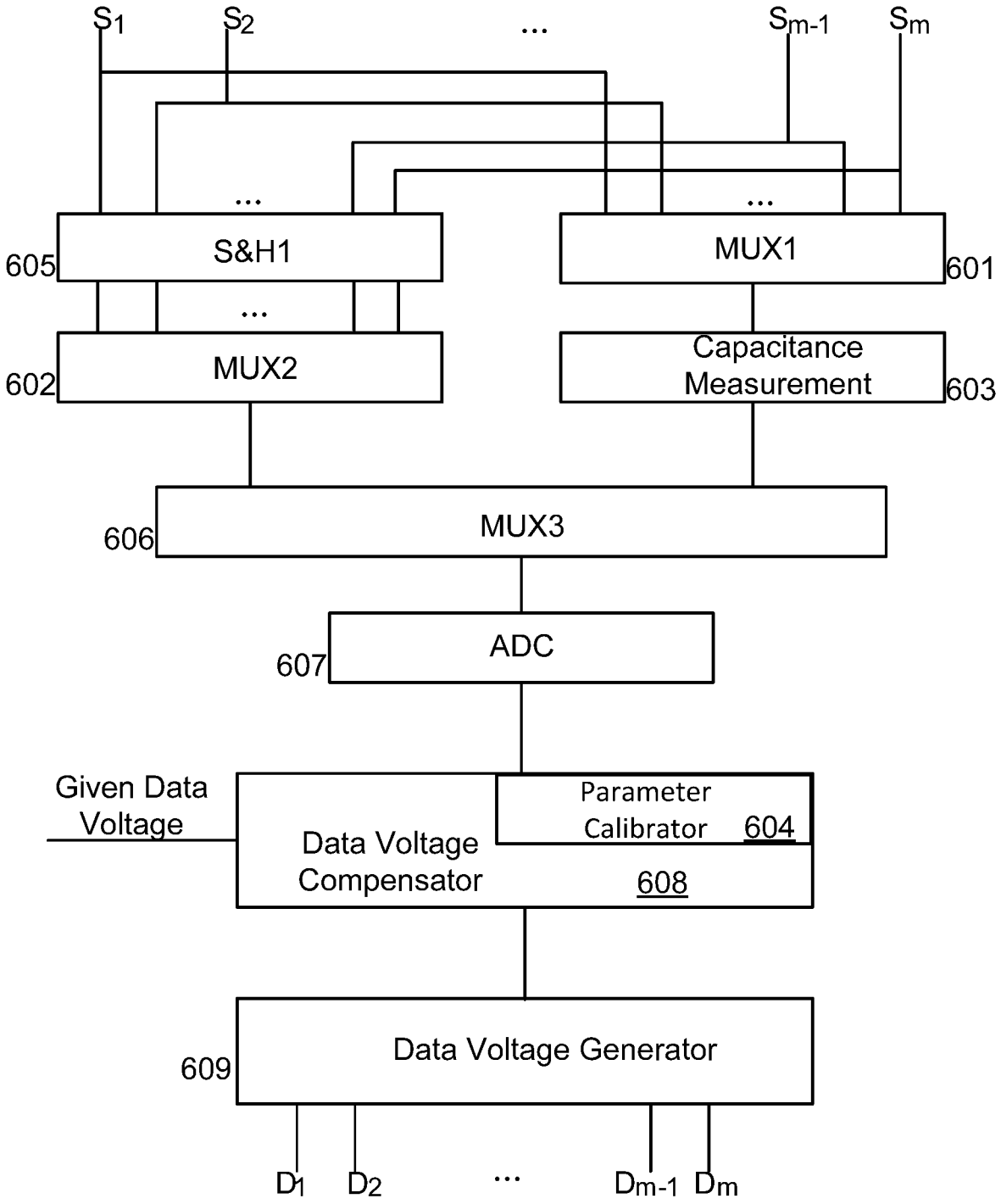

S1
S2
...
Sm-1
Sm
605
S&H1
MUX1
601
MUX2
602
Capacitance Measurement
603
606
MUX3
607
ADC
Given Data Voltage
Parameter Calibrator
604
Data Voltage Compensator
608
609
Data Voltage Generator
D1
D2
Dm-1
Dm

FIG. 7

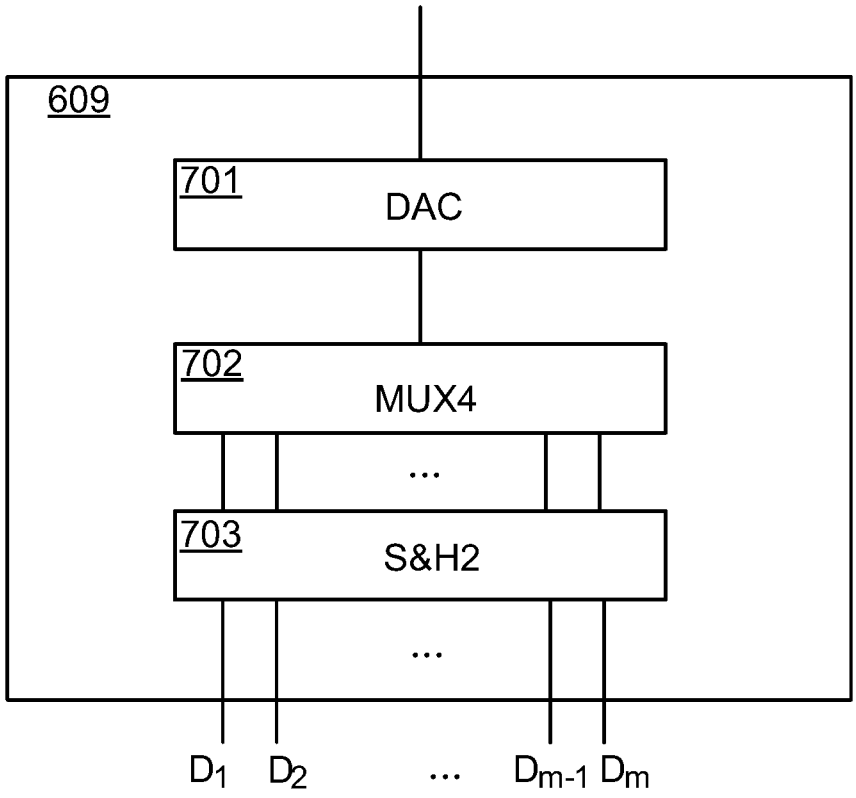


FIG. 8

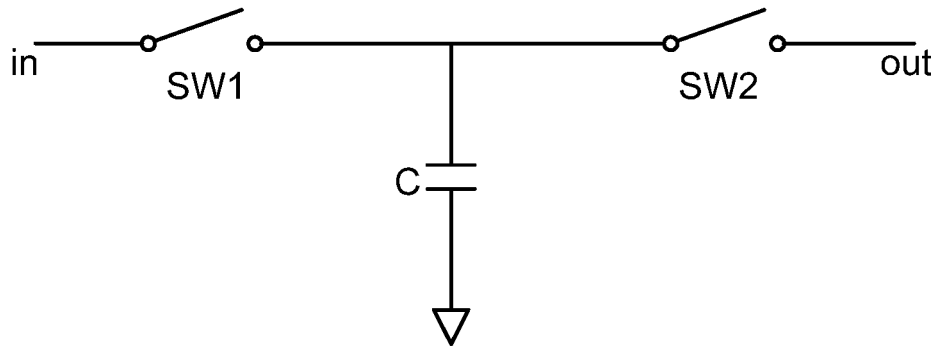
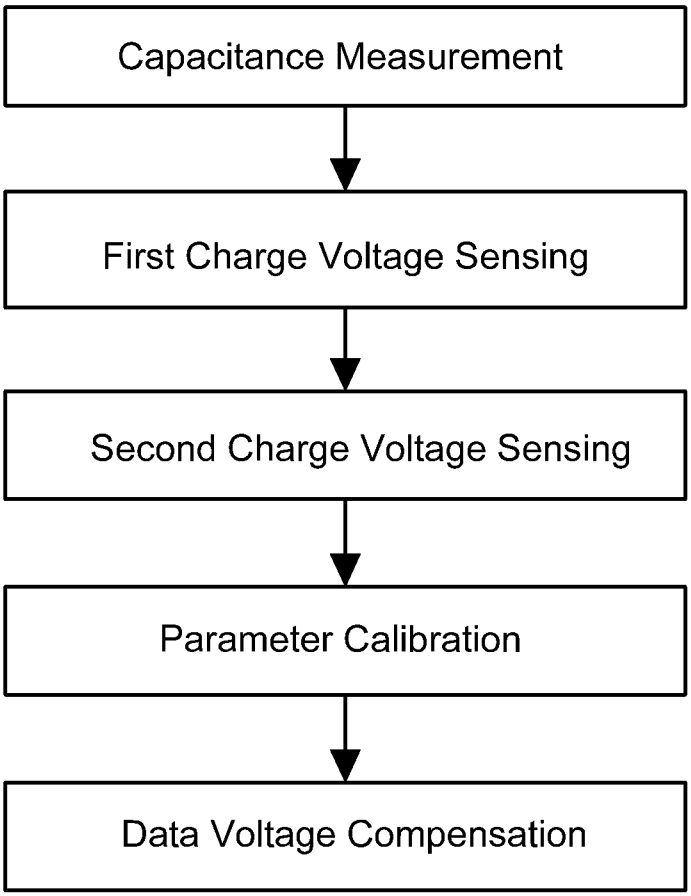


FIG. 9


Capacitance Measurement
First Charge Voltage Sensing
Second Charge Voltage Sensing
Parameter Calibration
Data Voltage Compensation

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2016/111468

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/3225(2016.01)i; G09G 3/3275(2016.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI; EPODOC; CNPAT; CNKI; IEEE: AMOLED, compensat+, calibrat+, sense, parasitic, capacit+, charg+, threshold voltage, carrier mobility rate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 106097969 A (BOE TECHNOLOGY GROUP CO., LTD.) 09 November 2016 (2016-11-09) description, paragraphs [0036]-[0140], claims 1-13 and figures 1-9	1-20
X	CN 105321455 A (LG DISPLAY CO., LTD.) 10 February 2016 (2016-02-10) description, paragraphs [0052]-[0089] and Figs. 3-6	1-5
X	CN 104700772 A (LG DISPLAY CO., LTD.) 10 June 2015 (2015-06-10) description, paragraphs [0047]-[0078] and Figs. 6-12	1-5
A	CN 104700761 A (BOE TECHNOLOGY GROUP CO., LTD.) 10 June 2015 (2015-06-10) the whole document	1-20
A	CN 105321456 A (LG DISPLAY CO., LTD.) 10 February 2016 (2016-02-10) the whole document	1-20
A	CN 102968954 A (LG DISPLAY CO., LTD.) 13 March 2013 (2013-03-13) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 February 2017	**27 March 2017**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**HAN,Bing**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)62414062**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2016/111468

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
CN 106097969 A	09 November 2016	None	
CN 105321455 A	10 February 2016	JP 2016009185 A	18 January 2016
		EP 2960894 A1	30 December 2015
		KR 101597037 B1	24 February 2016
		KR 20160001822 A	07 January 2016
		TW 201601136 A	01 January 2016
		US 2015379937 A1	31 December 2015
CN 104700772 A	10 June 2015	EP 2881932 A3	08 July 2015
		US 2015154908 A1	04 June 2015
		JP 2015108828 A	11 June 2015
		US 9262964 B2	16 February 2016
		KR 101661016 B1	29 September 2016
		JP 5933672 B2	15 June 2016
		TW 201523564 A	16 June 2015
		KR 20150064798 A	12 June 2015
		EP 2881932 A2	10 June 2015
		TW I547925 B1	01 September 2016
CN 104700761 A	10 June 2015	WO 2016155177 A1	06 October 2016
CN 105321456 A	10 February 2016	US 9449560 B2	20 September 2016
		KR 20160007971 A	21 January 2016
		US 2016012798 A1	14 January 2016
CN 102968954 A	13 March 2013	US 2016086539 A1	24 March 2016
		CN 102968954 B	03 June 2015
		US 9236011 B2	12 January 2016
		US 2013050292 A1	28 February 2013
		KR 20130024744 A	08 March 2013

专利名称(译)	用于OLED子像素电路的校准装置，源电极驱动电路和数据电压补偿方法		
公开(公告)号	EP3472826A1	公开(公告)日	2019-04-24
申请号	EP2016869392	申请日	2016-12-22
[标]申请(专利权)人(译)	京东方科技集团股份有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司.		
当前申请(专利权)人(译)	京东方科技集团股份有限公司.		
[标]发明人	WU ZHONGYUAN		
发明人	WU, ZHONGYUAN		
IPC分类号	G09G3/3225 G09G3/3275		
CPC分类号	G09G3/3225 G09G3/3275 G09G3/3233 G09G3/3291 G09G2300/0842 G09G2310/0297 G09G2320/0295 G09G2320/043 G09G2320/0693 G09G2320/04		
代理机构(译)	COHAUSZ & FLORACK		
优先权	201610440604.7 2016-06-17 CN		
其他公开文献	EP3472826A4		
外部链接	Espacenet		

摘要(译)

公开了一种与子像素电路相关联的校准装置（300），源电极驱动电路，以及用于补偿施加到与数据线和感测线相关联的子像素电路的数据线的数据电压的方法。校准装置（300）包括：电容测量电路（301,603），用于输出与感测线相关的电容测量电压（Vout）;电荷感测电路（302），用于在数据线为时感测感测线上的充电电压。应用参考数据电压和参数校准器（303,604），基于电容测量电压（Vout），参考数据电压和充电电压计算子像素电路中的驱动晶体管（DT）的参数，以及配置成确定用于源电极驱动电路的驱动晶体管（DT）的电参数漂移，以确定补偿数据电压，以补偿由于电参数漂移引起的亮度的不均匀性。