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# (54) PIXEL CIRCUIT AND DISPLAY DEVICE

PIXELSCHALTUNG UND ANZEIGEVORRICHTUNG

CIRCUIT POUR PIXELS ET DISPOSITIF D'AFFICHAGE

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## Description

### TECHNICAL FIELD OF THE DISCLOSURE

**[0001]** The present invention relates to a pixel circuit and a display apparatus.

### BACKGROUND

**[0002]** Nowadays, organic light emitting displays (OLED) have become one of the hotspots in the study field of flat panel displays. Compared with liquid crystal displays, OLED has the advantages of low power consumption, low production cost, self light emitting, wide viewing angle and fast response and so on. Currently, OLED has begun to replace the traditional liquid crystal displays (LCD) in the display areas such as mobile-phones, PDAs and digital cameras. Pixel driving circuit design is the core technical content of OLED displays and has important meaning for the study.

**[0003]** OLED is current-driven and needs a stable current to control light emission, which is different from the TFT (Thin Film Transistor)-LCD that uses a stable voltage to control brightness.

**[0004]** CN 103 474 026 A discloses a pixel circuit and a displayer. The pixel circuit comprises a first pixel sub circuit, a second pixel sub circuit, an initializing module and a data voltage write-in module, wherein the initializing module and the data voltage write-in module are connected with the first pixel sub circuit and the second pixel sub circuit. The initializing module is connected with a reset signal end and a low potential end and for initializing the first pixel sub circuit and the second pixel sub circuit under the control of a reset signal input by the reset signal end. The data voltage write-in module is connected with data voltage and a gate signal end and for writing first data voltage in the first pixel sub circuit under the control of a signal input by the gate signal end, compensating a driving module of the first pixel sub circuit, writing second data voltage in the second pixel sub circuit and compensating a driving module of the second pixel sub circuit.

**[0005]** US 2009/207158 A1 discloses a display device which includes a light emitting element to emit light having an intensity that varies depending on a magnitude of a driving current, a capacitor connected between a first node and a second node, a driving transistor having an input terminal connected to a first voltage, an output terminal, and a control terminal connected to the second node, a first switching unit to connect a data voltage and a second voltage to the first node, a second switching unit to switch a connection between the second voltage and the second node, a third switching unit to connect the second node and the light emitting element to the output terminal of the driving transistor, and a fourth switching unit to switch a connection between the control terminal and the input terminal of the driving transistor.

**[0006]** US 2007/279337 A1 discloses an OLED display device and driving method thereof. The OLED device including a driving voltage source; a reference voltage source that generates a reference voltage; a reference current source; and a storage capacitor connected between a first node and a second node. An OLED device is connected between a third node and a ground voltage source. A first scanning signal is supplied to a first scan line. A second scanning signal is supplied to a second scan line, the second scanning signal having an inverse-phase against the first scanning signal.Due to process technology, device aging and other reasons, in the original 2T1C driving circuit (comprising two thin film transistors and one capacitor), the threshold voltages of driving TFTs at each pixel are not uniform, which causes changes in the current flowing through the OLED at each pixel so that the display brightness are not uniform, thus affecting the display effect of the entire image.

**[0007]** In the known technology, one pixel circuit generally corresponds to one pixel. Each pixel circuit comprises at least one data voltage line, one operating voltage line and a plurality of scanning signal lines, which causes the corresponding production process more complicated, and not conducive to reducing the pixel pitch.

### SUMMARY

**[0008]** It is an object of the present invention to provide a pixel circuit and a display apparatus comprising the same.

**[0009]** The object is achieved by the features of the respective independent claims. Further embodiments and developments are defined in the dependent claims.

**[0010]** In the pixel circuit provided by the present invention, the operating current flowing through the electroluminescent unit is not affected by the threshold voltage of the corresponding driving transistor, thus the problem that the display brightness is uneven due to the drift of the threshold voltage of the driving transistor is addressed thoroughly. Meanwhile, the driving of two pixels is accomplished using one compensation circuit, and two adjacent pixels use multiple signal lines in common, which can reduce the number of signal lines for the pixel circuit in the display apparatus and lower the cost of the integration circuit, as well as can shorten the pixel pitch and increase the pixel density.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0011]**

Fig.1 is a schematic structural diagram of a pixel circuit provided by an embodiment of the present disclosure;

Fig.2 is a timing chart of critical signals in a pixel circuit provided by an embodiment of the present disclosure;

Figs.3(a) to (e) are a schematic diagram of the flowing direction of a current and a voltage value in different timings of a pixel circuit in an embodiment of

the present disclosure;

Fig.4 is a schematic diagram of a position relationship between the pixel circuit and the pixel in a display apparatus provided by an embodiment of the present disclosure; and

Fig.5 is a schematic diagram of another position relationship between the pixel circuit and the pixel in a display apparatus provided by an embodiment of the present disclosure.

## DETAILED DESCRIPTION

**[0012]** In the following, specific implements of the present disclosure are further described in conjunction with attached drawings and embodiments. The following embodiments are only used for explaining the technical solution of the present disclosure more clearly, but not for limiting the protection scope of the present disclosure.

**[0013]** In one embodiment of the present disclosure, there is provided a pixel circuit, as shown in Fig.1 or Figs. 3(a)-(e), comprising two sub-pixel circuits PI and P2, wherein each of the sub-pixel circuit comprises five switch units T1, T2, T3, T4, T5, one driving unit DT, one energy storage unit C, and one electroluminescent unit L (to facilitate the distinction, in Fig.1 or Figs.3(a)-(e), the five switch units in P2 are denoted as T1', T2', T3', T4' and T5' respectively, the driving unit is denoted as DT', the energy storage unit is denoted as C', and the electroluminescent unit is denoted as L', the same below); a first terminal of T1 is connected to a first terminal of C, terminal a1, (as shown in the figure, a second terminal of C is terminal b1; for C', a first terminal thereof is terminal a2 and a second terminal thereof is terminal b2), a second terminal of T1 is grounded, and T1 is configured to ground the first terminal a1 of the energy storage unit C under the control of a scan signal line connected to a control terminal of T1; a first terminal of T2 is connected to the terminal a1 of C, a second terminal of T2 is connected to a data voltage line $V_{data}$, and T2 is configured to write the voltage in the data voltage line into the first terminal of the energy storage unit C under the control of a scan signal line connected to a control terminal of T2; a first terminal of T3 is connected to the terminal b1, a second terminal of T3 is grounded, and T3 is configured to ground the second terminal b1 of the energy storage unit C under the control of a scan signal line connected to a control terminal of T3; a first terminal of T4 is connected to an output terminal of DT, a second terminal of T4 is connected to the terminal b1, and T4 is configured to connect the output terminal of the driving unit DT to a control terminal of the driving unit DT under the control of a scan signal line connected to a control terminal of T4; a first terminal of T5 is connected to the output terminal of DT, a second terminal of T5 is connected to L, and T5 is configured to introduce a driving current provided by the driving unit DT into the electroluminescent unit L under the control of a scan signal line connected to a control terminal of T5; the control terminal of the driving unit DT is connected to the terminal b1; in the two sub-pixel circuits PI and P2, control terminals of T1 and T4 are connected to a third scan signal line Scan[3], and the control terminal of the third switch unit T3 is connected to a second scan signal line Scan[2]; the control terminals of T2 and T5 in a first sub-pixel circuit P1 are connected to a first scan signal line Scan[1]; the control terminals of T2' and T5' in a second sub-pixel circuit P2 are connected to a fourth scan signal line Scan[4]; in addition to the two sub-pixel circuits PI and P2, the pixel circuit further comprises a sixth switch unit T6, a first terminal of which is connected to an operating voltage line $V_{dd}$, a second terminal of which is connected to input terminals of the two driving units DT and DT', a control terminal of which is connected to a fifth scan signal line Em, and T6 is configured to provide an operating voltage for the driving unit DT under the control of the fifth scan signal line Em.

**[0014]** It can be understood that, in one embodiment of the present disclosure, the plurality of switch units whose control terminals are connected to the same scanning signal line (for example, the four switch units T1, T1', T4 and T4' connected to Scan[3], the two switch units T2, T5 connected to Scan[1], and the two switch units T3 and T3' connected to Scan[2]) should be switches of the same channel type, that is, are all turned on by a high level or all turned on by a low level, thus ensuring the turn-on or turn-off states of the two switch units connected to the same scanning signal line are the same.

**[0015]** In the pixel circuit provided by the embodiment of the present disclosure, the operating current flowing through the electroluminescent unit is not affected by the threshold voltage of the corresponding driving transistor, which completely solves the problem of non-uniformity in the display brightness due to drifting of the threshold voltage of the driving transistor. Meanwhile, one compensation circuit is used to drive two pixels, which narrows down the number of TFT devices for compensation, and reduces the number of data voltage lines by one, thus the number of signal lines. In this way, it is possible to reduce the pixel pitch significantly and lower the IC cost, thus obtaining a higher pixel density.

**[0016]** Alternatively, the switch units and the driving units are thin film transistors (TFTs). The control terminal of each switch unit is a gate of the thin film transistor, the first terminal of each switch unit is a source of the thin film transistor, and the second terminal of each switch unit is a drain of the thin film transistor. The input terminal of each driving unit is a source of the thin film transistor, the control terminal of each driving unit is a gate of the thin film transistor, and the output terminal of each driving unit is a drain of the thin film transistor. Of course, the switch units and the driving units may also be other suitable devices or a combination of the devices.

**[0017]** Further, in an embodiment of the present embodiment, all of the TFTs are of P channel type. By using the same type of transistors, it is possible to unify production process, thereby improving the product yield. The skilled in the art will understand that, in practice, the types

of respective transistors may not be identical. For example, T2 and T5 may be a N-channel transistor, while T2' and T5' may be a P-channel transistor. As long as the turn-on/turn-off states of the two switch units whose control terminals are connected to the same scanning signal line are identical, the technical solution provided by the present application can be realized. The exemplary embodiments of the present disclosure should not be construed as limiting the protection scope of the present disclosure.

**[0018]** Alternatively, the energy storage unit C is a capacitor. Of course, in practice, other elements with energy storage function can also be adopted according to the design requirements.

**[0019]** Alternatively, the electroluminescent unit L can be an organic light emitting diode (OLED). Of course, other elements with electroluminescent function can also be adopted according to the design requirements.

**[0020]** In the following, the detailed explanation of the work principle of the pixel circuit provided by an exemplary embodiment of the present disclosure is made in conjunction with Fig.2 and Figs. 3(a)-(e). Figure 2 shows a time sequence diagram of scanning signals input into respective scanning signal lines when the pixel circuit provided by the present disclosure is working. It can be divided into five stages, which are respectively represented in Fig.2 as a reset stage W1, a discharge stage W2, a first pixel compensation stage W3, a second pixel compensation stage W4, and a light emitting stage W5. In each stage, the current flow directions and voltage values of the pixel circuit are shown in Fig.3 (a), Fig. 3(b), Fig. 3(c), Fig. 3(d) and Fig. 3(e) respectively. To facilitate explanation, it is assumed that the respective switch units are all TFTs of P channel type.

**[0021]** At the reset stage W1, as shown in Fig.2, Scan[2] is at a low level, and the other scan signal lines are at high levels. At this time, as shown in Fig.3(a), T3 and T3' are turned on, the other TFTs are all turned off, the terminal b1 of the capacitor C and the terminal b2 of the capacitor C' are grounded at the same time, and the potentials at the two points are 0V.

**[0022]** At the discharge stage W2, as shown in Fig.2, the Em and Scan[3] are at low levels, the other scan signal lines are at high levels, and $V_{data}=V_1$, with $V_1$ being the voltage corresponding to the light emitting L this time. At this time, T6, T1, T1', T4 and T4' are turned on, the other TFTs are all turned off, and the flowing direction of the current is as shown by Lb and Lb' in Fig.3(b). After the discharge, the potential at point b1 is $V_{dd}$-$V_{th1}$, and the potential at point b2 is $V_{dd}$-$V_{th2}$. During this discharge procedure, the current still doesn't flow through the OLED. Points a1 and a2 are grounded, and their potentials are 0V. At this time, the voltage difference between a1 and b1 is $V_{dd}$-$V_{th1}$, and the voltage difference between a2 and b2 is $V_{dd}$-$V_{th2}$, with $V_{th1}$ and $V_{th2}$ being the threshold voltages of DT and DT' respectively.

**[0023]** At the first pixel compensation stage W3, as shown in Fig.2, Scan[1] is at a low level, the other scan signal lines are at high levels, and $V_{data}=V_1$. At this time, T2 and T5 are turned on, and the other TFTs are turned off. As shown in Fig.3(c), at this time, the potential at point a1 is changed into the potential V1 of $V_{data}$, while point b1 is in a floating state. Thus, if the original voltage difference ($V_{dd}$-$V_{th1}$) between the two points a1 and b1 is to be maintained, an equal-voltage jump will occur in the potential at point b1, and the potential at point b1 will jump to $V_{dd}$-$V_{th1}$ +$V_1$.

**[0024]** At the second pixel compensation stage W4, as shown in Fig.2, Scan[4] is at a low level, the other scan signal lines are at high levels, and $V_{data}=V_2$, with $V_2$ being the voltage corresponding to the light emitting L' this time. At this time, T2' and T5' are turned on, and the other TFTs are turned off. As shown in Fig.3(d), at this time, the potential at point a2 is changed into the potential V2 of $V_{data}$, while point b2 is in a floating state. Thus, if the original voltage difference ($V_{dd}$-$V_{th2}$) between the two points a2 and b2 is to be maintained, an equal-voltage jump will occur in the potential at the gate of DT' (point bl), and the potential at point b2 will jump to $V_{dd}$-$V_{th2}$ +$V_2$.

**[0025]** At the light emitting stage W5, as shown in Fig. 2, among the scan signal lines, the Em, Scan[1] and Scan[4] are at low levels, and the other scan signal lines are at high levels. At this time, T6, T2, T5, T2', T5', DT and DT' are turned on, and the other TFTs are turned off. $V_{dd}$ supplies a current to L and L' along Le in Fig.3(e) to make L and L' emit light.

**[0026]** It can be known from the saturation current formula that the current flowing through L at this time $I_L=K(V_{GS}-V_{th1})^2=[V_{dd}-(V_{dd}-V_{th1}+V_1)-V_{th1})]^2= K*(V_1)^2$.

**[0027]** Similarly, $I_{L'}= K*(V_2)^2$.

**[0028]** As can be seen from the above formula, at this time, the operating current flowing through the two electroluminescent units is not affected by the threshold voltages of the driving transistors, and is only related to the data voltage $V_{data}$. The problem of threshold voltage($V_{th}$) drift of the driving TFT due to the process technology and the long-time operation is completely solved, thus eliminating its influence on the current flowing through the electroluminescent unit, and ensuring the normal operation of the electroluminescent unit. Meanwhile, in the embodiment of the present disclosure, two pixels share the same data voltage line and the same operating voltage line, and use only three scan signal lines, thereby reducing the number of the corresponding signal lines significantly, lowering the cost of the integration circuit, decreasing the pixel pitch and increasing the pixel density.

**[0029]** Based on the same conception, in another embodiment of the present disclosure, there is further provided a display apparatus comprising the pixel circuit as shown by any one as described above.

**[0030]** Alternatively, in the display apparatus, the two sub-pixel circuits of the pixel circuit are positioned within two adjacent pixels respectively. In this way, components and parts can be distributed more uniformly on the respective substrates.

**[0031]** Alternatively, the two adjacent pixels are positioned on the same side of their data voltage line. Fig.4 shows a case in which two adjacent pixels corresponding to one pixel circuit PU are at one side of the their corresponding data voltage line $V_{data}$. Alternatively, the two adjacent pixels are positioned on both sides of their data voltage line respectively. Fig.5 shows a case in which two adjacent pixels corresponding to one pixel circuit PU are at both sides of the their corresponding data voltage line $V_{data}$.

**[0032]** The display apparatus can be any products or means with a display function, such as electronic paper, mobile phones, tablets, televisions, displays, notebook computers, digital photo frames and navigators, etc.

## Claims

1. A pixel circuit comprising two sub-pixel circuits (P1, P2), **characterized in that**:

   each of the sub-pixel circuits (P1, P2) comprises a first to a fifth switch units (T1, T2, T3, T4, T5; T1', T2', T3', T4', T5'), a driving unit (DT, DT'), an energy storage unit (C, C') and an electroluminescent unit (L, L');
   a first terminal of the first switch unit (T1, T1') is connected to a first terminal of the energy storage unit (C, C'), a second terminal of the first switch unit (T1, T1') is grounded, and the first switch unit (T1, T1') is configured to ground the first terminal of the energy storage unit (C, C') under the control of a scan signal line connected to a control terminal of the first switch unit (T1, T1');
   a first terminal of the second switch unit (T2, T2') is connected to a data voltage line (Vdata), a second terminal of the second switch unit (T2, T2') is connected to the first terminal of the energy storage unit (C, C'), and the second switch unit (T2, T2') is configured to write the voltage in the data voltage line (Vdata) into the first terminal of the energy storage unit (C, C') under the control of a scan signal line connected to a control terminal of the second switch unit (T2, T2');
   a first terminal of the third switch unit (T3, T3') is connected to the second terminal of the energy storage unit (C, C'), a second terminal of the third switch unit (T3, T3') is grounded, and the third switch unit (T3, T3') is configured to ground the second terminal of the energy storage unit (C, C') under the control of a scan signal line connected to a control terminal of the third switch unit (T3, T3');
   a first terminal of the fourth switch unit (T4, T4') is connected to an output terminal of the driving unit (DT, DT'), a second terminal of the fourth switch unit (T4, T4') is connected to the second terminal of the energy storage unit (C, C'), and the fourth switch unit (T4, T4') is configured to connect the output terminal of the driving unit (DT, DT') to a control terminal of the driving unit (DT, DT') under the control of a scan signal line connected to a control terminal of the fourth switch unit (T4, T4');
   a first terminal of the fifth switch unit (T5, T5') is connected to the output terminal of the driving unit (DT, DT'), a second terminal of the fifth switch unit (T5, T5') is connected to the electroluminescent unit, and the fifth switch unit (T5, T5') is configured to introduce a driving current provided by the driving unit (DT, DT') into the electroluminescent unit under the control of a scan signal line connected to a control terminal of the fifth switch unit (T5, T5');
   the control terminal of the driving unit (DT, DT') is connected to the second terminal of the energy storage unit (C, C');
   in the two sub-pixel circuits (P1, P2), the control terminals of the first switch unit (T1, T1') and the fourth switch unit (T4, T4') are connected to a third scan signal line (Scan[3]), and the control terminals of the third switch unit (T3, T3') are connected to a second scan signal line (Scan[2]); the control terminals of the second switch unit (T2) and the fifth switch unit (T5) in a first sub-pixel circuit (P1) are connected to a first scan signal line (Scan[1]), and the control terminals of the second switch unit (T2') and the fifth switch unit (T5') in a second sub-pixel circuit (P2) are connected to a fourth scan signal line (Scan[4]);
   the pixel circuit further comprises a sixth switch unit (T6), a first terminal of which is connected to an operating voltage line (Vdd), a second terminal of which is connected to the input terminals of the driving units (DT, DT') of the two sub-pixel circuits (P1, P2) respectively, and a control terminal of which is connected to a fifth scan signal line (Em), and the sixth switch unit (T6) is configured to provide an operating voltage for the driving unit (DT, DT') under the control of the fifth scan signal line (Em).

2. The pixel circuit according to claim 1, wherein the switch units (T1, T2, T3, T4, T5, T1', T2', T3', T4', T5', T6) and the driving units (DT, DT') are thin film transistors, the control terminal of each switch unit (T1, T2, T3, T4, T5, T1', T2', T3', T4', T5', T6) is a gate of the thin film transistor, the first terminal of each switch unit (T1, T2, T3, T4, T5, T1', T2', T3', T4', T5', T6) is a source of the thin film transistor, the second terminal of each switch unit (T1, T2, T3, T4, T5, T1', T2', T3', T4', T5', T6) is a drain of the thin film transistor, the input terminal of the driving unit

(DT, DT') is a source of the thin film transistor, the control terminal of the driving unit (DT, DT') is a gate of the thin film transistor, and the output terminal of the driving unit (DT, DT') is a drain of the thin film transistor.

**3.** The pixel circuit according to claim 2, wherein all of the respective thin film transistors are of P channel type.

**4.** The pixel circuit according to any one of claims 1-3, wherein the energy storage unit (C, C') is a capacitor.

**5.** The pixel circuit according to any one of claims 1-4, wherein the electroluminescent unit is an organic light emitting diode.

**6.** A display apparatus comprising the pixel circuit according to any one of claims 1-5.

**7.** The display apparatus according to claim 6, wherein two sub-pixel circuits (P1, P2) of the pixel circuit are located respectively within two adjacent pixels.

**8.** The display apparatus according to claim 7, wherein the two adjacent pixels are located respectively at two sides of the data voltage line (Vdata).

**9.** The display apparatus according to claim 7, wherein the two adjacent pixels are located at a same side of the data voltage line (Vdata).

**Patentansprüche**

**1.** Pixel-Sschaltung mit zwei Sub-Pixel-Schaltungen (P1, P2), **dadurch gekennzeichnet, dass:**

jede der Sub-Pixel-Schaltungen (P1, P2) aufweist erste bis fünfte Schalteinheiten (T1, T2, T3, T4, T5; T1', T2', T3', T4', T5'), eine Ansteuereinheit (DT, DT'), eine Energiespeichereinheit (C, C') und eine Elektrolumineszenzeinheit (L, L');

ein erster Anschluss der ersten Schalteinheit (T1, T1') mit einem ersten Anschluss der Energiespeichereinheit (C, C') verbunden ist, ein zweiter Anschluss der ersten Schalteinheit (T1, T1') mit Masse verbunden ist, und die erste Schalteinheit (T1, T1') konfiguriert ist, den ersten Anschluss der Energiespeichereinheit (C, C') unter der Steuerung einer Abtastsignalleitung, die mit einem Steuer-Anschluss der ersten Schalteinheit (T1, T1') verbunden ist, auf Masse zu ziehen;

ein erster Anschluss der zweiten Schalteinheit (T2, T2') mit einer Datenspannungsleitung (Vdata) verbunden ist, ein zweiter Anschluss der zweiten Schalteinheit (T2, T2') mit dem ersten Anschluss der Energiespeichereinheit (C, C') verbunden ist, und die zweite Schalteinheit (T2, T2') konfiguriert ist, die Spannung der Datenspannungsleitung (Vdata) in den ersten Anschluss der Energiespeichereinheit (C, C') unter der Steuerung einer Abtastsignalleitung, die mit einem Steuer-Anschluss der zweiten Schalteinheit (T2, T2') verbunden ist, zu schreiben;

ein erster Anschluss der dritten Schalteinheit (T3, T3') mit dem zweiten Anschluss der Energiespeichereinheit (C, C') verbunden ist, ein zweiter Anschluss der dritten Schalteinheit (T3, T3') mit Masse verbunden ist, und die dritte Schalteinheit (T3, T3') konfiguriert ist, den zweiten Anschluss der Energiespeichereinheit (C, C') unter der Steuerung einer Abtastsignalleitung, die mit einem Steuer-Anschluss der dritten Schalteinheit (T3, T3') verbunden ist, auf Masse zu ziehen;

ein erster Anschluss der vierten Schalteinheit (T4, T4') mit einem Ausgabe-Anschluss der Ansteuereinheit (DT, DT') verbunden ist, ein zweiter Anschluss der vierten Schalteinheit (T4, T4') mit dem zweiten Anschluss der Energiespeichereinheit (C, C') verbunden ist, und die vierte Schalteinheit (T4, T4') konfiguriert ist, den Ausgabe-Anschluss der Ansteuereinheit (DT, DT') mit einem Steuer-Anschluss der Ansteuereinheit (DT, DT') unter der Steuerung einer Abtastsignalleitung, die mit einem Steuer-Anschluss der vierten Schalteinheit (T4, T4') verbunden ist, zu verbinden;

ein erster Anschluss der fünften Schalteinheit (T5, T5') mit dem Ausgabe-Anschluss der Ansteuereinheit (DT, DT') verbunden ist, ein zweiter Anschluss der fünften Schalteinheit (T5, T5') mit der Elektrolumineszenzeinheit verbunden ist, und die fünfte Schalteinheit (T5, T5') konfiguriert ist, einen Ansteuerstrom, der durch die Ansteuereinheit (DT, DT') bereitgestellt wird, in die Elektrolumineszenzeinheit unter der Steuerung einer Abtastsignalleitung, die mit einem Steuer-Anschluss der fünften Schalteinheit (T5, T5') verbunden ist, einzuleiten;

der Steuer-Anschluss der Ansteuereinheit (DT, DT') mit dem zweiten Anschluss der Energiespeichereinheit (C, C') verbunden ist;

in den zwei Sub-Pixel-Schaltungen (P1, P2), die Steueranschlüsse der ersten Schalteinheit (T1, T1') und der vierten Schalteinheit (T4, T4') mit einer dritten Abtastsignalleitung (Scan[3]) verbunden sind, und die Ansteueranschlüsse der dritten Schalteinheit (T3, T3') mit einer zweiten Abtastsignalleitung (Scan[2]) verbunden sind;

die Steueranschlüsse der zweiten Schalteinheit (T2) und der fünften Schalteinheit (T5) in einer ersten Sub-Pixel-Schaltung (P1) mit einer ers-

ten Abtastsignalleitung (Scan[1]) verbunden sind, und die Steueranschlüsse der zweiten Schalteinheit (T2') und der fünften Schalteinheit (T5') in einer zweiten Sub-Pixel-Schaltung (P2) mit einer fünften Abtastsignalleitung (Scan[4]) verbunden sind;
die Pixelschaltung weiter aufweist eine sechste Schalteinheit (T6), deren erster Anschluss mit einer Betriebsspannungsleitung (Vdd) verbunden ist, an der ein zweiter Anschluss mit den Eingangsanschlüssen der Ansteuereinheiten (DT, DT') der zwei Sub-Pixel-Schaltungen (P1, P2) jeweils verbunden sind, und deren Steuer-Anschluss mit einer fünften Abtastsignalleitung (Em) verbunden ist, und wobei die sechste Schalteinheit (T6) konfiguriert ist, eine Betriebsspannung für die Ansteuereinheit (DT, DT') unter der Steuerung der fünften Abtastsignalleitung (Em) bereitzustellen.

**2.** Pixelschaltung gemäß Anspruch 1, wobei die Schalteinheiten (T1, T2, T3, T4, T5; T1', T2', T3', T4', T5', T6) und die Ansteuereinheiten (DT, DT') Dünnschichttransistoren sind, die Steueranschlüsse von jeder Schalteinheit (T1, T2, T3, T4, T5; T1', T2', T3', T4', T5', T6) ein Gate-Anschluss des Dünnschichttransistors sind, der erste Anschluss jeder Schalteinheit (T1, T2, T3, T4, T5; T1', T2', T3', T4', T5', T6) ein Source-Anschluss des Dünnschichttransistors sind, die zweiten Anschlüsse jeder Schalteinheit (T1, T2, T3, T4, T5; T1', T2', T3', T4', T5', T6) ein Drain-Anschluss des Dünnschichttransistors sind, der Eingabe-Anschluss der Ansteuereinheit (DT, DT') ein Source-Anschluss des Dünnschichttransistors ist, der Steuer-Anschluss der Ansteuereinheit (DT, DT') ein Gate-Anschluss des Dünnschichttransistors ist, und der Ausgabe-Anschluss der Ansteuereinheit (DT, DT') ein Drain-Anschluss des Dünnschichttransistors ist.

**3.** Pixelschaltung gemäß Anspruch 2, wobei alle der jeweiligen Dünnschichttransistoren vom P-Kanal-Typ sind.

**4.** Pixelschaltung gemäß einem der Ansprüche 1 bis 3, wobei die Energiespeichereinheit (C, C') ein Kondensator ist.

**5.** Pixelschaltung gemäß einem der Ansprüche 1 bis 4, wobei die Elektrolumineszenzeinheit eine organische lichtemittierende Diode ist.

**6.** Displayvorrichtung mit der Pixelschaltung gemäß einem der Ansprüche 1 bis 5.

**7.** Displayvorrichtung gemäß Anspruch 6, wobei zwei Sub-Pixel-Schaltungen (P1, P2) der Pixelschaltung jeweils innerhalb zwei benachbarter Pixel angeordnet sind.

**8.** Displayvorrichtung gemäß Anspruch 7, wobei die zwei benachbarten Pixel jeweils an zwei Seiten der Datenspannungsleitung (Vdata) angeordnet sind.

**9.** Displayvorrichtung gemäß Anspruch 7, wobei die zwei benachbarten Pixel derselben Seite er Datenspannungsleitung (Vdata) angeordnet sind.

**Revendications**

**1.** Circuit de pixel comprenant deux circuits de sous-pixel (P1, P2), **caractérisé en ce que** :

chacun des circuits de sous-pixel (P1, P2) comprend des première à cinquième unités de commutation (T1, T2, T3, T4, T5 ; T1', T2', T3', T4', T5'), une unité de pilotage (DT, DT'), une unité de stockage d'énergie (C, C') et une unité électroluminescente (L, L') ;
une première borne de la première unité de commutation (T1, T1') est connectée à une première borne de l'unité de stockage d'énergie (C, C'), une seconde borne de la première unité de commutation (T1, T1') est reliée à la masse, et la première unité de commutation (T1, T1') est configurée de manière à ce qu'elle relie à la masse la première borne de l'unité de stockage d'énergie (C, C') sous la commande d'une ligne de signal de balayage qui est connectée à une borne de commande de la première unité de commutation (T1, T1') ;
une première borne de la deuxième unité de commutation (T2, T2') est connectée à une ligne de tension de données (Vdata), une seconde borne de la deuxième unité de commutation (T2, T2') est connectée à la première borne de l'unité de stockage d'énergie (C, C'), et la deuxième unité de commutation (T2, T2') est configurée de manière à ce qu'elle écrive la tension dans la ligne de tension de données (Vdata) à l'intérieur de la première borne de l'unité de stockage d'énergie (C, C') sous la commande d'une ligne de signal de balayage qui est connectée à une borne de commande de la deuxième unité de commutation (T2, T2') ;
une première borne de la troisième unité de commutation (T3, T3') est connectée à la seconde borne de l'unité de stockage d'énergie (C, C'), une seconde borne de la troisième unité de commutation (T3, T3') est reliée à la masse, et la troisième unité de commutation (T3, T3') est configurée de manière à ce qu'elle relie à la masse la seconde borne de l'unité de stockage d'énergie (C, C') sous la commande d'une ligne de signal de balayage qui est connectée à une

borne de commande de la troisième unité de commutation (T3, T3') ;
une première borne de la quatrième unité de commutation (T4, T4') est connectée à une borne de sortie de l'unité de pilotage (DT, DT'), une seconde borne de la quatrième unité de commutation (T4, T4') est connectée à la seconde borne de l'unité de stockage d'énergie (C, C'), et la quatrième unité de commutation (T4, T4') est configurée de manière à ce qu'elle connecte la borne de sortie de l'unité de pilotage (DT, DT') à une borne de commande de l'unité de pilotage (DT, DT') sous la commande d'une ligne de signal de balayage qui est connectée à une borne de commande de la quatrième unité de commutation (T4, T4') ;
une première borne de la cinquième unité de commutation (T5, T5') est connectée à la borne de sortie de l'unité de pilotage (DT, DT'), une seconde borne de la cinquième unité de commutation (T5, T5') est connectée à l'unité électroluminescente, et la cinquième unité de commutation (T5, T5') est configurée de manière à ce qu'elle introduise un courant de pilotage qui est fourni par l'unité de pilotage (DT, DT') à l'intérieur de l'unité électroluminescente sous la commande d'une ligne de signal de balayage qui est connectée à une borne de commande de la cinquième unité de commutation (T5, T5') ; la borne de commande de l'unité de pilotage (DT, DT') est connectée à la seconde borne de l'unité de stockage d'énergie (C, C') ;
dans les deux circuits de sous-pixel (P1, P2), les bornes de commande de la première unité de commutation (T1, T1') et de la quatrième unité de commutation (T4, T4') sont connectées à une troisième ligne de signal de balayage (Scan[3]), et les bornes de commande de la troisième unité de commutation (T3, T3') sont connectées à une deuxième ligne de signal de balayage (Scan[2]) ; les bornes de commande de la deuxième unité de commutation (T2) et de la cinquième unité de commutation (T5) dans un premier circuit de sous-pixel (P1) sont connectées à une première ligne de signal de balayage (Scan[1]), et les bornes de commande de la deuxième unité de commutation (T2') et de la cinquième unité de commutation (T5') dans un second circuit de sous-pixel (P2) sont connectées à une quatrième ligne de signal de balayage (Scan[4]) ;
le circuit de pixel comprend en outre une sixième unité de commutation (T6) dont une première borne est connectée à une ligne de tension de fonctionnement (Vdd), dont une seconde borne est connectée aux bornes d'entrée des unités de pilotage (DT, DT') des deux circuits de sous-pixel (P1, P2), de façon respective, et dont une borne de commande est connectée à une cinquième ligne de signal de balayage (Em), et la sixième unité de commutation (T6) est configurée de manière à ce qu'elle fournisse une tension de fonctionnement pour l'unité de pilotage (DT, DT') sous la commande de la cinquième ligne de signal de balayage (Em).

**2.** Circuit de pixel selon la revendication 1, dans lequel les unités de commutation (T1, T2, T3, T4, T5 ; T1', T2', T3', T4', T5') et les unités de pilotage (DT, DT') sont des transistors à film mince, la borne de commande de chaque unité de commutation (T1, T2, T3, T4, T5 ; T1', T2', T3', T4', T5') est une grille du transistor à film mince, la première borne de chaque unité de commutation (T1, T2, T3, T4, T5 ; T1', T2', T3', T4', T5') est une source du transistor à film mince, la seconde borne de chaque unité de commutation (T1, T2, T3, T4, T5 ; T1', T2', T3', T4', T5') est un drain du transistor à film mince, la borne d'entrée de l'unité de pilotage (DT, DT') est une source du transistor à film mince, la borne de commande de l'unité de pilotage (DT, DT') est une grille du transistor à film mince, et la borne de sortie de l'unité de pilotage (DT, DT') est un drain du transistor à film mince.

**3.** Circuit de pixel selon la revendication 2, dans lequel tous les transistors à film mince respectifs sont du type à canal P.

**4.** Circuit de pixel selon l'une quelconque des revendications 1 à 3, dans lequel l'unité de stockage d'énergie (C, C') est un condensateur.

**5.** Circuit de pixel selon l'une quelconque des revendications 1 à 4, dans lequel l'unité électroluminescente est une diode émettrice de lumière organique.

**6.** Appareil d'affichage comprenant le circuit de pixel selon l'une quelconque des revendications 1 à 5.

**7.** Appareil d'affichage selon la revendication 6, dans lequel deux circuits de sous-pixel (P1, P2) du circuit de pixel sont respectivement localisés à l'intérieur de deux pixels adjacents.

**8.** Appareil d'affichage selon la revendication 7, dans lequel les deux pixels adjacents sont respectivement localisés au niveau de deux côtés de la ligne de tension de données (Vdata).

**9.** Appareil d'affichage selon la revendication 7, dans lequel les deux pixels adjacents sont localisés au niveau d'un même côté de la ligne de tension de données (Vdata).

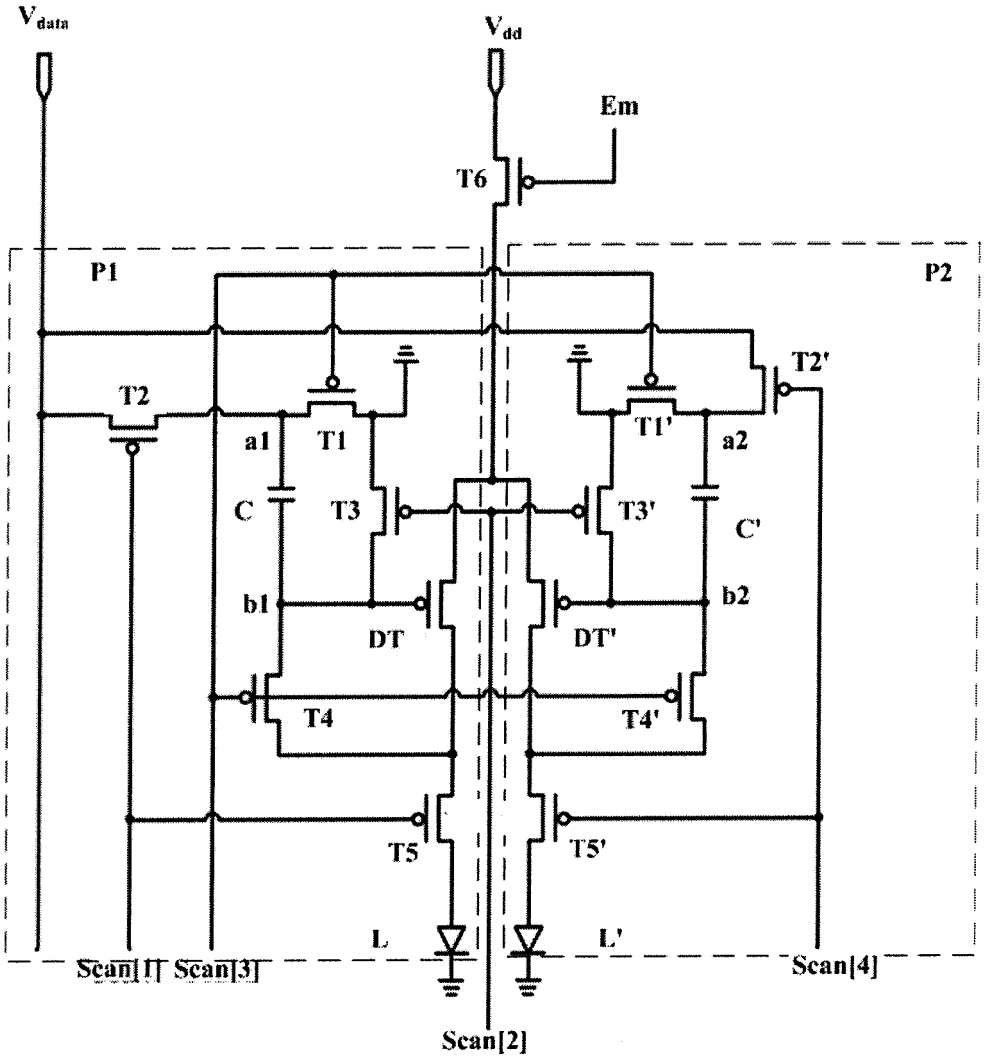
$V_{data}$
$V_{dd}$
Em
T6
P1
P2
T2'
T2
T1
T1'
a1
a2
C
T3
T3'
C'
b1
b2
DT
DT'
T4
T4'
T5
T5'
L
L'
Scan[1]
Scan[3]
Scan[4]
Scan[2]

Fig. 1

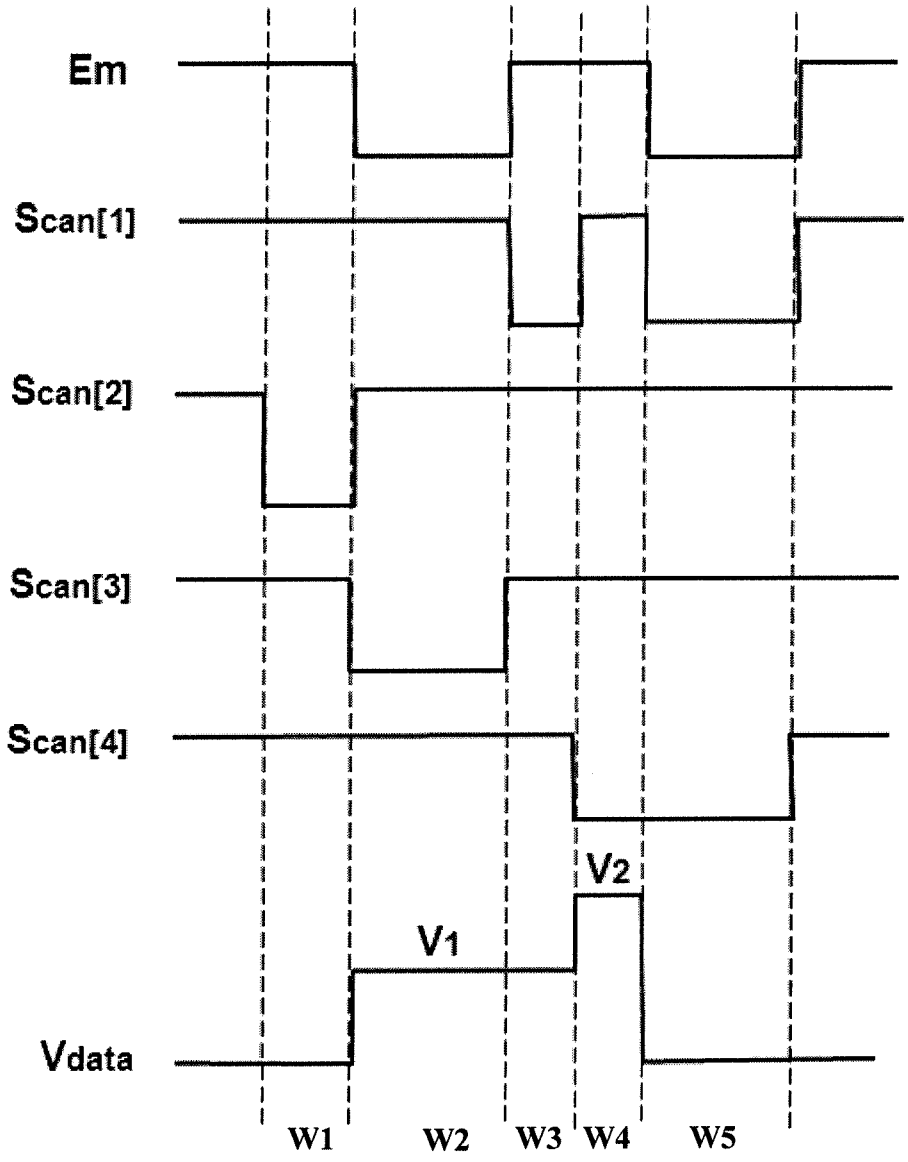


Fig. 2

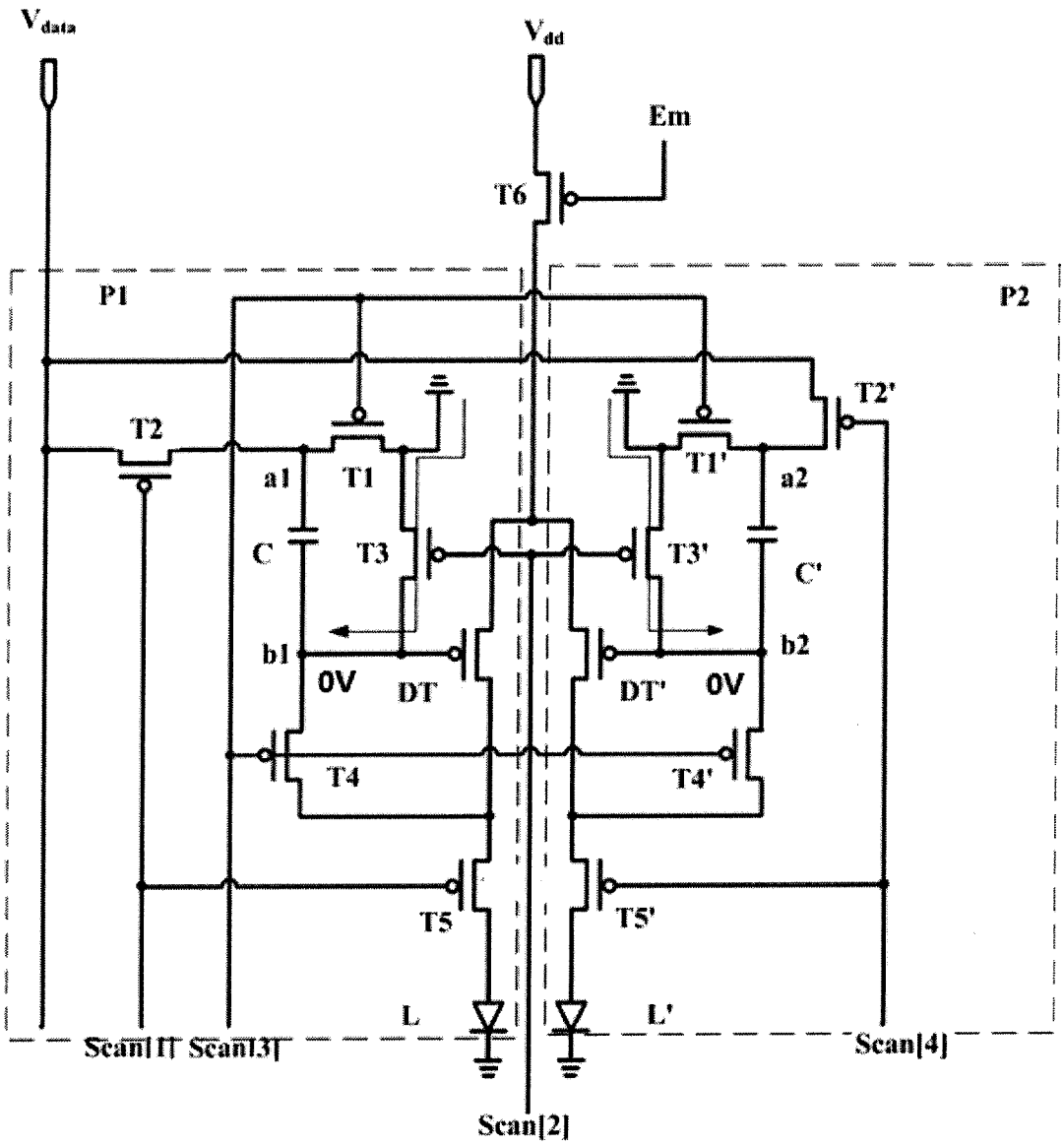
Vdata
Vdd
Em
T6
P1
P2
T2
T2'
a1
T1
T1'
a2
C
T3
T3'
C'
b1
b2
0V
DT
DT'
0V
T4
T4'
T5
T5'
L
L'
Scan[1]
Scan[3]
Scan[4]
Scan[2]

Fig. 3(a)

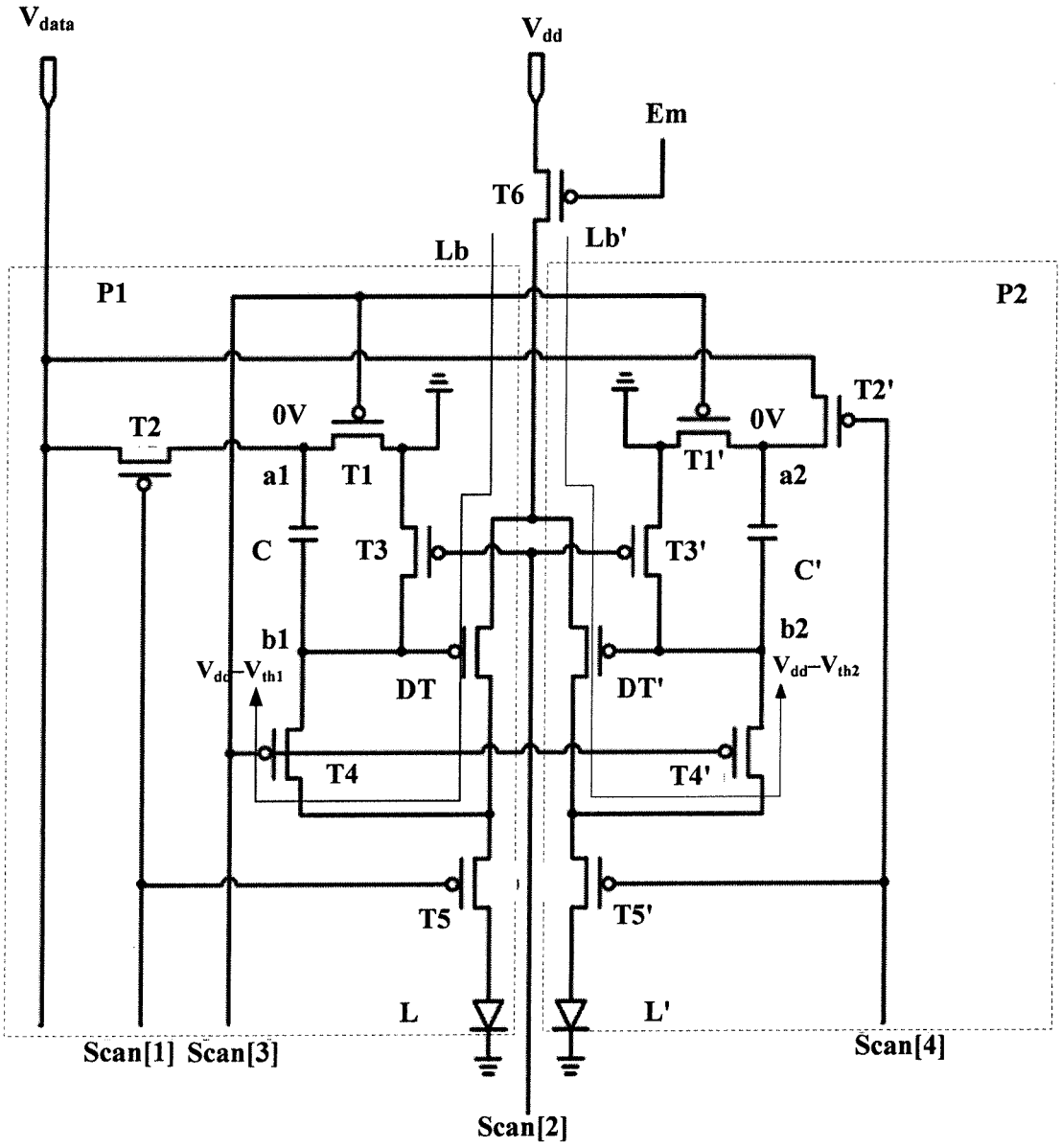
$V_{data}$
$V_{dd}$
Em
T6
Lb
Lb'
P1
P2
T2
0V
T1
a1
C
T3
b1
$V_{dd}-V_{th1}$
DT
T4
T5
L
Scan[1]
Scan[3]
T2'
0V
T1'
a2
T3'
C'
b2
$V_{dd}-V_{th2}$
DT'
T4'
T5'
L'
Scan[4]
Scan[2]

Fig. 3(b)

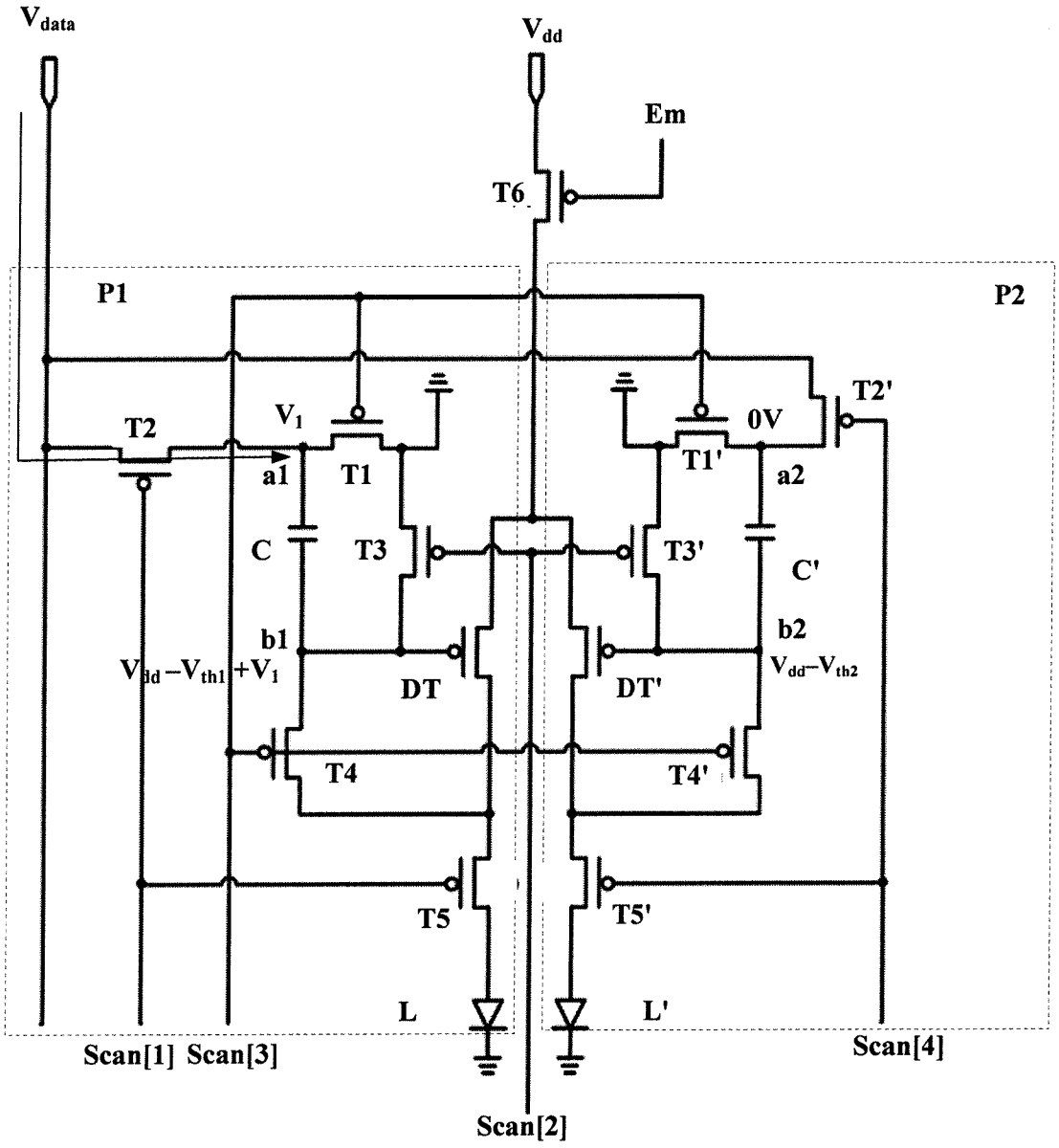
$V_{data}$
$V_{dd}$
Em
T6
P1
P2
T2
$V_1$
T1
0V
T1'
T2'
a1
a2
C
T3
T3'
C'
b1
b2
$V_{dd}-V_{th1}+V_1$
DT
DT'
$V_{dd}-V_{th2}$
T4
T4'
T5
T5'
L
L'
Scan[1] Scan[3]
Scan[4]
Scan[2]

Fig. 3(c)

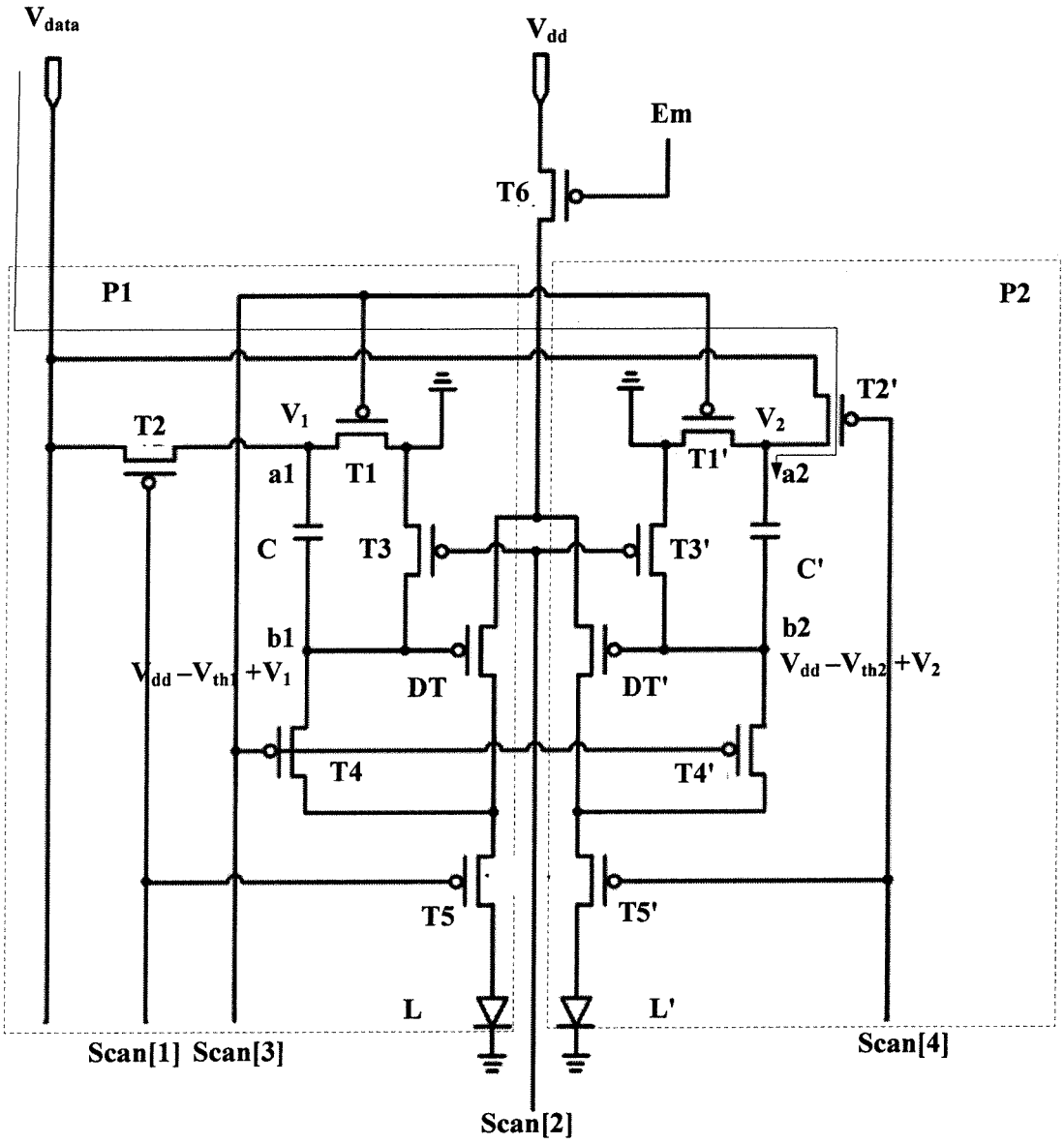
$V_{data}$
$V_{dd}$
Em
T6
P1
P2
T2
$V_1$
T2'
$V_2$
T1'
a1
T1
a2
C
T3
T3'
C'
b1
b2
$V_{dd}-V_{th1}+V_1$
DT
DT'
$V_{dd}-V_{th2}+V_2$
T4
T4'
T5
T5'
L
L'
Scan[1] Scan[3]
Scan[4]
Scan[2]

Fig. 3(d)

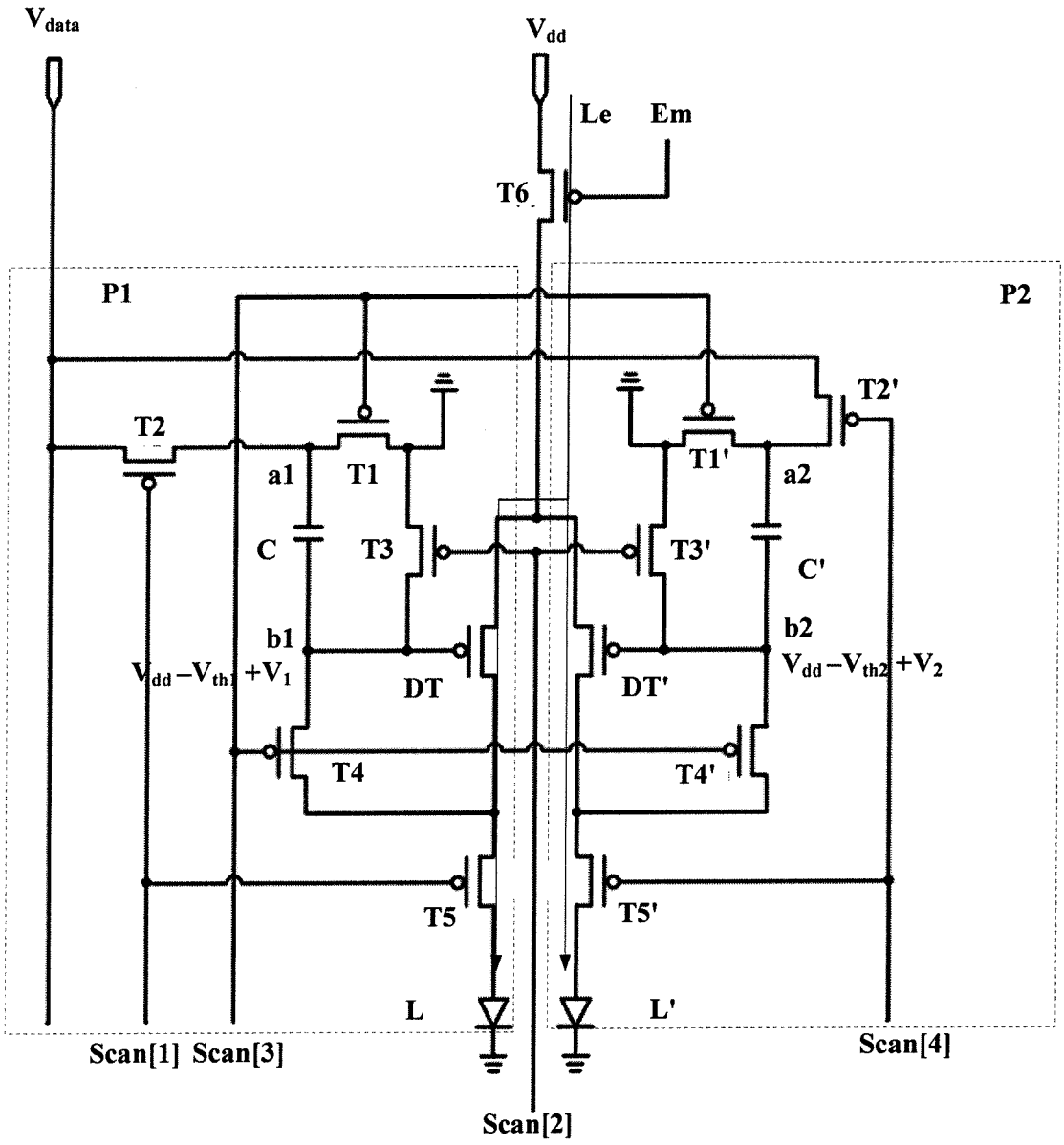
$V_{data}$
$V_{dd}$
Le
Em
T6
P1
P2
T2
T2'
a1
T1
T1'
a2
C
T3
T3'
C'
b1
b2
$V_{dd}-V_{th1}+V_1$
DT
DT'
$V_{dd}-V_{th2}+V_2$
T4
T4'
T5
T5'
L
L'
Scan[1]
Scan[3]
Scan[4]
Scan[2]

Fig. 3(e)

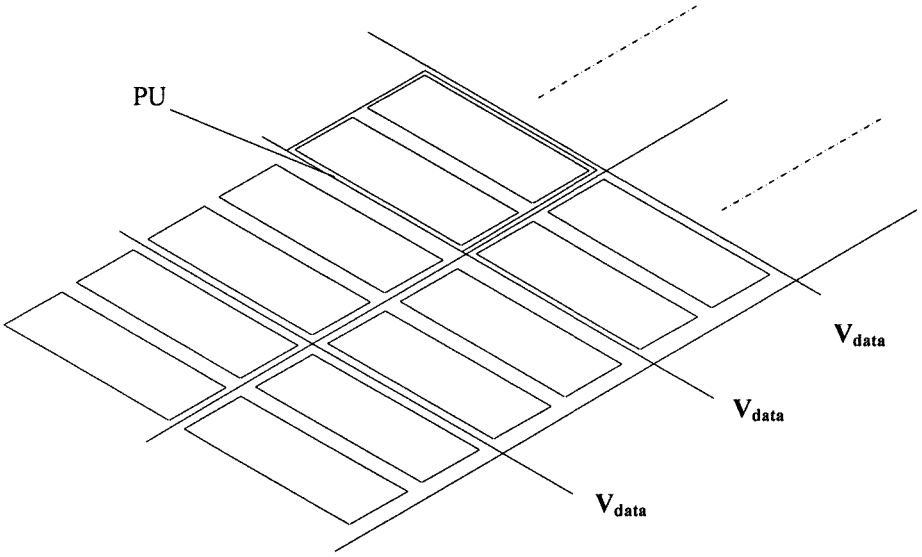


Fig. 4

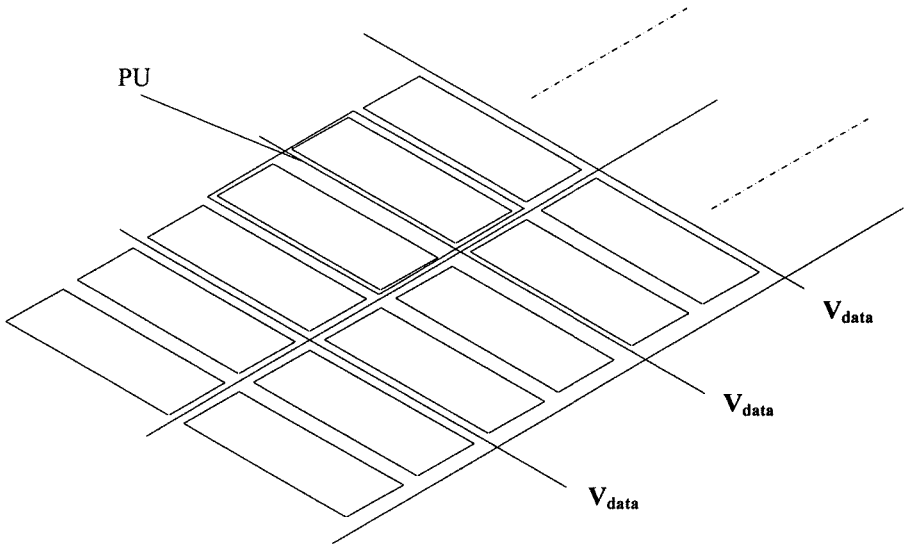


Fig. 5

## REFERENCES CITED IN THE DESCRIPTION

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| | | | |
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| 优先权 | 201410265700.3 2014-06-13 CN | | |
| 其他公开文献 | EP3159879A4<br>EP3159879A1 | | |
| 外部链接 | Espacenet | | |


摘要(译)

像素电路，包括两个子像素电路（P1，P2）和第六开关单元（T6）;第六开关单元（T6）的第一端连接到工作电压线（Vdd），第六开关单元的控制端连接到第一扫描信号线（Em）;每个子像素电路（P1，P2）包括五个开关单元（T1，T2，T3，T4，T5），驱动单元（DT），储能单元（C）和电致发光单元（L），第一子像素电路（P1）中的第一开关单元（T1）和第四开关单元（T4）与第一开关单元（T1'）和第四开关单元共享扫描信号线（Scan [3]）第二子像素电路（P2）中的（T4'）和第一子像素电路（P1）中的第三开关单元（T3）与第三开关单元共享扫描信号线（Scan [2]）（ T3'）在第二子像素电路（P2）中。像素电路完全解决了由于驱动晶体管的阈值电压的漂移导致的显示器亮度不均匀的问题。同时，一个补偿电路用于驱动两个像素，两个相邻的像素共用多条信号线，可以减少显示装置中像素电路的信号线数量，降低集成电路的成本，减小像素间距，并增加像素密度。


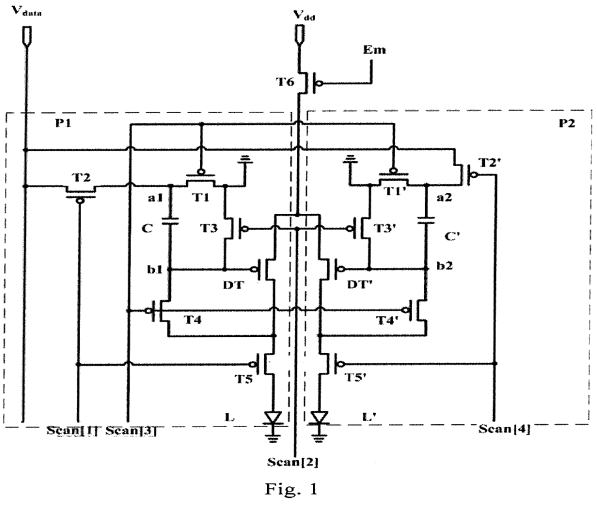

Fig. 1