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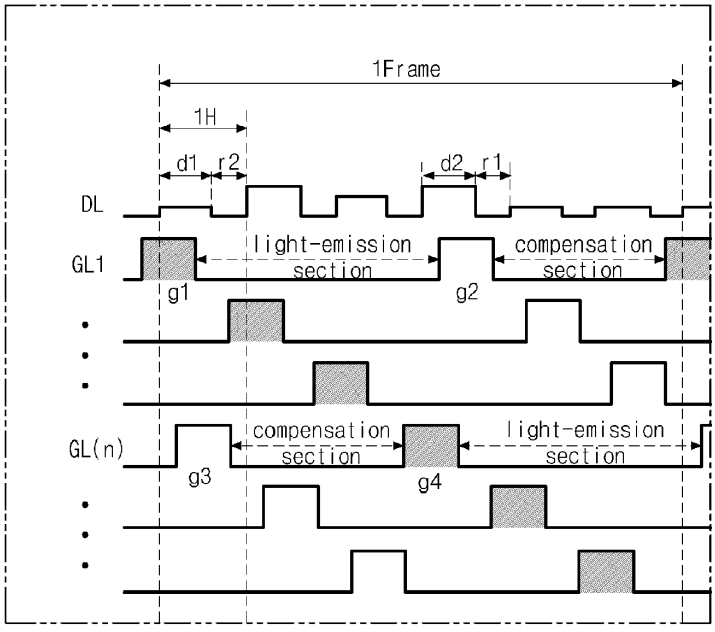
(54) METHOD OF DRIVING ORGANIC LIGHT EMITTING DIODE DISPLAY

(57) Disclosed is a organic light emitting diode display and a method of driving an organic light emitting diode display that includes a first organic light emitting diode (D1), and a first driving circuit (110) to operate the first organic light emitting diode, the method includes supplying a first gate pulse (g1) and a second gate pulse (g1) to a first gate line (GL1) connected to the first driving circuit (110), and supplying a first data signal (d1) and a first compensation signal (r1) to a data line (DL) connected to the first driving circuit (110).

FIG. 4



EP 3 121 805 A1

Description

[0001] The present application claims the priority benefit of Korean Patent Application No. 10-2015-0104280 filed in Republic of Korea on July 23, 2015.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to an organic light emitting diode display (OLED) and a method for driving the OLED display. In particular, the present invention relates to a OLED display device and a method of driving an OLED that can periodically reduce variances of threshold voltages of a driving thin film transistor and a organic light emitting diode.

Discussion of the Related Art

[0003] Recently, flat display devices, such as a plasma display panel (PDP), a liquid crystal display (LCD), and an organic light emitting diode display (OLED), have been researched.

[0004] Among the flat display devices, the OLED is a self luminescent device and can have a thin profile because the OLED does not need a backlight used for the LCD.

[0005] Further, compared with the LCD, the OLED has advantages of excellent viewing angle and contrast ratio, low power consumption, operation in low DC voltage, fast response speed, being strong to an external impact because of its solid internal components, and wide operating temperature range.

[0006] Particularly, since processes of manufacturing the OLED are simple, production cost of the OLED can be reduced more than that of the LCD.

[0007] FIG. 1 is a view illustrating organic light emitting diodes and driving circuits arranged at respective pixel regions of a display region of an OLED according to the related art, and FIG. 2 is a timing chart of gate pulses and data signals applied to the driving circuits of FIG. 1.

[0008] Referring to FIG. 1, the related art OLED includes first and second organic light emitting diodes D1 and D2 and first and second driving circuits 11 and 12 to operate the first and second organic light emitting diodes D1 and D2, respectively, in a display region 10.

[0009] In detail, the first driving circuit 11 is connected to a first gate line GL1 and each data line DL and operates the first organic light emitting diode D1, and the second driving circuit 12 is connected to a second gate line GL2 and each data line DL and operates the second organic light emitting diode D2.

[0010] For the purpose of explanations, the first and second driving circuits 11 and 12 are shown. However, a plurality of driving circuits may be arranged below the first and second driving circuits 11 and 12, and thus a plurality of gate lines may be arranged below the first and second gate lines GL1 and GL2 connected to the first and second driving circuits 11 and 12.

[0011] A method of driving the OLED is explained below.

[0012] The method of driving the OLED includes sequentially supplying first and second gate pulses g1 and g2 to the first and second gate lines GL1 and GL2, respectively, and sequentially supplying first and second data signals d1 and d2 to each data line DL.

[0013] Referring to FIG. 2, during a frame, the first gate pulse g1 is supplied to the first gate line GL1 and then the second gate pulse g2 is supplied to the second gate line GL2.

[0014] Further, the first and second data signals are sequentially supplied per horizontal period H.

[0015] Further, the first data signal d1 is supplied to the first driving circuit 11 during a overlapping section between the first gate pulse g1 and the first data signal d1, and the second data signal d2 is supplied to the second driving circuit 12 during a overlapping section between the second gate pulse g2 and the second data signal d2.

[0016] Further, the first organic light emitting diode D1 emits light in a section (i.e., a light-emission section) from a falling point of the first gate pulse g1 in the frame to a rising point of a first gate pulse g1 in a next frame, and the second organic light emitting diode D2 emits light in a section (i.e., a light-emission section) from a falling point of the second gate pulse g2 in the frame to a rising point of a second gate pulse g2 in a next frame.

[0017] As shown in FIG. 1, the first driving circuit 11 is supplied with the first data signal d1 by the first gate pulse g1, and the second driving circuit 12 is supplied with the second data signal d2 by the second gate pulse g2.

[0018] In detail, the first driving circuit 11 is supplied with the first gate pulse g1 from the first gate line GL1 and the first data signal d1 from the data line DL to make the first organic light emitting diode D1 emit light.

[0019] Then, the second driving circuit 12 is supplied with the second gate pulse g2 from the second gate line GL2 and the second data signal d2 from the data line DL to make the second organic light emitting diode D2 emit light.

[0020] Unlike an LCD including a thin film transistor which is turned on only during a relatively short time in one frame, the OLED includes a driving thin film transistor which is included in each of the first and second driving circuits 11 and 12 and maintains a turn-on state during a relatively long time in one frame. Accordingly, the driving thin film transistor of the OLED is prone to deterioration.

[0021] Accordingly, a threshold voltage (Vth) of the driving thin film transistor is varied, and this variation negatively affects a display quality of the OLED.

[0022] In other words, because of the variation of the threshold voltage (Vth), a grey level different from a grey level of a data signal is displayed, and thus the display quality of the OLED is deteriorated.

[0023] Further, when the organic light emitting diodes D1 and D2 emit light continuously during a certain time, threshold voltages of the organic light emitting diodes D1 and D2 are also varied. Accordingly, a brightness of a light emitted from the organic light emitting diode is different from a target brightness, and a lifetime of the organic light emitting diode is reduced.

SUMMARY OF THE INVENTION

[0024] Accordingly, the present invention is directed to an OLED and a method of driving an OLED that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0025] An object of the present invention is to periodically reduce variances of threshold voltages of a driving thin film transistor and an organic light emitting diode.

[0026] Additional features and advantages of the disclosure will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the disclosure. The advantages of the disclosure will be realized and attained by the structure particularly pointed out in the written description and claims as well as the appended drawings.

[0027] The object is solved by the features of the independent claims.

[0028] To achieve these and other advantages, and in accordance with the purpose of the present invention, as embodied and broadly described herein, a method of driving an organic light emitting diode display that includes a first organic light emitting diode, and a first driving circuit to operate the first organic light emitting diode, the method includes supplying a first gate pulse and a second gate pulse to a first gate line connected to the first driving circuit, and supplying a first data signal and a first compensation signal to a data line connected to the first driving circuit.

[0029] Preferably, the organic light emitting diode display further includes a n^{th} organic light emitting diode, and a n^{th} driving circuit to operate the n^{th} organic light emitting diode, where n is an integer of 2 or greater.

[0030] Preferably, the method may comprise sequentially supplying a third gate pulse and a fourth gate pulse to a n^{th} gate line connected to the n^{th} driving circuit.

[0031] Preferably, the method may comprise sequentially supplying a second compensation signal and a second data signal to a data line connected to the n^{th} driving circuit.

[0032] Preferably, the first gate pulse and the second gate pulse are sequentially supplied to the first gate line connected to the first driving circuit, and the first data signal and the first compensation signal are sequentially supplied to the data line connected to the first driving circuit.

[0033] Preferably, the third gate pulse and the fourth gate pulse are sequentially supplied to the n^{th} gate line connected to the n^{th} driving circuit, and the second compensation signal and the second data signal are sequentially supplied to the data line connected to the n^{th} driving circuit.

[0034] Preferably, the first and second gate pulses are supplied during one frame,

[0035] Preferably, the third and fourth gate pulses are supplied during one frame.

[0036] Preferably, the first data signal and the second compensation signal are sequentially supplied during one horizontal period.

[0037] Preferably, the second data signal and the first compensation signal are sequentially supplied during one horizontal period.

[0038] Preferably, the first and second compensation signals have a voltage level lower than the first and second data signals.

[0039] Preferably, the first and third gate pulses are sequentially supplied.

[0040] Preferably, the fourth and second gate pulses are sequentially supplied.

[0041] Preferably, the first driving circuit is supplied with the first data signal and the first compensation signal by the first gate pulse and the second gate pulse, respectively, and the n^{th} driving circuit is supplied with the second compensation signal and the second data signal by the third gate pulse and the fourth gate pulse, respectively.

[0042] Preferably, the third gate signal overlaps the first gate signal, and the third gate signal overlaps the first data signal and the second compensation signal.

[0043] Preferably, the organic light emitting diode display further includes: a gate driver that supplies the first gate pulse and the second gate pulse to the first gate line connected to the first driving circuit; and a data driver that supplies the first data signal and the first compensation signal to the data line connected to the first driving circuit.

[0044] Preferably, the gate driver supplies the third gate pulse and the fourth gate pulse to the n^{th} gate line connected to the n^{th} driving circuit, and the data driver supplies the second compensation signal and the second data signal to the data line connected to the n^{th} driving circuit.

[0045] Preferably, a ratio of supplying sections of the first data signal and the second compensation signal is adjusted and a ratio of supplying sections of the second data signal and the first compensation signal is adjusted.

[0046] Preferably, the object is also solved by an organic light emitting diode display including a display panel including a first organic light emitting diode and a first driving circuit to operate the first organic light emitting diode; a gate driver that supplies a first gate pulse and a second gate pulse to a first gate line connected to the first driving circuit; and a data driver that supplies a first data signal and a first compensation signal to a data line connected to the first driving circuit.

[0047] Preferably, the display panel further includes a n^{th} organic light emitting diode and a n^{th} driving circuit to operate the n^{th} organic light emitting diode, where n is an integer of 2 or greater, the gate driver supplies a third

gate pulse and a fourth gate pulse to a n^{th} gate line connected to the n^{th} driving circuit, and the data driver supplies a second compensation signal and a second data signal to a data line connected to the n^{th} driving circuit.

[0048] Preferably, the gate driver sequentially supplies the first gate pulse and the second gate pulse to the first gate line connected to the first driving circuit, and sequentially supplies the third gate pulse and the fourth gate pulse to the n^{th} gate line connected to the n^{th} driving circuit, and the data driver sequentially supplies the first data signal and the first compensation signal to the data line connected to the first driving circuit, and sequentially supplies the second compensation signal and the second data signal to the data line connected to the n^{th} driving circuit.

[0049] The object is also solved by an organic light emitting diode display including first and n^{th} organic light emitting diodes, and first and n^{th} driving circuits to operate the first and n^{th} organic light emitting diodes, respectively, where n is an integer of 2 or greater, wherein each driving circuit includes a driving thin film transistor, a switching thin film transistor, a sensing thin film transistor and a capacitor, wherein each driving circuit is operated in a charging section of the data signal for charging the data signal to a gate electrode of the driving transistor and for charging a reference voltage to a source electrode of the driving transistor, and in a light-emission section of the organic light emitting diode, and wherein each driving circuit is operated in a charging section of the compensation signal for charging the compensation signal to the gate electrode of the driving transistor and to the source electrode of the driving transistor and in a compensation section of the driving transistor.

[0050] Preferably, the switching thin film transistor is turned on by a first gate pulse supplied through a first gate line and the sensing thin film transistor is turned on by a sensing signal supplied through a sensing line in charging section of the data signal

[0051] Preferably, the switching thin film transistor and the sensing thin film transistor are turned off in a light-emission section of the organic light emitting diode.

[0052] Preferably, the switching thin film transistor is turned on by a second gate pulse supplied through a first gate line and the sensing thin film transistor is turned off in a charging section of the compensation signal.

[0053] Preferably, the sensing thin film transistor is adapted to reset or initialize a current flowing to the organic light emitting diode according to the reference voltage supplied through the sensing sync line.

[0054] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0055] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this specification, illustrate embodiments of the disclosure and together with the description serve to explain the principles of the disclosure. In the drawings:

FIG. 1 is a view illustrating organic light emitting diodes and driving circuits arranged at respective pixel regions of a display region of an OLED according to the related art;

FIG. 2 is a timing chart of gate pulses and data signals applied to the driving circuits of FIG. 1;

FIG. 3 is a view illustrating organic light emitting diodes and driving circuits arranged at respective pixel regions of a display region of an OLED according to an embodiment of the present invention;

FIG. 4 is a timing chart of gate pulses, data signals and compensation signals applied to the driving circuits of FIG. 3;

FIGs. 5A to 5D are views illustrating an organic light emitting diode and a driving circuit of one pixel of an OLED according to the embodiment of the present invention; and

FIG. 6 is a timing chart of signals, including a gate pulse, a data signal and a compensation signal, supplied to the driving circuit of FIGs. 5A to 5D.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0056] Reference will now be made in detail to embodiments, examples of which are illustrated in the accompanying drawings. The same or like reference numbers may be used throughout the drawings to refer to the same or like parts.

[0057] FIG. 3 is a view illustrating organic light emitting diodes and driving circuits arranged at respective pixel regions of a display region of an OLED according to an embodiment of the present invention, and FIG. 4 is a timing chart of gate pulses, data signals and compensation signals applied to the driving circuits of FIG. 3.

[0058] Referring to FIG. 3, the OLED of the embodiment includes first and nth organic light emitting diodes D1 and D(n) and first and nth driving circuits 110 and 120 to operate the first and nth organic light emitting diodes D1 and D(n), respectively, in a display region 100, and n is an integer greater than 1.

[0059] In detail, the first driving circuit 110 is connected to a first gate line GL1 and each data line DL and operates the first organic light emitting diode D1, and the nth driving circuit 120 is connected to an nth gate line GL(n) and each data line DL and operates the nth organic light emitting diode D(n).

[0060] For the purpose of explanations, the first and

nth driving circuits 110 and 120 are shown. However, a plurality of driving circuits may be arranged between the first and nth driving circuits 110 and 120, and thus a plurality of gate lines may be arranged between the first and nth gate lines GL1 and GL(n) connected to the first and nth driving circuits 110 and 120.

[0061] Further, a plurality of driving circuits may be arranged below the nth driving circuit 120, and thus a plurality of gate lines may be arranged below the nth gate line GL(n).

[0062] A method of driving the OLED of the embodiment is explained below.

[0063] The method of driving the OLED includes sequentially supplying a first gate pulse g1 and a second gate pulse g2 to the first gate line GL1 connected to the first driving circuit 110, and sequentially supplying a first data signal d1 and a first compensation signal r1 to each data line DL connected to the first driving circuit 110.

[0064] Further, the method further includes sequentially supplying a third gate pulse g3 and a fourth gate pulse g4 to the nth gate line GL(n) connected to the nth driving circuit 120, and sequentially supplying a second compensation signal r2 and a second data signal d2 to each data line DL connected to the nth driving circuit 120.

[0065] Referring to FIG. 4, during a frame, the first gate pulse g1 and the second gate pulse g2 are sequentially supplied to the first gate line GL1, and the third gate pulse g3 and the fourth gate pulse g4 are sequentially supplied to the nth gate line GL(n).

[0066] In other words, during a frame, two gate pulses are sequentially supplied to each gate line.

[0067] Further, the first gate pulse g1 and the third gate pulse g3 are sequentially supplied, and the fourth gate pulse g4 and the second gate pulse g2 are sequentially supplied.

[0068] In detail, the first gate pulse g1 is supplied to the first gate line GL1, and then the third gate pulse g3 is supplied to the nth gate line GL(n).

[0069] Next, the fourth gate pulse g4 is supplied to the nth gate line GL(n), and then the second gate pulse g2 is supplied to the first gate line GL1.

[0070] The first to fourth gate pulses g1 to g4 may have the same pulse width.

[0071] Further, the first data signal d1 and the second compensation signal r2 are sequentially supplied during a horizontal period H, and the second data signal d2 and the first compensation signal r1 are sequentially supplied during another horizontal period H

[0072] In other words, during each horizontal period H, each data signal d1 or d2 and each compensation signal r1 or r2 are sequentially supplied to each data line.

[0073] A ratio of supplying sections of the first data signal d1 and the second compensation signal r2 may be adjusted, and a ratio of supplying sections of the second data signal d2 and the first compensation signal r1 may be adjusted.

[0074] Further, gate pulses supplied to different gate lines may overlap each other, and by sequentially supplying the data signal d1 or d2 and the compensation signal r1 or r2 during one horizontal period H, the data signal d1 or d2 and the compensation signal r1 or r2 interfering with each other can be prevented. In this regard, for example, the third gate signal g3 may be overlap the first gate signal g1, and the third gate signal g3 may overlap the second compensation signal r2 and the first data signal d1 as well during the corresponding horizontal period H.

[0075] In this case, the first and second compensation signals r1 and r2 have voltage levels lower than the first and second data signals d1 and d2.

[0076] For example, because the first and second data signals d1 and d2 generally have a voltage level greater than 0V i.e., a positive polarity, the first and second compensation signals r1 and r2 preferably have a voltage level of 0V.

[0077] Further, in an overlapping section between the first gate pulse g1 and the first data signal d1, the first data signal d1 is supplied to the first driving circuit 110. In an overlapping section between the second gate pulse g2 and the first compensation signal r1, the first compensation signal r1 is supplied to the first driving circuit 110.

[0078] Further, in an overlapping section between the third gate pulse g3 and the second compensation signal r2, the second compensation signal r2 is supplied to the nth driving circuit 120. In an overlapping section between the fourth gate pulse g4 and the second data signal d2, the second data signal d2 is supplied to the nth driving circuit 120.

[0079] Further, in a section (i.e., a light-emission section) from a falling point of the first gate pulse g1 to a rising point of the second gate pulse g2, the first organic light emitting diode D1 emits light. In a section (i.e., a compensation section) from a falling point of the second gate pulse g2 to a rising point of a first gate pulse g1 of a next frame, the first organic light emitting diode D1 does not emit light.

[0080] Further, in a section (i.e., a compensation section) from a falling point of the third gate pulse g3 to a rising point of the fourth gate pulse g4, the nth organic light emitting diode D(n) does not emit light. In a section (i.e., a light-emission section) from a falling point of the fourth gate pulse g4 to a rising point of a third gate pulse g3 of a next frame, the nth organic light emitting diode D(n) emits light.

[0081] Further, a ratio of the light-emission section and the compensation section may be adjusted according to the ratio of supplying sections of the data signal d1 or d2 and the compensation signal r1 or r2. Further, when adjusting the ratio of the light-emission section and the compensation section, the third gate signal g3 may not overlap the first gate signal g1 (e.g., the third gate signal g3 and the first gate signal g1 may be at different horizontal periods), and the second compensation signal r2 by the third gate signal g3 may not be immediately next to the first data signal d1 by the first gate signal g1 (e.g., the second compensation signal r2 and the first data signal

d1 may be at different horizontal periods).

[0082] As shown in FIG. 3, the first driving circuit 110 is supplied with the first data signal d1 and the first compensation signal r1 by the first gate pulse g1 and the second gate pulse g2, and the nth driving circuit 120 is supplied with the second compensation signal r2 and the second data signal d2 by the third gate pulse g3 and the fourth gate signal g4.

[0083] In detail, the first driving circuit 110 is supplied with the first gate pulse g1 from the first gate line GL1 and the first data signal d1 from the data line DL to make the first organic light emitting diode D1 emit light, and then is supplied with the second gate pulse g2 from the first gate line GL1 and the first compensation signal r1 from the data line DL to make the first organic light emitting diode D 1 not emit light

[0084] Further, the nth driving circuit 120 is supplied with the third gate pulse g3 from the nth gate line GL(n) and the second compensation signal r2 from the data line DL to make the nth organic light emitting diode D(n) not emit light, and then is supplied with the fourth gate pulse g4 from the nth gate line GL(n) and the second data signal d2 from the data line DL to make the nth organic light emitting diode D(n) emit light.

[0085] Accordingly, the method of driving the OLED of the embodiment substantially divides one frame into the light-emission section when the first or nth organic light emitting diode D1 or D(n) emits light, and the compensation section when the first or nth organic light emitting diode D1 and D(n) does not emit light. In the compensation section, the first or second compensation signal r1 or r2 having a voltage level lower than the first or second data signal d1 or d2 is supplied to the first or nth driving circuit 110 or 120, and thus a variance of a threshold voltage of a driving thin film transistor of the first or nth driving circuit 110 or 120 and a variance of a threshold voltage of the first or nth organic light emitting diodes D1 or D(n), which are caused by a voltage corresponding to the first or second data signal d1 or d2, can be reduced periodically.

[0086] FIGs. 5A to 5D are views illustrating an organic light emitting diode and a driving circuit of one pixel of an OLED according to the embodiment of the present invention.

[0087] For the purpose of explanations, a pixel including a first organic light emitting diode D1 and a first driving circuit 110 are shown. Other pixel including an nth organic light emitting diode (D(n) of FIG. 3) and an nth driving circuit (120 of FIG. 3) have the same configuration as the pixel in FIGs. 5A to 5D.

[0088] Referring to FIGs. 5A to 5D, the first driving circuit 110 includes a driving thin film transistor DT, a switching thin film transistor SWT, a sensing thin film transistor SST and a capacitor C.

[0089] In detail, the first organic light emitting diode D1 includes an anode connected to a first node N1, and a cathode supplied with a low power voltage VSS.

[0090] The first organic light emitting diode D1 generates light having a brightness corresponding to a drain current Ids supplied from the driving thin film transistor DT.

[0091] Further, the driving thin film transistor DT includes a gate electrode G connected to a switching thin film transistor SWT, a source electrode S connected to the first node N1, and a drain electrode D supplied with a high power voltage VDD greater than the low power voltage VSS.

[0092] When the driving thin film transistor DT is supplied with a first data signal d1 from the switching thin film transistor SWT, the drain current Ids generated according to a voltage between the gate electrode G and the source electrode S of the driving thin film transistor DT flows into the first node N1.

[0093] Further, the switching thin film transistor SWT includes a gate electrode G connected to a first gate line GL1, a source electrode S connected to a data line DL, and a drain electrode D connected to the gate electrode G of the driving thin film transistor DT.

[0094] The switching thin film transistor SWT is supplied with a first or second gate pulses g1 or g2 and turned on, and thus a first data signal d1 or a first compensation signal r1 is supplied to the driving thin film transistor DT.

[0095] Further, the sensing thin film transistor SST includes a gate electrode G connected to a first sensing driving line SL1, a source electrode S connected to the first node N1, and a drain electrode D connected to a sensing sync line SSL.

[0096] The sensing thin film transistor SST functions to reset (or initialize) a current flowing on the first node N1 according to a reference voltage Vref supplied through the sensing sync line SSL.

[0097] Further, the capacitor C is connected between the first node N1 and the gate electrode G of the driving thin film transistor DT.

[0098] The capacitor C stores (i.e., is charged with) voltages corresponding to a first data signal d1 and the first compensation signal r1, respectively, and maintains the stored voltages during a frame.

[0099] Timings of the signals supplied to the first driving circuit 110 are explained below with reference to FIGs. 5A to 5D and FIG. 6.

[0100] FIG. 5A shows signals supplied to the first driving circuit 110 in a charging section of the first data signal d1, FIG. 5B shows signals supplied to the first driving circuit 110 in a light-emission section of the first organic light emitting diode D1, FIG. 5C shows signals supplied to the first driving circuit 110 in a charging section of the first compensation signal r1, and FIG. 5D shows signals supplied to the first driving circuit 110 in a compensation section of the driving thin film transistor.

[0101] FIG. 6 is a timing chart of signals, including a gate pulse, a data signal and a compensation signal, supplied to the driving circuit of FIGs. 5A to 5D.

[0102] First, in the charging section of the first data signal d1, the switching thin film transistor SWT is turned on by the first gate pulse g1 supplied through the first

gate line GL1, and the first data signal d1 from the data line DL is supplied to the gate electrode G of the driving thin film transistor DT.

[0103] At the same timing as the first gate pulse g1, the sensing thin film transistor SST is turned on by a sensing signal s1 supplied through the first sensing driving line SL1, and the reference voltage Vref from the sensing sync line SSL is supplied to the first node N1 i.e., the source electrode S of the driving thin film transistor DT.

[0104] By the capacitor C, the gate electrode G and the source electrode S of the driving thin film transistor DT are charged with a voltage corresponding to the first data signal d1 and the reference voltage Vref, respectively.

[0105] Next, in the light-emission section of the first organic light emitting diode D1, the switching thin film transistor SWT and the sensing thin film transistor SST are turned off. The voltage corresponding to the first data signal d1 and the reference voltage Vref at the gate electrode G and the source electrode S of the driving thin film transistor DT are boosted, and the drain current Ids according to the voltages at the gate electrode G and the source electrode S of the driving thin film transistor DT flows onto the first node N1.

[0106] In this case, the first organic light emitting diode D1 emits light having a brightness according to a level of the drain current Ids.

[0107] Next, in the charging section of the first compensation signal r1, the switching thin film transistor SWT is turned on by the second gate pulse g2 supplied through the first gate line GL1, and the first compensation signal r1 from the data line DL is supplied to the gate electrode G of the driving thin film transistor DT.

[0108] In the charging section of the first compensation signal r1, the sensing thin film transistor SST is turned off.

[0109] Accordingly, by the capacitor C, the gate electrode G and the source electrode S of the driving thin film transistor DT are charged with a voltage lower than the voltage corresponding to the first data signal r1 and a voltage lower than the reference voltage Vref, respectively.

[0110] Next, in the compensation section of the driving thin film transistor DT, the switching thin film transistor SWT is turned off. Accordingly, by the capacitor C, the gate electrode G and the source electrode S of the driving thin film transistor DT are charged with a voltage corresponding to the first compensation signal r1 and a voltage lower than the low power voltage VSS, respectively.

[0111] The first compensation signal r1 has a voltage level lower than the first data signal d1.

[0112] Accordingly, the method of driving the OLED of the embodiment divides one frame into the light-emission section when the first organic light emitting diode D1 emit light, and the compensation section when the first organic light emitting diode D1 does not emit light. In the compensation section, the first compensation signal r1 having a voltage level lower than the first data signal d1 is supplied to the first driving circuit 110, and thus a variance of a threshold voltage of the driving thin film transistor DT and a variance of a threshold voltage of the first organic light emitting diode D1, which are caused by the voltage corresponding to the first data signal d1, can be reduced periodically.

[0113] In a preferred embodiment the light emission section is longer than the compensation section.

[0114] It will be apparent to those skilled in the art that various modifications and variations can be made in a display device of the present invention without departing from the scope of the disclosure. Thus, it is intended that the present invention covers the modifications and variations of this disclosure provided they come within the scope of the appended claims and their equivalents

Claims

1. A method of driving an organic light emitting diode display that includes a first organic light emitting diode (D1), and a first driving circuit (110) to operate the first organic light emitting diode (D1), the method comprising:

   supplying a first gate pulse (g1) and a second gate pulse (g2) to a first gate line (GL1) connected to the first driving circuit (110); and
   supplying a first data signal (d1) and a first compensation signal (r1) to a data line (DL) connected to the first driving circuit (110).

2. The method of claim 1, wherein the organic light emitting diode display further includes a n^{th} organic light emitting diode (Dn), and a n^{th} driving circuit (120) to operate the n^{th} organic light emitting diode (Dn), where n is an integer of 2 or greater,
   the method further comprising:

   supplying a third gate pulse (g3) and a fourth gate pulse (g4) to a n^{th} gate line (GLn) connected to the n^{th} driving circuit (120); and
   supplying a second compensation signal (r2) and a second data signal (d2) to a data line (DL) connected to the n^{th} driving circuit (120).

3. The method of claim 1 or 2, wherein the first gate pulse (g1) and the second gate pulse (g2) are sequentially supplied to the first gate line (GL1) connected to the first driving circuit (110), and the first data signal (d1) and the first compensation signal (r1) are sequentially supplied to the data line DL connected to the first driving circuit (110).

4. The method of claim 2 or 3, wherein the third gate pulse (g3) and the fourth gate pulse (g4) are sequentially supplied to the n^{th} gate line (GLn) connected to the n^{th} driving circuit (120), and the second com-

pensation signal (r2) and the second data signal (d2) are sequentially supplied to the data line (DL) connected to the n^{th} driving circuit (120).

5. The method as claimed in any one of claims 2 to 4, wherein the first and second gate pulses (g1, g2) are supplied during one frame, and the third and fourth gate pulses (g3, g4) are supplied during one frame.

6. The method as claimed in any one of the preceding claims 2 to 5, wherein the first data signal (d1) and the second compensation signal (r2) are sequentially supplied during one horizontal period (1H), and the second data signal (d2) and the first compensation signal (r1) are sequentially supplied during one horizontal period (1H).

7. The method as claimed in any one of the preceding claims 2 to 6, wherein the first and second compensation signals (r1, r2) have a voltage level lower than the first and second data signals (d1, d2).

8. The method as claimed in any one of the preceding claims 2 to 7, wherein the first and third gate pulses (g1, g3) are sequentially supplied, and the fourth and second gate pulses (g4, g2) are sequentially supplied.

9. The method as claimed in any one of the preceding claims 2 to 8, wherein the first driving circuit (110) is supplied with the first data signal (d1) and the first compensation signal (r1) by the first gate pulse (g1) and the second gate pulse (g2), respectively, and the n^{th} driving circuit (120) is supplied with the second compensation signal (r2) and the second data signal (d2) by the third gate pulse (g3) and the fourth gate pulse (g4), respectively.

10. The method as claimed in any one of the preceding claims 2 to 9, wherein the third gate signal (g3) overlaps the first gate signal (g1), and the third gate signal (g3) overlaps the first data signal (d1) and the second compensation signal (r2).

11. The method as claimed in any one of the preceding claims, wherein the organic light emitting diode display further includes:

a gate driver that supplies the first gate pulse (g1) and the second gate pulse (g2) to the first gate line (GL1) connected to the first driving circuit (110); and
a data driver that supplies the first data signal (d1) and the first compensation signal (r1) to the data line (DL) connected to the first driving circuit (110).

12. The method as claimed in any one of the preceding claims, wherein the gate driver supplies the third gate pulse (g3) and the fourth gate pulse (g4) to the n^{th} gate line (GLn) connected to the n^{th} driving circuit (120), and wherein the data driver supplies the second compensation signal (r2) and the second data signal (d2) to the data line DL connected to the n^{th} driving circuit (120).

13. An organic light emitting diode display, comprising:

a display panel including a first organic light emitting diode (D1) and a first driving circuit (110) to operate the first organic light emitting diode (D1);
a gate driver that supplies a first gate pulse (g1) and a second gate pulse (g2) to a first gate line (GL1) connected to the first driving circuit (110); and
a data driver that supplies a first data signal (d1) and a first compensation signal (r1) to a data line (DL) connected to the first driving circuit (120).

14. The display of claim 13, wherein the display panel further includes a n^{th} organic light emitting diode (Dn) and a n^{th} driving circuit (120) to operate the n^{th} organic light emitting diode (Dn), where n is an integer of 2 or greater,
wherein the gate driver supplies a third gate pulse (g3) and a fourth gate pulse (g4) to a n^{th} gate line (GLn) connected to the n^{th} driving circuit (120), and wherein the data driver supplies a second compensation signal (r2) and a second data signal (d2) to a data line (DL) connected to the n^{th} driving circuit (120).

15. The display of claim 14, wherein the gate driver sequentially supplies the first gate pulse (g1) and the second gate pulse (g2) to the first gate line (GL1) connected to the first driving circuit (110), and sequentially supplies the third gate pulse (g3) and the fourth gate pulse (g4) to the n^{th} gate line (GLn) connected to the n^{th} driving circuit (120), and
wherein the data driver sequentially supplies the first data signal (d1) and the first compensation signal (r1) to the data line (DL) connected to the first driving circuit (110), and sequentially supplies the second compensation signal (r2) and the second data signal (d2) to the data line (DL) connected to the n^{th} driving circuit (120).

FIG. 1 (RELATED ART)

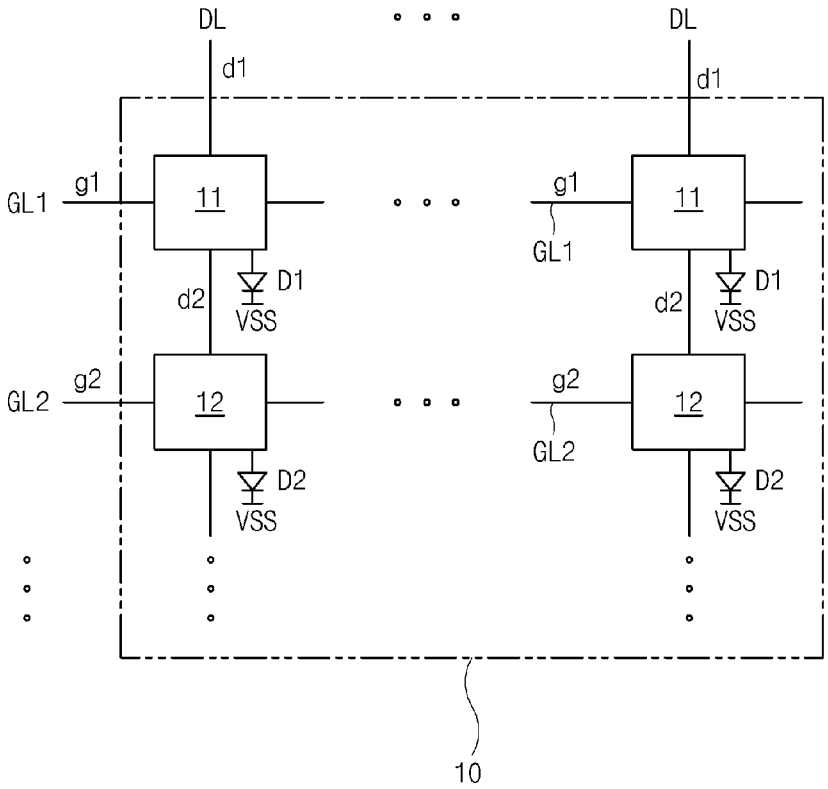


FIG. 2 (RELATED ART)

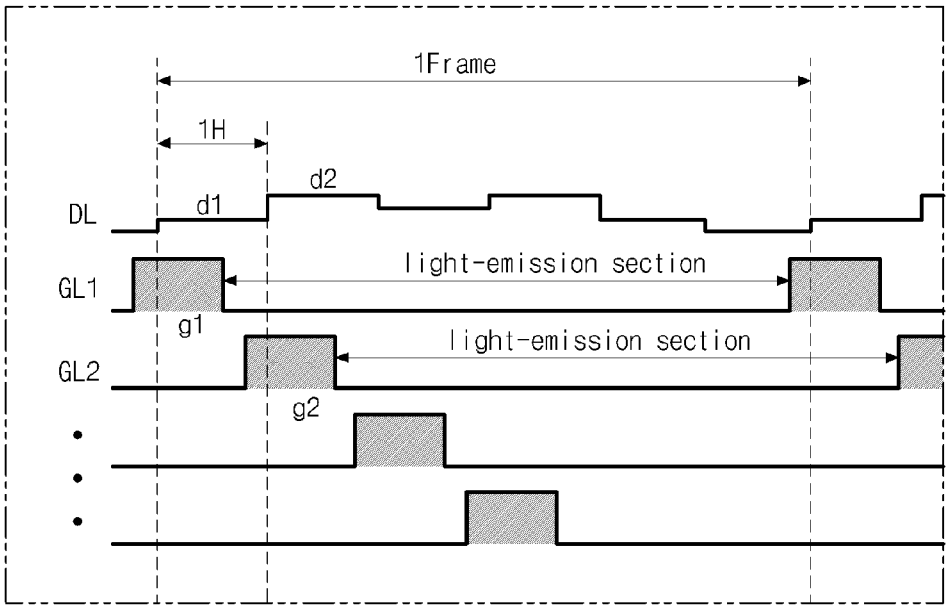


FIG. 3

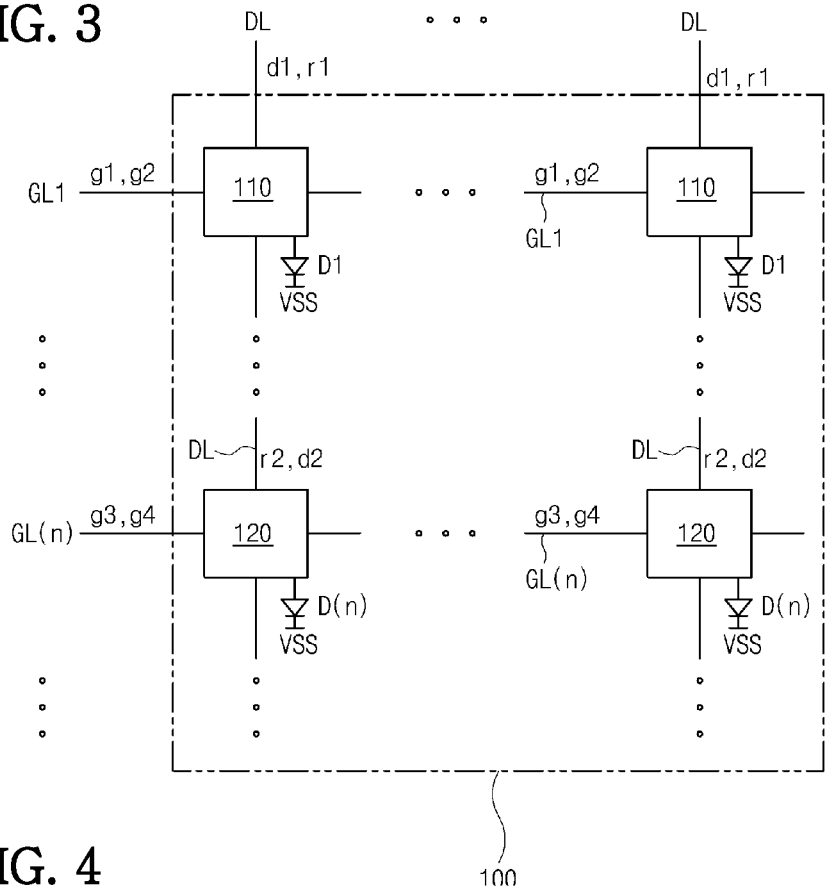

DL
d1,r1
GL1
g1,g2
110
D1
VSS
GL(n)
g3,g4
120
D(n)
r2,d2
100

FIG. 4

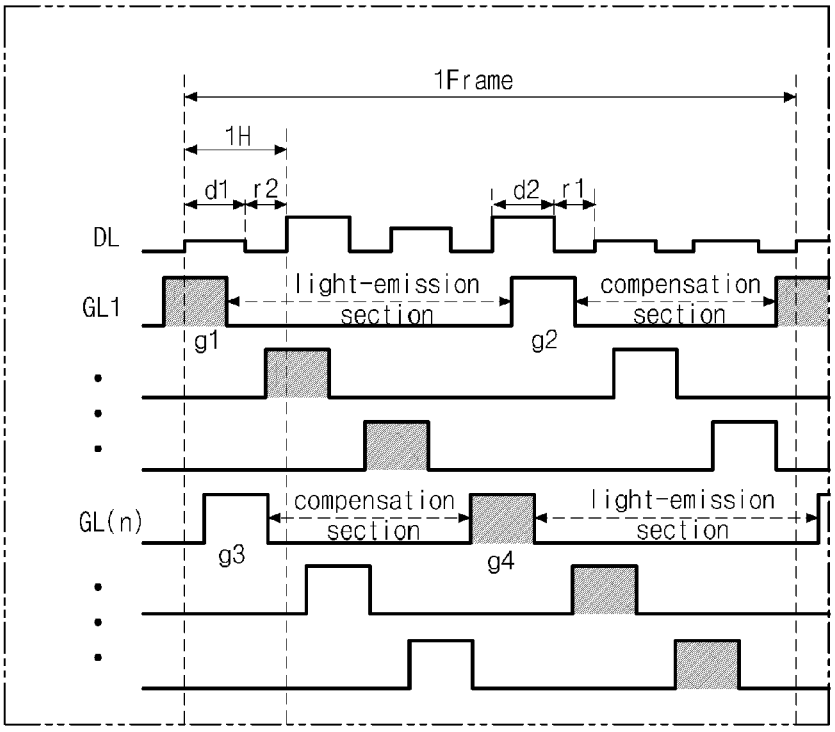

1Frame
1H
d1
r2
d2
r1
DL
GL1
light-emission section
compensation section
g1
g2
GL(n)
g3
g4

FIG. 5A

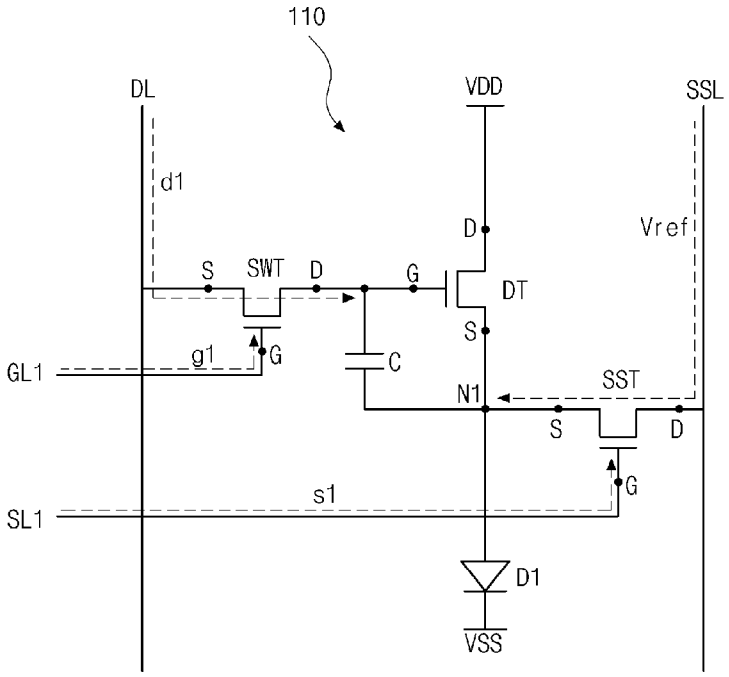

110
DL
VDD
SSL
d1
D
Vref
S
SWT
D
G
DT
S
g1
G
C
GL1
N1
SST
S
D
G
s1
SL1
D1
VSS

FIG. 5B

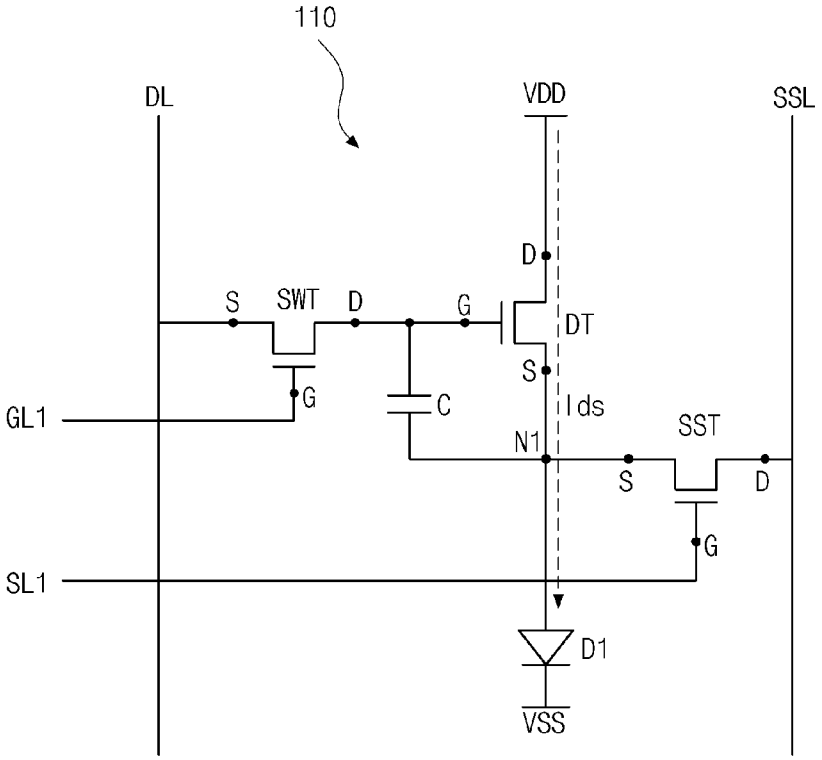

110
DL
VDD
SSL
D
S
SWT
D
G
DT
S
G
C
Ids
GL1
N1
SST
S
D
G
SL1
D1
VSS

FIG. 5C

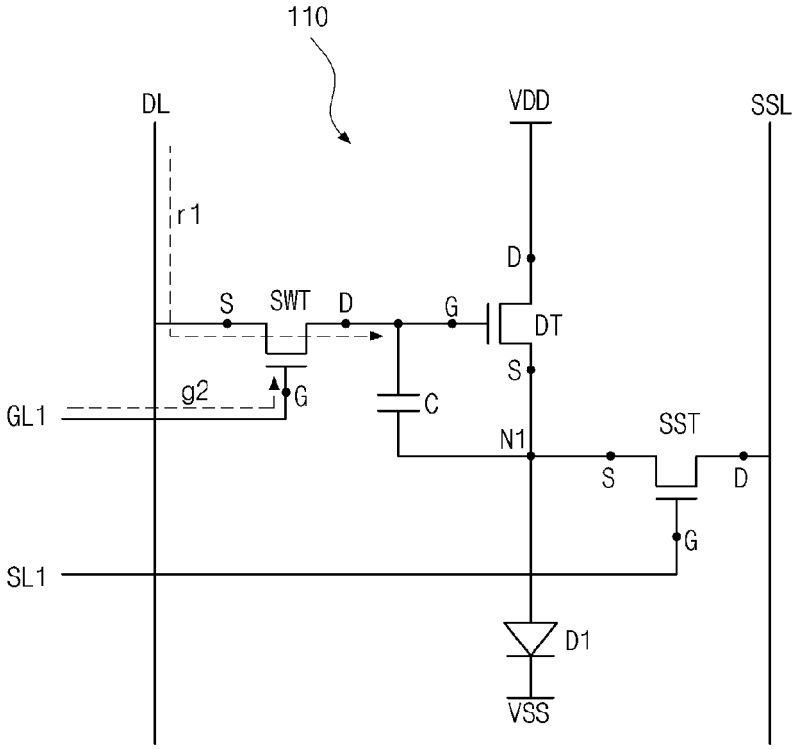

110
DL
VDD
SSL
r1
D
S
SWT
D
G
DT
S
g2
G
C
GL1
N1
SST
S
D
G
SL1
D1
VSS

FIG. 5D

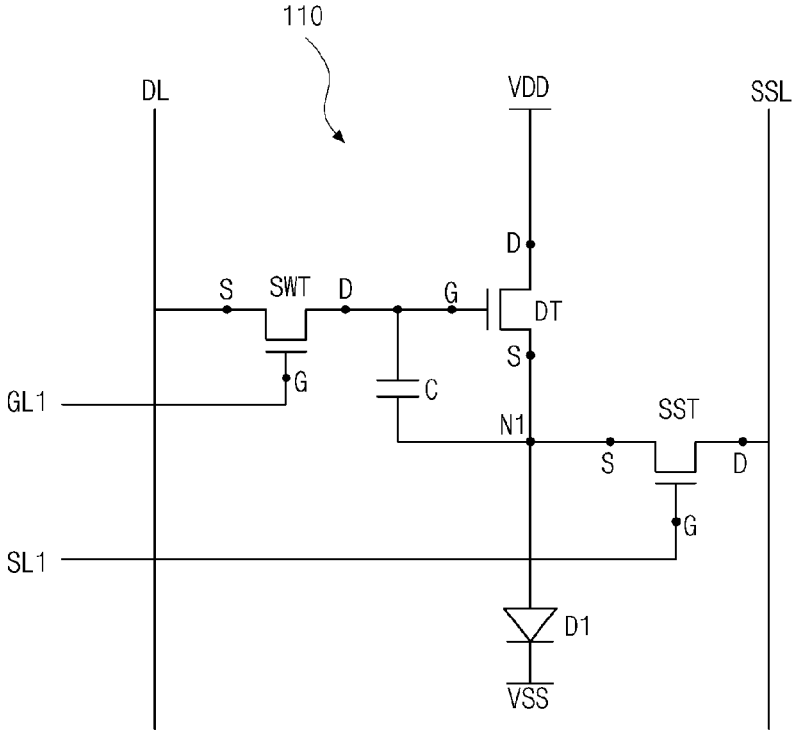
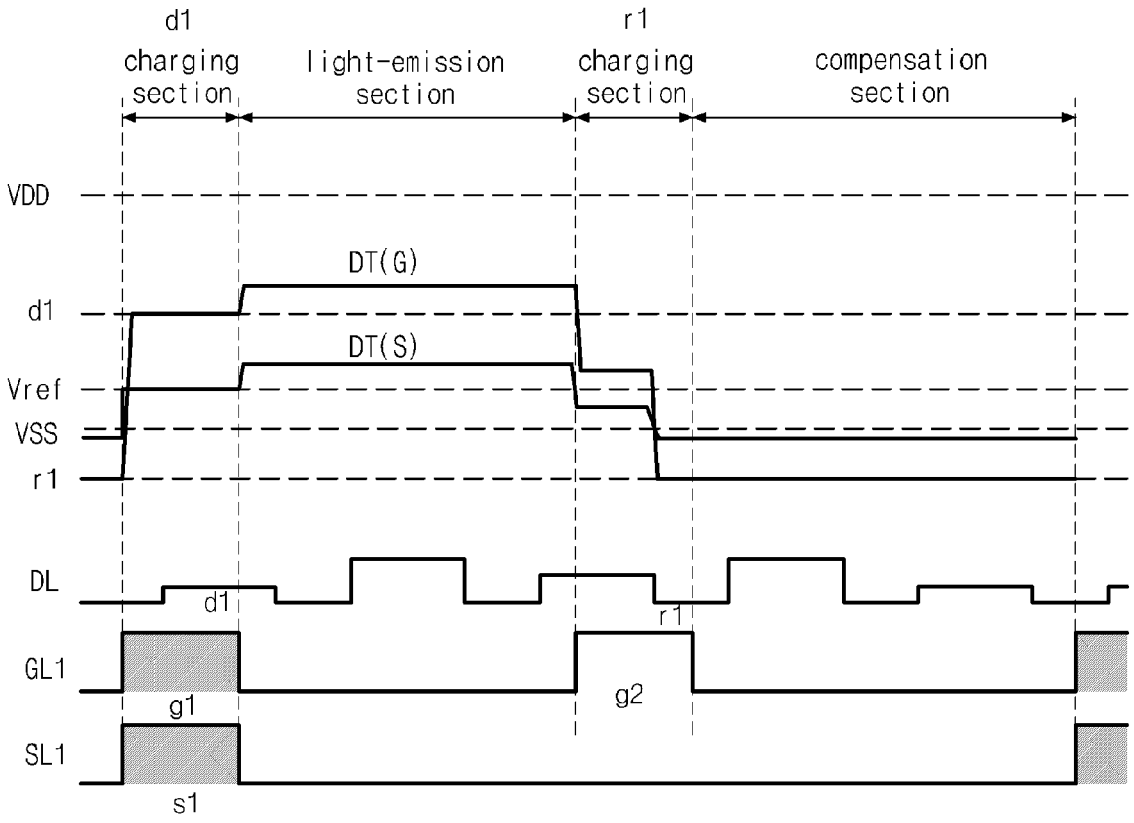

110
DL
VDD
SSL
D
S
SWT
D
G
DT
S
G
C
GL1
N1
SST
S
D
G
SL1
D1
VSS

FIG. 6


d1
charging
section
light-emission
section
r1
charging
section
compensation
section
VDD
DT(G)
d1
DT(S)
Vref
VSS
r1
DL
d1
r1
GL1
g1
g2
SL1
s1

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EUROPEAN SEARCH REPORT

Application Number
EP 16 18 0868

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X Y	US 2010/091006 A1 (YOO MYOUNG-HWAN [KR] ET AL) 15 April 2010 (2010-04-15) * paragraphs [0003], [0025] - [0033], [0043], [0048] - [0049], [0057] - [0060], [0062] *	1-5,7, 11-15 4,6,8-10	INV. G09G3/32
Y	US 2008/238897 A1 (KIMURA HIROAKI [JP]) 2 October 2008 (2008-10-02) * paragraphs [0042] - [0045], [0050], [0059] - [0060], [0085] - [0086], [0101]; figures 1,7,8 *	4,6,8-10	
Y	US 2001/003448 A1 (NOSE TAKASHI [JP] ET AL) 14 June 2001 (2001-06-14) * paragraphs [0014] - [0022], [0064] - [0069]; figures 1-2 *	4,6,8-10	
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Y	US 2012/235973 A1 (YOO MYOUNG-HWAN [KR]) 20 September 2012 (2012-09-20) * paragraph [0157]; figure 12H *	10	TECHNICAL FIELDS SEARCHED (IPC) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	22 September 2016	Taron, Laurent

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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22-09-2016

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专利名称(译)	驱动有机发光二极管显示的方法		
公开(公告)号	EP3121805A1	公开(公告)日	2017-01-25
申请号	EP2016180868	申请日	2016-07-22
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	RYU HON JIN KIM SEONG HYUN		
发明人	RYU, HON-JIN KIM, SEONG-HYUN		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3208 G09G3/2081 G09G3/3233 G09G2310/0205 G09G2310/0251 G09G2320/045 G09G3/3266 G09G3/3291		
优先权	1020150104280 2015-07-23 KR		
其他公开文献	EP3121805B1		
外部链接	Espacenet		

摘要(译)

公开了有机发光二极管显示器和驱动有机发光二极管显示器的方法，该有机发光二极管显示器包括第一有机发光二极管（D1）和用于操作第一有机发光二极管的第一驱动电路（110），该方法包括向连接到第一驱动电路（110）的第一栅极线（GL1）提供第一栅极脉冲（g1）和第二栅极脉冲（g1），并且提供第一数据信号（d1）和第一补偿信号r1）连接到与第一驱动电路（110）连接的数据线（DL）。

FIG. 4