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(54) **OVER-CURRENT CONTROL DEVICE AND ORGANIC LIGHT EMITTING DISPLAY DEVICE ADPOTING THE SAME**

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Description

1. Field of the invention

[0001] The present invention relates to an organic light emitting display device adopting a function of interrupting an over-current.

2. Description of the Prior Art

[0002] An organic light emitting display device, which is highly favoured as a display device, has a high response rate, a high light-emitting efficiency, a high brightness, and a wide viewing angle by using an organic light emitting diode (OLED) that emits light by itself.

[0003] The organic light emitting display device has pixels including the organic light emitting diodes, which are arranged in a matrix, and controls the brightness of the pixels selected by scan signals according to grayscale data.

[0004] The pixels of the organic light emitting display device further include data lines and gate lines, which intersect with each other, transistors, and storage capacitors, which are connected with the lines.

[0005] The transistors included in the pixel include a driving transistor for driving the organic light emitting diode, which has characteristic parameters, such as a threshold voltage, the mobility, or the like.

[0006] Meanwhile, a driving voltage (VDD) for the driving transistor may apply an over-current which causes the device to be shut down and a fire to break out. Therefore, technology for detecting and interrupting the over-current of the driving voltage is required.

[0007] US 2012/0256897 A1 discloses an OLED display that includes a pixel unit including pixels coupled to scan lines and data lines, a DC-DC converter for outputting a first power source and a second power source when a start signal is supplied, a first power source line and a second power source line for supplying the first power source and the second power source output from the DC-DC converter to the pixel unit, and a short detecting circuit for determining whether the first power source line and the second power source line are shorted before the DC-DC converter is driven and for supplying the start signal to the DC-DC converter when the first power source line and the second power source line are not shorted.

[0008] US 2014/0084792 A1 discloses an OLED device comprising a panel; a power supply supplying power to the panel; a current detection unit detecting a current flowing through power line wiring of the panel and outputting the detected current; and a power controller comparing the detected current with a current value configured internally and outputting a shutdown signal which turns off the power supply if the detected current exceeds the predetermined current value.

[0009] US 2012/0293562 A1 discloses a DC-DC converter that includes a voltage conversion unit and a short detection unit. The voltage conversion unit is configured to generate a DC voltage for driving a display panel based on an input voltage. The short detection unit is configured to generate a driving voltage based on the DC voltage and to output the driving voltage through a power line. The short detection unit is configured to perform a short detection to detect whether the display panel is shorted based on a short detection reference that is adjusted according to an operation mode of the display panel.

[0010] US 2013/0328854 A1 discloses a display power circuit that includes a power supply circuit that receives an input voltage and generates an output voltage to power a display. A power switching device couples the output voltage from the power supply circuit to provide a display voltage for the display. A monitor circuit that generates a shut down signal based on a change of the output voltage relative to the input voltage exceeding a predetermined threshold indicating a short circuit condition of the display voltage. A control circuit disables the power switching device based on the shut down signal if the short circuit of the display voltage is detected.

[0011] US 2014/0176622 A1 discloses an OLED device that includes a display panel including a plurality of pixels formed in intersection areas between a plurality of gate lines, a plurality of data lines, and a plurality of sensing lines, a gate driver supplying a gate signal to the gate lines, a plurality of data driving ICs including a data driver, supplying data voltages to the data lines, and a sensing unit including a plurality of ADCs that each sense characteristic change of a driving transistor included in a corresponding pixel to generate sensing data, a memory storing a gain error and offset error of each ADC, and a timing controller correcting the sensing data on a basis of the gain error and offset error, modulating input data on a basis of the corrected sensing data, and supplying the modulated data to the data driving ICs.

SUMMARY OF THE INVENTION

[0012] The object is to provide an over current control device and an OLED device including, coupled to or using the same, which allow a fast and reliable detection of an over current.

[0013] The object is solved by the features of the independent claims. Preferred embodiments are given in the dependent claims.

[0014] The main idea of the present invention is to detect an over-current outside of the display panel to avoid that an over current is entering the panel and flowing through the panel.

[0015] According to one aspect of the present invention an over current control device is provided for detecting an over current provided to an OLED, comprising: an over-current identification unit adapted to compare a driving voltage on a supply line for driving the OLED with a reference voltage on a reference voltage line for identifying the over-current; an interruption unit connected between the supply line supplying the driving voltage and

the OLED for interrupting the power supply if the over-current identification unit recognizes an over-current flowing through the supply line.

[0016] Preferably, the over current control device may comprise a comparator having a first and second input and an output, the first input is connected to the supply line and the second input is connected to the reference voltage line, wherein the output of the comparator is connected with an input of the interruption unit.

[0017] Preferably, a resistor is directly connected between the supply line carrying the driving voltage and the interruption unit.

[0018] Preferably, the first input is connected to the supply line at the resistor to detect a voltage drop at the resistor on supply line.

[0019] Preferably, the comparator is realized as operational amplifier.

[0020] Preferably, the over current control device may be located on a control board which is separated from the display panel. The control board is directly receiving the driving voltage on a supply line, without any further change or influence on the driving voltage by other units. By this direct supply any change of the flowing current might be reliable detected. The control board might be connected via a connection line or flexible board to a display panel comprising the OLED. Due to this physical separation of the control board and the display panel it is avoided that the current flows for a noticeable time on the display panel. Thus, any damages on the display panel due to an over-current might be avoided.

[0021] Preferably, the interruption unit is realized as PMOS or NMOS transistor.

[0022] Preferably, the supply voltage is supplied from an external host system to the display panel comprising the OLED via a control PCB.

[0023] Preferably, the control board may be directly connected to the supply line.

[0024] Preferably, the over current control device further includes a reference voltage increasing/decreasing unit for adopting the reference voltage. Thus, an adaptation of the over-current is possible due to any external influences or due to different voltage values. So, also after manufacturing it is possible to reprogram the over current detection. Furthermore, changed external conditions like temperature or drift due to long operation time might by considered for over current detection.

[0025] Preferably, if the supply voltage on the supply line reaches the reference voltage or becomes lower than the reference voltage corresponding to the over-current, the over-current identification unit recognizes that the over-current flows through the supply line and then the interruption unit interrupts the power supply through the supply line.

[0026] Preferably, the over current control device may include a resistor connected between the supply line and the interruption unit.

[0027] Preferably, the reference voltage is the voltage applied to the sensing transistor among the thin film transistors of the pixel.

[0028] Preferably, the over current control device may comprise a reference voltage increasing/decreasing unit for adopting the reference voltage.

[0029] According to another aspect of invention a display device is provided comprising: display panel having data lines and gate lines, wherein subpixels are disposed at intersections of the data lines and gate lines; at least one source driver integrated circuit for supplying data signals to the data lines; at least one gate driver integrated circuit for supplying scanning signals to the gate lines; a controller for controlling the source driver IC and the gate driver IC and an over-current controller as described above between a power supply line and the OLED.

[0030] Preferably, the sub-pixel includes a driving transistor, an organic light emitting diode, a switching transistor, a storage capacitor and a sensing transistor, the driving transistor is connected between the supply line and the OLED and is controlled by a data voltage supplied to the gate of the driving transistor via the data line, wherein the sensing transistor is controlled by a sense signal to connect a reference voltage line with a node between the driving transistor and the OLED used for sensing a characteristic of the driving transistor.

[0031] Preferably, the reference voltage supplied to the second input of the comparator may be the voltage applied to the sensing transistor of the subpixel.

[0032] Preferably, the control board may comprise the controller for controlling the display panel.

[0033] Preferably, the driving voltage is provided from the control board to the display panel by passing through the data driver.

[0034] According to a further aspect a method for operating a display device comprising a display panel coupled to or including an over current control device is provided, wherein the method comprises the steps of: supplying a driving voltage on a supply line to an OLED of the display panel; identifying a voltage supplied to the display panel outside the display panel, wherein if identified voltage reaches a reference voltage corresponding to the over-current or becomes lower than the reference voltage corresponding to the over-current interrupting the power supply through the EVDD line outside of the display panel.

[0035] According to a further aspect an organic light emitting display device is provided, comprising: display panel that includes a plurality of data lines in the first direction, a plurality of gate lines in the second direction, and pixels defined on the intersections of the data lines and the gate lines; a driving voltage supply line that applies a driving voltage to a driving transistor among thin film transistors for controlling the pixels; and an over-current controller that comprises an over-current identification unit that identifies the over-current of the display panel by a voltage drop of the driving voltage power line, and an interruption unit that, if the over-current is identified by the over-current identification unit, interrupts the voltage of the driving voltage supply line.

[0036] Preferably, the over-current identification unit takes the driving voltage supply line as a first input port, and the reference voltage line as a second input port, and the reference voltage is equal to or greater than the voltage of the driving voltage supply line, which drops due to the over-current in the display panel, and less than the driving voltage.

[0037] Preferably, the reference voltage is the voltage that is applied to a sensing transistor among the thin film transistors positioned at the pixels.

[0038] Preferably, one end of a sensing resistor is connected with the driving voltage supply line, and the other end thereof is connected with a source of a PMOS as the interruption unit, and the over-current identification unit is an OP-Amp in which the "-" terminal of the OP-Amp is connected with the other end of the sensing resistor, the "+" terminal of the OP-Amp is applied with the reference voltage, and an output terminal of the OP-Amp is connected with a gate node of the PMOS.

[0039] Preferably, one end of a sensing resistor is connected with the driving voltage power line, and the other end thereof is connected with a source of an NMOS as the interruption unit, and the over-current identification unit is an OP-Amp in which the "+" terminal of the OP-Amp is connected with the other end of the sensing resistor, the "-" terminal of the OP-Amp is applied with the reference voltage, and an output terminal of the OP-Amp is connected with a gate node of the NMOS.

[0040] According to a further aspect an control device is provided comprising: an over-current identification unit that identifies the over-current of the display panel by identifying a voltage drop of a driving voltage power line for applying a driving voltage to a driving transistor among thin film transistors for controlling pixels of the display panel; and an interruption unit that, if the over-current is identified by the over-current identification unit, interrupts the voltage of the driving voltage power line.

[0041] Preferably, the over-current identification unit takes the driving voltage power line as a first input port, and the reference voltage line as a second input port, and the reference voltage is equal to or greater than the voltage of the driving voltage power line, which drops due to the over-current in the display panel, and less than the driving voltage.

[0042] Preferably, the reference voltage is the voltage that is applied to a sensing transistor among the thin film transistors positioned at the pixels.

[0043] Preferably, one end of a sensing resistor is connected with the driving voltage power line, and the other end thereof is connected with a source of a PMOS as the interruption unit, and the over-current identification unit is an OP-Amp in which the "-" terminal of the OP-Amp is connected with the other end of the sensing resistor, the "+" terminal of the OP-Amp is applied with the reference voltage, and an output terminal of the OP-Amp is connected with a gate node of the PMOS.

[0044] Preferably, one end of a sensing resistor is connected with the driving voltage power line, and the other end thereof is connected with a source of an NMOS as the interruption unit, and the over-current identification unit is an OP-Amp in which the "+" terminal of the OP-Amp is connected with the other end of the sensing resistor, the "-" terminal of the OP-Amp is applied with the reference voltage, and an output terminal of the OP-Amp is connected with a gate node of the NMOS.

[0045] Preferably, the over-current controller further comprises a reference voltage increasing/decreasing unit that increases or decreases the reference voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0046] The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0047]

FIG. 1 illustrates a system configuration of an organic light emitting display device 100 according to embodiments of the present invention;

FIG. 2 illustrates an equivalent circuit diagram of a sub-pixel (SP) adopting a sensing structure of a driving transistor (DRT) in an organic light emitting display device 100 according to embodiments of the present invention;

FIG. 3 illustrates a configuration of controlling the over-current by applying an automatic current limiting algorithm.

FIG. 4 illustrates a configuration of an over-current controller according to an embodiment of the present invention;

FIG. 5 illustrates a detailed configuration of an over-current controller according to an embodiment of the present invention;

FIG. 6 illustrates a detailed configuration of an over-current controller according to another embodiment of the present invention;

FIG. 7 illustrates the operation of interrupting the over-current in the configuration of FIG. 5 according to an embodiment of the present invention;

FIG. 8 illustrates the operation of interrupting the over-current in the configuration of FIG. 6 according to another embodiment of the present invention; and

FIG. 9 illustrates a configuration including a reference voltage increasing/decreasing unit for increasing and decreasing a reference voltage.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0048] Hereinafter, exemplary embodiments of the present invention will be described with reference to the accompanying drawings. In the following description, the same elements will be designated by the same reference numerals although they are shown in different drawings. Further, in the following description of the present inven-

tion, a detailed description of known functions and configurations incorporated herein will be omitted when it may make the subject matter of the present invention rather unclear.

[0049] In addition, terms, such as first, second, A, B, (a), (b) or the like may be used herein when describing components of the present invention. Each of these terminologies is not used to define an essence, order or sequence of a corresponding component but used merely to distinguish the corresponding component from other component(s). In the case that it is described that a certain structural element "is connected to", "is coupled to", or "is in contact with" another structural element, it should be interpreted that another structural element may "be connected to", "be coupled to", or "be in contact with" the structural elements as well as that the certain structural element is directly connected to or is in direct contact with another structural element.

[0050] FIG. 1 illustrates a system configuration of an organic light emitting display device 100 according to embodiments of the present invention.

[0051] Referring to FIG. 1, the organic light emitting display device 100, according to the present embodiments, may include an organic light emitting display panel 110, a data driving unit 120, a gate driving unit 130, and a timing controller 140.

[0052] The organic light emitting display panel 110 may include a plurality of data lines DL1 to DLm (m is a natural number equal to or more than 2) arranged in the first direction, a plurality of gate lines GL1 to GLn (n is a natural number equal to or more than 2) arranged in the second direction that intersects with the first direction, and a plurality of sub-pixels (SP) in a matrix.

[0053] The data driving unit 120 may supply a data voltage to the plurality of data lines DL1 to DLm to drive the same.

[0054] The gate driving unit 130 may supply scan signals in sequence to the plurality of gate lines GL1 to GLn to drive the same.

[0055] The timing controller 140 may supply control signals to the data driving unit 120 and the gate driving unit 130 to control the operations thereof.

[0056] The timing controller 140 may start scanning according to a timing implemented in each frame, and may convert image data (Data) input from a host system 150 into a data signal suitable for the data driving unit 120 to output the converted image data (Data'). In addition, the timing controller 140 may control the driving of data at proper time according to the scanning.

[0057] The gate driving unit 130 may supply voltage-on signals or voltage-off signals to the plurality of gate lines GL1 to GLn to thereby drive the same in sequence, under the control of the timing controller 140.

[0058] The gate driving unit 130 may be provided on one side of the organic light emitting display panel 110 as shown in FIG. 1, or may be on both sides thereof in some cases, according to a driving type.

[0059] In addition, the gate driving unit 130 may include a plurality of gate driver integrated circuits (ICs). The plurality of gate driver ICs may be connected to a bonding pad of the organic light emitting display panel 110 in a tape automated bonding (TAB) type or a chip-on-glass (COG) type, or may be directly mounted on the organic light emitting display panel 110 in a gate-in-panel (GIP) type. Alternatively, the gate driver ICs may be integrated on the organic light emitting display panel 110, in some cases.

[0060] The plurality of gate driver ICs set forth above may include a shift resistor, a level shifter, or the like.

[0061] When a specific gate line is opened, the data driving unit 120 may convert the image data (Data') received from the timing controller 140 into an analog data voltage (Vdata) to be thereby supplied to the plurality of data lines DL1 to DLm for driving the data lines DL1 to DLm.

[0062] The data driving unit 120 may include a plurality of source driver integrated circuits (ICs, referred to as a "data driver IC" as well). The plurality of source driver ICs may be connected to a bonding pad of the organic light emitting display panel 110 in a tape automated bonding (TAB) type or a chip-on-glass (COG) type, or may be directly mounted on the organic light emitting display panel 110. Alternatively, the source driver ICs may be integrated on the organic light emitting display panel 110, in some cases.

[0063] The plurality of source driver ICs set forth above may include a shift resistor, a latch, a digital analog converter (DAC), an output buffer, or the like, and in some cases, may further include an analog digital converter (ADC) that converts a sensed analog voltage value into a digital value to thereby output the sensed data for sub-pixel compensation (brightness difference compensation, or data compensation).

[0064] The plurality of source driver ICs may be implemented, for example, in a chip-on-film (COF) type. One end of each of the plurality of source driver ICs may be bonded with at least one source printed circuit board (S-PCB), and the other end thereof may be bonded with the bonding pad of the organic light emitting display panel 110.

[0065] Meanwhile, the host system 150 mentioned above may transmit various timing signals, such as vertical synchronization signals (Vsync), horizontal synchronization signals (Hsync), input data enable (DE) signals, or clock signals (CLK), together with the image data (Data) of an input image, to the timing controller 140.

[0066] The timing controller 140 may convert the image data (Data) received from the host system 150 into data signals suitable for the data driving unit 120 to thereby output the converted image data (Data'). In addition, the timing controller 140 may receive the timing signals, such as the vertical synchronization signal (Vsync), the horizontal synchronization signal (Hsync), the input DE signal, or the clock signal, and may create various control signals to be thereby transmitted to the data driving unit 120 and the gate driving unit 130 for controlling the same.

[0067] For example, in order to control the gate driving unit 130, the timing controller 140 may output gate control signals (GCS) including a gate start pulse (GSP) signal, a gate shift clock (GSC) signal, a gate output enable (GOE) signal, or the like.

[0068] The GSP signal may control an operation start timing of the gate driver IC constituting the gate driving unit 130. The GSC signal is a clock signal that is input to the gate driver ICs in common, and it may control a shift timing of a scan signal (a gate pulse). The GOE signal may indicate timing information of the gate driver ICs.

[0069] In order to control the data driving unit 120, the timing controller 140 may output data control signals (DCS) including a source start pulse (SSP) signal, a source sampling clock (SSC) signal, a source output enable (SOE) signal, or the like.

[0070] The SSP signal may control a data sampling start timing of the source driver ICs constituting the data driving unit 120. The SSC signal is a clock signal that controls a data sampling timing in the source driver ICs. The SOE signal may control an output timing of the data driving unit 120. In some cases, the DCS may further include a polarity control signal (POL) in order to control the polarity of the data voltage of the data driving unit 120. In the case where the image data (Data') input to the data driving unit 120 is transmitted according to the interface standard of mini low voltage differential signalling (LVDS), the SSP and the SSC may be omitted.

[0071] Referring to FIG. 1, the organic light emitting display device 100 may further include a power controller (not shown) that supplies voltages and currents to the organic light emitting display panel 110, the data driving unit 120, and the gate driving unit 130, or controls the voltages and currents. The power controller may be referred to as a power management IC (PMIC).

[0072] FIG. 2 illustrates an equivalent circuit diagram of a sub-pixel (SP) adopting a sensing structure of a driving transistor (DRT) in an organic light emitting display device 100 according to embodiments of the present invention.

[0073] Referring to FIG. 2, basically, the driving transistor (DRT) for driving the OLED is disposed in each sub-pixel (SP) of the organic light emitting display panel 110.

[0074] The driving transistor (DRT) has characteristic parameters, such as a threshold voltage, the mobility, or the like.

[0075] As the driving time increases, the driving transistor (DRT) tends to be degraded so that the characteristic parameters may be changed.

[0076] Since the degree of degradation of the driving transistors (DRT) between sub-pixels may be different from each other, there may be a difference in the characteristic parameters (the threshold voltage, and the mobility) between the driving transistors (DRT) of the sub-pixels.

[0077] This may bring about a difference in the brightness between the sub-pixels, which may cause deterioration of the picture quality.

[0078] Accordingly, in order to compensate the difference in the brightness between the sub-pixels, that is, in order to compensate the difference in the characteristic parameters between the driving transistors (DRT), it is required to sense the characteristic parameters of the driving transistors (DRT). Hereinafter, the sensing of the characteristic parameters of the driving transistor (DRT) will be referred to as "sensing of the driving transistor (DRT)."

[0079] Therefore, each sub-pixel of the organic light emitting display panel 110, according to the present embodiments, may further include a transistor {hereinafter, referred to as a sensing transistor (SENT)} that is used for the sensing of the driving transistor (DRT).

[0080] Referring to FIG. 2, more specifically, the sub-pixel (SP) having a sensing structure of the driving transistor (DRT) may include an organic light emitting diode (OLED), a driving transistor (DRT), a switching transistor (SWT), a storage capacitor (Cstg), a sensing transistor (SENT), or the like.

[0081] The driving transistor (DRT) may supply a driving current to the organic light emitting diode (OLED) to drive the same, and may have the first node (hereinafter, referred to as a "N1 node") that is electrically connected with the first electrode (e.g., an anode, or a cathode) of the organic light emitting diode (OLED), the second node (hereinafter, referred to as a "N2 node") corresponding to a gate node, and the third node (hereinafter, referred to as a "N3 node") that is electrically connected with a driving voltage line (DVL).

[0082] The switching transistor (SWT) may be controlled by a scan signal applied to the gate node through a corresponding gate line (GL), and may be electrically connected between the N2 node of the driving transistor (DRT) and the data line (DL).

[0083] The storage capacitor (Cstg) may be electrically connected between the N1 node and the N2 node of the driving transistor (DRT), and may maintain a constant voltage for one frame.

[0084] The first sensing transistor (SENT) may be controlled by the first sensing signal (SENSE), which is one of the scan signals applied to the gate node through a corresponding gate line (GL'), and may be electrically connected between the N1 node of the driving transistor (DRT) and a reference voltage line (RVL).

[0085] Referring to FIG. 2, the organic light emitting display device 100, according to the present embodiments, may further include an analog digital converter (ADC), as an entity for sensing the characteristic parameters of the driving transistor (DRT), which senses a voltage of the N1 node of the driving transistor (DRT) through the reference voltage line (RVL).

[0086] Here, the analog digital converter (ADC) may be included in the source driver IC.

[0087] Referring to FIG. 2, the organic light emitting display device 100, according to the present embodiments, may further include switches S1 and S2 that con-

nect a node (Nrvl), which is connected with the reference voltage line (RVL), to a node (Nadc), which is connected with the analog digital converter (ADC), or a supply node (Nref) of the reference voltage (Vref).

[0088] The structure of FIG. 2 may be applied to each of pixels of RGB colors. That is, the OLED of FIG. 2 is a circuit for controlling one of a blue pixel, a red pixel, or a green pixel.

[0089] As shown in FIG. 2, a single circuit controls a single pixel for a single color. The pixels emit lights of specific colors, such as R, G, B, or white (W).

[0090] The organic light emitting display panel 110 has a plurality of pixels of FIG. 2, and each pixel is applied with a driving voltage (VDD or EVDD). It is required to interrupt the over-current of the driving voltage in order to prevent the display panel 110 and the components thereof from being damaged by the over-current.

[0091] In the typical organic light emitting display device, the current flowing through the display panel varies with input images. A small current flows through the display panel in the case of a dark image, whereas a large current flows through the display panel in the case of a white or bright image. Therefore, in the case of an image that has many white patterns, the excessive current may flow through the display panel to increase power consumption. In order to address the problem of power consumption, an automatic current limiting (ACL) algorithm, which controls the current flowing through the display panel according to an input image of one frame, may be applied to limit the EVDD current through the display panel 110, but this may bring about degradation of the brightness of the display panel.

[0092] FIG. 3 illustrates a configuration of controlling the over-current by applying the automatic current limiting algorithm. In FIG. 2, the EVDD and the EVSS are connected with each pixel, and are extended to the outside of the panel as shown in FIG. 3. The EVDD voltage may be applied to the display panel 110 via a control PCB (C-PCB) 310 from the external host system (set) 150. In addition, the EVSS is connected to the outside of the display panel 110 as well.

[0093] The ACL algorithm set forth above may estimate a consumption current of the display panel 110 to obtain a gain with respect to a target current. More specifically, the ACL algorithm may calculate a total consumption current by estimating the current in each pixel, and may calculate a limiting gain from the calculated current and the target current to thereby implement the same by interworking with a peak brightness control block. Accordingly, the ACL algorithm can reduce the power consumption by limiting the peak luminance of the display panel according to the brightness of the input image, and can prevent the over-current by lowering the overall brightness when the excessive current more than a limit current is expected to flow according to a specific pattern. However, although the ACL algorithm can limit the current, the value calculated according to the ACL algorithm is not accurate, and no hardware for protecting the display panel from the over-current of the EVDD is provided. That is, in the ACL algorithm, the limit is determined by a data voltage when a configured current flows, and the current of the EVDD is not monitored directly to limit the same. Therefore, since the accurate current cannot be detected, it is more likely to fail to control the over-current.

[0094] Accordingly, the embodiment of the present invention provides a structure that prevents the inflow of the over-current through the EVDD line by adopting a simple circuit. More specifically, the embodiment of the present invention provides an over-current controller that prevents the inflow of the over-current through the EVDD line using a PMOS or NMOS and an OP-Amp. The over-current controller of the present invention may be included in the control PCB set forth above, or may be separated from the control PCB. According to another embodiment of the present invention, the over-current controller is formed between the pixel and the EVDD line to interrupt the over-current to the pixel of the display panel 110.

[0095] FIG. 4 illustrates a configuration of the over-current controller according to an embodiment of the present invention.

[0096] The over-current controller 400 may identify the over-current through a degree of a voltage drop through the EVDD line. More specifically, an over-current identification unit 410 may compare a voltage (V_evdd) of the EVDD line with a reference voltage (V_over) for identifying the over-current. If the voltage (V_evdd) of the EVDD line reaches or becomes lower than the reference voltage (V_over) corresponding to the over-current, the over-current identification unit 410 may recognize that the over-current flows through the EVDD line so the interruption unit 420 may interrupt the power through the EVDD line. That is, the over-current identification unit 400 may take the driving voltage supply line as the first input port and the reference voltage line as the second input port. Here, the reference voltage may be equal to, or greater than the voltage of the driving voltage supply line, which has dropped when the over-current flows to the display panel. In case of no over current the reference voltage may be configured to be less than the driving voltage on the supply line to make it easy to determine whether the voltage of the driving voltage supply line is within the range of the over-current. This enables the voltage drop of the driving voltage supply line due to the over-current to be easily determined, and provides a simple configuration and an accurate operation using circuits such as an OP-Amp that will be described later.

[0097] The reference voltage (V_over) of the over-current identification unit 410 may be configured as various values. For example, when the reference voltage (V_evdd) drops due to the over-current, the voltage of an allowable value may be applied as the V_over for comparison.

[0098] To make a summary of FIG. 4, the over-current identification unit 410 may identify a voltage drop of the driving voltage supply line, which applies the driving volt-

age to the driving transistor among thin film transistors for controlling the pixels of the display panel, and if it is determined that the over-current flows to the display panel 110, the interruption unit 420 interrupts the current of the driving voltage supply line to the display panel 110. That is, the over-current inside the display panel can be determined from the outside of the display panel to thereby lower the possibility of generating an over-current, so the over-current generated through the driving voltage supply line can be controlled in a manner of hardware. Therefore, the display panel may be prevented from deteriorating due to the over-current. In addition, the over-current control device 400 provided outside the display panel 110 as shown in FIG. 4 can be manufactured separately from the display panel 110 to be then combined to the same, and the over-current control device 400 is not affected by the malfunction of the display panel 110 due to the over-current to thereby maintain the normal operation thereof.

[0099] FIG. 5 illustrates a detailed configuration of the over-current controller according to an embodiment of the present invention. Here, the over-current identification unit is configured as an OP-Amp 510, and the interruption unit is configured as a PMOS 520. A resistor (Rsense) 505 may be connected between the EVDD and a source terminal of the PMOS 520. The "-" terminal of the OP-Amp 510 may be applied with the EVDD, and may be connected with the terminal "a" of the resistor (Rsense) 505. The "+" terminal of the OP-Amp 510 is applied with the reference voltage, i.e., Vref in FIG. 5, for identifying the over-current. The reference voltage (Vref) is the voltage that is applied to the sensing transistor among the thin film transistors of the pixels. Since the EVDD over-current is identified using the voltage, such as the reference voltage (Vref), applied to the display panel without applying a separate voltage as a reference voltage to the over-current identification unit, the configuration of the circuit can be simplified. The OP-Amp 510, as the over-current identification unit, may compare the voltage of the terminal "a" of the resistor (Rsense) with the reference voltage (Vref). As a result of the comparison, when the voltage of the terminal "a" of the resistor (Rsense) drops below the reference voltage (Vref) due to the over-current, the voltage of the terminal "b" increases. As a result, V_{SG} of the PMOS 520, as the interruption unit, is reduced to thereby turn off the PMOS 520. In the case of the over-current through the EVDD line, the PMOS 520 may interrupt the over-current so that the EVDD is no longer applied to the panel 110.

[0100] Equation 1 shows the relationship between the current and the voltage, which are applied to the PMOS 520.

Equation 1

$$I_{ds} = \frac{\beta_n}{2}\left(V_{SG} - |V_{th}|\right)^2\left(1 + \lambda V_{SD}\right)$$

[0101] Here, the current, which flows between the drain and the source of the PMOS 520, may be calculated using the voltage (Vsg) applied to the gate, the threshold voltage (Vth) of the PMOS, and the voltage between the source and the drain of the PMOS.

Equation 2

$$I_O \uparrow \rightarrow V_a \downarrow \rightarrow V_b \uparrow\uparrow \rightarrow V_{SG} \downarrow\downarrow$$

[0102] When the current (Io) of the resistor (Rsense) increases, according to Equation 2 above, the voltage (Va) of the terminal "a" drops, and the voltage (Vb) of the terminal "b" increases. As a result, the voltage (Vsg) of the PMOS 520 is reduced to thereby turn off the PMOS 520. Consequently, the current from the EVDD may be interrupted.

[0103] Although the Vref is applied as the reference voltage in FIG. 5, the present invention is not limited thereto, and the voltage lower than the voltage (EVDD) when no over-current flows may be applied to the "+" terminal.

[0104] The configuration of FIG. 5 can be summarized as follows. The interruption unit is configured as the PMOS 520, and the over-current identification unit is configured as the OP-Amp 510. One end of the sensing resistor 505 is connected with the driving voltage power line, and the other end thereof is connected with the source of the PMOS 520 as the interruption unit. In addition, the "-" terminal of the OP-Amp is connected with the other end of the sensing resistor 505, and the "+" terminal of the OP-Amp is applied with the reference voltage. Furthermore, the output terminal of the OP-Amp is connected with the gate node of the PMOS.

[0105] FIG. 6 illustrates a detailed configuration of the over-current controller according to another embodiment of the present invention. The embodiment of FIG. 6 adopts the NMOS instead of the PMOS of FIG. 5. In addition, the OP-Amp 610 may be used as the over-current identification unit as well, but it may be different from that of FIG. 5 in the connection thereof with the terminals.

[0106] FIG. 6 shows that the over-current identification unit is configured as an OP-Amp 610, and the interruption unit is configured as a NMOS 620. The resistor (Rsense) 505 may be connected between the EVDD and the drain terminal of the NMOS 620. The "+" terminal of the OP-Amp 610 may be applied with the EVDD, and may be connected with the terminal "c" of the resistor (Rsense) 505. The "-" terminal of the OP-Amp 610 is applied with the reference voltage, i.e., V_over1 in FIG. 6, for identifying the over-current. As a result, the OP-Amp 610, as the over-current identification unit, may compare the voltage of the terminal "c" of the resistor (Rsense) 505 with the reference voltage (V over1). As a result of the comparison, when the voltage (Vc) of the terminal "c" of the resistor (Rsense) drops below the reference voltage (V_over1) due to the over-current, the voltage (Vd) of the

terminal "d" drops. As a result, V_{SG} of the NMOS 620, as the interruption unit, is reduced to thereby turn off the NMOS 620 so that the current of the EVDD is no longer applied to the panel 110. The reference voltage (V_over1) may be configured to be lower than the voltage of the EVDD when no over-current flows.

[0107] The configuration of FIG. 6 can be summarized as follows. The interruption unit is configured as the NMOS 620, and the over-current identification unit is configured as the OP-Amp 610. One end of the sensing resistor 505 is connected with the driving voltage supply line, and the other end thereof is connected with the drain of the NMOS 620 as the interruption unit. In addition, the "+" terminal of the OP-Amp is connected with the other end of the sensing resistor 505, and the "-" terminal of the OP-Amp is applied with the reference voltage. Furthermore, the output terminal of the OP-Amp is connected with the gate node of the NMOS.

[0108] In FIGs. 5 and 6, when the voltage drops below a specific voltage due to the over-current, the current of the EVDD to the panel is interrupted to prevent the inflow of the over-current.

[0109] In FIGs. 5 and 6, the voltage applied to the panel is compared with a specific voltage to identify the over-current, and the EVDD is controlled to be applied to the panel according to the comparison result.

[0110] FIG. 7 illustrates the operation of interrupting the over-current in the configuration of FIG. 5 according to an embodiment of the present invention. The description will be made of the OP-Amp 510 as the over-current identification unit, and the PMOS 520 as the interruption unit of FIG. 5. In diagrams 710 and 720, the voltage (Va) of the terminal "a" and the reference voltage (Vref) of FIG. 5 are applied to the OP-Amp 510. The voltage (Vref) is an example of the reference voltage (V_over) for determining the over-current in FIG. 7, but a specific voltage, which is lower than the EVDD, may be applied as the reference voltage for identifying the over-current. Diagram 710 shows the case of Va > Vref. A "Low" value is output from the terminal "b" of the OP-Amp 510. As a result, the PMOS 520 is turned on, and the EVDD is applied to the panel through the PMOS 520. On the contrary, diagram 720 shows the case of Va < Vref. A "High" value is output from the terminal "b" of the OP-Amp 510. As a result, the PMOS 520 is turned off, and the EVDD is no longer applied to the panel.

[0111] Referring to FIGs. 5 and 7, one end of the sensing resistor is connected with the driving voltage supply line, and the other end of the sensing resistor is connected with the source of the PMOS 520 operating as the interruption unit. In addition, the OP-Amp 510 is used as the over-current identification unit, and the "-" terminal of the OP-Amp is connected with the other end of the sensing resistor 505. Furthermore, the "+" terminal of the OP-Amp is applied with the reference voltage to thereby identify the over-current. The output terminal of the OP-Amp is connected with the gate node of the PMOS as the interruption unit so that the PMOS may be turned off in the case of the over-current as shown in FIG. 7. The over-current of the EVDD can be prevented from flowing to the display panel by a combination of the OP-Amp and the PMOS.

[0112] FIG. 8 illustrates the operation of interrupting the over-current in the configuration of FIG. 6 according to another embodiment of the present invention. The description will be made of the OP-Amp 610 as the over-current identification unit, and the NMOS 620 as the interruption unit of FIG. 6. In diagrams 810 and 820, the voltage (Vc) of the *terminal* "c" and the reference voltage (V _over1) of FIG. 6 are applied to the OP-Amp 610. The voltage (V_over1) is the reference voltage for determining the over-current, and it may be selected from among various voltage values. Diagram 810 shows the case of Vc > V_over1. A "High" value is output from the terminal "d" of the OP-Amp 610. As a result, the NMOS 620 is turned on, and the EVDD is applied to the panel through the NMOS 620. On the contrary, diagram 820 shows the case of Vc < V_over1. A "Low" value is output from the terminal "d" of the OP-Amp 610. As a result, the NMOS 620 is turned off, and the EVDD is no longer applied to the panel.

[0113] Referring to FIGs. 6 and 8, one end of the sensing resistor is connected with the driving voltage supply line, and the other end of the sensing resistor is connected with the source of the NMOS 620 operating as the interruption unit. In addition, the OP-Amp 610 is used as the over-current identification unit. On the contrary to the configuration of FIGs. 5 and 7, the "+" terminal of the OP-Amp is connected with the other end of the sensing resistor 505, and the "-" terminal of the OP-Amp is applied with the reference voltage to thereby identify the over-current. The output terminal of the OP-Amp is connected with the gate node of the NMOS as the interruption unit so that the NMOS may be turned off in the case of the over-current as shown in FIG. 8. The over-current of the EVDD can be prevented from flowing to the display panel by a combination of the OP-Amp and the NMOS.

[0114] FIG. 9 illustrates a configuration including a reference voltage increasing/decreasing unit for increasing and decreasing the reference voltage. As described above, the reference voltage (V_over), which may be allocated with the Vref or another configured voltage, may be a reference value to identify whether or not the voltage of the driving voltage supply line corresponds to the over-current. The reference voltage may be a fixed value, or may be increased or decreased according to the frequency or features of the generation of the over-current. FIG. 9 shows the over-current controller 400 that further includes a reference voltage increasing/decreasing unit 950. The reference voltage increasing/decreasing unit 950 may apply the reference voltage (V_over) applied from the outside directly to the over-current identification unit 410. Meanwhile, the over-current identification unit 410 may feed the voltage value (V_evdd) applied to the driving voltage supply line back to the reference voltage increasing/decreasing unit 950, and the reference volt-

age increasing/decreasing unit 950 may increase or decrease the voltage (V_over'), which is to be applied to the over-current identification unit 410, with reference to the fed value.

[0115] As to an example of decreasing the voltage (V_over'), when the V_evdd decreases temporarily, it may be determined as the over-current even though it is not the over-current. In this case, the reference voltage increasing/decreasing unit 950 may reduce the voltage (V_over') to lower the reference value for identifying the over-current. As to an example of increasing the voltage (V_over'), when the V_evdd increases temporarily, it may not be determined as the over-current even though it is the over-current. In this case, the reference voltage increasing/decreasing unit 950 may increase the voltage (V_over') to raise the reference value for identifying the over-current.

[0116] Furthermore, the reference voltage increasing/decreasing unit 950 may increase or decrease the reference voltage according to the over-current identified in the display panel or the system. For example, even though the over-current identification unit 410 is not able to identify the over-current, when the over-current is identified through a separate feedback signal, the reference voltage increasing/decreasing unit 950 may increase the reference voltage to detect the over-current more accurately. Therefore, the reference voltage increasing/decreasing unit 950 may receive a signal indicating the generation of the over-current from the outside of the over-current controller 400 in order to determine the increase and the decrease in the reference voltage.

[0117] An embodiment of the present invention, in the operation of the display device, such as OLED TV sets, may prevent the over-current of the EVDD voltage from flowing to the panel of the display device to thereby attenuate the damage to the components and the panel. The EVDD current to the panel has been controlled through the ACL algorithm in the prior art, but it is not likely to detect the over-current accurately because it does not directly monitor the current.

[0118] On the contrary, according to the present invention, the over-current identification unit and the over-current interruption unit can be configured as simple hardware. In an embodiment, the current may be directly monitored in order to interrupt the EVDD over-current flowing to the panel and the components using the OP-Amp and the PMOS (or NMOS). In addition, in the case of the over-current, the PMOS or the NMOS may be promptly turned off to minimize the damage to the device.

[0119] A control device, according to an embodiment of the present invention, may be combined to the C-PCB as shown in FIG. 3. The control device may include the over-current identification unit and the over-current controller, as set forth above. A single OP-Amp and the PMOS or the NMOS may be connected to the driving voltage supply line. The OP-Amp may provide a function of identifying the over-current, and the PMOS or the NMOS may provide a function of interrupting the over-current. More specifically, a control device including the over-current controller 400 shown in FIGs. 4 to 9 may be combined to the C-PCB. The over-current identification unit, such as the OP-Amp, may identify a voltage drop of the driving voltage supply line for applying the driving voltage to the driving transistor among the thin film transistors for controlling the pixels of the display device to thereby recognize the over-current to the display panel, and the interruption unit, such as the NMOS or the PMOS, may interrupt the voltage of the driving voltage supply line when the over-current is identified by the over-current identification unit. The OP-Amp may receive the voltage of the driving voltage supply line and the reference voltage to thereby identify the over-current, and the sensing resistor may be interposed between the OP-Amp and the driving voltage supply line. The voltage (Vref) provided to the sensing transistor of the pixel may be an example of the reference voltage. In addition, the over-current interruption unit may be configured as the PMOS or the NMOS, and the type of signal input to the input terminal of the over-current identification unit has been described in FIGs. 5 to 8 above. In addition, as set forth in FIG. 9, the over-current controller may further comprise the reference voltage increasing/decreasing unit that increases or decreases the reference voltage according to the increase and the decrease in the over-current to thereby control the monitoring of the over-current of the driving voltage and the interruption of the over-current more accurately.

[0120] As shown in the embodiment of the present invention, the PMOS (or the NMOS), the OP-Amp, and the sensing resistor (Rsense) may be provided on the path of the EVDD inside the C-PCB in order to interrupt the over-current. Here, the sensing resistor may be connected between the driving voltage supply line (the EVDD line) and the source terminal of the PMOS (or the NMOS).

[0121] In the case where the over-current of the driving voltage supply line is interrupted by the PMOS, an inverting terminal of the OP-Amp is connected to the source terminal of the PMOS, and a non-inverting terminal of the OP-Amp is connected to the voltage (Vref) line for configuration. In addition, the output terminal of the OP-Amp is connected with the gate terminal of the PMOS.

[0122] In the case where the over-current of the driving voltage supply line is interrupted by the NMOS, an inverting terminal of the OP-Amp may be connected with the voltage (Vref) line. A non-inverting terminal of the OP-Amp is connected to the source terminal of the NMOS. In addition, the output terminal of the OP-Amp is connected with the gate terminal of the NMOS.

[0123] As describe above, the embodiment of the present invention provides a configuration that interrupts the EVDD applied to the OLED in the case of the over-current in order to detect the over-current and prevent damage to the panel. The embodiment of the present invention may be operated in cooperation with a conventional system or elements for detecting the over-current.

[0124] The description and the attached drawings are

provided only to exemplarily describe the technical the present invention, and it will be appreciated by those skilled in the art to which the present invention pertains that the present invention may be variously corrected and modified, for example, by coupling, separating, replacing, and changing the elements. Accordingly, the embodiments disclosed in the present invention are merely to not limit but describe the technical idea of the present invention. Further, the scope of the present invention is not limited by the embodiments. The scope of the present invention shall be construed on the basis of the accompanying claims in such a manner that all of the technical ideas included within the scope of the claims belong to the present invention.

Claims

1. A display device comprising an over current control device (400) connected in series between a supply line (EVDD) of the display device and an OLED display panel (110) of the display device for detecting an over current provided to the OLED display panel (110), wherein the display panel (110) comprises a plurality of pixels, each pixel comprises a sensing transistor (SENT) and an organic light emitting diode (OLED), wherein the sensing transistor (SENT) comprises an input terminal connected to an anode of the organic light emitting diode (OLED) and an output terminal, the over current control device (400) comprising:

   an over-current identification unit (410) adapted to compare a driving voltage (V_evdd) on the supply line (EVDD) for driving the OLED display panel (110) with a reference voltage (Vref) on a voltage line (Vref) for identifying the over-current;
   an interruption unit (420) connected between the supply line (EVDD) supplying the driving voltage (V_evdd) and the OLED display panel (110) for interrupting the power supply if the over-current identification unit (410) recognizes an over-current flowing through the supply line (EVDD);
   wherein the over-current identification unit (410) comprises:

      a comparator (510) having a first and second input and an output, the first input is connected to the supply line (EVDD) and the second input is connected to the voltage line (Vref) and is also connected to an input terminal (Nref) of a switching element (S2) of the display panel (110), wherein the output of the comparator (510) is connected with an input of the interruption unit (420),
      wherein an output terminal (Nrvl) of the switching element (S2) is connected to output terminals of the sensing transistors (SENT) of the display panel (110).

2. The display device as claimed in claim 1, wherein the over current control device further comprising: a resistor (RSense) directly connected between the supply line (EVDD) carrying the driving voltage (V_evdd) and the interruption unit (420), wherein the first input is connected to the supply line (EVDD) at the resistor (Rsense) to detect a voltage drop at the resistor (RSense) on supply line (EVDD).

3. The display device as claimed in claim 1 or 2, wherein the comparator (510) is realized as operational amplifier.

4. The display device as claimed in any one of the preceding claims, wherein the over current control device (400) is located on a control board (310) connected via a connection line or flexible board to a display panel (110) comprising the OLED, wherein the control board (310) is separated from the display panel (110).

5. The display device as claimed in claim 4, wherein the control board (310) is directly connected to the supply line (EVDD).

6. The display device as claimed in any one of the preceding claims, wherein the interruption unit (420) of the over current control device is realized as PMOS or NMOS transistor.

7. The display device as claimed in any one of the preceding claims, wherein if the voltage (V_evdd) on the supply line (EVDD) reaches the reference voltage (V_over) or becomes lower than the reference voltage (V_over) corresponding to the over-current, the over-current identification unit (410) is configured to recognize that the over-current flows through the supply line (EVDD) and then the interruption unit (420) is configured to interrupt the supply of the driving voltage (V_evdd) through the supply line (EVDD).

8. The display device according to one of the preceding claims, wherein the display panel (110) further comprises data lines (DL) and gate lines (GL), wherein subpixels are disposed at intersections of the data lines (DL) and gate lines (GL), the display device further comprises:

   at least one source driver integrated circuit (SD-IC) for supplying data signals to the data lines (DL);
   at least one gate driver integrated circuit (GDIC) for supplying scanning signals to the gate lines (GL);

a controller (140) for controlling the source driver IC (SDIC #k) and the gate driver IC (GDIC).

9. The display device as claimed in claim 8, wherein the pixel (SP) further includes a driving transistor (DRT), a switching transistor (SWT), and a storage capacitor (Cstg), the driving transistor (DRT) is connected between the supply line (EVDD) and the anode of the organic light emitting diode (OLED) and is controlled by a data voltage supplied to the gate of the driving transistor (DRT) via the data line (DL), wherein the sensing transistor (SENT) is controlled by a sense signal (Sense).

10. The display device as claimed in any one of the preceding claims 8 to 9, wherein the driving voltage (V_evdd) is provided from the control board (310) to the display panel (110) by passing through the data driver (120).

11. The display device as claimed in any one of the preceding claims 8 to 10, wherein the driving voltage (V_evdd) is supplied from an external host system (150) to the display panel (110) comprising the OLED via the control board (310).

12. A method for operating a display device according to one of the claims 8 to 11 comprising an over current control device (400) and a display panel (110) connected in series to the over current control device (400), comprising the steps of:

supplying a driving voltage (V_evdd) on a supply line (EVDD) to an OLED of the display panel (110);
identifying a voltage (V_evdd) supplied to the display panel (110) outside the display panel (110),
wherein if the identified voltage (V_evdd) reaches a reference voltage (Vref) corresponding to an over-current or becomes lower than the reference voltage (Vref) corresponding to the over-current interrupting the power supply through the supply line (EVDD) outside of the display panel (110).

Patentansprüche

1. Anzeigevorrichtung, umfassend eine Überstrom-Steuerungsvorrichtung (400), die in Reihe zwischen einer Versorgungsleitung (EVDD) der Anzeigevorrichtung und einem OLED-Anzeigefeld (110) der Anzeigevorrichtung verbunden ist, um einen dem OLED-Anzeigefeld (110) bereitgestellten Überstrom zu detektieren, wobei das Anzeigefeld (110) eine Vielzahl von Pixeln umfasst, wobei jedes Pixel einen Erfassungstransistor (SENT) und eine organische lichtemittierende Diode (OLED) umfasst, wobei der Erfassungstransistor (SENT) einen mit einer Anode der organischen lichtemittierenden Diode (OLED) verbundenen Eingangsanschluss und einen Ausgangsanschluss umfasst, wobei die Überstromsteuerungsvorrichtung (400) umfasst:

eine Überstromidentifizierungseinheit (410), die eingerichtet ist, eine Ansteuerspannung (V_evdd) an der Versorgungsleitung (EVDD) zum Ansteuern des OLED-Anzeigefelds (110) mit einer Referenzspannung (Vref) auf einer Spannungsleitung (Vref) zum Identifizieren des Überstroms zu vergleichen;
eine Unterbrechungseinheit (420), die zwischen der Versorgungsleitung (EVDD), die die Ansteuerspannung (V_evdd) zuführt, und dem OLED-Anzeigefeld (110) verbunden ist, zum Unterbrechen der Energieversorgung, wenn die Überstromidentifizierungseinheit (410) einen durch die Versorgungsleitung (EVDD) fließenden Überstrom erkennt;
wobei die Überstromidentifizierungseinheit (410) umfasst:

einen Komparator (510) mit einem ersten und einem zweiten Eingang und einem Ausgang, wobei der erste Eingang mit der Versorgungsleitung (EVDD) verbunden ist und der zweite Eingang mit der Spannungsleitung (Vref) verbunden ist und auch mit einem Eingangsanschluss (Nref) eines Schaltelements (S2) des Anzeigefeldes (110) verbunden ist, wobei der Ausgang des Komparators (510) mit einem Eingang der Unterbrechungseinheit (420) verbunden ist,
wobei ein Ausgangsanschluss (Nrvl) des Schaltelements (S2) mit Ausgangsanschlüssen der Erfassungstransistoren (SENT) des Anzeigefelds (110) verbunden ist.

2. Anzeigevorrichtung nach Anspruch 1, wobei die Überstromsteuerungsvorrichtung ferner umfasst: einen Widerstand (RSense), der direkt zwischen der Versorgungsleitung (EVDD), die die Ansteuerspannung (V_evdd) trägt, und der Unterbrechungseinheit (420) verbunden ist, wobei der erste Eingang mit der Versorgungsleitung (EVDD) an dem Widerstand (Sense) verbunden ist, um einen Spannungsabfall am Widerstand (RSense) auf der Versorgungsleitung (EVDD) zu detektieren.

3. Anzeigevorrichtung nach Anspruch 1 oder 2, wobei der Komparator (510) als Operationsverstärker realisiert ist.

4. Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die Überstromsteuerungsvorrichtung (400) auf einer Steuerplatine (310) angeordnet ist, die über eine Verbindungsleitung oder flexible Platine mit einem Anzeigefeld (110) verbunden ist, das die OLED umfasst, wobei die Steuerplatine (310) von dem Anzeigefeld (110) getrennt ist.

5. Anzeigevorrichtung nach Anspruch 4, wobei die Steuerplatine (310) direkt mit der Versorgungsleitung (EVDD) verbunden ist.

6. Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die Unterbrechungseinheit (420) der Überstromsteuerungsvorrichtung als PMOS-oder NMOS-Transistor realisiert ist.

7. Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die Spannung (V_evdd) an der Versorgungsleitung (EVDD) die Referenzspannung (V_over) erreicht oder niedriger als die Referenzspannung (V_over) wird, die dem Überstrom entspricht, wobei die Überstromidentifizierungseinheit (410) dazu konfiguriert ist, zu erkennen, dass der Überstrom durch die Versorgungsleitung (EVDD) fließt, und dann ist die Unterbrechungseinheit (420) dazu konfiguriert ist, die Zufuhr der Ansteuerspannung (V_evdd) durch die Versorgungsleitung (EVDD) zu unterbrechen.

8. Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei das Anzeigefeld (110) ferner Datenleitungen (DL) und Gateleitungen (GL) umfasst, wobei Subpixel an Kreuzungen der Datenleitungen (DL) und Gateleitungen (GL) angeordnet sind, wobei die Anzeigevorrichtung ferner umfasst:

mindestens eine integrierte Source-Treiberschaltung (SDIC) zum Zuführen von Datensignalen zu den Datenleitungen (DL);
mindestens eine integrierte Gate-Treiberschaltung (GDIC) zum Zuführen von Abtastsignalen zu den Gateleitungen (GL);
eine Steuerung (140) zur Steuerung der Sourcetreiber-IC (SDIC #k) und der Gatetreiber-IC (GDIC).

9. Anzeigevorrichtung nach Anspruch 8, wobei das Pixel (SP) ferner einen Ansteuertransistor (DRT), einen Schalttransistor (SWT) und einen Speicherkondensator (Cstg) aufweist, wobei der Ansteuertransistor (DRT) zwischen der Versorgungsleitung (EVDD) und der Anode der organischen lichtemittierenden Diode (OLED) verbunden ist und durch eine Datenspannung gesteuert wird, die dem Gate des Treibertransistors (DRT) über die Datenleitung (DL) zugeführt wird, wobei der Erfassungstransistor (SENT) durch ein Erfassungssignal (Sense) gesteuert wird.

10. Anzeigevorrichtung nach einem der vorhergehenden Ansprüche 8 bis 9, wobei die Ansteuerungsspannung (V evdd), indem sie den Datentreiber (120) passiert, von der Steuerplatine (310) an das Anzeigefeld (110) bereitgestellt wird.

11. Anzeigevorrichtung nach einem der vorhergehenden Ansprüche 8 bis 10, wobei die Ansteuerspannung (V_evdd) von einem externen Host-System (150) dem Anzeigefeld (110), das die OLED umfasst, über die Steuerplatine (310) zugeführt wird.

12. Verfahren zum Betreiben einer Anzeigevorrichtung nach einem der Ansprüche 8 bis 11, umfassend eine Überstromsteuerungsvorrichtung (400) und ein Anzeigefeld (110), das in Reihe mit der Überstromsteuerungsvorrichtung (400) verbunden ist, umfassend die Schritte:

Zuführen einer Ansteuerspannung (V_evdd) auf einer Versorgungsleitung (EVDD) zu einer OLED des Anzeigefelds (110);
Identifizieren einer Spannung (V_evdd), die dem Anzeigefeld (110) zugeführt wird, außerhalb des Anzeigefelds (110),
wobei, wenn die identifizierte Spannung (V_evdd) eine Referenzspannung (Vref) erreicht, die einem Überstrom entspricht, oder kleiner als die Referenzspannung (Vref) wird, die dem Überstrom entspricht, Unterbrechen der Energieversorgung durch die Versorgungsleitung (EVDD), außerhalb des Anzeigefelds (110).

Revendications

1. Dispositif d'affichage comprenant un dispositif de commande de surintensité (400) connecté en série entre une ligne d'alimentation (EVDD) du dispositif d'affichage et un panneau d'affichage OLED (110) du dispositif d'affichage pour la détection d'une surintensité fournie au panneau d'affichage OLED (110), dans lequel le panneau d'affichage (110) comprend une pluralité de pixels, chaque pixel comprend un transistor de détection (SENT) et une diode électroluminescente organique (OLED), dans lequel le transistor de détection (SENT) comprend une borne d'entrée connectée à une anode de la diode électroluminescente organique (OLED) et une borne de sortie, le dispositif de commande de surintensité (400) comprenant :

une unité d'identification de surintensité (410) apte à comparer une tension d'entraînement (V_evdd) sur la ligne d'alimentation (EVDD)

pour l'entraînement du panneau d'affichage OLED (110) avec une tension de référence (Vref) sur une ligne de tension (Vref) pour l'identification de la surintensité ;
une unité d'interruption (420) connectée entre la ligne d'alimentation (EVDD) fournissant la tension d'entraînement (V_evdd) et le panneau d'affichage OLED (110) pour l'interruption de l'alimentation électrique si l'unité d'identification de surintensité (410) reconnaît une surintensité s'écoulant à travers la ligne d'alimentation (EVDD) ;
dans lequel l'unité d'identification de surintensité (410) comprend :

un comparateur (510) ayant des première et deuxième entrées et une sortie, la première entrée est connectée à la ligne d'alimentation (EVDD) et la deuxième entrée est connectée à la ligne de tension (Vref) et est également connectée à une borne d'entrée (Nref) d'un élément de commutation (S2) du panneau d'affichage (110), dans lequel la sortie du comparateur (510) est connectée à une entrée de l'unité d'interruption (420),
dans lequel une borne de sortie (Nrvl) de l'élément de commutation (S2) est connectée à des bornes de sortie des transistors de détection (SENT) du panneau d'affichage (110).

2. Dispositif d'affichage selon la revendication 1, dans lequel le dispositif de commande de surintensité comprend en outre : une résistance (RSense) connectée directement entre la ligne d'alimentation (EVDD) portant la tension d'entraînement (V_edd) et l'unité d'interruption (420), dans lequel la première entrée est connectée à la ligne d'alimentation (EVDD) à la résistance (RSense) pour détecter une baisse de tension à la résistance (RSense) sur la ligne d'alimentation (EVDD).

3. Dispositif d'affichage selon la revendication 1 ou 2, dans lequel le comparateur (510) est réalisé en tant qu'un amplificateur opérationnel.

4. Dispositif d'affichage selon l'une quelconque des revendications précédentes, dans lequel le dispositif de commande de surintensité (400) est situé sur une carte de commande (310) connectée par l'intermédiaire d'une ligne de connexion ou d'une carte souple à un panneau d'affichage (110) comprenant l'OLED, dans lequel la carte de commande (310) est séparée du panneau d'affichage (110).

5. Dispositif d'affichage selon la revendication 4, dans lequel la carte de commande (310) est connectée directement à la ligne d'alimentation (EVDD).

6. Dispositif d'affichage selon l'une quelconque des revendications précédentes, dans lequel l'unité d'interruption (420) du dispositif de commande de surintensité est réalisée en tant qu'un transistor PMOS ou NMOS.

7. Dispositif d'affichage selon l'une quelconque des revendications précédentes, dans lequel, si la tension (V_evdd) sur la ligne d'alimentation (EVDD) atteint la tension de référence (V_over) ou devient inférieure à la tension de référence (V_over) correspondant à la surintensité, l'unité d'identification de surintensité (410) est configurée pour reconnaître que la surintensité s'écoule à travers la ligne d'alimentation (EVDD) puis l'unité d'interruption (420) est configurée pour interrompre l'alimentation de la tension d'entraînement (V_evdd) par l'intermédiaire de la ligne d'alimentation (EVDD).

8. Dispositif d'affichage selon l'une quelconque des revendications précédentes, dans lequel le panneau d'affichage (110) comprend en outre des lignes de données (DL) et des lignes de grille (GL), dans lequel des sous-pixels sont disposés à des intersections des lignes de données (DL) et des lignes de grille (GL), le dispositif d'affichage comprenant en outre :

au moins un circuit intégré d'entraînement de source (SDIC) pour l'alimentation de signaux de données aux lignes de données (DL) ;
au moins un circuit intégré d'entraînement de grille (GDIC) pour l'alimentation de signaux de balayage aux lignes de grille (GL) ;
un organe de commande (140) pour commander l'IC d'entraînement de source (SDIC #k) et l'IC d'entraînement de grille (GDIC).

9. Dispositif d'affichage selon la revendication 8, dans lequel le pixel (SP) inclut en outre un transistor d'entraînement (DRT), un transistor de commutation (SWT), et un condensateur de stockage (Cstg), le transistor d'entraînement (DRT) est connecté entre la ligne d'alimentation (EVDD) et l'anode de la diode électroluminescente organique (OLED) et est commandé par une tension de données fournie à la grille du transistor d'entraînement (DRT) par l'intermédiaire de la ligne de données (DL), dans lequel le transistor de détection (SENT) est commandé par un signal de détection (Sense).

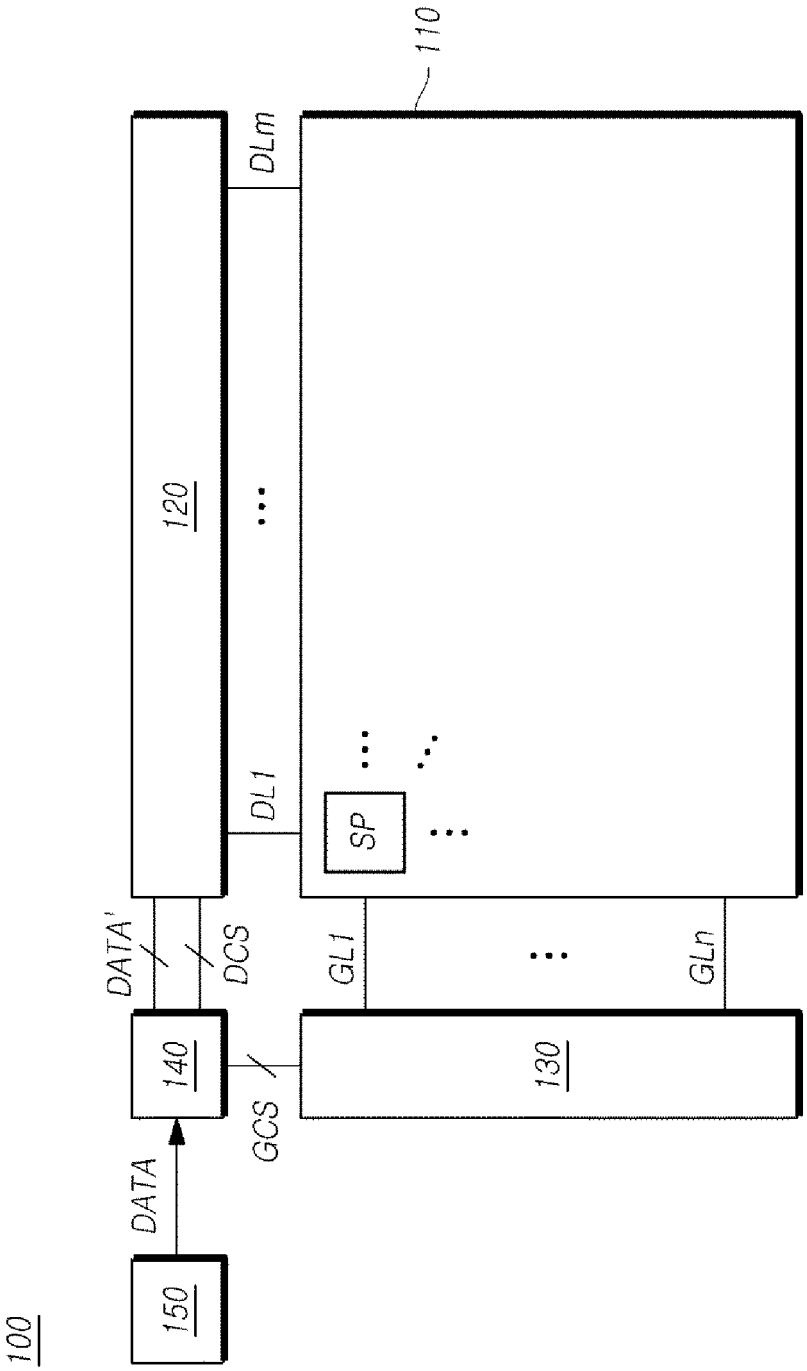
10. Dispositif d'affichage selon l'une quelconque des revendications précédentes 8 à 9, dans lequel la tension d'entraînement (V_evdd) est fournie de la carte de commande (310) au panneau d'affichage (110) en traversant le circuit d'entraînement de données (120).

11. Dispositif d'affichage selon l'une quelconque des revendications précédentes 8 à 10, dans lequel la tension d'entraînement (V_evdd) est fournie d'un système hôte externe (150) au dispositif d'affichage (110) comprenant l'OLED par l'intermédiaire de la carte de commande (310).

12. Procédé de fonctionnement d'un dispositif d'affichage selon l'une des revendications 8 à 11 comprenant un dispositif de commande de surintensité (400) et un panneau d'affichage (110) connecté en série au dispositif de commande de surintensité (400), comprenant les étapes de :

la fourniture d'une tension d'entraînement (V_evdd) sur une ligne d'alimentation (EVDD) à une OLED du panneau d'affichage (110) ;
l'identification d'une tension (V_evdd) fournie au panneau d'affichage (110) à l'extérieur du panneau d'affichage (110),
dans lequel, si la tension identifiée (V_evdd) atteint une tension de référence (Vref) correspondant à une surintensité ou devient inférieure à la tension de référence (Vref) correspondant à la surintensité, l'interruption de l'alimentation électrique par l'intermédiaire de la ligne d'alimentation (EVDD) à l'extérieur du panneau d'affichage (110).

FIG. 1



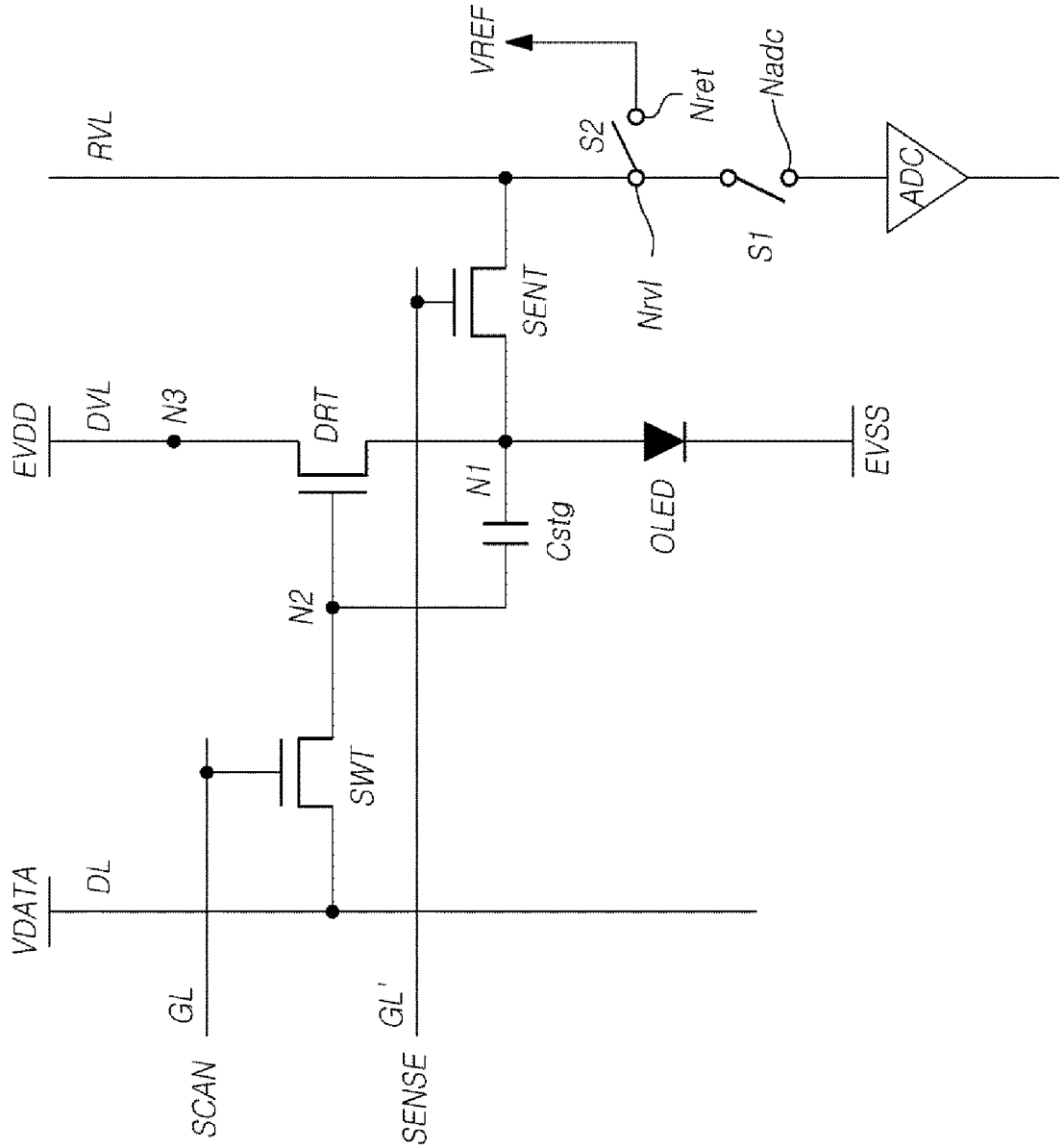

VREF
Nret
Nadc
RVL
S2
ADC
S1
Nrvl
SENT
EVDD
DVL
N3
DRT
N1
EVSS
Cstg
OLED
N2
SWT
VDATA
DL
GL
GL'
SCAN
SENSE

FIG.2

FIG.3

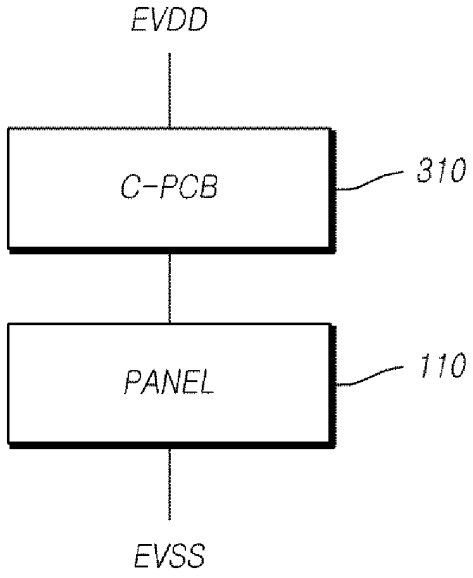

EVDD
C-PCB
310
PANEL
110
EVSS

FIG.4

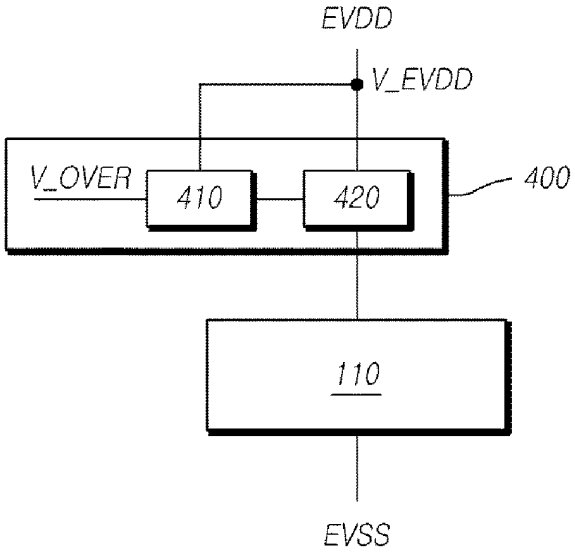

EVDD
V_EVDD
V_OVER
410
420
400
110
EVSS

FIG.5

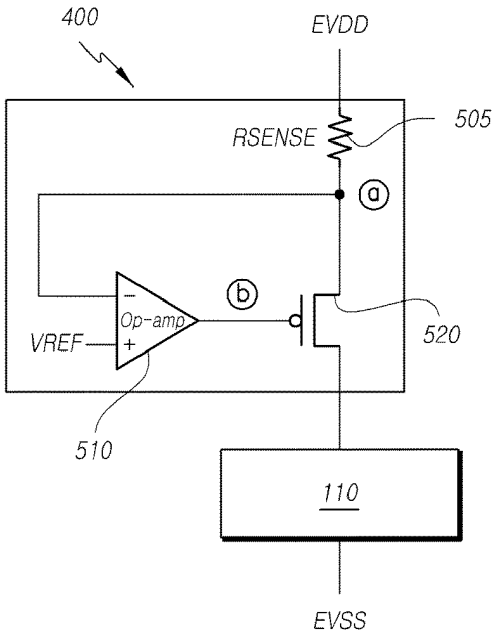

400
EVDD
RSENSE
505
a
b
Op-amp
VREF
520
510
110
EVSS

FIG.6

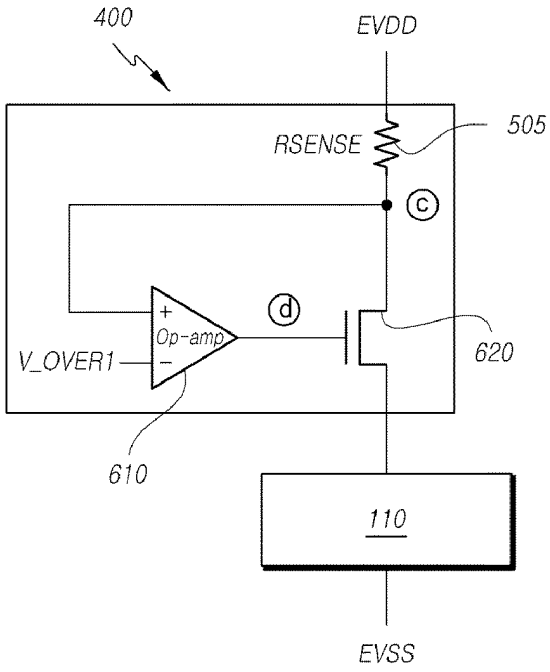

400
EVDD
RSENSE
505
c
d
Op-amp
V_OVER1
620
610
110
EVSS

FIG. 7

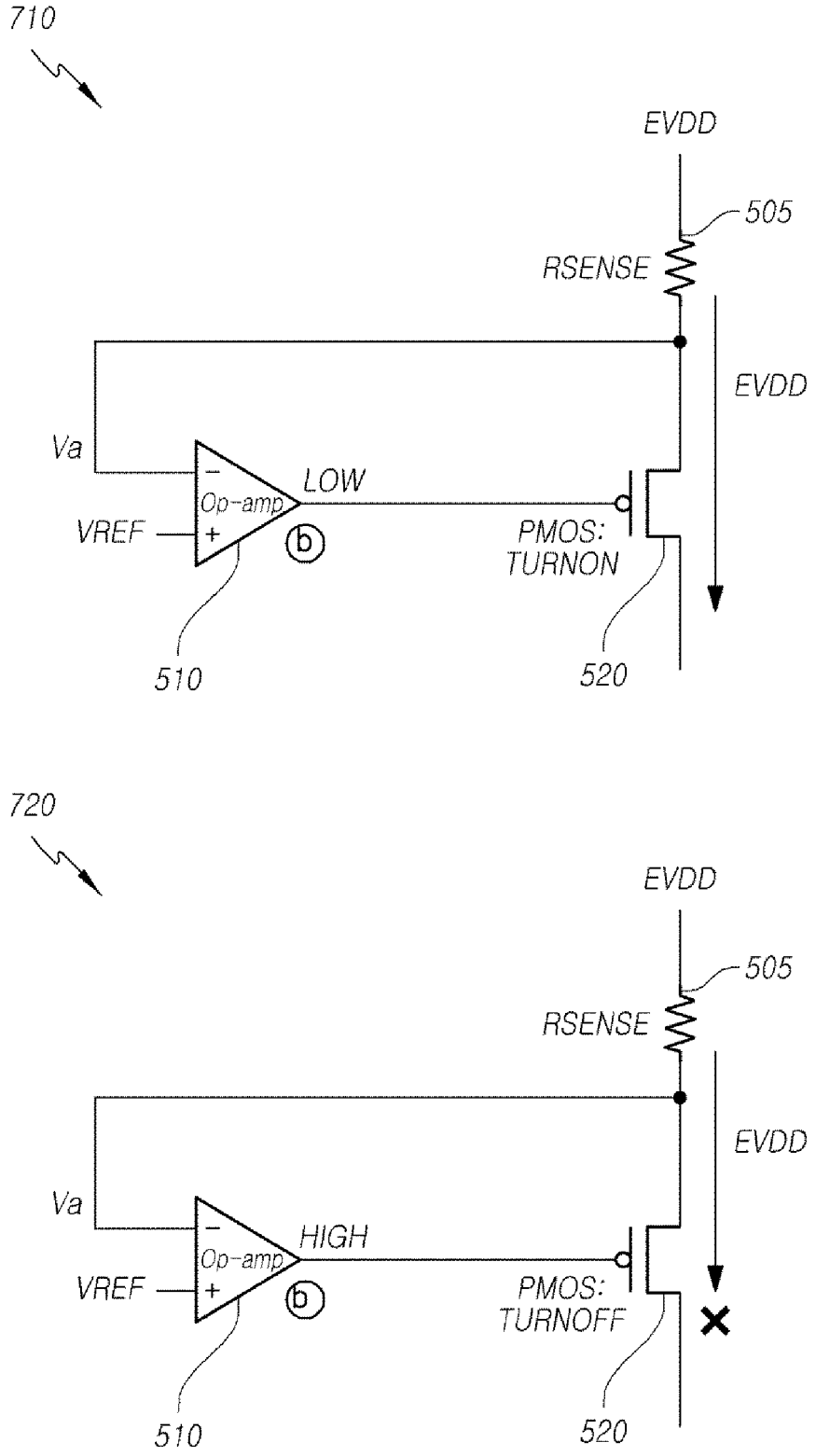

710
EVDD
505
RSENSE
EVDD
Va
Op-amp
LOW
VREF
b
PMOS:
TURNON
510
520
720
EVDD
505
RSENSE
EVDD
Va
Op-amp
HIGH
VREF
b
PMOS:
TURNOFF
510
520

FIG.8

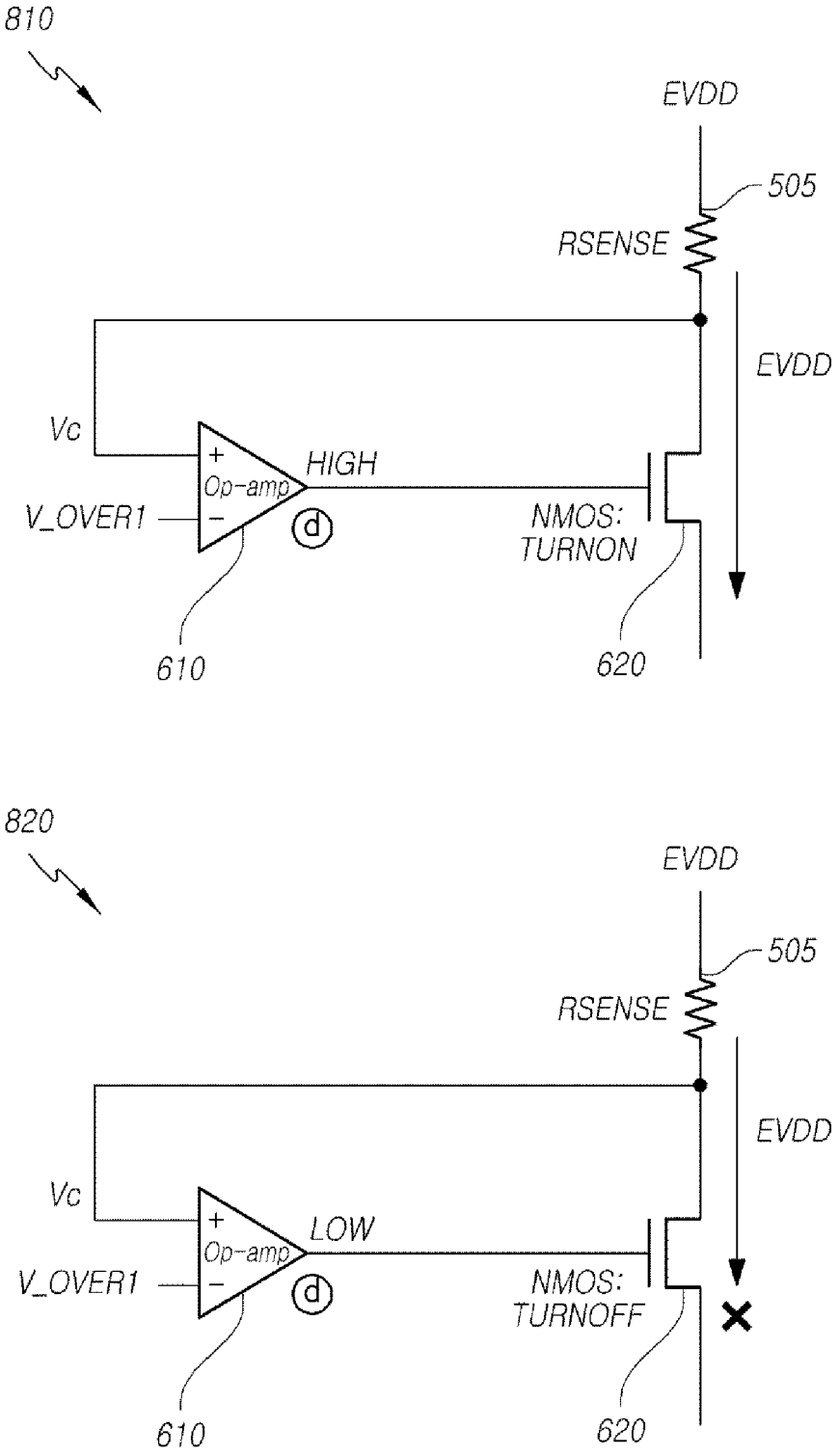
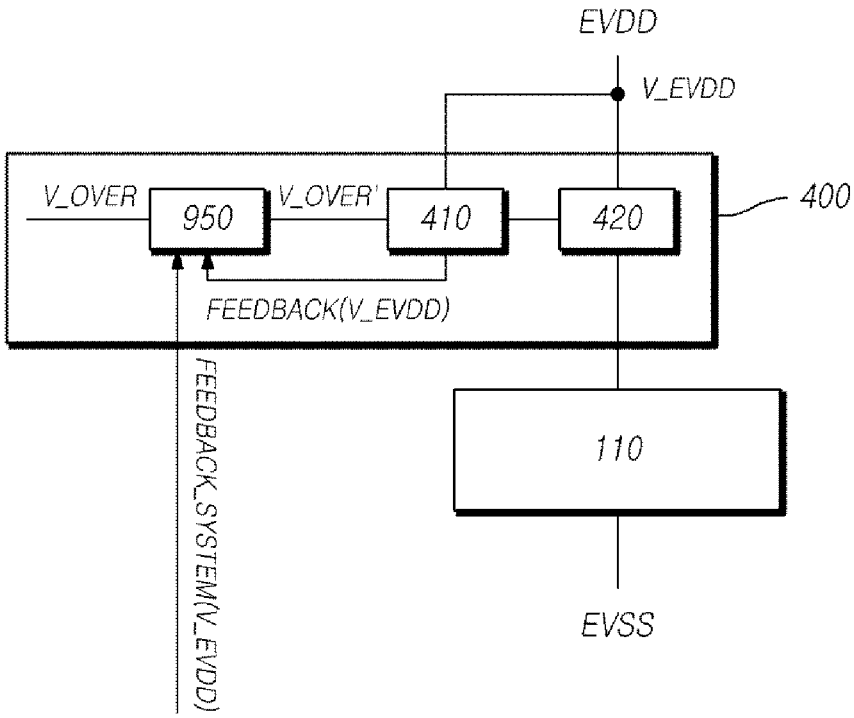

810
EVDD
505
RSENSE
EVDD
Vc
HIGH
Op-amp
V_OVER1
d
NMOS:
TURNON
610
620
820
EVDD
505
RSENSE
EVDD
Vc
LOW
Op-amp
V_OVER1
d
NMOS:
TURNOFF
610
620

FIG.9


EVDD
V_EVDD
V_OVER
950
V_OVER'
410
420
400
FEEDBACK(V_EVDD)
FEEDBACK_SYSTEM(V_EVDD)
110
EVSS

REFERENCES CITED IN THE DESCRIPTION

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- US 20140084792 A1 **[0008]**
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专利名称(译)	过电流控制装置和有机发光显示装置也是相同的		
公开(公告)号	EP3038079B1	公开(公告)日	2019-09-04
申请号	EP2015199085	申请日	2015-12-10
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	LEE JUSEOK		
发明人	LEE, JUSEOK		
IPC分类号	G09G3/00 G01R31/02 G09G3/32 H05B33/08		
CPC分类号	G01R19/0092 G01R31/2635 G09G3/006 G09G3/3225 G09G2330/025 G09G2330/028 G09G2330/045 G09G2330/12 H02H3/087 H01L27/32 H01L27/3202 H01L51/56 G09G3/2092 G09G3/3208 G09G2330/04 H05B45/50		
优先权	1020140188105 2014-12-24 KR		
其他公开文献	EP3038079A3 EP3038079A2		
外部链接	Espacenet		

摘要(译)

过电流控制装置和有机发光显示装置技术领域本发明涉及一种过电流控制装置和一种采用中断过电流功能的有机发光显示装置。为了提供过电流控制装置和使用该过电流控制装置的OLED装置，其允许快速且可靠地检测过电流，提供了用于检测提供给OLED的过电流的过电流控制装置，包括：过电流识别单元（410），用于将用于驱动OLED的供电线上的驱动电压（EVDD）与参考电压线上的参考电压（V_over）进行比较，以识别过电流;如果过电流识别单元（410）识别出流过供电线的过电流，则连接在提供驱动电压（EVDD）的供电线和包括OLED的像素之间的中断单元（420）用于中断电源。

Equation 1

$$I_{ds} = \frac{\beta_n}{2}\left(V_{SG} - |V_{th}|\right)^2\left(1 + \lambda V_{SD}\right)$$