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(54) PIXEL UNIT DRIVE CIRCUIT AND METHOD, PIXEL UNIT, AND DISPLAY APPARATUS

TREIBERSCHALTUNG UND -VERFAHREN FÜR PIXELEINHEITEN SOWIE ANZEIGEVORRICHTUNG DAMIT

CIRCUIT ET PROCÉDÉ DE COMMANDE D'UNITÉ DE PIXEL, UNITÉ DE PIXEL, ET APPAREIL D'AFFICHAGE

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to an organic light-emitting display field, and particularly to a driving circuit and method for a pixel unit of an Active Matrix Organic Light Emitting Diode (AMOLED), a pixel unit and a display apparatus.

BACKGROUND

[0002] An existing driving circuit for a pixel unit is shown in Figure 1. Such driving circuit comprises 2 transistors and a capacitor, wherein one transistor is a switching transistor T1, controlled by a scanning signal Vscan output from a scan line, for controlling an input of a data signal Vdata on a data line, and another transistor is a driving transistor T2 controlling light emission of an OLED; Cs is a storage capacitor for maintain a voltage applied to the driving transistor T2 during non-scanning period. The above circuit is referred to as a 2T1C driving circuit for a pixel unit.

[0003] An AMOLED is driven by a current that is generated by a driving transistor in saturation state to emit light. Because when the same gray scale voltage is input, different threshold voltages of the driving transistor lead to different driving currents, causing inconsistencies of the currents. During the manufacturing process of a Low Temperature Polycrystalline Silicon (LTPS), the uniformity of threshold voltage Vth is very bad, and at the same time the Vth drifts as well, therefore, the brightness uniformity of the traditional 2T1C driving circuit for a pixel unit has always been very bad.

[0004] EP 2 237 254 A2 concerns compensating for variations of the threshold voltages of driving transistors and compensating for the deterioration of an organic light emitting diode, wherein a pixel includes an organic light emitting diode (OLED), two transistors, a storage capacitor, and a compensation unit. A driving transistor supplies a current to the OLED corresponding to the voltage in the storage capacitor. The compensation unit controls a voltage of a gate electrode of the driving transistor corresponding to a deterioration of the organic light emitting diode, and couples one electrode of the driving transistor to the data line during a compensation period, during which a threshold voltage of the driving transistor is compensated.

[0005] US 2006/055336 A1 concerns an organic light emitting display including a plurality of pixels, at least one of the pixels comprises a driving circuit having the features in the preamble of claim 1. In this display, the amount of current leaking out through a switching transistor is decreased, and thus a voltage variance applied to a gate electrode of a driving transistor is decreased, thereby enhancing the contrast of an image.

SUMMARY

[0006] The object of the present invention is to provide a driving circuit and method for driving a pixel unit, a pixel unit and a display apparatus, by which the brightness uniformity of an OLED panel is improved.

[0007] The object is achieved by the features of the respective independent claims. Further embodiments are defined in the dependent claims.

[0008] An embodiment of the present invention provides a driving circuit for a pixel unit, for driving an OLED, the driving circuit for a pixel unit comprises: a driving thin-film transistor, a first switching element, a storage capacitor and a driving control unit;

a first end of said storage capacitor is connected to a gate of said driving thin-film transistor, and a second end of said storage capacitor is connected to a high level output of a driving power supply;

a source of said driving thin-film transistor is connected to a data line via said first switching element;

a drain of said driving thin-film transistor is connected to an anode of said OLED and a low level output of the driving power supply respectively via said driving control unit, a source of said driving thin-film transistor is connected to said high level output of the driving power supply, and a gate of said driving thin-film transistor is connected to the drain of said driving thin-film transistor via the driving control unit;

said driving control unit is used to control said storage capacitor to be charged/discharged so as to control said driving thin-film transistor to operate in a saturation region, so that the threshold voltage Vth of said driving thin-film transistor is compensated by utilizing the gate-source voltage of said driving thin-film transistor.

[0009] In one embodiment, said driving thin-film transistor is a p-type thin-film transistor.

[0010] In one embodiment, said first switching element is a p-type thin-film transistor;

a gate of said first switching element is connected to a scan line for transmitting a control signal, a source of said first switching element is connected to a data line, and a drain of said first switching element is connected to the source of said driving thin-film transistor.

[0011] According to the invention, said driving control unit further comprises: a second switching element, a third switching element, a fourth switching element and a fifth switching element.

[0012] In one embodiment, said second switching element is connected between the drain of said driving thin-film

transistor and said low level output of the driving power supply;
said third switching element is connected between the gate of said driving thin-film transistor and the drain of said driving thin-film transistor;
said fourth switching element is connected between the drain of said driving thin-film transistor and the anode of said OLED; and
said fifth switching element is connected between the source of said driving thin-film transistor and said high level output of the driving power supply.

[0013] In one embodiment, said second switching element, said third switching element, said fourth switching element and said fifth switching element are p-type TFTs.

[0014] According to the invention, a gate of said second switching element is connected to a first control line, a source of said second switching element is connected to the drain of said driving thin-film transistor, and a drain of said second switching element is connected to said low level output of the driving power supply;
a gate of said third switching element is connected to said scan line, a source of said third switching element is connected to the gate of said driving thin-film transistor, and a drain of said third switching element is connected to the drain of said driving thin-film transistor;
a gate of said fourth switching element is connected to a second control line, a source of said fourth switching element is connected to the drain of said driving thin-film transistor, and a drain of said fourth switching element is connected to the anode of said OLED;
a gate of said fifth switching element is connected to said second control line, a source of said fifth switching element is connected to said high level output of the driving power supply, and a drain of said fifth switching element is connected to the source of said driving thin-film transistor.

[0015] The present invention also provides a method for driving a pixel unit, and it is applied to the above driving circuit for pixel unit, said method for driving a pixel unit comprising the steps of:

pixel charging: by a driving control unit controlling a storage capacitor to be charged;
pixel discharging: by the driving control unit controlling said storage capacitor to be discharged via the driving thin-film transistor, until a gate-source voltage of said driving thin-film transistor is equal to the threshold voltage Vth of said driving thin-film transistor;
switch buffering: by the driving control unit controlling the gate voltage of the driving thin-film transistor to remain stable;
driving the OLED to emit light and display: by said driving control unit controlling said driving thin-film transistor to operate in a saturation region, and controlling the voltage difference between two ends of said storage capacitor to remain unchanged, so as to compensate the threshold voltage Vth of said driving thin-film transistor by the gate-source voltage of said driving thin-film transistor, and to drive OLED to emit light by said driving thin-film transistor.

[0016] In one embodiment, the step for pixel charging comprises: by a first switching element switching on a connection between the source of said driving thin-film transistor and a data line; by said driving control unit switching on a connection between the drain of said driving thin-film transistor and a cathode of said OLED, switching on a connection between the gate of said driving thin-film transistor and the drain of said driving thin-film transistor, switching off the connection between the source of said driving thin-film transistor and said high level output of the driving power supply, and controlling said storage capacitor to be charged;
the step for pixel discharging comprises: by said driving control unit switching off the connection between the drain of said driving thin-film transistor and the cathode of said OLED, by said driving control unit controlling said storage capacitor to be discharged via said driving thin-film transistor, until a gate-source voltage of said driving thin-film transistor is equal to the threshold voltage Vth of said driving thin-film transistor;
the step for switch buffering comprises: by said first switching element switching off the connection between the source of said driving thin-film transistor and the data line; by said driving control unit switching off the connection between the gate of said driving thin-film transistor and the drain of said driving thin-film transistor;
the step for driving the OLED to emit light and display comprises: by said driving control unit switching on a connection between the source of said driving thin-film transistor and said high level output of the driving power supply, switching on a connection between the drain of said driving thin-film transistor and the anode of said OLED, controlling said driving thin-film transistor to operate in the saturation region, and controlling voltage difference between two ends of said storage capacitor to remain unchanged, so as to compensate the threshold voltage Vth of said driving thin-film transistor by the gate-source voltage of said driving thin-film transistor, and to drive OLED to emit light by said driving thin-film transistor.

[0017] An embodiment of the present invention also provides a pixel unit, comprising: an OLED and the driving circuit for a pixel unit stated above, wherein the driving circuit for a pixel unit is connected to an anode of OLED, a cathode of OLED is connected to a low level output of the driving power supply.

[0018] An embodiment of the present invention also provides a display apparatus, comprising a plurality of pixel units

stated above.

[0019] Compared to prior art, in the driving circuit and method for a pixel unit, the pixel unit and the display apparatus provided by the embodiments of the present invention, by the driving control unit controlling the storage capacitor Cs to be discharged so as to compensate the threshold voltage of the driving thin-film transistor for driving OLED by a gate-source voltage of the driving thin-film transistor, solving the problems of the ununiformity and attenuation of the brightness in an OLED panel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020]

Figure 1 shows a circuit diagram of an existing 2T1C driving circuit for a pixel unit;
Figure 2 shows a circuit diagram of a driving circuit for a pixel unit according to the first embodiment of the present invention;
Figure 3A shows a circuit diagram of a driving circuit for a pixel unit according to the second embodiment of the present invention;
Figure 3B shows an equivalent circuit diagram of the driving circuit for a pixel unit according to the second embodiment of the present invention in a first time period;
Figure 3C shows an equivalent circuit diagram of the driving circuit for a pixel unit according to the second embodiment of the present invention in a second time period;
Figure 3D shows an equivalent circuit diagram of the driving circuit for a pixel unit according to the second embodiment of the present invention in a third time period;
Figure 3E shows an equivalent circuit diagram of the driving circuit for a pixel unit according to the second embodiment of the present invention in a fourth time period; and
Figure 4 shows a timing diagram of various signals in the driving circuit for a pixel unit of the embodiment.

DETAILED DESCRIPTION

[0021] The present invention provides a driving circuit and method for a pixel unit, a pixel unit and a display apparatus, wherein, by using a diode connection and controlling the storage capacitor to be discharged, it allows the gate-source voltage of a driving thin-film transistor for driving the OLED to compensate the threshold voltage of the driving thin-film transistor, so as to address the issues of ununiformity and attenuation of the brightness in the OLED panel.

[0022] Shown in Figure 2, in the circuit diagram of the driving circuit for a pixel unit according to the first embodiment of the present invention, the driving circuit for a pixel unit of the embodiment is used to drive an OLED, and the circuit comprises a driving thin-film transistor DTFT, a first switching element 21, a storage capacitor Cs and a driving control unit 22; wherein

a first end of the storage capacitor is connected to a gate of the driving thin-film transistor DTFT, and a second end of said storage capacitor is connected to a high level output of a driving power supply having an output voltage of VDD;

a source of the driving thin-film transistor DTFT is connected to a data line Data via said first switching element 21;

a drain of the driving thin-film transistor DTFT is connected to an anode of said OLED and a low level output of the driving power supply having an output voltage of VSS respectively via the driving control unit 22, a source of the driving thin-film transistor DTFT is connected to the high level output of the driving power supply via the driving control unit 22, and a gate of the driving thin-film transistor is connected to the drain of the driving thin-film transistor via the driving control unit 22;

the driving control unit 22 is used to control said storage capacitor Cs to be charged/discharged to control said driving thin-film transistor DTFT to operate in a saturation region, so as to compensate the threshold voltage Vth of said driving thin-film transistor DTFT by utilizing the gate-source voltage of said driving thin-film transistor DTFT;

the driving control unit 22 is also connected to a scan line SCAN and a control line CR for transmitting control signals, respectively.

[0023] As shown in Figure 2, in the driving circuit for a pixel unit of the first embodiment of the present invention, the first switching element 21 is a first switch TFT labeled as T1, and T1 is a p-type thin-film transistor.

[0024] A gate of the first switching element 21 is connected to a scan line SCAN for transmitting a control signal, a source of the first switching element 21 is connected to the data line Data, and a drain of the first switching element 21 is connected to the source of the driving thin-film transistor DTFT.

[0025] Shown in Figure 3A, it is the circuit diagram of the driving circuit for a pixel unit according to the second embodiment of the present invention. The driving circuit for a pixel unit in this embodiment employs a 6T1C circuit, wherein the threshold voltage Vth of the driving TFT is compensated so that the driving current of the driving TFT is independent of the threshold voltage Vth of the driving TFT, and thus achieves the consistency of the current, the

improved uniformity and reliability.

[0026] In this embodiment, the first switching element is a first switch TFT labeled as T1, the second switching element is a second switch TFT labeled as T2, the third switching element is a third switch TFT labeled as T3, the fourth switching element is a fourth switch TFT labeled as T4, the fifth switching element is a fifth switch TFT labeled as T5, and the driving TFT is labeled as DTFT, wherein,

the first switch TFT, the second switch TFT, the third switch TFT, the fourth switch TFT and the driving TFT are p-type TFTs, and the threshold voltage of the p-type TFT, Vth<0;

a drain of T4 is connected to an anode of the OLED, a source of T4 is connected to a drain of DTFT, a source of T2 and a drain of T3, and a gate of T4 is connected to a gate of T5;

a drain of T2 is connected to a cathode of OLED and to ground;

a source of T3 is connected to a gate of DTFT and a first end of the storage capacitor Cs, and a gate of T3 is connected to a gate of T1;

a drain of T1 is connected to a drain of T5, and a source of T1 is connected to a data line Data;

a source of T5 is connected to a high level output of a driving power supply having a output voltage of VDD, and a drain of T5 is connected to a source of DTFT;

a gate of T3 and a gate of T1 are connected to a scan line SCAN for transmitting a control signal;

a gate of T2 is connected to a control line CR1; and

a gate of T4 and a gate of T5 are connected to a control line CR2.

[0027] As shown in Figure 3B, when the driving circuit for a pixel unit of the second embodiment of the present invention is in operation, during the first time period (i.e. the pre-charging stage), the scan line SCAN and the control line CR1 output a low level, to control T2, T3 and T1 to switch on, and the control line CR2 is at a high level, to control T4 and T5 to cut off. At this time, the first end of the storage capacitor Cs is connected to ground, the second end of the storage capacitor Cs is connected to the high level output of the driving power supply having the output voltage of VDD, and the storage capacitor Cs is charged; the voltage at the node A (i.e. the drain of DTFT) and that at the node B (i.e. the gate of DTFT) are 0, and the voltage at the node C (i.e. the source of DTFT) is a voltage Vdata output from the data line Data.

[0028] As shown in Figure 3C, when the driving circuit for a pixel unit of the second embodiment of the present invention is in operation, during the second time period (i.e. data write-in and discharge compensation stage), the scan line SCAN outputs a low level, to control T3 and T1 to switch on, and the control line CR1 and control line CR2 output a high level, to control T4, T2 and T5 to cut off. The gate and drain of DTFT are connected together, and thus the DTFT serves as a diode; the first end of the storage capacitor Cs is connected to the gate of DTFT, and the second end of the storage capacitor Cs is connected to the high level output of the driving power supply having the output voltage of VDD; meanwhile, the source of DTFT (i.e. node C) is connected to the data line Data outputting a voltage VData.

[0029] The gate-source voltage of DTFT Vgs (i.e. (VB-VC)) is equal to (-Vdata), which is less than Vth, and therefore DTFT is switched on; the storage capacitor Cs discharges to the data line Data via DTFT, until the Vgs of DTFT increases to the threshold voltage Vth of the DTFT; at this time, DTFT enters into subthreshold turn-on, the voltage at the node C maintains at Vdata, the voltage difference between node B and node C (i.e. Vgs) is equal to the threshold voltage Vth of DTFT. Therefore, the gate voltage of DTFT (i.e. node B) is VD+Vth=Vdata+Vth, and the voltage difference between the second end and the first end of the storage capacitor Cs is VDD-VB, i.e. VDD-Vdata-Vth.

[0030] As shown in Figure 3D, when the driving circuit for a pixel unit of the second embodiment of the present invention is in operation, during the third time period (i.e. switch buffering stage), the scan line SCAN, the control line CR1 and the control line CR2 output a high level, to control T1, T2, T3, T4 and T5 to switch off, and the voltage at the gate of DTFT (i.e. node B) is stabilized by the storage capacitor to be (Vdata+Vth).

[0031] As shown in Figure 3E, when the driving circuit for a pixel unit of the second embodiment of the present invention is in operation, during the fourth time period (i.e. the driving stage for OLED), the control line CR2 outputs a low level, to control T4 and T5 to switch on, and the control line CR1 and the scan line SCAN output a high level, to control T2, T3 and T1 to switch off. At this time, DTFT operates in a saturation region, and a driving current flows through OLED to light it up.

[0032] The gate voltage of DTFT (i.e. node B) is (Vdata+Vth), the source of DTFT is connected to the high level output of the driving power supply having a output voltage of VDD via T5, i.e. the gate-source voltage of DTFT Vgs is (Vdata+Vth-VDD), and the current I flowing through OLED at this moment is calculated by equation (1) as below:

$$\begin{aligned} I &= K \times (Vgs\text{-}Vth)^2 \\ &= K \times (Vdata+Vth\text{-}VDD\text{-}Vth)^2 \\ &= K \times (Vdata\text{-}VDD)^2; \end{aligned} \qquad \text{Equation (1)}$$

wherein, K is the current coefficient of DTFT;

$$K = C_{ox} \cdot \mu \cdot W/L;$$

[0033] μ, C_{ox}, W and L. are field effect mobility, gate isolation layer unit-area capacitance, channel width and length of DTFT respectively.

[0034] The fourth time period is a light-emitting stage of OLED, and OLED will continue to emit light until the written-in of a next frame data on the data line Data.

[0035] Therefore, the driving current of the driving TFT (i.e. the current that flows through OLED) only depends on Vdata-VDD, and is not affected by the threshold voltage Vth of the driving TFT and the anode voltage Vth_oled of OLED, preventing the driving current from varying according to the drift of the threshold voltage of the driving TFT and that of the anode voltage of OLED, so that the uniformity of current is improved, to achieve the uniformity of the brightness of the OLED panel.

[0036] Figure 4 shows a timing diagram of various signals in the driving circuit for a pixel unit of the embodiment, wherein the scan line SCAN outputs the scan signal VSCAN, the data line DATA outputs a data signal Vdata, the first control line CR1 outputs a control signal VCR1 and the second control line CR2 outputs a control signal VCR2. In the Figure 4, D, E, F and G indicate the first time period, the second time period, the third time period and the fourth time period respectively.

Claims

1. A driving circuit for a pixel unit, for driving an OLED, wherein, the driving circuit for the pixel unit comprises: a driving thin-film transistor (DTFT), a first switching element (T1), a storage capacitor (Cs) and a driving control unit (22); wherein,
   a first end of said storage capacitor (Cs) is connected to a gate of said driving thin-film transistor (DTFT), and a second end of said storage capacitor (Cs) is connected to a high level output (VDD) of a driving power supply;
   a source of said driving thin-film transistor (DTFT) is connected to a data line (Data) via said first switching element (T1);
   said driving control unit (22) is configured for controlling said storage capacitor (Cs) to be charged and/or discharged to control said driving thin-film transistor (DTFT) to operate in a saturation region, so as to compensate a threshold voltage Vth of said driving thin-film transistor (DTFT) by a gate-source voltage of said driving thin-film transistor (DTFT);
   wherein said driving control unit (22) **further comprises:** a second switching element (T2), a third switching element (T3), a fourth switching element (T4) and a fifth switching element (T5); wherein,
   a gate of said second switching element (T2) is connected to a first control line (CR1), a source of said second switching element (T2) is connected to the drain of said driving thin-film transistor (DTFT);
   a gate of said third switching element (T3) is connected to a scan line for transmitting a control signal (SCAN), a source of said third switching element (T3) is connected to the gate of said driving thin-film transistor (DTFT), and a drain of said third switching element (T3) is connected to the drain of said driving thin-film transistor (DTFT);
   a gate of said fourth switching element (T4) is connected to a second control line (CR2), a source of said fourth switching element (T4) is connected to the drain of said driving thin-film transistor (DTFT), and a drain of said fourth switching element (T4) is connected to an anode of said OLED; and
   a gate of said fifth switching element (T5) is connected to said second control line (CR2), a source of said fifth switching element (T5) is connected to said high level output (VDD) of the driving power supply, and a drain of said fifth switching element (T5) is connected to the source of said driving thin-film transistor (DTFT);
   characterized in that a drain of said second switching element (T2) is connected to a low level output (VSS) of the driving power supply, and that a gate of said first switching element (T1) is connected to the scan line (SCAN).

2. The driving circuit for the pixel unit of claim 1, wherein, said driving thin-film transistor (DTFT) is a p-type thin-film transistor.

3. The driving circuit for the pixel unit of claim 2, wherein,
   said first switching element (T1) is a p-type thin-film transistor;
   a source of said first switching element (T1) is connected to the data line (Data), and a drain of said first switching element (T1) is connected to the source of said driving thin-film transistor (DTFT).

4. The driving circuit for the pixel unit of claim 3, wherein, said second switching element (T2), said third switching element (T3), said fourth switching element (T4) and said fifth switching element (T5) are p-type TFTs.

5. A method for driving a pixel unit, being applied to the driving circuit for the pixel unit of claim 1, wherein, said method for driving a pixel unit comprising the steps of:

pixel charging: by the driving control unit (22) controlling the storage capacitor (Cs) to be charged;
pixel discharging: by the driving control unit (22) controlling said storage capacitor (22) to be discharged via the driving thin-film transistor (DTFT), until a gate-source voltage of said driving thin-film transistor (DTFT) is equal to the threshold voltage Vth of said driving thin-film transistor (DTFT);
switch buffering: by the driving control unit (22) controlling the gate voltage of the driving thin-film transistor (DTFT) to remain stable;
driving the OLED to emit light and display: by said driving control unit (22) controlling said driving thin-film transistor (DTFT) to operate in a saturation region, and controlling the voltage difference between two ends of said storage capacitor (Cs) to remain unchanged, so as to compensate the threshold voltage Vth of said driving thin-film transistor (DTFT) by the gate-source voltage of said driving thin-film transistor (DTFT), and to drive OLED to emit light by said driving thin-film transistor (DTFT).

6. The method for driving the pixel unit according to claim 5, wherein,
the step for pixel charging comprises: by said first switch element (T1) switching on a connection between the source of said driving thin-film transistor (DTFT) and a data line (Data); by said driving control unit (22) switching on a connection between the drain of said driving thin-film transistor (DTFT) and a cathode of said OLED, switching on a connection between the gate of said driving thin-film transistor (DTFT) and the drain of said driving thin-film transistor (DTFT), switching off the connection between the source of said driving thin-film transistor (DTFT) and said high level output (VDD) of the driving power supply, and controlling said storage capacitor (Cs) to be charged;
the step for pixel discharging comprises: by said driving control unit (22) switching off the connection between the drain of said driving thin-film transistor (DTFT) and the cathode of said OLED, by said driving control unit (22) controlling said storage capacitor (Cs) to be discharged via said driving thin-film transistor (DTFT), until a gate-source voltage of said driving thin-film transistor (DTFT) is equal to the threshold voltage Vth of said driving thin-film transistor (DTFT);
the step for switch buffering comprises: by said first switching element (T1) switching off the connection between the source of said driving thin-film transistor (DTFT) and the data line (Data); by said driving control unit (22) switching off the connection between the gate of said driving thin-film transistor (DTFT) and the drain of said driving thin-film transistor (DTFT);
the step for driving OLED to emit light and display comprises: by the driving control unit (22) switching on a connection between the source of said driving thin-film transistor (DTFT) and said high level output (VDD) of the driving power supply, switching on a connection between the drain of said driving thin-film transistor (DTFT) and the anode of said OLED, controlling said driving thin-film transistor (DTFT) to operate in the saturation region, and controlling the voltage difference between two ends of said storage capacitor (Cs) to remain unchanged, so as to compensate the threshold voltage Vth of said driving thin-film transistor (DTFT) by the gate-source voltage of said driving thin-film transistor (DTFT), and to drive OLED to emit light by said driving thin-film transistor (DTFT).

7. A pixel unit comprising an OLED and the driving circuit for the pixel unit of any one of claims 1 to 4, wherein, the driving circuit for the pixel unit is connected to an anode of the OLED, and a cathode of the OLED is connected to the low level output (VDD) of the driving power supply.

8. A display apparatus comprising a plurality of pixel units of claim 7.

Patentansprüche

1. Treiberschaltung für eine Pixeleinheit zum Treiben einer OLED, wobei die Treiberschaltung für die Pixeleinheit aufweist: einen Treiber-Dünnschichttransistor (DTFT), ein erstes Schaltelement (T1), einen Speicherkondensator (Cs) und eine Treibersteuereinheit (22); wobei
ein erstes Ende des Speicherkondensators (Cs) mit einem Gate des Treiber-Dünnschichttransistors (DTFT) verbunden ist und ein zweites Ende des Speicherkondensators (Cs) mit einem Hochpegelausgang (VDD) einer Treiberenergieversorgung verbunden ist;
eine Source des Treiber-Dünnschichttransistors (DTFT) mit einer Datenleitung (Data) des ersten Schaltelements

(T1) verbunden ist;
die Treibersteuereinheit (22) zum Steuern des zu ladenden und/oder zu entladenden Speicherkondensators (Cs) konfiguriert ist, um den Treiber-Dünnschichttransistor (DTFT) zu steuern, im Sättigungsbereich zu arbeiten, um eine Schwellspannung Vth des Treiber-Dünnschichttransistors (DTFT) durch eine Gate-Source-Spannung des Treiber-Dünnschichttransistors (DTFT) zu kompensieren;
wobei die Treibersteuereinheit (22) weiter aufweist: ein zweites Schaltelement (T2), ein drittes Schaltelement (T3), ein viertel Schaltelement (T4) und ein fünftes Schaltelement (T5); wobei,
ein Gate des zweiten Schaltelements (T2) mit einer ersten Steuerleitung (CR1) verbunden ist, eine Source des zweiten Schaltelements (T2) mit dem Drain des Treiber-Dünnschichttransistor (DTFT) verbunden ist;
ein Gate des dritten Schaltelements (T3) mit einer Abtastleitung zum Übertragen eines Steuersignals (SCAN) verbunden ist, eine Source des dritten Schaltelements (T3) mit dem Gate des Treiber-Dünnschichttransistors (DTFT) verbunden ist und ein Drain des dritten Schaltelements (T3) mit dem Drain des Treiber-Dünnschichttransistors (DTFT) verbunden ist;
ein Gate des vierten Schaltelements (T4) mit einer zweiten Steuerleitung (CR2) verbunden ist, eine Source des vierten Schaltelements (T4) mit dem Drain des Treiber-Dünnschichttransistors (DTFT) verbunden ist und ein Drain des vierten Schaltelements (T4) mit einer Anode der OLED verbunden ist; und
ein Gate des fünften Schaltelements (T5) mit der zweiten Steuerleitung (CR2) verbunden ist, eine Source des fünften Schaltelements (T5) mit dem Hochpegelausgang (VDD) der Treiberenergieversorgung verbunden ist und ein Drain des fünften Schaltelements (T5) mit der Source des Treiber-Dünnschichttransistors (DTFT) verbunden ist;
dadurch gekennzeichnet, dass ein Drain des zweiten Schaltelements (T2) mit einem Niedrigpegelausgang (VSS) der Treiberenergieversorgung verbunden ist und dass ein Gate des ersten Schaltelements (T1) mit der Abtastleitung (SCAN) verbunden ist.

2. Treiberschaltung für die Pixeleinheit gemäß Anspruch 1, wobei der Treiber-Dünnschichttransistor (DTFT) ein p-Typ-Dünnschichttransistor ist.

3. Treiberschaltung für die Pixeleinheit gemäß Anspruch 2, wobei
das erste Schaltelement (T1) ein p-Typ-Dünnschichttransistor ist;
eine Source des ersten Schaltelements (T1) mit der Datenleitung (Data) verbunden ist und ein Drain des ersten Schaltelements (T1) mit der Source des Treiber-Dünnschichttransistors (DTFT) verbunden ist.

4. Treiberschaltung für die Pixeleinheit gemäß Anspruch 3, wobei das zweite Schaltelement (T2), das dritte Schaltelement (T3), das vierte Schaltelement (T4) und das fünfte Schaltelement (T5) p-Typ-TFTs sind.

5. Verfahren zum Treiben einer Pixeleinheit, welches auf die Treiberschaltung für die Pixeleinheit gemäß Anspruch 1 angewendet wird, wobei das Verfahren zum Treiben einer Pixeleinheit die Schritte aufweist:

Pixelaufladen: durch die Treibersteuereinheit (22), Steuern des Speicherkondensators (Cs), um geladen zu werden;
Pixelentladen: durch die Treibersteuereinheit (22), Steuern des Speicherkondensators über den Treiber-Dünnschichttransistor (DTFT) entladen zu werden, bis eine Gate-Source-Spannung des Treiber-Dünnschichttransistors (DTFT) gleich der Schwellspannung Vth des Treiber-Dünnschichttransistors (DTFT) ist;
Schaltpuffern: durch die Treibersteuereinheit (22), Steuern der Gate-Spannung des Treiber-Dünnschichttransistors (DTFT), um stabil zu bleibt;
Treiben der OLED Licht auszusenden und anzuzeigen: durch die Treibersteuereinheit (22), Steuern des Treiber-Dünnschichttransistors (DTFT), um in einem Sättigungsbereich zu arbeiten, und Steuern der Spannungsdifferenz zwischen zwei Enden des Speicherkondensators (Cs), um unverändert zu bleiben, sodass die Schwellspannung Vth des Treiber-Dünnschichttransistors (DTFT) durch die Gate-Source-Spannung des Treiber-Dünnschichttransistors (DTFT) kompensiert wird und die OLED durch den Treiber-Dünnschichttransistor (DTFT) getrieben Licht auszusenden.

6. Verfahren zum Treiben der Pixeleinheit gemäß Anspruch 5, wobei
der Schritt zum Pixelladen aufweist: durch das erste Schaltelement (T1), Herstellen einer Verbindung zwischen der Source des Treiber-Dünnschichttransistors (DTFT) und einer Datenleitung (Data); durch die Treibersteuereinheit (22), Herstellen einer Verbindung zwischen dem Drain des Treiber-Dünnschichttransistors (DTFT) und einer Katode der OLED, Herstellen einer Verbindung zwischen dem Gate des Treiber-Dünnschichttransistors (DTFT) und des Drains des Treiber-Dünnschichttransistors (DTFT), Lösen der Verbindung zwischen der Source des Treiber-Dünnschichttransistors (DTFT) und des Hochpegelausgangs (VDD) der Treiberenergieversorgung und Steuern des Spei-

cherkondensators (Cs), damit dieser geladen wird;
der Schritt zum Pixelentladen aufweist: durch die Treibersteuereinheit (22), Herstellen der Verbindung zwischen dem Drain des Treiber-Dünnschichttransistors (DTFT) und der Katode der OLED, durch die Treibersteuereinheit (22), Steuern des Speicherkondensators (Cs), um über den Treiber-Dünnschichttransistor (DTFT) entladen zu werden, bis eine Gate-Source-Spannung des Treiber-Dünnschichttransistors (DTFT) gleich der Schwellspannung Vth des Treiber-Dünnschichttransistors (DTFT) ist;
der Schritt zum Schaltpuffern aufweist: durch das erste Schaltelement (T1), Lösen der Verbindung zwischen der Source des Treiber-Dünnschichttransistors (DTFT) und der Datenleitung (Data);
durch die Treibersteuereinheit (22), Lösen der Verbindung zwischen dem Gate des Treiber-Dünnschichttransistors (DTFT) und des Drains des Treiber-Dünnschichttransistors (DTFT);
der Schritt zum Treiben der OLED Licht auszusenden und anzuzeigen aufweist: durch die Treibersteuereinheit (22), Herstellen einer Verbindung zwischen der Source des Treibers-Dünnschichttransistors (DTFT) und dem Hochpegelausgang (VDD) der Treiberenergieversorgung, Herstellen einer Verbindung zwischen dem Drain des Treiber-Dünnschichttransistors (DTFT) und der Anode der OLED, Steuern des Treiber-Dünnschichttransistors (DTFT) im Sättigungsbereich zu arbeiten und Steuern der Spannungsdifferenz zwischen zwei Enden des Speicherkondensators (Cs) unverändert zu bleiben, um die Schwellspannung Vth des Treiber-Dünnschichttransistors (DTFT) durch die Gate-Source-Spannung des Treiber-Dünnschichttransistors (DTFT) zu kompensieren und die OLED durch den Treiber-Dünnschichttransistor (DTFT) zu treiben, um Licht auszusenden.

7. Einheit mit einer OLED und der Treiberschaltung für die Pixeleinheit gemäß einem der Ansprüche 1 bis 4, wobei die Treiberschaltung für die Pixeleinheit mit einer Anode der OLED verbunden ist und eine Katode der OLED mit dem Niedrigpegelausgang (VDD) der Treiberenergieversorgung verbunden ist.

8. Anzeigevorrichtung mit einer Vielzahl von Pixeleinheiten gemäß Anspruch 7.

Revendications

1. Circuit d'attaque pour une unité de pixel, destiné à exciter une OLED, dans lequel le circuit d'attaque pour l'unité de pixel comprend : un transistor à couches minces d'attaque (DTFT), un premier élément de commutation (T1), un condensateur de stockage (Cs) et une unité de commande d'attaque (22), dans lequel
une première extrémité dudit condensateur de stockage (Cs) est connectée à une grille dudit transistor à couches minces d'attaque (DTFT), et une seconde extrémité dudit condensateur de stockage (Cs) est connectée à une sortie de niveau haut (VDD) d'une alimentation électrique d'attaque ;
une source dudit transistor à couches minces d'attaque (DTFT) est connectée à une ligne de données (Data) via ledit premier élément de commutation (T1) ;
ladite unité de commande d'attaque (22) est configurée pour commander ledit condensateur de stockage (Cs) devant être chargé et/ou déchargé pour commander ledit transistor à couches minces d'attaque (DTFT) pour un fonctionnement dans une région de saturation, de manière à compenser une tension de seuil Vth dudit transistor à couches minces d'attaque (DTFT) par une tension grille-source dudit transistor à couches minces d'attaque (DTFT) ;
dans lequel ladite unité de commande d'attaque (22) comprend en outre : un deuxième élément de commutation (T2), un troisième élément de commutation (T3), un quatrième élément de commutation (T4), et un cinquième élément de commutation (T5), dans lequel
une grille dudit deuxième élément de commutation (T2) est connectée à une première ligne de commande (CR1), une source dudit deuxième élément de commutation (T2) est connectée au drain dudit transistor à couches minces d'attaque (DTFT) ;
une grille dudit troisième élément de commutation (T3) est connectée à une ligne de balayage pour transmettre un signal de commande (SCAN), une source dudit troisième élément de commutation (T3) est connectée à la grille dudit transistor à couches minces d'attaque (DTFT), et un drain dudit troisième élément de commutation (T3) est connecté au drain dudit transistor à couches minces d'attaque (DTFT) ;
une grille dudit quatrième élément de commutation (T4) est connectée à une seconde ligne de commande (CR2), une source dudit quatrième élément de commutation (T4) est connectée au drain dudit transistor à couches minces d'attaque (DTFT), et un drain dudit quatrième élément de commutation (T4) est connecté à une anode de ladite OLED, et
une grille dudit cinquième élément de commutation (T5) est connectée à ladite seconde ligne de commande (CR2), une source dudit cinquième élément de commutation (T5) est connectée à ladite sortie de niveau haut (VDD) de l'alimentation électrique d'attaque, et un drain dudit cinquième élément de commutation (T5) est connecté à la

source dudit transistor à couches minces d'attaque (DTFT) ;
caractérisé en ce qu'un drain dudit deuxième élément de commutation (T2) est connecté à une sortie de niveau bas (VSS) de l'alimentation électrique d'attaque, et **en ce qu'**une grille dudit premier élément de commutation (T1) est connectée à la ligne de balayage (SCAN).

2. Circuit d'attaque pour l'unité de pixel selon la revendication 1, dans lequel ledit transistor à couches minces d'attaque (DTFT) est un transistor à couches minces de type p.

3. Circuit d'attaque pour l'unité de pixel selon la revendication 2, dans lequel :

ledit premier élément de commutation (T1) est un transistor à couches minces de type p ;
une source dudit premier élément de commutation (T1) est connectée à la ligne de données (Data), et un drain dudit premier élément de commutation (T1) est connecté à la source dudit transistor à couches minces d'attaque (DTFT).

4. Circuit d'attaque pour l'unité de pixel selon la revendication 3, dans lequel ledit deuxième élément de commutation (T2), ledit troisième élément de commutation (T3), ledit quatrième élément de commutation (T4) et ledit cinquième élément de commutation (T5) sont des TFT de type p.

5. Procédé destiné à exciter une unité de pixel, appliqué au circuit d'attaque pour l'unité de pixel selon la revendication 1, ledit procédé destiné à exciter une unité de pixel comprenant les étapes pour :

la charge de pixel : par l'unité de commande d'attaque (22) commandant le condensateur de stockage (Cs) à charger ;
la décharge de pixel : par l'unité de commande d'attaque (22) commandant le condensateur de stockage (22) à décharger via le transistor à couches minces d'attaque (DTFT), jusqu'à ce qu'une tension grille-source dudit transistor à couches minces d'attaque (DTFT) soit égale à la tension de seuil Vth dudit transistor à couches minces d'attaque (DTFT) ;
la mise en tampon de commutateur : par l'unité de commande d'attaque (22) commandant la tension de grille du transistor à couches minces d'attaque (DTFT) pour qu'elle demeure stable ;
l'excitation de l'OLED pour l'émission de lumière et l'affichage : par ladite unité de commande d'attaque (22) commandant le transistor à couches minces d'attaque (DTFT) pour un fonctionnement dans une région de saturation, et la commande de la différence de tension entre deux extrémités dudit condensateur de stockage (Cs) pour qu'elle demeure inchangée, de manière à compenser la tension de seuil Vth dudit transistor à couches minces d'attaque (DTFT) par la tension grille-source dudit transistor à couches minces d'attaque (DTFT) et à exciter l'OLED pour émettre une lumière par ledit transistor à couches minces d'attaque (DTFT).

6. Procédé destiné à exciter l'unité de pixel selon la revendication 5, dans lequel
l'étape pour la charge de pixel comprend : par ledit premier élément de commutateur (T1), la mise sous tension d'une connexion entre la source dudit transistor à couches minces d'attaque (DTFT) et une ligne de données ; par ladite unité de commande d'attaque (22), la mise sous tension d'une connexion entre le drain dudit transistor à couches minces d'attaque (DTFT) et une cathode de ladite OLED, la mise sous tension d'une connexion entre la grille dudit transistor à couches minces d'attaque (DTFT) et le drain dudit transistor à couches minces d'attaque (DTFT), la mise hors tension de la connexion entre la source dudit transistor à couches minces d'attaque (DTFT) et ladite sortie de niveau haut (VDD) de l'alimentation électrique d'attaque, et la commande dudit condensateur de stockage (Cs) à charger ;
l'étape pour la décharge de pixel comprend : par ladite unité de commande d'attaque (22), la mise hors tension de la connexion entre le drain dudit transistor à couches minces d'attaque (DTFT) et la cathode de ladite OLED ; par ladite unité de commande d'attaque (22) commandant ledit condensateur de stockage (Cs) à décharger via ledit transistor à couches minces d'attaque (DTFT), jusqu'à ce qu'une tension grille-source dudit transistor à couches minces d'attaque (DTFT) soit égale à la tension de seuil Vth dudit transistor à couches minces d'attaque (DTFT) ;
l'étape pour la mise en tampon de commutateur comprend : par ledit premier élément de commutation (T1), la mise hors tension de la connexion entre la source dudit transistor à couches minces d'attaque (DTFT) et la ligne de données (Data) ; par ladite unité de commande d'attaque (22), la mise hors tension de la connexion entre la grille dudit transistor à couches minces d'attaque (DTFT) et le drain dudit transistor à couches minces d'attaque (DTFT) ;
l'étape pour l'excitation de l'OLED pour l'émission de lumière et l'affichage comprend : par l'unité de commande d'attaque (22), la mise sous tension d'une connexion entre la source dudit transistor à couches minces d'attaque (DTFT) et ladite sortie de niveau haut (VDD) de l'alimentation électrique d'attaque, la mise sous tension d'une

connexion entre le drain dudit transistor à couches minces d'attaque (DTFT) et l'anode de ladite OLED, la commande dudit transistor à couches minces d'attaque (DTFT) pour un fonctionnement dans la région de saturation, et la commande de la différence de tension entre deux extrémités dudit condensateur de stockage (Cs) pour qu'elle demeure inchangée, de manière à compenser la tension de seuil Vth dudit transistor à couches minces d'attaque (DTFT) par la tension grille-source dudit transistor à couches minces d'attaque (DTFT) et à exciter l'OLED pour émettre une lumière par ledit transistor à couches minces d'attaque (DTFT).

7. Unité de pixel comprenant une OLED et le circuit d'attaque pour l'unité de pixel selon l'une quelconque des revendications 1 à 4, dans laquelle le circuit d'attaque pour l'unité de pixel est connecté à une anode de l'OLED, et une cathode de l'OLED est connectée à la sortie de niveau bas (VDD) de l'alimentation électrique d'attaque.

8. Appareil d'affichage comprenant une pluralité d'unités de pixel selon la revendication 7.

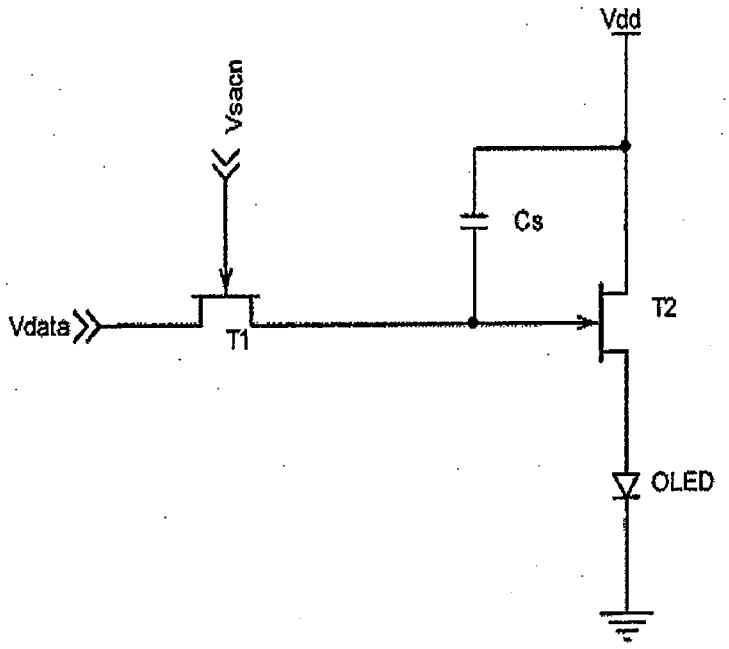
Vdd
Vsacn
Cs
Vdata
T1
T2
OLED

Fig. 1

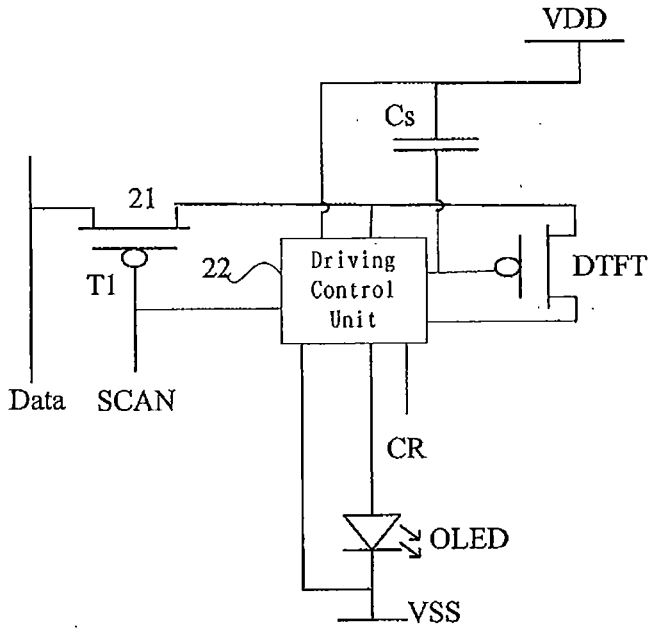
VDD
Cs
21
T1
22
Driving
Control
Unit
DTFT
Data
SCAN
CR
OLED
VSS

Fig. 2

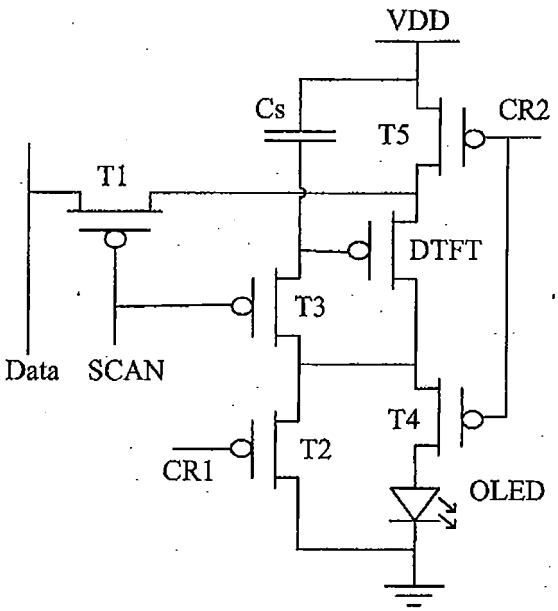
VDD
Cs
T5
CR2
T1
DTFT
T3
Data
SCAN
T4
T2
CR1
OLED

Fig. 3a

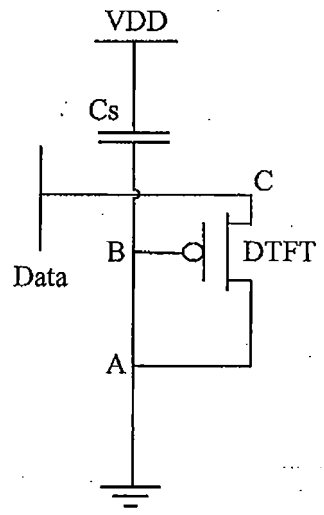
VDD
Cs
C
B
DTFT
Data
A

Fig. 3b

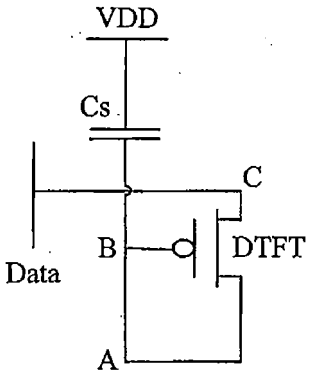

Fig. 3c

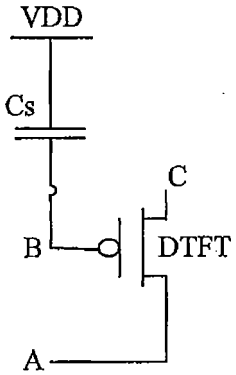

Fig. 3d

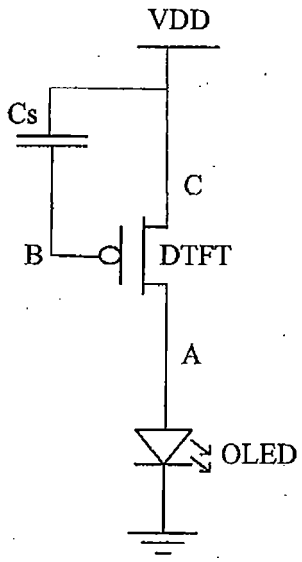

Fig. 3e

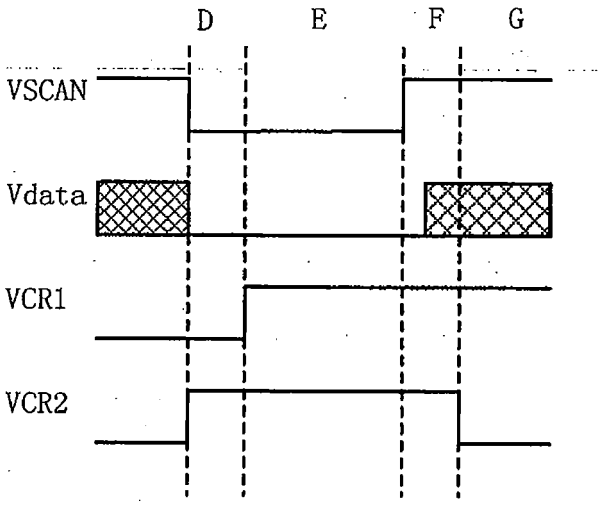

Fig. 4

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 2237254 A2 **[0004]**
- US 2006055336 A1 **[0005]**

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摘要(译)

本发明提供一种用于像素单元的驱动电路和方法，像素单元和显示装置。用于像素单元的驱动电路包括：驱动薄膜晶体管，第一开关元件，存储电容器和驱动控制单元;驱动薄膜晶体管的源极通过第一开关元件连接到数据线;驱动薄膜晶体管的漏极分别通过所述驱动控制单元连接到OLED的阳极和驱动电源的低电平输出，所述驱动薄膜晶体管的源极连接到高电平输出驱动电源的栅极和驱动薄膜晶体管的栅极连接到驱动薄膜晶体管的漏极;所述驱动控制单元用于控制所述待充电/放电的存储电容，以控制所述驱动薄膜晶体管工作在饱和区，从而利用所述驱动薄膜晶体管的阈值电压Vth进行补偿。所述驱动薄膜晶体管的栅极 - 源极电压。本发明可以解决OLED面板亮度不均匀和衰减的问题。

$$I = K \times (Vgs - Vth)^2$$

$$= K \times (Vdata - Vth - VDD - Vth)^2$$

$$= K \times (Vdata - VDD)^2; \quad \text{Equation (1)}$$