(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 2 624 244 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
07.08.2013 Bulletin 2013/32

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **12182862.8**

(22) Date of filing: **04.09.2012**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

(30) Priority: **03.02.2012 KR 20120011161**

(71) Applicant: **Samsung Display Co., Ltd.**
Yongin-City, Gyeonggi-Do, 446-711 (KR)

(72) Inventors:
- **Ahn, Jeong-Keun**
  446-711 Yongin-City (KR)
- **Lee, Wang-Jo**
  446-711 Yongin-City (KR)

(74) Representative: **Gulde Hengelhaupt Ziebig & Schneider**
Patentanwälte - Rechtsanwälte
Wallstrasse 58/59
10179 Berlin (DE)

(54) **Pixel and organic light emitting display using the same**

(57) A pixel (10) for an organic emitting display includes a first transistor (P1) coupled between a first power source (ELVDD) and a first node (N1), the first transistor (P1) including a gate electrode coupled to a second node (N2), an organic light emitting diode (OLED) coupled between the first node (N1) and a second power source (ELVSS), a second transistor (P2) for supplying a data signal to the second node (N2) in response to a scan signal, a third transistor (P3) having a source electrode (106a) and a drain electrode (106b) electrically coupled to each other, the third transistor (P3) being coupled between the first power source (ELVDD) and the second node (N2), and a fourth transistor (P4) having a source electrode and a drain electrode electrically coupled to each other, the fourth transistor (P4) being coupled between the second node (N2) and the first node (N1).

EP 2 624 244 A1

Description

BACKGROUND

1. Field

[0001] Embodiments relate to a pixel and an organic light emitting display using the same.

2. Description of the Related Art

[0002] Recently, various flat panel displays (FPD) capable of reducing weight and volume, which are disadvantages of cathode ray tubes (CRT), have been developed. The FPDs include liquid crystal displays (LCD), field emission displays (FED), plasma display panels (PDP), and organic light emitting displays.

[0003] Among the FPDs, the organic light emitting displays may display images using organic light emitting diodes (OLED) that generate light by the re-combination of electrons and holes. The organic light emitting display may have a high response speed and may be driven with low power consumption.

[0004] The organic light emitting display may be divided into a passive matrix type (PMOLED) and an active matrix type (AMOLED) in accordance with a method of driving the OLEDs in the display.

SUMMARY

[0005] According to an embodiment, there is provided a pixel including a first transistor coupled between a first power source and a first node, the first transistor including a gate electrode coupled to a second node, an organic light emitting diode (OLED) coupled between the first node and a second power source, a second transistor for supplying a data signal to the second node in response to a scan signal, a third transistor having a source electrode and a drain electrode electrically coupled to each other, the third transistor being coupled to the first power source and the second node, and a fourth transistor having another source electrode and another drain electrode electrically coupled to each other, the fourth transistor being coupled between the second node and the first node.

[0006] The data signal may have a first voltage or a second voltage set to have a larger value than the first voltage.

[0007] The third transistor may be configured to operate as a MOS capacitor when a data signal having the first voltage is supplied to the second node. The fourth transistor may be configured to operate as a MOS capacitor when a data signal having the second voltage is supplied to the second node.

[0008] The third transistor may be configured to be driven in a strong inversion mode when the data signal having the first voltage is supplied to the second node. The fourth transistor is configured to be driven in a strong inversion mode when the data signal having the second voltage is supplied to the second node.

[0009] The third transistor and the fourth transistor may each include a semiconductor layer on a substrate, a gate insulating layer on the semiconductor layer, a gate electrode on the gate insulating layer, an interlayer insulating layer on the gate electrode and the gate insulating layer. The source electrode and the drain electrode of the third transistor and the other source electrode and other drain electrode of the fourth transistor may be on the interlayer insulating layer and may be electrically coupled to the semiconductor layer through contact holes in the gate insulating layer and in the interlayer insulating layer.

[0010] The source electrode, the drain electrode, the other source electrode and the other drain electrode may be in a form of one plate above the gate electrode. A plurality of contact holes may be formed at an edge of the plate such that a contact area between the source and drain electrodes and the semiconductor layer of the third transistor and another contact area between the other source and drain electrodes and the semiconductor layer of the fourth transistor are increased.

[0011] The first to fourth transistors may be PMOS transistors or NMOS transistors.

[0012] According to an embodiment, there is provided an organic light emitting display, including a pixel unit including pixels coupled to scan lines, data lines, a first power source, and a second power source, a scan driver for supplying scan signals to the pixels through the scan lines, and a data driver for supplying data signals to the pixels through the data lines, wherein each pixel includes an organic light emitting diode (OLED) coupled between a first node and the second power source, a first transistor coupled between the first power source and the first node, the first transistor including a gate electrode coupled to a second node, a second transistor for supplying a data signal to the second node in response to a scan signal, a third transistor having a source electrode and a drain electrode electrically coupled to each other, the third transistor being coupled between the first power source and the second node, and a fourth transistor having another source electrode and another drain electrode electrically coupled to each other, the fourth transistor being coupled between the second node and the first node.

[0013] The data signal may have a first voltage or a second voltage, the second voltage having a larger value than the first voltage.

[0014] The third transistor may be configured to operate as a MOS capacitor when the data signal having the first voltage is supplied to the second node. The fourth transistor may be configured to operate as a MOS capacitor when the data signal having the second voltage is supplied to the second node.

[0015] The third transistor may be configured to be driven in a strong inversion mode when the data signal having the first voltage is supplied to the second node. The fourth transistor may be configured to be driven in a

strong inversion mode when the data signal having the second voltage is supplied to the second node.

[0016] The third transistor and the fourth transistor may each include a semiconductor layer on a substrate, a gate insulating layer on the semiconductor layer, a gate electrode on the gate insulating layer, an interlayer insulating layer on the gate electrode and the gate insulating layer. The source electrode and the drain electrode of the third transistor and the other source electrode and other drain electrode of the fourth transistor may be on the interlayer insulating layer and may be electrically coupled to the semiconductor layer through contact holes in the gate insulating layer and in the interlayer insulating layer.

[0017] The source electrode, the drain electrode, the other source electrode and the other drain electrode may be in a form of one plate above the gate electrode.

[0018] A plurality of contact holes may be formed at an edge of the plate such that a contact area between the source and drain electrodes and the semiconductor layer of the third transistor and another contact area between the other source and drain electrodes and the semiconductor layer of the fourth transistor may be increased.

[0019] The first to fourth transistors may be PMOS transistors or NMOS transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The accompanying drawings, together with the specification, illustrate exemplary embodiments, and, together with the description, serve to explain the principles.

[0021] FIG. 1 is a view illustrating an organic light emitting display according to an embodiment.

[0022] FIG. 2 is a view illustrating a pixel of the organic light emitting display of Fig. 1 according to an embodiment.

[0023] FIG. 3 is a waveform chart illustrating a method of driving the pixel of FIG. 2.

[0024] FIG. 4 is a view illustrating a pixel of the organic light emitting display of Fig. 1 according to another embodiment.

[0025] FIG. 5 is a view illustrating the section of the pixel of FIG. 2.

[0026] FIG. 6 is a layout diagram illustrating the pixel of FIG. 5.

[0027] FIG. 7 is a view illustrating the section of a pixel when each of the source and drain electrodes of a third transistor and the source and drain electrodes of a fourth transistor is formed above each of the gate electrode of the third transistor and the gate electrode of the fourth transistor as one plate.

[0028] FIG. 8 is a layout diagram illustrating the pixel of FIG. 7.

[0029] FIG. 9 is a layout diagram illustrating a pixel in which contact holes are additionally formed.

DETAILED DESCRIPTION

[0030] Detailed items of the other embodiments are included in detailed description and drawings.

[0031] Embodiments will now be described more fully with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. However, these may be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. In the drawings, when a part is coupled to another part, the part may be directly coupled to another part and the part may be electrically coupled to another part with another element interposed. In the drawings, parts that are not related to the embodiments may be omitted for clarity of description. The same reference numerals in different drawings represent the same element, and thus their description will be omitted.

[0032] Hereinafter, a pixel according to an embodiment and an organic light emitting display using the same will be described with reference to the embodiments and the drawings for describing the embodiments.

[0033] FIG. 1 is a view illustrating an organic light emitting display according to an embodiment.

[0034] Referring to FIG. 1, the organic light emitting display according to the embodiment includes a pixel unit 20 including pixels 10 coupled to scan lines S1 to Sn, data lines D1 to Dm, a first power source ELVDD, and a second power source ELVSS, a scan driver 30 for supplying scan signals to the pixels 10 through the scan lines S1 to Sn, and a data driver 40 for supplying data signals to the pixels 10 through the data lines D1 to Dm. The organic light emitting display may further include a timing controller 50 for controlling the scan driver 30 and the data driver 40.

[0035] Each of the pixels 10 is coupled to the first power source ELVDD and the second power source ELVSS.

[0036] Each of the pixels 10 that receive the first power source ELVDD and the second power source ELVSS generates light corresponding to a data signal by the current that flows from the first power source ELVDD to the second power source ELVSS via an organic light emitting diode (OLED).

[0037] The scan driver 30 generates the scan signals by the control of the timing controller 50 and supplies the generated scan signals to the pixels 10 through the scan lines S1 to Sn.

[0038] The data driver 40 generates the data signals by the control of the timing controller 50 and supplies the generated data signals to the pixels 10 through the data lines D1 to Dm.

[0039] In addition, the data driver 40 may operate so that the data signals have a first voltage V1 or a second voltage V2. Here, the second voltage V2 may be set to be larger than the first voltage V1.

[0040] FIG. 2 is a view illustrating a pixel according to an embodiment. In FIG. 2, for convenience sake, the pixel 10 coupled to the nth scan line Sn and the mth data line Dm will be illustrated.

[0041] In particular, in this embodiment, transistors P1 to P4 that constitute the pixel 10 may be p-type metal oxide semiconductor field effect (PMOS) transistors.

[0042] Referring to FIG. 2, each of the pixels 10 according to an embodiment includes an organic light emitting diode (OLED) and a pixel circuit 12 coupled to the data line Dm and the scan line Sn to control the amount of current supplied to the OLED.

[0043] The anode electrode of the OLED may be coupled to the pixel circuit 12 and the cathode electrode of the OLED is coupled to the second power source ELVSS. The OLED generates light of predetermined brightness to correspond to the current supplied from the pixel circuit 12.

[0044] The pixel circuit 12 controls the current that flows from the first power source ELVDD to the second power source ELVSS via the OLED to correspond to the data signal supplied to the data line Dm when the scan signal is supplied to the scan line Sn. Therefore, the pixel circuit 12 may include a first transistor P1, a second transistor P2, a third transistor P3, and a fourth transistor P4.

[0045] The OLED is coupled between a first node N1 and the second power source ELVSS. In detail, the anode electrode of the OLED may be coupled to the first node N1 and the cathode electrode of the OLED may be coupled to the second power source ELVSS.

[0046] The first transistor P1 as a driving transistor generates the current corresponding to the data signal supplied to the gate electrode of the first transistor P1 to supply the generated current to the OLED. Therefore, the first transistor P1 is coupled between the first power source ELVDD and the first node N1 and the gate electrode of the first transistor P1 is coupled to a second node N2.

[0047] In detail, the source electrode of the first transistor P1 may be coupled to the first power source ELVDD and the drain electrode of the first transistor P1 may be coupled to the first node N1.

[0048] The second transistor P2 may supply the data signal to the second node N2 in response to the supply of the scan signal. The second transistor P2 is turned on when the scan signal is supplied from the scan line Sn and supplies the data signal from the data line Dm to the gate electrode of the first transistor P1.

[0049] Therefore, the first transistor P1 generates the current corresponding to the voltage level of the data signal supplied to the gate electrode thereof to supply the generated current to the OLED.

[0050] In detail, the gate electrode of the second transistor P2 may be coupled to the scan line Sn, the source electrode of the second transistor P2 may be coupled to the data line Dm, and the drain electrode of the second transistor P2 may be coupled to the second node N2.

[0051] The third transistor P3 may operate as a kind of metal oxide semiconductor (MOS) capacitor. The source electrode of the third transistor P3 may be electrically coupled to the drain electrode of the third transistor P3. In detail, the source electrode and the drain electrode of the third transistor P3 may be coupled to the first power source ELVDD, and the gate electrode of the third transistor P3 may be coupled to the second node N2. Therefore, the source and drain electrodes of the third transistor P3 may be electrically coupled to each other and may be electrically coupled to the source electrode of the first transistor P1.

[0052] In particular, when a voltage (for example, the first voltage V1 of the data signal) low enough - so that a channel is formed in a semiconductor layer - is supplied to the gate electrode of the third transistor P3, the semiconductor layer and the gate electrode of the third transistor P3 between which a gate insulating layer is interposed may operate as one capacitor having predetermined capacitance.

[0053] The fourth transistor P4 may operate as a kind of MOS capacitor like the third transistor P3. The source electrode and the drain electrode of the fourth transistor P4 may be electrically coupled to each other. In detail, the source and drain electrodes of the fourth transistor P4 may be coupled to the second node N2, and the gate electrode of the fourth transistor P4 may be coupled to the first node N1. Therefore, the source and drain electrodes of the fourth transistor P4 may be electrically coupled to each other and may be electrically coupled to the gate electrode of the first transistor P1.

[0054] In particular, when a voltage (for example, the second voltage V2 of the data signal) high enough - so that the channel is formed in the semiconductor layer - is supplied to the source and drain electrodes of the fourth transistor P4, the semiconductor layer and the gate electrode of the fourth transistor P4, between which the gate insulating layer is interposed, may operate as one capacitor having predetermined capacitance.

[0055] The first node N1 may be defined as a contact point at which the anode electrode of the OLED, the drain electrode of the first transistor P1, and the gate electrode of the fourth transistor P4 are coupled to each other.

[0056] The second node N2 may be defined as a contact point at which the gate electrode of the first transistor P1, the drain electrode of the second transistor P2, the gate electrode of the third transistor P3, and the source and drain electrodes of the fourth transistor P4 are coupled to each other.

[0057] The first power source ELVDD as a high potential power source is coupled to the source electrode of the first transistor P1.

[0058] The second power source ELVSS as a low potential power source having a voltage of a lower level than the first power source ELVDD is coupled to the cathode electrode of the OLED.

[0059] FIG. 3 is a waveform chart illustrating a method of driving the pixel of FIG. 2. Hereinafter, referring to FIGS. 2 and 3, the operation of the pixel 10 according to the embodiment will be described.

[0060] First, in a first period T1, a scan signal having a voltage of a low level is supplied and a data signal having the first voltage V1 is supplied.

[0061] As the scan signal is supplied, the second transistor P2 is turned on and the data signal is supplied to the second node N2 by the turned-on second transistor P2.

[0062] The data signal supplied to the second node N2 has the first voltage V1, which is a sufficiently low voltage such that, as the first voltage V1 is supplied to the gate electrode of the third transistor P3, a channel is formed in the semiconductor layer of the third transistor P3 so that the third transistor P3 operates as a MOS capacitor.

[0063] However, as the first voltage V1 is supplied to the source and drain electrodes of the fourth transistor P4, since the channel is not formed in the semiconductor layer of the fourth transistor P4, the fourth transistor P4 does not operate as a MOS capacitor.

[0064] Therefore, a voltage corresponding to a difference between the first power source ELVDD and the first voltage V1 may be charged in the third transistor P3 that operates as a MOS capacitor so that the gate-source voltage of the first transistor P1 may be uniformly maintained until a next scan signal is supplied. Thus, the first transistor P1 generates current corresponding to the corresponding gate-source voltage so that the OLED may emit light.

[0065] Then, in a second period T2, a scan signal having a voltage of a low level is supplied and a data signal having the second voltage V2 is supplied.

[0066] As the scan signal is supplied, the second transistor P2 is turned on and the data signal is supplied to the second node N2 by the turned-on second transistor P2.

[0067] The data signal supplied to the second node N2 has the second voltage V2, which is a sufficiently high voltage such that, as the second voltage V2 is supplied to the gate electrode of the third transistor P3, the channel is not formed in the semiconductor layer of the third transistor P3, and the third transistor P3 does not operate as a MOS capacitor.

[0068] However, as the second voltage V2 is supplied to the source and drain electrodes of the fourth transistor P4, the channel is formed in the semiconductor layer of the fourth transistor P4 so that the fourth transistor P4 operates as a MOS capacitor.

[0069] Therefore, a voltage corresponding to a difference between the second voltage V2 and the voltage (the anode electrode voltage of the OLED) of the first node N1 may be charged in the fourth transistor P4 that operates as a MOS capacitor so that the first transistor P1 is turned off, until a next scan signal is supplied, to stop the emission of the OLED.

[0070] Thus, in the first period T1 where the data signal having the first voltage V1 is supplied, the third transistor P3 may operate as a MOS capacitor. However, in the second period T2 where the data signal having the second voltage V2 is supplied, the fourth transistor P4 may operate as the MOS capacitor.

[0071] In addition, when the data signal having the first voltage V1 is supplied to enhance the capacitor characteristic of the third transistor P3, the third transistor P3 may operate in a strong inversion mode. When the data signal having the second voltage V2 is supplied in order to enhance the capacitor characteristic of the fourth transistor P4, the fourth transistor P4 may operate in the strong inversion mode.

[0072] Therefore, the first voltage V1 of the data signal may be set to have a voltage value of no more than the anode electrode voltage of the OLED and the second voltage V2 of the data signal may be set to have a voltage value of no less than that of the first power source ELVDD.

[0073] FIG. 4 is a view illustrating a pixel according to another embodiment. In particular, in this embodiment, the transistors P1 to P4 that constitute the pixel 10 are n-type metal oxide semiconductor field effect (NMOS) transistors.

[0074] In this case, most of the elements of the pixel illustrated in FIG. 4 are the same as the elements of the pixel illustrated in FIG. 2. However, the conduction type of the pixel illustrated in FIG. 4 is the reverse of the conduction type of the pixel illustrated in FIG. 2. Accordingly, the coupling relationship between the third transistor P3 and the fourth transistor P4 is reversed.

[0075] That is, the source and drain electrodes of the third transistor P3 are coupled to the second node N2 and the gate electrode of the third transistor P3 is coupled to the first power source ELVDD.

[0076] In addition, the source and drain electrodes of the fourth transistor P4 are coupled to the first node N1 and the gate electrode of the fourth transistor P4 is coupled to the second node N2.

[0077] As a description of the operation of the pixel according to the present embodiment, in the case where the scan signal having the voltage of the high level is supplied and the data signal having the first voltage V1 is supplied, the data signal is supplied to the second node N2 by the turned-on second transistor P2.

[0078] The data signal supplied to the second node N2 has the first voltage V1, which is a sufficiently low voltage such that, as the first voltage V1 is supplied to the source and drain electrodes of the third transistor P3, a channel is formed in the semiconductor layer of the third transistor P3 so that the third transistor P3 operates as a MOS capacitor.

[0079] However, as the first voltage V1 is supplied to the gate electrode of the fourth transistor P4, since the channel is not formed in the semiconductor layer of the fourth transistor P4, the fourth transistor P4 does not operate as a MOS capacitor.

[0080] Therefore, the voltage corresponding to the difference between the first power source ELVDD and the first voltage V1 may be charged in the third transistor P3, which operates as a MOS capacitor. The gate-source voltage of the first transistor P1 may be uniformly maintained until a next scan signal is supplied. Therefore, the first transistor P1 may be turned off in a predetermined period so that the emission of the OLED may be stopped.

[0081] When a scan signal having a voltage of a high

level is supplied and a data signal having the second voltage V2 is supplied, the data signal is supplied to the second node N2 by the turned-on second transistor P2.

[0082] The data signal supplied to the second node N2 has the second voltage V2, which is a sufficiently high voltage such that, as the second voltage V2 is supplied to the source and drain electrodes of the third transistor P3, the channel is not formed in the semiconductor layer of the third transistor P3, and the third transistor does not operate as a MOS capacitor.

[0083] However, as the second voltage V2 is supplied to the gate electrode of the fourth transistor P4, the channel is formed in the semiconductor layer of the fourth transistor P4 so that the fourth transistor P4 operates as a MOS capacitor.

[0084] Therefore, the voltage corresponding to the difference between the second voltage V2 and the voltage (the voltage of the anode electrode of the OLED) of the first node N1 may be charged in the fourth transistor P4, which operates as a MOS capacitor so that the first transistor P1 generates a current corresponding to the corresponding gate-source voltage until a next scan signal is supplied and that the OLED may emit light.

[0085] In addition, when the data signal having the first voltage V1 is supplied to enhance the capacitor characteristic of the third transistor P3, the third transistor P3 may operate in a strong inversion mode. When the data signal having the second voltage V2 is supplied in order to enhance the capacitor characteristic of the fourth transistor P4, the fourth transistor P4 may operate in a strong inversion mode.

[0086] FIG. 5 is a view illustrating a cross-section of the pixel of FIG. 2. FIG. 6 is a layout diagram illustrating the pixel of FIG. 5.

[0087] Referring to FIGS. 5 and 6, the structures of the first to fourth transistors P1 to P4 that constitute the pixel 10 will be described in detail.

[0088] The first to fourth transistors P1 to P4 are formed on a substrate 100. The substrate 100 may be formed of a material having an insulation property such as glass, plastic, silicon, or synthetic resin and is preferably formed of a transparent substrate such as a glass substrate.

[0089] First, the structure of the third transistor P3 will be representatively described. The third transistor P3 includes a semiconductor layer 102, a gate insulating layer 103, a gate electrode 104, an interlayer insulating layer 105, and source/drain electrodes 106a and 106b.

[0090] In addition, a buffer layer 101 may be formed on the substrate 100. The buffer layer 101 for preventing contamination by impurities contained in the substrate 100 may be formed of an insulating material such as a silicon oxide layer SiO_2 or a silicon nitride layer SiN_x.

[0091] The semiconductor layer 102 is formed on the buffer layer 101 in a predetermined pattern. The semiconductor layer 102 may be formed of low temperature polysilicon (LTPS) obtained by crystallizing amorphous silicon deposited on the buffer layer 101 using a laser.

[0092] The gate insulating layer 103 is formed on the semiconductor layer 102. The gate insulating layer 103 may be formed as a nitride layer or an oxide layer, for example, a silicon oxide layer or a silicon nitride layer, or other suitable materials.

[0093] The gate electrode 104 is formed on the gate insulating layer 103 in a predetermined pattern. The interlayer insulating layer 105 is formed on the gate electrode 104.

[0094] The gate insulating layer 103 insulates the semiconductor layer 102 from the gate electrode 104. The interlayer insulating layer 105 insulates the gate electrode 104 from the source/drain electrodes 106a and 106b.

[0095] The source/drain electrodes 106a and 106b are formed on the interlayer insulating layer 105. The source/drain electrodes 106a and 106b are electrically coupled to both sides of the semiconductor layer 102 through contact holes ch formed in the gate insulating layer 103 and the interlayer insulating layer 105.

[0096] The gate electrode 104 and the source/drain electrodes 106a and 106b may be formed of a metal such as Mo, W, Ti, and A1 or an alloy or a lamination of the above metals or other suitable materials.

[0097] A planarizing layer 107 is formed on the interlayer insulating layer 105 and the source/drain electrodes 106a and 106b and may be formed of a nitride or a oxide or other suitable materials. The anode electrode 110 of the OLED is formed in a part where the planarizing layer 107 is partially removed. The anode electrode 110 of the OLED is electrically coupled to the drain electrode of the first transistor P1.

[0098] In addition, a light emitting layer 112 is formed on the anode electrode 110 of the OLED. The light emitting layer 112 has a structure in which a hole transport layer, an organic light emitting layer, and an electron transport layer are laminated. A hole injection layer and an electron injection layer may be further included.

[0099] In addition, the cathode electrode 114 of the OLED is formed on the light emitting layer 112. The cathode electrode 114 of the OLED is coupled to the second power source ELVSS.

[0100] The above-described structure of the third transistor P3 may be applied to the remaining transistors P1, P2, and P4. Accordingly, a description of the structure as applied to remaining transistors P1, P2, and P4 will not be repeated.

[0101] FIG. 7 is a view illustrating the cross-section of a pixel wherein the source and drain electrodes of a third transistor and the source and drain electrodes of a fourth transistor are each formed above the respective gate electrode of the third transistor and the gate electrode of the fourth transistor as one plate. FIG. 8 is a layout diagram illustrating the pixel of FIG. 7.

[0102] Referring to FIGS. 5 and 6, the source electrode 106a and the drain electrode 106b of each of the third transistor P3 and the fourth transistor P4 may be coupled to each other without contacting the gate electrode 104. However, referring to FIGS. 7 and 8, the source electrode

106a and the drain electrode 106b of each of the third transistor P3 and the fourth transistor P4 may be formed as one plate 130 above the gate electrode 104.

[0103] Therefore, additional capacitance may be secured through an overlapping area formed between the plate 130 formed by the source electrode 106a and the drain electrode 106b and the gate metal 104.

[0104] FIG. 9 is a layout diagram illustrating a pixel in which contact holes are additionally formed. Referring to FIG. 9, a plurality of contact holes ch for coupling the source/drain electrodes 106a and 106b of the third transistor P3 and the fourth transistor P4 to the respective semiconductor layer 102 may be formed at the edge of the plate 130 to increase the contact area between the source/drain electrodes 106a and 106b and the semiconductor layer 102.

[0105] As the contact area between the source/drain electrodes 106a and 106b and the semiconductor layer 102 increases, the data signal may be stably maintained.

[0106] Thus, in the third transistor P3, the contact holes ch may be formed at the edge on the upper and lower sides of the plate 130 formed by the source electrode 106a and the drain electrode 106b, and additional contact holes ch may be formed at the edge on the right and left sides of the plate 130.

[0107] In addition, in the fourth transistor P4, additional contact holes ch may be formed at the edge only on the left side so that the contact area of the source/drain electrodes 106a and 106b and the semiconductor layer 102 may be increased.

[0108] By way of summation and review, an active matrix type organic light emitting display (AMOLED) includes a storage capacitor for charging data signals. The storage capacitor may be in the form of a metal-insulator-metal (MIM) capacitor by doping polycrystalline silicon with impurities. However, in this case, since a channel doping mask for doping semiconductor is to be added, manufacturing time and manufacturing cost are increased. In contrast, exemplary embodiments may provide a pixel of a simple structure and an organic light emitting display using the same, whereby manufacturing time and manufacturing costs may be reduced by omitting a channel doping mask.

[0109] While the embodiments been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims, and equivalents thereof.

Claims

1. A pixel (10) for an organic light emitting display, the pixel comprising:

a first transistor (P1) coupled between a first power source (ELVDD) and a first node (N1), the first transistor (P1) including a gate electrode coupled to a second node (N2);
an organic light emitting diode (OLED) coupled between the first node (N1) and a second power source (ELVSS);
a second transistor (P2) for supplying a data signal to the second node (N2) in response to a scan signal;
a third transistor (P3) having a source electrode (106a) and a drain electrode (106b) electrically coupled to each other, the third transistor (P3) being coupled between the first power source (ELVDD) and the second node (N2); and
a fourth transistor (P4) having a source electrode and a drain electrode electrically coupled to each other, the fourth transistor (P4) being coupled between the second node (N2) and the first node (N1).

2. The pixel as claimed in claim 1, wherein:

the third transistor (P3) is configured to operate as a metal oxide semiconductor (MOS) capacitor when a data signal having a first voltage (V1) is supplied to the second node (N2), and
the fourth transistor (P4) is configured to operate as a MOS capacitor when a data signal having a second voltage (V2) is supplied to the second node (N2), wherein the second voltage (V2) has a larger value than the first voltage (V1).

3. The pixel as claimed in claim 2, wherein
the third transistor (P3) is configured to be driven in a strong inversion mode when a data signal having the first voltage (V1) is supplied to the second node (N2), and
the fourth transistor (P4) is configured to be driven in a strong inversion mode when a data signal having the second voltage (V2) is supplied to the second node (N2).

4. The pixel as claimed in one of the preceding claims, wherein:

the third transistor (P3) and the fourth transistor (P4) each include:

a semiconductor layer (102) on a substrate (100);
a gate insulating layer (103) on the semiconductor layer (102);
a gate electrode (104) on the gate insulating layer (103);
an interlayer insulating layer (105) on the gate electrode (104) and the gate insulating layer (103); and

wherein the source electrode (106a) and the drain electrode (106b) of the third transistor (P3) and the source electrode and drain electrode of the fourth transistor (P4) are on the interlayer insulating layer (105) and are electrically coupled to the semiconductor layer (102) through contact holes (ch) in the gate insulating layer (103) and in the interlayer insulating layer (105).

5. The pixel as claimed in claim 4, wherein the source electrode (106a) and the drain electrode (106b) of the third transistor (P3) are formed as one plate above the gate electrode (104) and the source electrode and drain electrode of the fourth transistor (P4) are formed as one plate above the gate electrode (104).

6. The pixel as claimed in claim 5, wherein a plurality of contact holes (ch) are formed at an edge of the plate such that a contact area between the source and drain electrodes (106a, 106b) of the third transistor (P3) and the semiconductor layer (102) of the third transistor (P3) and a contact area between the source and drain electrodes of the fourth transistor (P4) and the semiconductor layer of the fourth transistor (P4) are increased.

7. The pixel as claimed in one of the preceding claims, wherein the first to fourth transistors (P1, P2, P3, P4) are p-type metal oxide semiconductor (PMOS) transistors or n-type metal oxide semiconductor (NMOS) transistors.

8. An organic light emitting display, comprising:

a pixel unit (20) including pixels (10) according to one of the preceding claims, the pixels (10) being coupled to scan lines (S1, S2, Sn), data lines (D1, D2, Dm), a first power source (ELVDD), and a second power source (ELVSS);
a scan driver (30) for supplying scan signals to the pixels (10) through the scan lines (S1, S2, Sn); and
a data driver (40) for supplying data signals to the pixels (10) through the data lines (D1, D2, Dm).

9. The organic light emitting display as claimed in claim 8, wherein the second transistor (P2) is coupled between a respective one of the data lines (Dm) and the second node (N2), the second transistor (P2) including a gate electrode coupled to a respective one of the scan lines (Sn).

10. The organic light emitting display as claimed in one of claims 8 and 9, wherein the data driver (40) is adapted to supply a data signal having a first voltage (V1) or a second voltage (V2), the second voltage (V2) having a larger value than the first voltage (V1).

FIG. 1

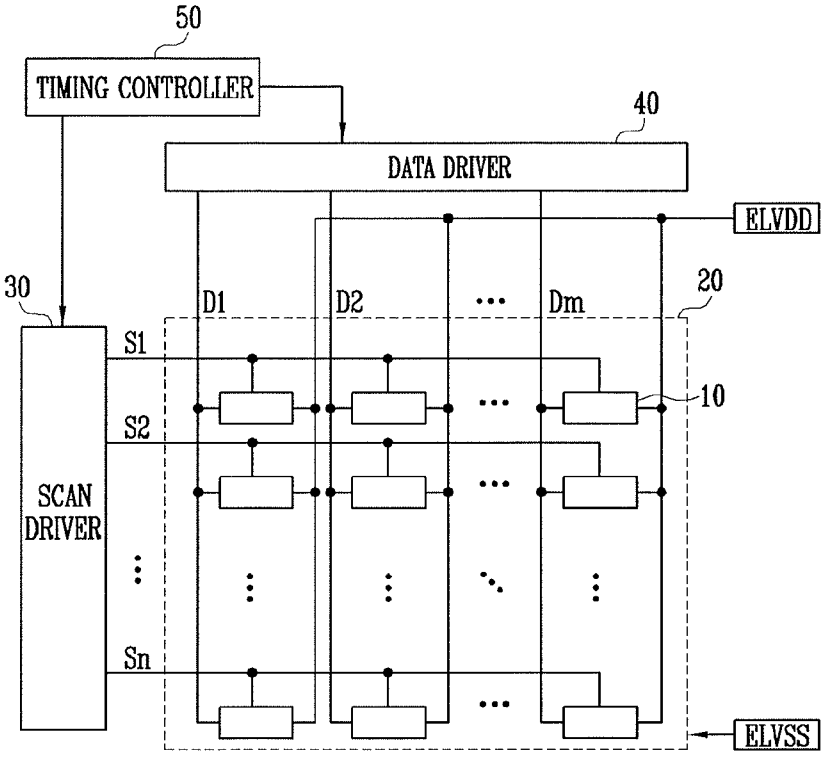

50
TIMING CONTROLLER
40
DATA DRIVER
ELVDD
30
D1
D2
Dm
20
S1
S2
10
SCAN DRIVER
Sn
ELVSS

FIG. 2

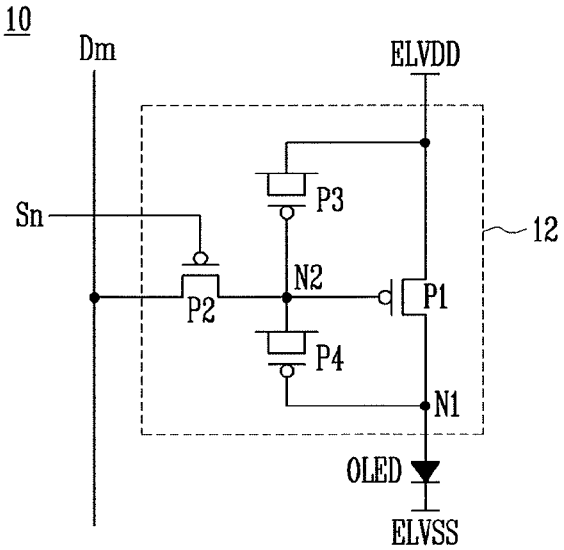

10
Dm
ELVDD
P3
Sn
12
N2
P2
P1
P4
N1
OLED
ELVSS

FIG. 3

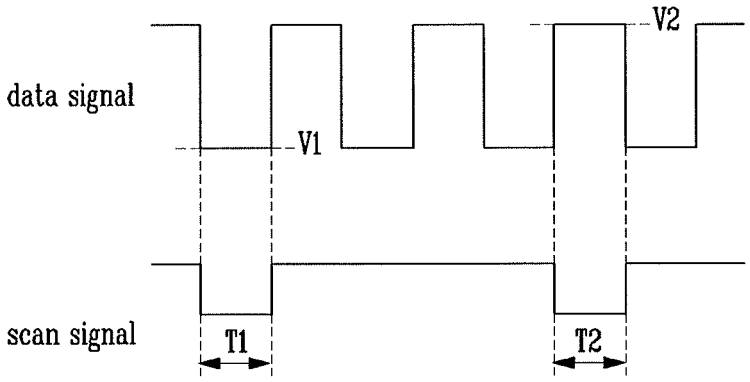

V2
data signal
V1
scan signal
T1
T2

FIG. 4

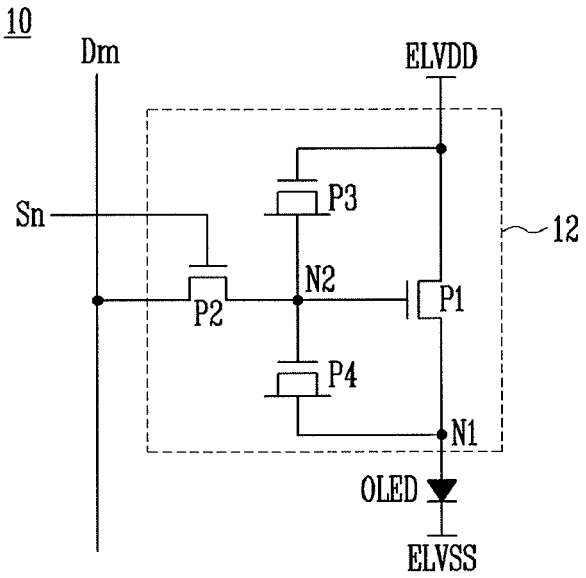

10
Dm
ELVDD
Sn
P3
12
N2
P2
P1
P4
N1
OLED
ELVSS

FIG. 5

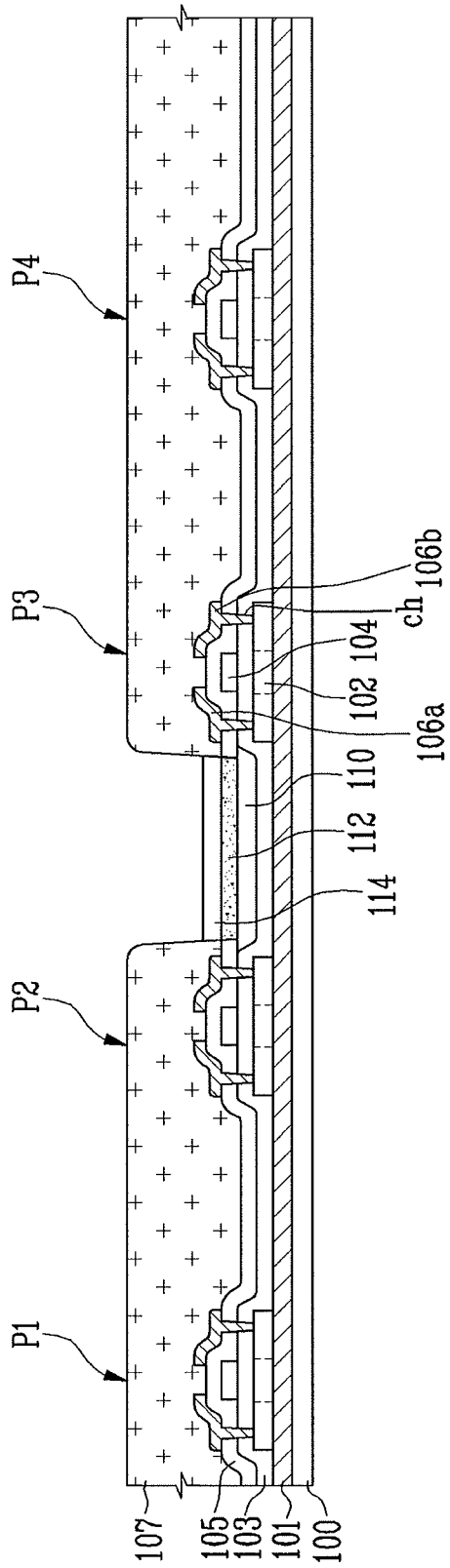


FIG. 6

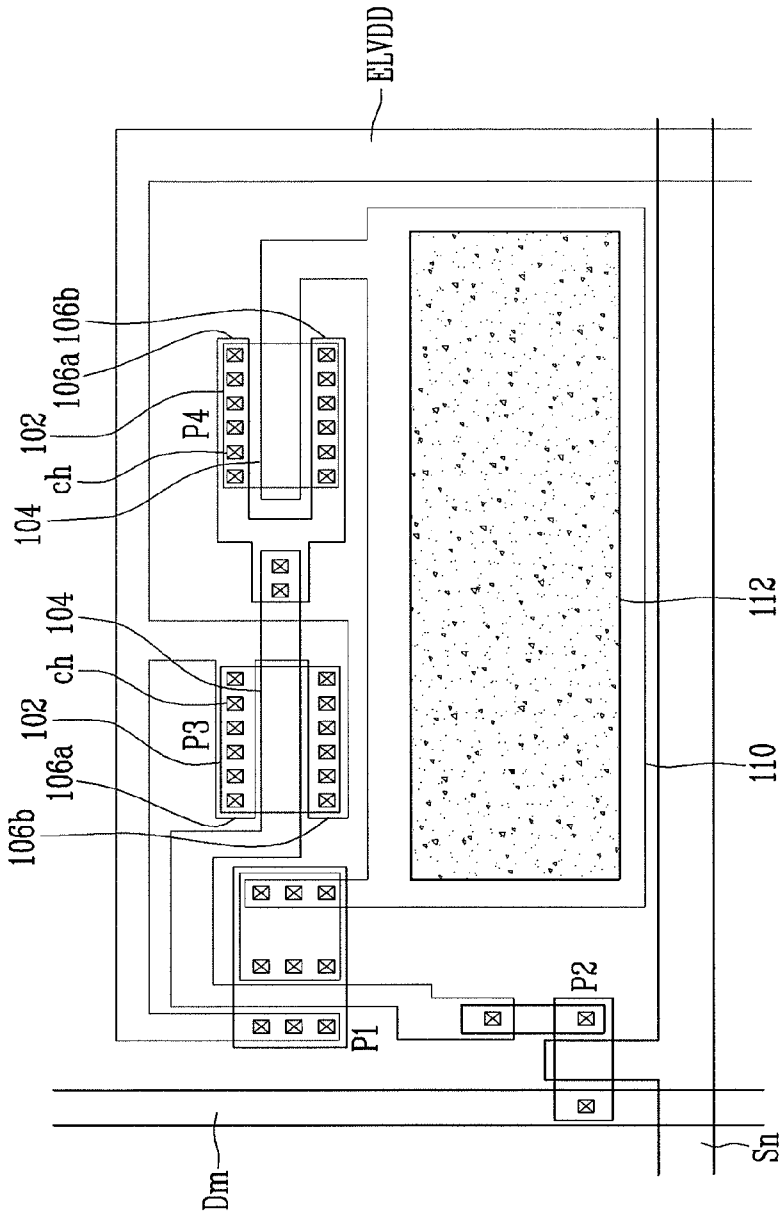

ELVDD
106b
106a
102
ch
104
P4
104
ch
102
106a
106b
P3
112
110
P2
P1
Dm
Sn

FIG. 7

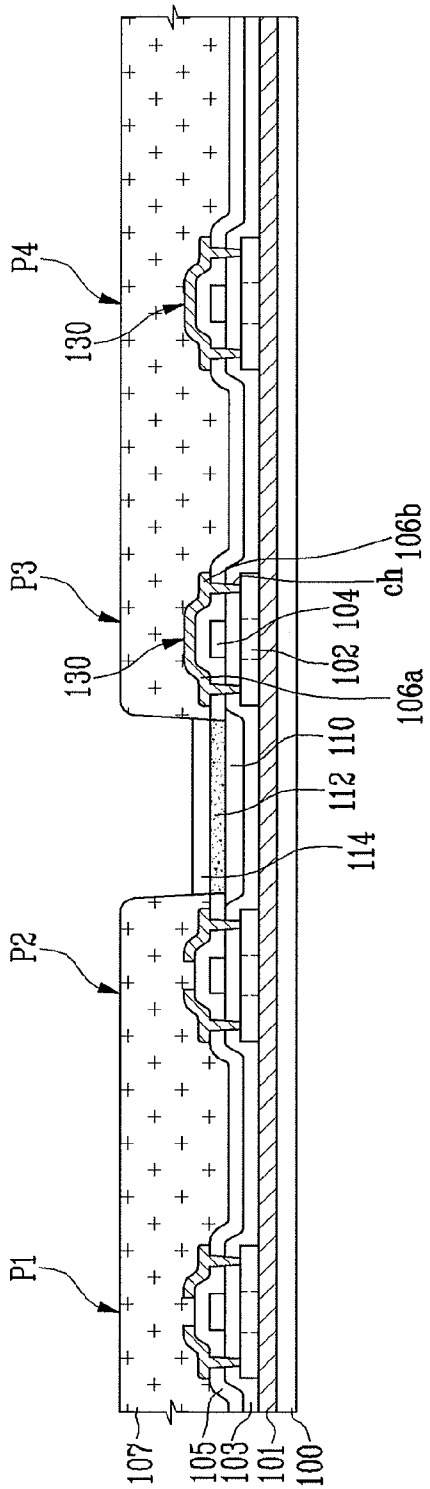

P4
130
P3
130
P2
P1
106b
ch
104
102
106a
110
112
114
107
105
103
101
100

FIG. 8

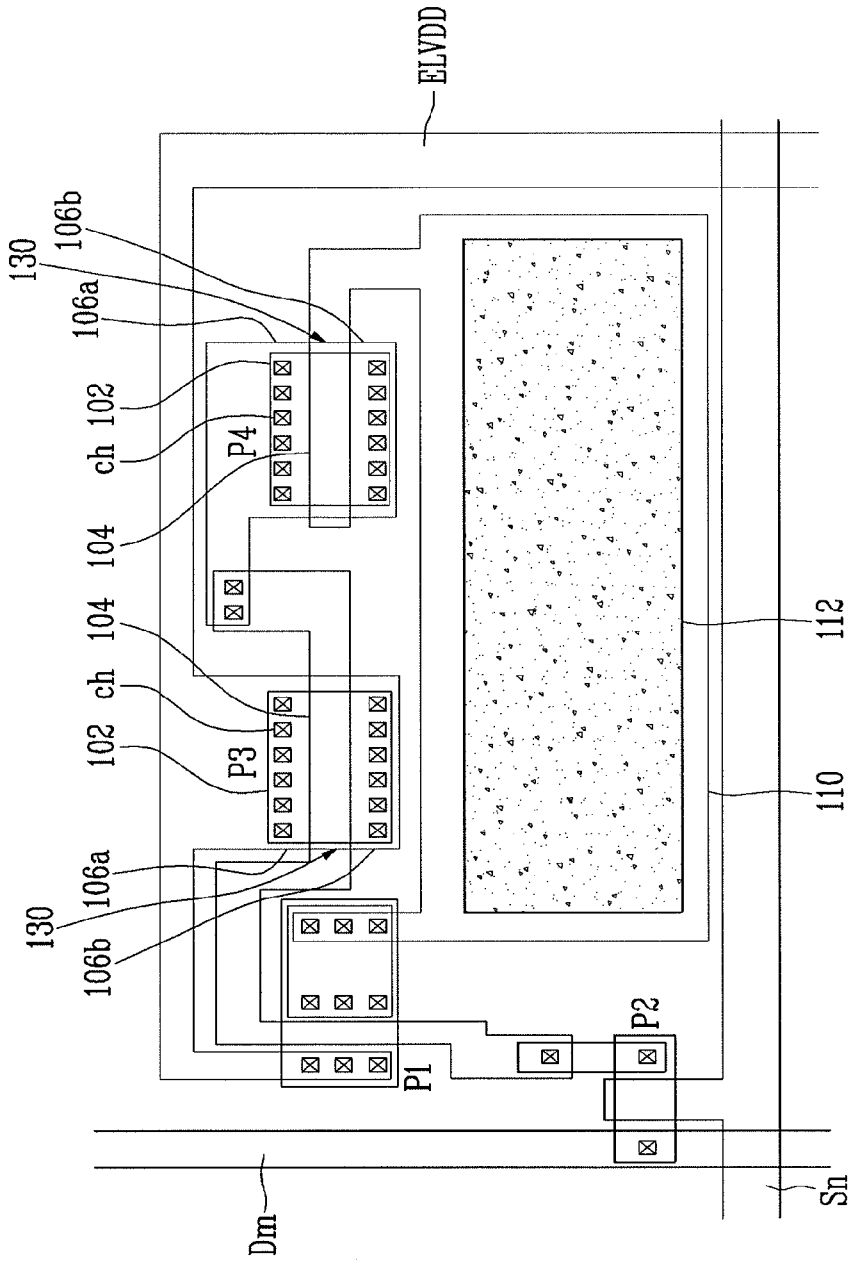
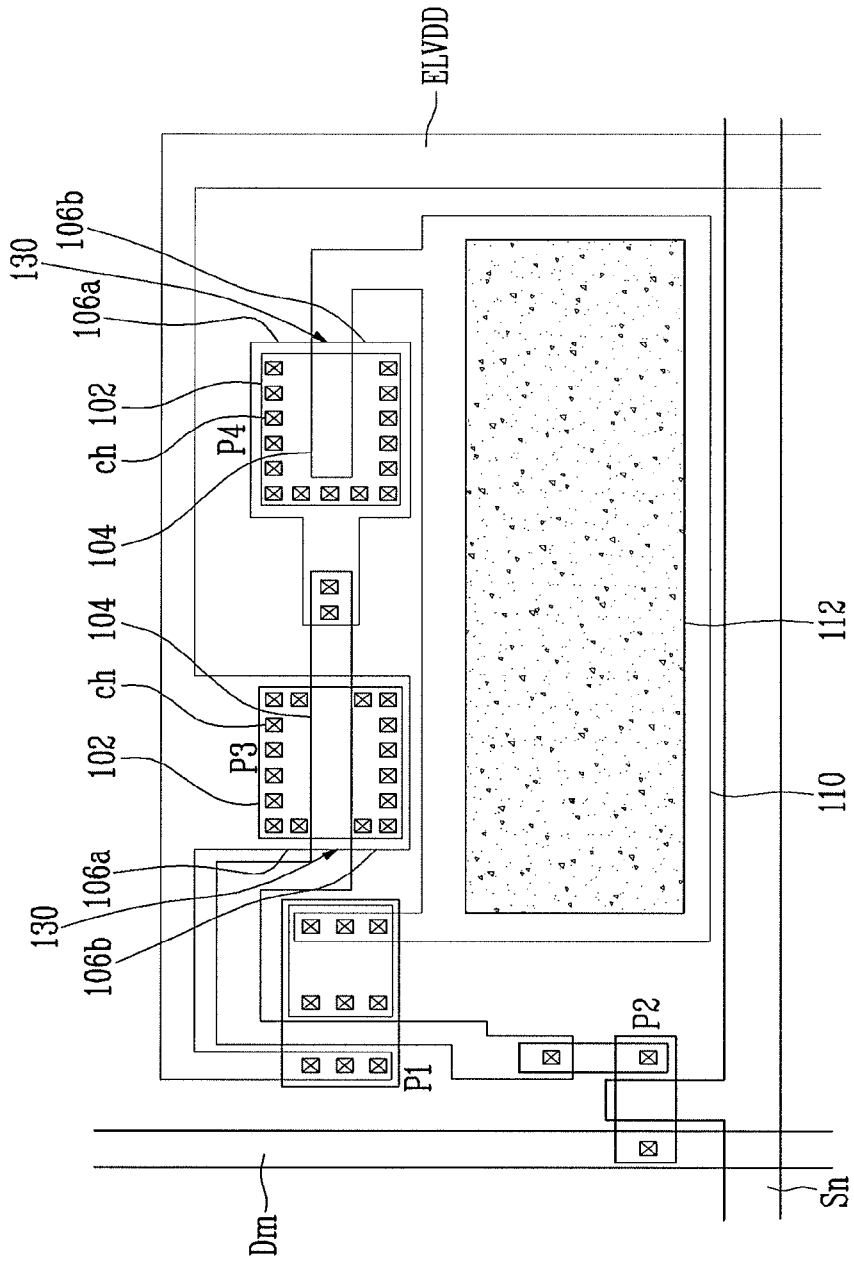

ELVDD
130
106b
106a
ch 102
P4
104
104
ch
102
P3
106a
130
106b
112
110
P2
P1
Dm
Sn

FIG. 9


ELVDD
130
106b
106a
ch 102
P4
104
104
ch
102
P3
106a
130
106b
112
110
P2
P1
Dm
Sn

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 12 18 2862

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	US 2008/150437 A1 (IIDA YUKIHITO [JP] ET AL) 26 June 2008 (2008-06-26) * paragraphs [0010], [0014], [0018]; figure 2 *	1-10	INV. G09G3/32
Y	US 2010/207863 A1 (YEN CHENG-CHI [TW] ET AL) 19 August 2010 (2010-08-19) * paragraphs [0027], [0028]; figure 2A *	1-10	
A	EP 2 006 904 A2 (SAMSUNG SDI CO LTD [KR] SAMSUNG MOBILE DISPLAY CO LTD [KR]) 24 December 2008 (2008-12-24) * paragraph [0039] *	1-10	
Y	EP 0 717 446 A2 (EASTMAN KODAK CO [US]) 19 June 1996 (1996-06-19) * page 5, line 9 - line 14; figure 1 *	1-10	
A	WO 2005/015532 A1 (KONINKL PHILIPS ELECTRONICS NV [NL]; EDWARDS MARTIN J [GB]; AYRES JOHN) 17 February 2005 (2005-02-17)	1-10	TECHNICAL FIELDS SEARCHED (IPC) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	18 December 2012	Bellatalla, Filippo

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

1

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 12 18 2862

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

18-12-2012

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008150437 A1	26-06-2008	JP 4353237 B2	28-10-2009
		JP 2008129157 A	05-06-2008
		US 2008150437 A1	26-06-2008
		US 2012176297 A1	12-07-2012
US 2010207863 A1	19-08-2010	NONE	
EP 2006904 A2	24-12-2008	CN 101330094 A	24-12-2008
		EP 2006904 A2	24-12-2008
		JP 4989415 B2	01-08-2012
		JP 2009003405 A	08-01-2009
		KR 100867926 B1	10-11-2008
		US 2008315189 A1	25-12-2008
EP 0717446 A2	19-06-1996	EP 0717446 A2	19-06-1996
		JP 3694078 B2	14-09-2005
		JP 8234683 A	13-09-1996
		US 5684365 A	04-11-1997
WO 2005015532 A1	17-02-2005	AT 385023 T	15-02-2008
		CN 1833269 A	13-09-2006
		DE 602004011521 T2	13-08-2009
		EP 1654723 A1	10-05-2006
		JP 4851326 B2	11-01-2012
		JP 2007502068 A	01-02-2007
		KR 20060065671 A	14-06-2006
		US 2006232577 A1	19-10-2006
		WO 2005015532 A1	17-02-2005

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	使用其的像素和有机发光显示器		
公开(公告)号	EP2624244A1	公开(公告)日	2013-08-07
申请号	EP2012182862	申请日	2012-09-04
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	AHN JEONG KEUN LEE WANG JO		
发明人	AHN, JEONG-KEUN LEE, WANG-JO		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G3/2014 G09G2300/0847		
优先权	1020120011161 2012-02-03 KR		
其他公开文献	EP2624244B1		
外部链接	Espacenet		

摘要(译)

用于有机发光显示器的像素（10）包括耦合在第一电源（ELVDD）和第一节点（N1）之间的第一晶体管（P1），第一晶体管（P1）包括耦合到第二节点的栅电极（ N2），耦合在第一节点（N1）和第二电源（ELVSS）之间的有机发光二极管（OLED），用于响应于第二节点（N2）向第二节点（N2）提供数据信号的第二晶体管（P2）扫描信号，第三晶体管（P3），具有彼此电耦合的源电极（106a）和漏电极（106b），第三晶体管（P3）耦合在第一电源（ELVDD）和第二节点之间（ N2）和第四晶体管（P4）具有彼此电耦合的源电极和漏电极，第四晶体管（P4）耦合在第二节点（N2）和第一节点（N1）之间。

FIG. 1

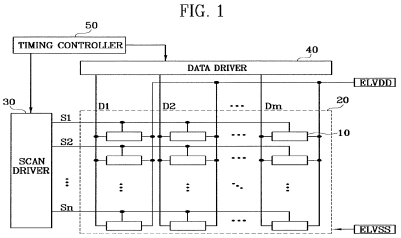


FIG. 2