



(11) **EP 2 293 274 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention
of the grant of the patent:
20.11.2013 Bulletin 2013/47

(51) Int Cl.:
G09G 3/00 (2006.01) G09G 3/32 (2006.01)

(21) Application number: **10171396.4**

(22) Date of filing: **30.07.2010**

(54) **Organic light emitting display and driving method thereof**

Organische lichtemittierende Anzeige und Verfahren zu ihrer Ansteuerung

Affichage électroluminescent organique et procédé de commande correspondant

(84) Designated Contracting States:
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO
PL PT RO SE SI SK SM TR**

(30) Priority: **03.08.2009 KR 20090071280**

(43) Date of publication of application:
09.03.2011 Bulletin 2011/10

(73) Proprietor: **Samsung Display Co., Ltd.
Yongin-City, Gyeonggi-Do, 446-711 (KR)**

(72) Inventor: **Lee, Baek-Woon
Gyeonggi-do (KR)**

(74) Representative: **Gulde Hengelhaupt Ziebig &
Schneider
Patentanwälte - Rechtsanwälte
Wallstrasse 58/59
10179 Berlin (DE)**

(56) References cited:
**EP-A2- 1 418 566 WO-A1-2007/021458
US-A- 5 990 629 US-A1- 2004 239 664
US-A1- 2005 083 270 US-A1- 2008 036 706
US-A1- 2009 058 843 US-B1- 6 229 506
US-B1- 6 380 689 US-B1- 6 731 276**

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2009-0071280, filed on August 3, 2009, in the Korean Intellectual Property Office.

BACKGROUND

1. Field

[0002] An aspect of one embodiment of the present invention is directed to an organic light emitting display, and a driving method thereof.

2. Description of Related Art

[0003] Various flat panel displays with reduced weight and volume in comparison to a cathode ray tube display have been developed. The various flat panel displays include a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), an organic light emitting display, etc.

[0004] Among the various flat panel displays, the organic light emitting display, which displays an image using organic light emitting diodes (OLEDs) that emit light by a re-combination of electrons and holes, has a high response speed and low power consumption.

[0005] Generally, organic light emitting displays can be classified as a passive matrix type OLED (PMOLED) display and an active matrix type OLED (AMOLED) display according to a method of driving the OLEDs.

[0006] The AMOLED display includes a plurality of gate lines, a plurality of data lines, a plurality of power lines, and a plurality of pixels that are coupled to the lines and arranged in a matrix form. Also, each of the pixels generally includes an OLED, two transistors, e.g., a switching transistor that transfers a data signal and a driving transistor that drives the OLED according to the data signal, and a capacitor that maintains the data voltage.

[0007] The AMOLED display has low power consumption, but the amount of current flowing through its OLEDs varies according to deviations in the threshold voltage of its transistors to cause display non-uniformity.

[0008] In other words, since the characteristics of the transistors provided in each pixel fluctuate according to variables in their manufacturing processes, it is difficult to manufacture the transistors so that the characteristics of all of the transistors in the AMOLED display are identical, thereby causing deviations in the threshold voltage of the driving transistors of the pixels.

[0009] A compensation circuit that includes a plurality of transistors and capacitors can be additionally included in the respective pixels. However, if the compensation circuit is added in the respective pixels as described

above beside the transistors and capacitors that constitute each pixel and the signal lines that control the transistors in a bottom emission type AMOLED display, an aperture ratio is reduced, and the probability that defects are generated is increased due to the increased complexity of the circuit.

[0010] Moreover, there is a recent demand for a high-speed scan driving of 120Hz or more in order to reduce or eliminate the screen motion blur phenomenon. However, in this case, a charging time available for each scan line is significantly reduced. In other words, when the compensation circuit is provided in each pixel so that a plurality of transistors are additionally provided in each pixel coupled to one scan line, its capacitive load becomes larger, such that the high-speed scan driving is difficult to be implemented.

[0011] US Patent 6,380,689 B1 discloses a electroluminescent display comprising a plurality of pixels coupled to address lines and data lines, and a power supply circuit for applying a first power to the pixels and adapted to apply voltage values at three different levels to the pixels during periods of one frame, wherein the emission period and the address period do not overlap. Furthermore, US patent application 2009/0058843 A1 deals with an electroluminescent display comprising: a plurality of pixels coupled to scan lines, bias lines, and data lines; a bias application circuit for providing control signals to the pixels through the bias lines; and a power source for applying a first power to the pixels and adapted to apply voltage values at two different levels to the pixels during periods of one frame.

Furthermore, US patent 6,229,506 B1 discloses a LED pixel structure comprising a first and a second transistor, first to third capacitors, and an organic light emitting diode.

SUMMARY OF THE INVENTION

[0012] Aspects of an embodiment of the present invention are directed toward an organic light emitting diode (OLED) display that includes OLEDs, where each pixel includes an OLED and a pixel circuit coupled thereto, and a driving method thereof. The pixel circuit includes three transistors and two capacitors, the pixels being driven in a simultaneous (or concurrent) emission scheme, and is able to perform the threshold voltage compensation of the driving transistors provided in the pixels and the high-speed driving thereof.

[0013] The present invention comprises an organic light emitting display according to claim 1.

[0014] Each of the pixels includes: a first transistor having a gate electrode coupled to a scan line of the scan lines, a first electrode coupled to a data line of the data lines, and a second electrode coupled to a first node; a second transistor having a gate electrode coupled to a second node, a first electrode coupled to the first power, and a second electrode; a first capacitor coupled between the first node and the first electrode of the second

transistor; a second capacitor coupled between the first node and the second node; a third transistor having a gate electrode coupled to a control line of the control lines, a first electrode coupled to the gate electrode of the second transistor, and a second electrode coupled to the second electrode of the second transistor; and an organic light emitting diode having an anode electrode coupled to the second electrode of the second transistor and a cathode electrode coupled to the second power, wherein the first to third transistors are PMOS transistors.

[0015] Alternatively, each of the pixels includes a first transistor having a gate electrode coupled to a scan line of the scan lines, a first electrode coupled to a data line of the data lines, and a second electrode coupled to a first node; a second transistor having a gate electrode coupled to a second node, a first electrode coupled to a second power, and a second electrode; a first capacitor coupled between the first node and the first electrode of the second transistor; a second capacitor coupled between the first node and the second node; a third transistor having a gate electrode coupled to a control line of the control lines, a first electrode coupled to the gate electrode of the second transistor, and a second electrode coupled to the second electrode of the second transistor; and an OLED having a cathode electrode coupled to the second electrode of the second transistor and an anode electrode coupled to the first power, wherein the first to third transistors are NMOS transistors.

[0016] Also the present invention is directed to a driving method of claim 2 of driving of an organic light emitting display according to claim 1. The method includes: (a) initializing voltages of respective nodes of a plurality of pixel circuits included in respective pixels by concurrently applying a first power, a second power, scan signals, control signals, and data signals, having voltage values at respective levels, to all of the pixels that constitute a display unit; (b) dropping a voltage of an anode electrode of an OLED included in the respective pixels below a voltage of a cathode electrode of the OLED by concurrently applying the first power, the second power, the scan signals, the control signals, and the data signals, having the voltage values at respective levels, to all of the pixels; (c) storing a threshold voltage of a driving transistor included in the respective pixels by concurrently applying the first power, the second power, the scan signals, the control signals, and the data signals, having the voltage values at respective levels, to all of the pixels; (d) applying the scan signals sequentially to the pixels coupled to scan lines of the display unit and applying the data signals to the pixels by each of the scan lines corresponding to the sequentially applied scan signals; (e) light-emitting concurrently all of the pixels at brightness corresponding to the data signals stored in the respective pixels by concurrently applying the first power, the second power, the scan signals, the control signals, and the data signals, having the voltage values at respective levels, to all of the pixels; and (f) turning off emission of the pixels by concurrently applying the first power, the sec-

ond power, the scan signals, the control signals, and the data signals, having the voltage values at respective levels, to all of the pixels and thus lowering the voltage of the anode electrode of the OLED included in the respective pixels.

[0017] One frame may be implemented through (a) to (f).

[0018] For a progressively displayed frame, an n th frame may display a left-eye image and an $(n+1)$ th frame may display a right-eye image.

[0019] An entire time between an emission period of the n th frame and an emission frame of the $(n+1)$ th frame may be synchronized with a response time of a shutter glasses.

[0020] Each of the pixels may include a first PMOS transistor having a gate electrode coupled to a scan line of the scan lines, a first electrode coupled to a data line, and a second electrode coupled to a first node; a second PMOS transistor having a gate electrode coupled to a second node, a first electrode coupled to the first power, and a second electrode; a first capacitor coupled between the first node and the first electrode of the second transistor; a second capacitor coupled between the first node and the second node; a third PMOS transistor having a gate electrode coupled to a control line, a first electrode coupled to the gate electrode of the second transistor, and a second electrode coupled to the second electrode of the second transistor; and an organic light emitting diode (OLED) having an anode electrode coupled to the second electrode of the second transistor and a cathode electrode coupled to the second power.

[0021] In (a), the first power may be applied at a middle level, the scan signals may be applied at a low level, and the control signals may be applied at a high level.

[0022] Here, (b) may include: (b1) wherein the first power is applied at a low level, the scan signal may be applied at a high level or a low level, and the control signals may be applied at a high level; (b2) wherein the first power may be applied at a low level, the scan signals may be applied at a high level or a low level, and the control signals may be applied at a high level; (b3) wherein the first power may be applied at a middle level, the scan signals may be applied at a high level or a low level, and the control signals may be applied at a high level.

[0023] In (b1) and (b2), if the scan signals are applied at a low level, the data signals corresponding thereto may be applied at a low level.

[0024] In (b3), if the scan signals are applied at a low level, the data signals corresponding thereto may be applied at a high level.

[0025] Here (c) may include: (c1) wherein the first power may be applied at a middle level, the scan signals may be applied at a high level or a low level, and the control signals may be applied at a high level; and (c2) and (c3), wherein the first power may be applied at a middle level, the scan signals may be applied at a low level, and the control signals may be applied at a low level.

[0026] In (c1), if the scan signals are applied at a low

level, the data signals corresponding thereto may be applied at a high level.

[0027] In (d), the control signals may be applied at a low level.

[0028] In (d), widths of the sequentially applied scan signals may be applied at two horizontal time, adjacently applied ones of the scan signals being applied to be overlapped with each other by one horizontal time.

[0029] In (e), the first power may be applied at a high level, and the scan signals and the control signals may be applied at a high level.

[0030] In (f), the first power may be applied at a middle level, and the scan signal and the control signal may be applied at a high level.

[0031] Moreover, other embodiments with more improved performance can be implemented through the simultaneous (or concurrent) emission scheme as described for a three dimensional (3D) display.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The accompanying drawings, together with the specification, illustrate exemplary embodiments of the present invention, and, together with the description, serve to explain the principles of the present invention.

[0033] FIG. 1 is a block diagram of an organic light emitting display according to an embodiment of the present invention;

[0034] FIG. 2 is a diagram showing a driving operation in a simultaneous emission scheme according to an embodiment of the present invention;

[0035] FIG. 3 is a diagram showing an example where a pair of shutter glasses for 3D display is implemented in a progressive emission scheme according to a related art;

[0036] FIG. 4 is a diagram showing an example where a pair of shutter glasses for 3D display is implemented in a simultaneous emission scheme according to an embodiment of the present invention;

[0037] FIG. 5 is a graph comparing the duty ratios obtained in the simultaneous emission scheme and the progressive emission scheme;

[0038] FIG. 6 is a circuit diagram of a pixel in FIG. 1 according to one embodiment of the present invention;

[0039] FIGS. 7A, 7B, and 7C are driving timing diagrams of the pixel in FIG. 6;

[0040] FIGS. 8A, 8B, 8C, 8D, 8E, 8F, 8G, 8H, 8I, and 8J are diagrams for explaining the driving of an organic light emitting display according to an embodiment of the present invention; and

[0041] FIG. 9 is a circuit diagram of the pixel in FIG. 1 according to another embodiment of the present invention.

DETAILED DESCRIPTION

[0042] Hereinafter, certain exemplary embodiments according to the present invention will be described with

reference to the accompanying drawings. Here, when a first element is described as being coupled to a second element, the first element may be directly coupled to the second element or indirectly coupled to the second element via a third element. Further, some of the elements that are not essential to a complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0043] FIG. 1 is a block diagram of an organic light emitting display according to an embodiment of the present invention, and FIG. 2 is a diagram showing a driving operation in a simultaneous emission scheme according to an embodiment of the present invention.

[0044] Referring to FIG. 1, the organic light emitting display according to one embodiment of the present invention includes a display unit 130 that includes pixels 140 that are coupled to scan lines S1 to Sn, control lines GC1 to GCn and data lines D1 to Dm, a scan driver 110 that provides scan signals to the respective pixels through the scan lines S1 to Sn, a control line driver 160 that provides control signals to the respective pixels through the control lines GC1 to GCn, a data driver 120 that provides data signals to the respective pixels through the data lines D1 to Dm, and a timing controller 150 that controls the scan driver 110, the data driver 120, and the control line driver 160.

[0045] The pixels 140 are positioned in regions defined by the crossings of the scan lines S1 to Sn and the data lines D1 to Dm. The pixels 140 receive first power ELVDD and second power ELVSS from the outside. Each of the pixels 140 controls the amount of current supplied to the second power ELVSS from the first power ELVDD through an organic light emitting diode (OLED) corresponding to the data signal. Then, light having a brightness (e.g., a predetermined brightness) is generated from the OLED.

[0046] However, in the embodiment of FIG. 1, the first power ELVDD and/or the second power ELVSS is applied to the respective pixels 140 of the display unit at voltage values at different levels during one frame.

[0047] To this end, a first power ELVDD driver 170 that controls the supply of the first power ELVDD and/or a second power ELVSS driver 180 that controls the supply of the second power ELVSS are further provided, and the first power ELVDD driver 170 and the second power ELVSS driver 180 are controlled by the timing controller 150.

[0048] In a related art, the first power ELVDD is supplied having a voltage at a fixed high level, and the second power ELVSS is supplied having a voltage at a fixed low level to the pixels of a display unit.

[0049] However, in the embodiment of FIG. 1, the first power ELVDD and the second power ELVSS are applied in accordance with the following three schemes.

[0050] In a first scheme, the first power ELVDD is applied having voltage values at three different levels, and the second power ELVSS is applied having a voltage at a fixed low level (for example, ground).

[0051] In the first scheme, the second power ELVSS driver 180 outputs the second power ELVSS with a voltage value at a constant level (e.g., GND) so that there is no need to implement the second power ELVSS driver 180 as a separate driving circuit, thereby making it possible to reduce circuit costs. The first power ELVDD has a negative voltage value (for example, -3V) as one of the three levels so that the circuit constitution of the first power ELVDD driver 170 may be complicated in the first scheme, however.

[0052] In a second scheme, the first power ELVDD and the second power ELVSS are applied each having voltage values at two levels. In this case, both the first power driver 170 and the second power driver 180 are provided.

[0053] In a third scheme, the first power ELVDD is applied having a voltage value at a fixed high level, and the second power ELVSS is applied having voltage values at three different levels, being opposite to the first scheme.

[0054] In other words, in the third scheme, the first power driver 170 outputs the voltage value at a constant level so that there is no need to implement the first power driver 170 as a separate driving circuit, thereby making it possible to reduce circuit costs. The second power ELVSS has a positive voltage value as one of its three levels so that the circuit constitution of the second power ELVSS driver 180 may be complicated, in the third scheme, however.

[0055] The timing control diagram for the above described three schemes to apply the first power ELVDD and the second power ELVSS will be shown in more detail in FIG. 4.

[0056] Moreover, in the embodiment of FIG. 1, the organic light emitting display is driven in a simultaneous emission scheme rather than in a progressive emission scheme. As shown in FIG. 2, this means that data is input in sequence during the period of one frame, and after the input of the data is completed, the lighting of the pixels in accordance with the data of one frame is implemented through the entire display unit 130, that is, all of the pixels 140 of the display unit.

[0057] In other words, in the progressive emission scheme according to the related art, the emission is performed in sequence right after data is input in sequence per scan line. However, in the embodiment of FIG. 1, the input of the data is performed in sequence, but the emission is concurrently performed with all of the pixels 140 after the input of the data is completed.

[0058] Referring to FIG. 2, the driving step according to an embodiment of the present invention is divided into (a) an initialization step, (b) a reset step, (c) a threshold voltage compensation step, (d) a scanning step (a data input step), (e) an emission step, and (f) an emission turn-off step. Herein, (d) the scanning step (the data input step) is performed in sequence per the respective scan lines, but (a) the initialization step, (b) the reset step, (c) the threshold voltage compensation step, (e) the emission step, and (f) the emission turn-off step are performed

simultaneously (or concurrently) on the entire display unit 130.

[0059] Here, (a) the initialization step is a period where voltages at nodes of the pixel circuits respectively provided in the pixels are initialized to be identical with those in the threshold voltage compensation step (c) of the driving transistor, and (b) the reset step, which is a step where the data voltage applied to each pixel 140 of the display unit 130 is reset, is a period where the voltage of the anode electrode of the OLED of each pixel 140 is dropped below the voltage of the cathode electrode so that the organic light emitting diode is not light-emitting.

[0060] Further, (c) the threshold voltage compensation step is a period where the threshold voltage of the driving transistor provided in each pixel 140 is compensated for, and (f) the emission turn-off step is a period where the emission of each pixel 140 is turned off for a black insertion or a dimming after the emission is performed in each pixel.

[0061] Therefore, the signals applied during (a) the initialization step, (b) the reset step, (c) the threshold voltage compensation step, (e) the emission step, and (f) the emission turn-off step, that is, the scan signals applied to the respective scan lines S1 to Sn, the first power ELVDD and/or the second power ELVSS applied to the respective pixels 140, and the control signals applied to the respective control lines GC1 to GCn are simultaneously (or concurrently) applied to the pixels 140 provided in the display unit 130 at respective voltage levels (e.g., predetermined voltage levels).

[0062] In the case of the "simultaneous emission scheme" according to one embodiment of FIG. 2, the respective operation periods ((a) to (f) steps) are clearly divided in time. Therefore, the number of the transistors of the compensation circuit provided in the respective pixels 140 and the number of the signal lines that control thereof can be reduced such that the pair of shutter glasses for 3D display can be easily implemented.

[0063] When a user wears the pair of shutter glasses for 3D display that switches transmittance of left eye and right eye between 0% and 100% to see a screen, which is displayed on the display unit of the organic light emitting display, the screen is output as a left-eye image and a right-eye image for each frame so that the user sees the left-eye image with only his or her left-eye and the right-eye image with only his or her right-eye, thereby implementing three-dimensional effects.

[0064] FIG. 3 is a diagram showing an example where a pair of shutter glasses for 3D display is implemented in a progressive emission scheme according to a related art, and FIG. 4 is a diagram showing an example where a pair of shutter glasses for 3D display is implemented in a simultaneous emission scheme according to an embodiment of the present invention.

[0065] FIG. 5 is a graph comparing the duty ratio (emission time) that can be obtained in the cases of the simultaneous emission scheme and the progressive emission scheme.

[0066] When the screen is output in the progressive emission scheme according to the related art as aforementioned in the case of implementing such a pair of shutter glasses for 3D display, as shown in FIG. 3, the response time (for example, 2.5ms) of the pair of shutter glasses is finite (e.g., non-zero) so that the emission of pixels should be turned off during the response time in order to prevent a cross talk phenomenon between the left eye/right eye images.

[0067] In other words, a non-light emitting period during the response time is additionally generated between a frame (n^{th} frame) where the left-eye image is output and a frame ($(n+1)^{\text{st}}$ frame) where the right-eye image is output. Therefore, having a disadvantage that the securing of the emission time, that is, the duty ratio of the emission time decreases.

[0068] In the case of the "simultaneous emission scheme" according to an embodiment of the present invention, referring to FIG. 4, the light-emitting step is simultaneously (or concurrently) performed on all the pixels as aforementioned, and the non-emission period is performed during the periods other than the light-emitting step so that the non-emission period between the period where the left-eye image is output and the period where the right-eye image is output is naturally provided.

[0069] In other words, the emission turn-off period, the reset period, and the threshold voltage compensation period, which are the periods between the emission period of the n^{th} frame and the emission period of the $(n+1)^{\text{th}}$ frame, are non-light emitting so that if the overall time of these periods is synchronized with the response time (for example, 2.5ms) of the pair of shutter glasses, there is no need to separately reduce the duty ratio, which is different from the progressive emission scheme according to the related art.

[0070] Therefore, when implementing the pair of shutter glasses for 3D display, the "simultaneous emission scheme" can secure the duty ratio by the response time of the pair of shutter glasses as compared to the "progressive emission scheme" according to the related art, making it possible to improve performance as shown in the graph of FIG. 5.

[0071] FIG. 6 is a circuit diagram of the pixel 140 of FIG. 1 according to one embodiment of the present invention, and FIGS. 7A to 7C are driving timing diagrams of the pixel in FIG. 6.

[0072] Referring to FIG. 6, the pixel 140 according to one embodiment of the present invention includes an OLED and a pixel circuit 142 that supplies current to the OLED.

[0073] The anode electrode of the OLED is coupled to the pixel circuit 142, and the cathode electrode of the OLED is coupled to a second power ELVSS. The OLED generates light having a brightness (e.g., a predetermined brightness) corresponding to the current supplied from the pixel circuit 142.

[0074] However, in the embodiment of FIG. 1, the respective pixels 140 that constitute the display unit 130

receive data signals supplied to the data lines D1 to Dm when scan signals are supplied sequentially to the scan lines S1 to Sn for a partial period (the aforementioned (d) step) of one frame, but the scan signals applied to the respective scan lines S1 to Sn, the first power ELVDD and/or second power ELVSS applied to the respective pixels 140, control signals applied to the respective control lines GC1 to GCn are simultaneously (or concurrently) applied to the respective pixels 140, having respective voltage levels (e.g., predetermined voltages), for other periods ((a), (b), (c), (e), and (f) steps) of one frame.

[0075] Therefore, the pixel circuit 142 provided in each of the pixels 140 includes three transistors M1 to M3 and two capacitors C1 and C2 according to one embodiment of the present invention.

[0076] Moreover, in the embodiment of FIG. 6, a parasitic capacitor Coled is generated by the anode electrode and the cathode electrode of the organic light emitting diode OLED, the coupling effects by the second capacitor C2 and the parasitic capacitor Coled are utilized. This will be described in more detail with reference to FIG. 8.

[0077] Here, the gate electrode of the first transistor M1 is coupled to a scan line S and the first electrode of the first transistor M1 is coupled to a data line D. And, the second electrode of the first transistor M1 is coupled to a first node N1.

[0078] In other words, a scan signal Scan(n) is input into the gate electrode of the first transistor M1, and a data signal Data(t) is input into the first electrode.

[0079] In addition, the gate electrode of the second transistor M2 is coupled to a second node N2, the first electrode of the second transistor M2 is coupled to a first power ELVDD(t), and the second electrode of the second transistor M2 is coupled to the anode electrode of the OLED. Here, the second transistor M2 serves as a driving transistor.

[0080] The first capacitor C1 is coupled between the first node N1 and the first electrode of the second transistor M2, that is, the first power ELVDD(t), and the second capacitor C2 is coupled between the first node N1 and the second node N2.

[0081] Further, the gate electrode of the third transistor M3 is coupled to a control line GC, the first electrode of the third transistor M3 is coupled to the gate electrode of the second transistor M2, and the second electrode of the third transistor M3 is coupled to the anode electrode of the OLED, which is coupled to the second electrode of the second transistor M2.

[0082] Here, a control signal GC(t) is applied to the gate electrode of the third transistor M3, wherein when the third transistor M3 is turned on, the second transistor M2 is diode-connected.

[0083] In addition, the cathode electrode of the organic light emitting diode OLED is coupled to the second power ELVSS(t).

[0084] In the embodiment shown in FIG. 6, all of the first to third transistors M1 to M3 are implemented as

PMOS transistors.

[0085] As described above, the respective pixels 140 according to an embodiment of the present invention are driven in the "simultaneous emission scheme," which includes an initialization period Init, a reset period Reset, a threshold voltage compensation period Vth, a scan/data input period Scan, an emission period Emission, and an emission turn-off period Off for each frame, as shown in FIGS. 7A to 7C.

[0086] Here, the scan signals are input sequentially to the scan lines and the data signals are input sequentially into the pixels corresponding thereto for the scan/data input period Scan, but the signals having voltage values at respective levels (e.g., predetermined levels), that is, the first power ELVDD(t) and/or the second power ELVSS(t), the scan signal Scan(n), the control signal GC(t), and the data signal Data(t), are concurrently applied to all of the pixels 140 that constitute the display unit for periods other than the scan/data input period Scan.

[0087] In other words, the threshold voltage compensation of the driving transistor provided in the respective pixels 140 and the emission operations of the respective pixels are simultaneously (or concurrently) performed in all of the pixels 140 of the display unit for each frame.

[0088] However, in one embodiment of the present invention, the first power ELVDD(t) and/or the second power ELVSS(t) may be provided in the following three schemes as shown in FIGS. 7A to 7C, respectively.

[0089] In the first scheme, referring to FIG. 7A, the first power ELVDD(t) is applied having voltage values at three different levels (for example, 12V, 2V, and -3V), and the second power ELVSS(t) is applied at a fixed low level (for example, 0V), wherein the voltage range of the data signal is between 0V and 6V.

[0090] In other words, in this case, the second power ELVSS driver 180 outputs a voltage value at a constant level GND so that there is no need to be implemented as a separate driving circuit, making it possible to reduce the circuit costs. Here, the first power ELVDD(t) has a negative voltage value (for example, -3V) as one of the three levels so that the circuit constitution of the first power ELVDD driver 170 may be complicated.

[0091] Moreover, when driven in signal waveforms shown in FIG. 7A, the scan signal Scan(n) may be applied at "high level (H), high level (H), high level (H)," "high level (H), low level (L), high level (H)," and "low level (L), low level (L), low level (L)" during the reset period. This will be described in more detail with reference to FIGS. 8B to 8D.

[0092] In the second scheme, referring to FIG. 7B, the first power ELVDD(t) is applied having voltage values at two levels (for example, 12V and 7V), and the second power ELVSS(t) is also applied having voltage values at two levels (for example, 0V and 10V), wherein the voltage range of the data signal is between 0V and 12V.

[0093] In other words, in this case, the driving waveforms may be simplified but both the first power ELVDD driver 170 and the second power driver ELVSS 180

should be provided in order to output the voltage values at different levels.

[0094] In the third scheme, referring to FIG. 7C, the first power ELVDD(t) is applied having a voltage value at a fixed high level (for example, 12V), and the second power ELVSS(t) is applied having voltage values at three different levels (for example, 0V, 10V, and 15V), being opposite to the embodiment of FIG. 7A.

[0095] In other words, in this case, the first power ELVDD driver 170 outputs the voltage value at the always constant level so that there is no need to be implemented as a separate driving circuit, making it possible to reduce the circuit costs. Here, the second power ELVSS(t) has a positive voltage value among the three levels so that the circuit constitution of the second power ELVSS driver 180 may be complicated.

[0096] Hereinafter, the driving in the simultaneous emission scheme according to an embodiment of the present invention will be described in more detail with reference to FIGS. 8A to 8J.

[0097] In FIGS. 8A to 8J, a case where the scan signal Scan(n) is applied at "high level (H), low level (L), high level (H)" during the reset period among the driving schemes of FIG. 7A will be described by way of example.

[0098] FIGS. 8A to 8J are diagrams for explaining the driving of an organic light emitting display according to an embodiment of the present invention.

[0099] For convenience of explanation, although the voltage levels of the input signals are described using concrete numerical values, these are exemplary values for facilitating understanding but are not actual design values.

[0100] Moreover, the embodiment of FIGS. 8A to 8J will be described assuming that the capacitance ratio of the first capacitor C1, the second capacitor C2, and the parasitic capacitor Coled of the organic light emitting diode OLED is 1:1:4.

[0101] First, referring to FIG. 8A, the voltages of the respective nodes N1 and N2 for the respective pixels 140 of the display unit 130, that is, the pixels in FIG. 6, are initialized to be identical with those during the threshold voltage compensation period to be processed later.

[0102] Here, during the initialization period, the first power ELVDD(t) is applied at a middle level (for example, 2V), the scan signal Scan(n) is applied at a low level (for example, -5V), and the control signal GC(t) is applied at a high level (for example, 6V).

[0103] Moreover, the data signal Data(t) applied during the initialization period is an initialization voltage Vsus. In the embodiment of FIGS. 8A to 8J, the data signal Data(t) of 5V is applied by way of example, and it is assumed that the voltage difference across the second capacitor C2 is 5V.

[0104] The assumption that the voltage difference across the second capacitor C2 is 5V will be described further through the explanation on the threshold voltage compensation period (FIGS. 8D to 8F).

[0105] Further, the initialization step is concurrently ap-

plied to the pixels 140 that constitute the display unit 130, wherein the signals applied during the initialization step, that is, the first power ELVDD(t), the scan signal Scan(n), the control signal GC(t), and the data signal Data(t), are applied simultaneously or concurrently to all of the pixels, having the voltage values at respective levels (e.g., predetermined levels).

[0106] According to the application of the signals as described above, the first transistor M1 is turned on, and the second transistor M2 and the third transistor M3 are turned off.

[0107] Therefore, the voltage 5V that is applied as the initialization signal is applied to the first node N1 through the data line, and the voltage 5V is stored in the second capacitor C2 so that the voltage of the second node N2 becomes 0V.

[0108] Next, referring to FIGS. 8B to 8D, this is a period where the data voltages applied to the pixels 140 of the display unit 130, that is, the pixel of FIG. 6, are reset, wherein the voltage of the anode electrode of the organic light emitting diode OLED is dropped below the cathode electrode thereof in order that the organic light emitting diode OLED is not light-emitted.

[0109] In the embodiment of FIGS. 8A to 8J, the reset period is processed by being divided into three steps shown in FIGS. 8B to 8D.

[0110] First, referring to FIG. 8B, during a first reset period, the first power ELVDD(t) is applied at a low level (for example, -3V), the scan signal Scan(n) is applied at a high level (for example, 6V), and the control signal GC(t) is applied at a high level (for example, 6V).

[0111] In other words, as the scan signal Scan(n) is applied at a high level, the first transistor M1, which is a PMOS transistor, is turned off so that the data signal Data(t) is applied having a voltage value at a lower level than the voltage value of the scan signal Scan(n) for the period.

[0112] Moreover, the voltage value at a low level that is applied as the first power ELVDD(t) is a negative voltage below the voltage value (for example, 0V) of the second power ELVSS(t), wherein it will be assumed as -3V in FIG. 8B.

[0113] As described above, if -3V is applied as the first power ELVDD(t), which is lower by 5V than the voltage value of the first power ELVDD(t) provided during the initialization period of FIG. 8A, that is, 2V, such that the voltage of the first node N1 is also lowered by 5V than its voltage (i.e., 5V) during the initialization period due to the coupling effects of the first capacitor C1 and the second capacitor C2 to become 0V, and the voltage of the second node N2 becomes -5V that is lowered by 5V than its voltage (i.e., 0V) during the initialization period.

[0114] However, as mentioned in reference to FIG. 8A, here, the scan signal Scan(n) may be applied at a low level (for example, -5V). In this case, since the first transistor M1 is turned on, the voltage 0V is applied as the data signal Data(t) so that the voltage of the first node N1 becomes 0V.

[0115] In other words, considering the case where the voltages of the first node N1 and the second node N2 cannot be sufficiently lowered by the desired voltage due to the parasitic coupling under design limitation conditions, the scan signal may be applied at a low level as described above and the data signal corresponding thereto may be applied at 0V.

[0116] If the voltage at the second node N2 becomes -5V as described above, the voltage applied to the gate electrode of the second transistor M2 coupled to the second node N2 becomes -5V so that the second transistor M2 that is implemented as a PMOS transistor is turned on.

[0117] Here, as a current path is formed between the first and second electrodes of the second transistor M2, the voltage at the anode electrode of the OLED coupled to the first electrode is gradually dropped to the voltage value of the first power ELVDD(t), that is, -3V.

[0118] Next, referring to FIG. 8C, during a second reset period, the first power ELVDD(t) is applied at a low level (for example, -3V), the scan signal Scan(n) is applied at a low level (for example, -5V), and the control signal GC(t) is applied at a high level (for example, 6V). In this case, the first transistor M1 is turned on so that the voltage 0V is applied as the data signal Data(t).

[0119] In other words, compared with the first reset period, during the second reset period, the scan signal Scan(n) is applied at a low level (for example, -5V) and the data signal Data(t) corresponding thereto is applied with 0V, wherein this is performed in consideration of the case where the voltages of the first node N1 and the second node N2 cannot be sufficiently lowered by the desired voltage due to the parasitic coupling under design limitation conditions.

[0120] Therefore, in another embodiment, the second reset period may maintain the same waveforms as those during the first reset period. In other words, the scan signal Scan(n) applied during the second reset period may be applied at a high level.

[0121] Next, referring to FIG. 8D, during a third reset period, the first power ELVDD(t) is applied at a middle level (for example, 2V), the scan signal Scan(n) is applied at a high level (for example, 6V), and the control signal GC(t) is applied at a high level (for example, 6V).

[0122] In other words, in the case of the third reset period, the first power ELVDD(t) is restored to have the same voltage value as that during the initialization period as described in FIG. 8A so that the voltage value of the first power ELVDD(t) is increased by 5V from that during the second reset period. Therefore, the voltages of the first node N1 and the second node N2 are raised to 5V and 0V, respectively, due to the coupling effects of the first capacitor C1 and the second capacitor C2.

[0123] In other words, the voltages of the respective nodes and the voltage value of the first power ELVDD(t) become the same as those during the initialization period of FIG. 8A.

[0124] However, the voltage of the anode electrode of

the OLED is applied with -3V that is lower than the voltage value (0V) of the cathode electrode of the OLED throughout the first to third reset periods.

[0125] Moreover, in another embodiment, during the third reset period, the scan signal Scan(n) may also be applied at a low level (for example, -5V). However, the data signal Data(t) corresponding to the scan signal Scan(n) should be applied at 5V so that the voltage of the first node N1 can be maintained at 5V.

[0126] The reset steps are concurrently applied to all the pixels of the display unit 130 through FIGS. 8B to 8D as described above. Therefore, the signals applied during the first to third reset steps, that is, the first power ELVDD(t), the scan signal Scan(n), the control signal GC(t), and the data signal Data(t), should be applied to all of the pixels, having the voltage values at levels set during the respective periods.

[0127] Next, referring to FIGS. 8E to 8G, this is a period where the threshold voltage of the driving transistor M2 provided in the respective pixels 140 of the display unit 130 is stored in the capacitor C2. This will serve to remove the defects due to the deviation in the threshold voltage of the driving transistor when data voltage is charged in the respective pixels 140.

[0128] In the embodiment of FIGS. 8E to 8G, the threshold voltage compensation period is processed by being divided into three steps shown in FIGS. 8E to 8G.

[0129] First, referring to FIG. 8E, a first threshold voltage compensation period is a step for storing the threshold voltage of the driving transistor, that is, the second transistor, wherein compared with the previous period of FIG. 8D, it is different in that the scan signal Scan(n) is applied at a low level (-5V). In this case, the first transistor M1 is turned on so that the data signal Data(t) applied to the first electrode of the first transistor is applied at 5V that is the same as the voltage of the first node N1 of the previous period shown in FIG. 8D.

[0130] In another embodiment, in the case of the first threshold voltage compensation period, the scan signal may be applied at a high level, that is, the signal application waveform of FIG. 8D may be maintained as it is, but the first threshold voltage compensation period of FIG. 8E is implemented in order to prevent the risk that the voltages of the respective nodes N1 and N2 are deviated from the set values due to parasitic coupling.

[0131] Next, referring to FIG. 8F, this is a second threshold voltage compensation period, wherein the voltage of the second node N2 is pulled-down.

[0132] To this end, the first power ELVDD(t) and the scan signal Scan(n) are applied at a middle level (2V) and a low level (-5V), respectively, in the same manner as in the previous step, and the control signal GC(t) is applied at a low level (for example, -8V).

[0133] In other words, the third transistor M3 is turned on according to the application of the signals as described above, and as the third transistor M3 is turned on, the gate electrode and the second electrode of the second transistor M2 are electrically coupled so that the transis-

tor M2 is operated as a diode.

[0134] Therefore, the voltage at the second node N2, that is, the voltage applied to the gate electrode of the second transistor M2, is divided by $Coled/(C2+Coled)$ due to the coupling effects of the second capacitor C2 and the parasitic capacitor Coled of the organic light emitting diode OLED.

[0135] Here, in one embodiment, when the capacitance ratio between C2 and Coled is 1:4, the voltage of the second node N2 is dropped from 0V to -2.4V (i.e., $-3V \times 4/5$) that is the voltage of the anode electrode of the OLED.

[0136] In addition, the second node N2 and the anode electrode of the OLED are electrically coupled together as the same node so that the voltage at the anode electrode of the OLED also becomes -2.4V.

[0137] Thereafter, referring to FIG. 8G, this is a third threshold voltage compensation period, wherein the waveforms of the applied signals are the same as those during the second threshold voltage compensation period.

[0138] However, if the voltage at the second node N2 is dropped to -2.4V as described during the second threshold voltage compensation period, the second transistor M2 as the driving transistor is turned on. Since the second transistor M2 serves as the diode, it is turned on so that current flows until the voltage difference between the first power ELVDD(t) and the anode electrode of the OLED corresponds to the magnitude of the threshold voltage of the second transistor M2 and thereafter, it is turned off.

[0139] In other words, for example, the first power ELVDD(t) is applied at 2V and the threshold voltage of the second transistor is -2V so that current flows until the voltage at the anode electrode of the OLED becomes 0V.

[0140] Moreover, there is no potential difference between the second node N2 and the anode electrode of the OLED so that if the voltage at the anode electrode becomes 0V, the voltage at the second node N2 also becomes 0V.

[0141] However, since the threshold voltage V_{th} of the second transistor M2 has the deviation (ΔV_{th}), the actual threshold voltage becomes $-2V + \Delta V_{th}$ so that the voltage of the second node N2 becomes ΔV_{th} .

[0142] Further, the first to third threshold voltage compensation steps are also concurrently applied to all the pixels 140 of the display unit 130. Therefore, the signals applied in the threshold voltage compensation steps, that is, the first power ELVDD(t), the scan signal Scan(n), the control signal GC(t), and the data signal Data(t), are simultaneously (or concurrently) applied to all of the pixels 140, having the voltage values at levels set during the respective periods.

[0143] Next, referring to FIG. 8H, this is a step where the scan signals Scan(n) are applied sequentially to the respective pixels 140 of the display unit 130, the pixels being coupled to the scan lines S1 to Sn, so that the data signals Data(t) supplied to the respective data lines D1

to Dm are applied to the pixels 140.

[0144] In other words, for the scan/data input period Scan of FIG. 8H, the scan signals Scan(n) are input sequentially to the scan lines S1 to Sn, the data signals corresponding thereto are input sequentially to the pixels 140 coupled to the respective scan lines S1 to Sn, and the control signal GC(t) is applied at a high level (for example, 6V) during the period.

[0145] However, in the embodiment of FIG. 8H, the widths of the sequentially applied scan signals are exemplarily applied at two horizontal time 2H, as shown in FIG. 8H. In other words, the width of the (n-1)th scan signals Scan(n-1) and the width of the nth scan signal Scan(n) applied following thereof are applied to be overlapped by 1H. Moreover, as the control signal GC(t) is applied at a high level, the third transistor M3, which is a PMOS transistor, is turned off.

[0146] In the case of the pixel shown in FIG. 8H, if the scan signal Scan(n) at a low level is applied so that the first transistor M1 is turned on, the data signal Data having a voltage value (e.g., a predetermined voltage value) is applied to the first node N1 via the first and second electrodes of the first transistor M1.

[0147] Here, the voltage value of the applied data signal Data is applied in the range of about 1V to about 6V by way of example, and in this case, the voltage 1V is the voltage value representing white, and the voltage 6V is the voltage value representing black.

[0148] Here, assuming that the applied data is 6V, the voltage of the first node N1 is increased from 5V, which is the previous initialization voltage Vsus, by 1V. Therefore, the voltage of the second node N2 is also increased by 1V so that the voltage of the second node N2 becomes Vth+1V.

[0149] This may be represented by the following equation.

[0150] Voltage of second node N2 = $\Delta V_{th} + (V_{data} - V_{sus}) = \Delta V_{th} + (6V - 5V)$.

[0151] However, during the period of FIG. 8H, the voltage 2V is applied to the first power ELVDD(t) so that the second transistor M2 is in a turn-off state. Therefore, a current path is not formed between the OLED and the first power ELVDD(t) so that substantially no current flows to the OLED. In other words, the emission is not performed.

[0152] Next, referring to FIG. 8I, this is a period where current corresponding to the data voltage stored in the respective pixels 140 of the display unit 130 is supplied to the organic light emitting diode OLED provided in the respective pixels 140 so that the emission is performed.

[0153] In other words, during the emission period Emission of FIG. 8I, the first power ELVDD(t) is applied at a high level (for example, 12V), and the scan signal Scan(n) and the control signal GC(t) are applied at a high level (for example, 6V), respectively.

[0154] Therefore, as the scan signal Scan(n) is applied at a high level, the first transistor M1, which is a PMOS transistor, is turned off so that the data signal Data may

be supplied at any levels for the period.

[0155] Moreover, the emission step is also concurrently applied to all of the pixels 140 of the display unit 130 so that the signals applied during the emission step, that is, the first power ELVDD(t), the scan signal Scan(n), the control signal GC(t), and the data signal Data(t), are simultaneously (or concurrently) applied to all of the pixels 140, having the voltage values set at respective levels.

[0156] Further, as the control signal GC(t) is applied at a high level, the third transistor M3, which is a PMOS transistor, is turned off so that the second transistor M2 serves as a driving transistor.

[0157] Therefore, the voltage applied to the gate electrode of the second transistor M2, which is the voltage applied to the second node N2, is $\Delta V_{th} + 1$, and the first power ELVDD(t) applied to the first electrode of the second transistor M2 is applied at a high level (for example, 12V) so that the second transistor M2, which is a PMOS transistor, is turned on.

[0158] As the second transistor M2 is turned on as described above, a current path is formed between the first power ELVDD(t) and the cathode electrode of the OLED. Therefore, the current corresponding to the Vgs voltage value of the second transistor M2, that is, the voltage corresponding to the voltage difference between the gate electrode and the first electrode of the second transistor M2, is applied to the organic light emitting diode OLED so that it is light-emitted at brightness corresponding thereto.

[0159] In other words, the current flowing through the organic light emitting diode OLED is represented by $I_{oled} = \beta/2(V_{gs} - V_{th})^2 = \beta/2(V_{data} - V_{sus})^2$, wherein β represents constant value so that in the above described embodiment of the present invention, the current flowing through the organic light emitting diode OLED compensates for the deviation ΔV_{th} in the threshold voltage of the second transistor M2.

[0160] After the emission is performed on all of the pixels 140 of the display unit 130 as described above, an emission turn-off step Off is performed as shown in FIG. 8J.

[0161] Referring to FIG. 8J, during the emission turn-off period Off, the first power ELVDD(t) is applied at a middle level (for example, 2V), the scan signal Scan(n) is applied at a high level (for example, 6V), and the control signal is applied at a high level (for example, 6V).

[0162] In other words, compared with the emission period of FIG. 8I, it is the same except that the first power ELVDD(t) is changed from the high level to the middle level (for example, 2V).

[0163] This is the period where the emission is turned off for a black insertion or a dimming after the emission operation, wherein if the OLED is formerly light-emitting, the voltage value of the anode electrode of the OLED is dropped in voltage within several tens of micro seconds (us) such that the emission is turned off.

[0164] As described above, one frame is implemented through the periods of FIGS. 8A to 8J, and it is continu-

ously repeated, thereby forming the following frames. In other words, after the emission turn-off period Off of FIG. 8J, the initialization period Init of FIG. 8A is processed again.

[0165] FIG. 9 is a circuit diagram of a pixel of FIG. 1 according to another embodiment of the present invention.

[0166] Referring to FIG. 9, compared with the embodiment of FIG. 6, it is different in that transistors that constitute a pixel circuit are implemented as NMOS transistors.

[0167] In this case, compared with the driving timing diagrams of FIGS. 7A to 7C, the driving waveforms and the polarities of a scan signal Scan(n), a control signal GC(n), first power ELVDD(t), second power ELVSS(t), and a data signal Data(t) supplied other than during a data write period are inverted and supplied.

[0168] Consequently, compared with the embodiment of FIG. 6, in the embodiment of FIG. 9, the transistors are implemented as NMOS transistors and not PMOS transistors, but the driving operations and the principles thereof are the same as the embodiment of FIG. 6, and thus, the detailed description thereof will be omitted.

[0169] Referring to FIG. 9, the pixel 240 in the embodiment of the present invention includes an OLED and a pixel circuit 242 that supplies current to the OLED.

[0170] The cathode electrode of the OLED is coupled to the pixel circuit 242, and the anode electrode thereof is coupled to the first power supply ELVDD(t). The OLED generates light having a brightness (e.g., a predetermined brightness) corresponding to the current supplied by the pixel circuit 242.

[0171] However, in the embodiment of FIG. 9, the pixels 240 that constitute the display unit 130 receive data signals supplied to the data lines D1 to Dm when scan signals are supplied sequentially to the scan lines S1 to Sn for a partial period (the aforementioned (d) step) of one frame, but the scan signals applied to the respective scan signals S1 to Sn, the first power ELVDD(t) and/or the second power ELVSS(t) applied to the respective pixels 240, control signals applied to respective control lines GC1 to GCn are simultaneously (or concurrently) applied to the pixels 240, having respective voltage levels (e.g., predetermined voltage levels), for other periods ((a), (b), (c), (e), and (f) steps) of one frame.

[0172] In the embodiment of FIG. 9, the pixel circuit 242 that is provided in the respective pixels 240 includes three transistors NM1 to NM3 and two capacitors C1 and C2.

[0173] Herein, the gate electrode of the first transistor NM1 is coupled to a scan line S and the first electrode of the first transistor NM1 is coupled to a data line D. And, the second electrode of the first transistor NM1 is coupled to a first node N1.

[0174] In other words, the scan signal Scan(n) is applied to the gate electrode of the first transistor NM1, and the data signal Data(t) is input into the first electrode of the first transistor NM1.

[0175] The gate electrode of the second transistor NM2 is coupled to a second node N2, the first electrode of the second transistor NM2 is coupled to the second power supply ELVSS(t), and the second electrode thereof is coupled to the cathode electrode of the organic light emitting diode OLED. Here, the second transistor NM2 serves as a driving transistor.

[0176] Further, the first capacitor C1 is coupled between the first node N1 and the first electrode of the second transistor NM2, that is, the second power supply ELVSS(t), and the second capacitor C2 is coupled between the first node N1 and the second node N2.

[0177] In addition, the gate electrode of the third transistor NM3 is coupled to a control line GC, the first electrode of the third transistor NM3 is coupled to the gate electrode of the second transistor NM2, and the second electrode of the third transistor NM3 is coupled to the cathode electrode of the OLED, which is coupled to the second electrode of the second transistor NM2.

[0178] Therefore, the control signal GC(t) is applied to the gate electrode of the third transistor NM3, wherein when the third transistor NM3 is turned on, the second transistor NM2 is diode-connected.

[0179] In addition, the anode electrode of the organic light emitting diode OLED is coupled to the first power supply ELVDD(t).

[0180] In the embodiment of FIG. 9, all of the first to third transistors NM1 to NM3 are implemented as NMOS transistors.

[0181] While the present invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

Claims

1. An organic light emitting display comprising:

a display unit (130) comprising a plurality of pixels (140, 240), each pixel being coupled to a respective one of a plurality of scan lines (S1, S2, S3, Sn), a respective one of a plurality of control lines (GC1, GC2, GC3, GCn), and a respective one of a plurality of data lines (D1, D2, Dm);

a control line driver (160) for providing control signals to the pixels (140, 240) through the control lines (GC1, GC2, GC3, GCn);

a first power driver (170) for applying a first power (ELVDD) to the pixels (140, 240) and a second power driver (180) for applying a second power (ELVSS) to the pixels (140, 240);

wherein the first power driver (170) and/or the second power driver (180) are adapted to apply voltage values at different levels to the pixels

(140, 240) during periods of one frame;
 wherein control line driver (160) is adapted to
 concurrently provide control signals to all of the
 pixels (140, 240) and the first power driver (170)
 and the second power driver (180) are adapted
 to concurrently provide the first and second power
 (ELVDD; ELVSS) to all of the pixels (140,
 240);
 wherein the pixels (140, 240) fulfill one of the
 following configurations (i) and (ii):

(i) wherein each of the pixels (140) comprises:

a first transistor (M1) having a gate
 electrode coupled to a scan line (S) of
 the scan lines (S1, S2, S3, Sn), a first
 electrode coupled to a data line (D) of
 the data lines (D1, D2, Dm), and a second
 electrode coupled to a first node
 (N1);
 a second transistor (M2) having a gate
 electrode coupled to a second node
 (N2), a first electrode coupled to the first
 power (ELVDD), and a second electrode;
 a first capacitor (C1) coupled between
 the first node (N1) and the first electrode
 of the second transistor (M2);
 a second capacitor (C2) coupled between
 the first node (N1) and the second
 node (N2);
 a third transistor (M3) having a gate
 electrode coupled to a control line (GC)
 of the control lines (GC1, GC2, GC3,
 GCn), a first electrode coupled to the
 gate electrode of the second transistor
 (M2), and a second electrode coupled
 to the second electrode of the second
 transistor (M2); and
 an organic light emitting diode (OLED)
 having an anode electrode coupled to
 the second electrode of the second
 transistor (M2) and a cathode electrode
 coupled to the second power (ELVSS),
 wherein the first to third transistors (M1,
 M2, M3) are PMOS transistors;

(ii) wherein each of the pixels (240) comprises:

a first transistor (NM1) having a gate
 electrode coupled to a scan line (S) of
 the scan lines (S1, S2, S3, Sn), a first
 electrode coupled to a data line (D) of
 the data lines (D1, D2, Dm), and a second
 electrode coupled to a first node
 (N1);

a second transistor (NM2) having a
 gate electrode coupled to a second
 node (N2), a first electrode coupled to
 a second power (ELVSS), and a second
 electrode;
 a first capacitor (C1) coupled between
 the first node (N1) and the first electrode
 of the second transistor (NM2);
 a second capacitor (C2) coupled between
 the first node (N1) and the second
 node (N2);
 a third transistor (NM3) having a gate
 electrode coupled to a control line (GC)
 of the control lines (GC1, GC2, GC3,
 GCn), a first electrode coupled to the
 gate electrode of the second transistor
 (NM2), and a second electrode coupled
 to the second electrode of the second
 transistor (NM2); and
 an organic light emitting diode (OLED)
 having a cathode electrode coupled to
 the second electrode of the second
 transistor (NM2) and an anode electrode
 coupled to the first power
 (ELVDD),
 wherein the first to third transistors
 (NM1, NM2, NM3) are NMOS transistors,

and

wherein one and only one of conditions (i) to (iii)
 is fulfilled:

(i) the first power driver (170) is adapted to
 apply the first power (ELVDD) having voltage
 values at three different levels during
 the periods of one frame, and the second
 power driver (ELVSS) is adapted to apply
 the second power (ELVSS) having a voltage
 value at a fixed level during all of the
 periods of one frame;

(ii) the first power driver (170) is adapted to
 apply the first power (ELVDD) having a voltage
 value at a fixed level for all of the periods
 of one frame, and the second power driver
 (180) is adapted to apply the second power
 (ELVSS) having voltage values at three different
 levels during the periods of one
 frame; or

(iii) the first power driver (170) and the second
 power driver (180) are adapted to respectively
 apply the first and second powers
 (ELVDD, ELVSS) each having voltage values
 at two different levels during the periods
 of one frame.

2. A driving method of an organic light emitting display
 according to claim 1, the method comprising:

- (a) initializing voltages of respective nodes of a plurality of pixel circuits (142, 242) included in respective pixels (140, 240) by concurrently applying a first power (ELVDD), a second power (ELVSS), scan signals, control signals, and data signals, having voltage values at respective levels, to all of the pixels (140, 240) in a display unit (130);
- (b) decreasing a voltage of an anode electrode of an organic light emitting diode (OLED) included in the respective pixels (140, 240) below a voltage of a cathode electrode of the organic light emitting diode (OLED) by concurrently applying the first power (ELVDD), the second power (ELVSS), the scan signals, the control signals, and the data signals, having the voltage values at respective levels, to all of the pixels (140, 240);
- (c) storing a threshold voltage of a driving transistor (M2, NM2) included in the respective pixels (140, 240) by concurrently applying the first power (ELVDD), the second power (ELVSS), the scan signals, the control signals, and the data signals, having the voltage values at respective levels, to all of the pixels (140, 240);
- (d) applying the scan signals sequentially to the pixels (140, 240) coupled to scan lines (S1, S2, S3, Sn) of the display unit (130) and applying the data signals to the pixels (140, 240) through the data lines (D1, D2, Dm) corresponding to the sequentially applied scan signals;
- (e) controlling all of the pixels (140, 240) to concurrently emit light at a brightness corresponding to the data signals stored in the respective pixels (140, 240) by concurrently applying the first power (ELVDD), the second power (ELVSS), the scan signals, the control signals, and the data signals, having the voltage values at respective levels, to all of the pixels (140, 240); and
- (f) turning off emission of the pixels (140, 240) by concurrently applying the first power (ELVDD), the second power (ELVSS), the scan signals, the control signals, and the data signals, having the voltage values at respective levels, to all of the pixels (140, 240) and thus lowering the voltage of the anode electrode of the organic light emitting diode (OLED) included in the respective pixels (140, 240).
3. The driving method of claim 2, wherein each of the pixels (140) comprises:
- a first PMOS transistor (M1) having a gate electrode coupled to a scan line (S) of the scan lines (S1, S2, S3, Sn), a first electrode coupled to a data line (D), and a second electrode coupled to a first node (N1);
- a second PMOS transistor (M2) having a gate electrode coupled to a second node (N2), a first electrode coupled to the first power (ELVDD), and a second electrode;
- a first capacitor (C1) coupled between the first node (N1) and the first electrode of the second transistor (M2);
- a second capacitor (C2) coupled between the first node (N1) and the second node (N2);,
- a third PMOS transistor (M3) having a gate electrode coupled to a control line (GC), a first electrode coupled to the gate electrode of the second transistor (M2), and a second electrode coupled to the second electrode of the second transistor (M2); and
- an organic light emitting diode (OLED) having an anode electrode coupled to the second electrode of the second transistor (M2) and a cathode electrode coupled to the second power (ELVSS).
4. The driving method as claimed in claim 3, wherein in (a), the first power (ELVDD) is applied at a middle level, the scan signals are applied at a low level, and the control signals are applied at a high level, and/or wherein (b) comprises:
- (b1) wherein the first power (ELVDD) is applied at a low level, the scan signal is applied at a high level or a low level, and the control signals are applied at a high level;
- (b2) wherein the first power (ELVDD) is applied at a low level, the scan signals are applied at a high level or a low level, and the control signals are applied at a high level;
- (b3) wherein the first power (ELVDD) is applied at a middle level, the scan signals are applied at a high level or a low level, and the control signals are applied at a high level.
5. The driving method as claimed in claim 4, wherein in (b1) and (b2), if the scan signals are applied at a low level, the data signals corresponding thereto are applied at a low level, and/or wherein in (b3), if the scan signals are applied at a low level, the data signals corresponding thereto are applied at a high level.
6. The driving method as claimed in one of claims 3-5, wherein (c) comprises:
- (c1) wherein the first power (ELVDD) is applied at a middle level, the scan signals are applied at a high level or a low level, and the control signals are applied at a high level; and
- (c2) and (c3) wherein the first power (ELVDD) is applied at a middle level, the scan signals are

applied at a low level, and the control signals are applied at a low level.

7. The driving method of the organic light emitting display as claimed in claim 6, wherein in (c1), if the scan signals are applied at a low level, the data signals corresponding thereto are applied at a high level. 5
8. The driving method as claimed in one of claims 3-7, wherein in (d), the control signals are applied at a low level, and/or widths of the sequentially applied scan signals are applied during two horizontal periods, adjacently applied ones of the scan signals being applied to be overlapped with each other by one horizontal period. 10 15
9. The driving method as claimed in one of claims 3-8, wherein in (e), the first power (ELVDD) is applied at a high level, and the scan signals and the control signals are applied at a high level, and/or wherein in (f), the first power (ELVDD) is applied at a middle level, and the scan signal and the control signal are applied at a high level. 20 25

Patentansprüche

1. Organische lichtemittierende Anzeige, aufweisend:
 - eine Anzeigeeinheit (130), die eine Vielzahl von Pixeln (140, 240) aufweist, wobei jeder Pixel mit einer jeweiligen Ansteuerleitung aus einer Vielzahl von Ansteuerleitungen (S1, S2, S3, Sn), einer jeweiligen Steuerleitung aus einer Vielzahl von Steuerleitungen (GC1, GC2, GC3, GCn) und einer jeweiligen Datenleitung aus einer Vielzahl von Datenleitungen (D1, D2, Dm) gekoppelt ist; 30 35
 - einen Steuerleitungstreiber (160) zum Liefern von Steuersignalen zu den Pixeln (140, 240) über die Steuerleitungen (GC1, GC2, GC3, GCn); 40
 - einen ersten Spannungsquellentreiber (170) zum Anlegen einer ersten Spannungsquelle (ELVDD) an die Pixel (140, 240) und einen zweiten Spannungsquellentreiber (180) zum Anlegen einer zweiten Spannungsquelle (ELVSS) an die Pixel (140, 240); 45
 - wobei der erste Spannungsquellentreiber (170) und/oder der zweite Spannungsquellentreiber (180) ausgebildet sind, während Perioden eines Frame Spannungswerte mit verschiedenen Pegeln an die Pixel (140, 240) anzulegen; 50
 - wobei der Steuerleitungstreiber (160) ausgebildet ist, gleichzeitig Steuersignal zu allen der Pixel (140, 240) zu liefern, und wobei der erste Spannungsquellentreiber (170) und der zweite Spannungsquellentreiber (180) ausgebildet 55

sind, gleichzeitig alle der Pixel (140), 240) mit der ersten und zweiten Spannungsquelle (ELVDD; ELVSS) zu versorgen; wobei die Pixel (140, 240) einer der folgenden Konfigurationen (i) und (ii) genügen:

(i) wobei jeder der Pixel (140) aufweist:

einen ersten Transistor (M1), der eine Gate-Elektrode, die an eine Ansteuerleitung (S) der Ansteuerleitungen (S1, S2, S3, Sn) gekoppelt ist, eine erste Elektrode, die an eine Datenleitung (D) der Datenleitungen (D1, D2, Dm) gekoppelt ist, und eine zweite Elektrode, die an einen ersten Knoten (N1) gekoppelt ist, aufweist;
 einen zweiten Transistor (M2), der eine Gate-Elektrode, die mit einem zweiten Knoten (N2) gekoppelt ist, eine erste Elektrode, die mit der ersten Spannungsquelle (ELVDD) gekoppelt ist, und eine zweite Elektrode aufweist;
 einen ersten Kondensator (C1), der zwischen den ersten Knoten (N1) und die erste Elektrode des zweiten Transistors (M2) gekoppelt ist;
 einen zweiten Kondensator (C2), der zwischen den ersten Knoten (N1) und den zweiten Knoten (N2) gekoppelt ist;
 einen dritten Transistor (M3), der eine Gate-Elektrode, die mit einer Steuerleitung (GC) der Steuerleitungen (GC1, GC2, GC3, GCn) gekoppelt ist, eine erste Elektrode, die mit der Gate-Elektrode des zweiten Transistors (M2) gekoppelt ist, und eine zweite Elektrode, die mit der zweiten Elektrode des zweiten Transistors (M2) gekoppelt ist, aufweist; und
 eine organische lichtemittierende Diode (OLED), die eine Anodenelektrode, die mit der zweiten Elektrode des zweiten Transistors (M2) gekoppelt ist, und eine Kathodenelektrode, die mit der zweiten Spannungsquelle (ELVSS) gekoppelt ist, aufweist,
 wobei der erste bis dritte Transistor (M1, M2, M3) PMOS-Transistoren sind;

(ii) wobei jeder der Pixel (240) aufweist:

einen ersten Transistor (NM1), der eine Gate-Elektrode, die mit einer Ansteuerleitung (S) der Ansteuerleitungen (S1, S2, S3, Sn) gekoppelt ist, eine erste Elektrode, die mit einer Datenleitung

(D) der Datenleitungen (D1, D2, Dm) gekoppelt ist, und eine zweite Elektrode, die mit einem ersten Knoten (N1) gekoppelt ist, aufweist;
 einen zweiten Transistor (NM2), der eine Gate-Elektrode, die mit einem zweiten Knoten (N2) gekoppelt ist, eine erste Elektrode, die mit einer zweiten Spannungsquelle (ELVSS) gekoppelt ist, und
 eine zweite Elektrode aufweist;
 einen ersten Kondensator (C1), der zwischen den ersten Knoten (N1) und die erste Elektrode des zweiten Transistors (NM2) gekoppelt ist;
 einen zweiten Kondensator (C2), der zwischen den ersten Knoten (N1) und den zweiten Knoten (N2) gekoppelt ist;
 einen dritten Transistor (NM3), der eine Gate-Elektrode, die mit einer Steuerleitung (GC) der Steuerleitungen (GC1, GC2, GC3, GCn) gekoppelt ist, eine erste Elektrode, die mit der Gate-Elektrode des zweiten Transistors (NM2) gekoppelt ist, und eine zweite Elektrode, die mit der zweiten Elektrode des zweiten Transistors (NM2) gekoppelt ist, aufweist; und
 eine organische lichtemittierende Diode (OLED), die eine Kathodenelektrode, die mit der zweiten Elektrode des zweiten Transistors (NM2) gekoppelt ist, und eine Anodenelektrode, die mit der ersten Spannung (ELVDD) gekoppelt ist, aufweist,
 wobei der erste bis dritte Transistor (NM1, NM2, NM3) NMOS-Transistoren sind,

und
 wobei eine und nur eine einzige der Bedingungen (i) bis (iii) erfüllt ist:

- (i) der erste Spannungsquellentreiber (170) ist ausgebildet, während der Perioden eines Frame die erste Spannungsquelle (ELVDD) anzulegen, die Spannungswerte mit drei verschiedenen Pegeln aufweist, und der zweite Spannungsquellentreiber (ELVSS) ist ausgebildet, während aller Perioden eines Frame die zweite Spannungsquelle (ELVSS) anzulegen, die einen Spannungswert mit einem festgesetzten Pegel aufweist;
- (ii) der erste Spannungsquellentreiber (170) ist ausgebildet, während aller Perioden eines Frame die erste Spannungs-

quelle (ELVDD) anzulegen, die einen Spannungswert mit einem festgesetzten Pegel aufweist, und der zweite Spannungsquellentreiber (180) ist ausgebildet, während der Perioden eines Frame die zweite Spannungsquelle (ELVSS) anzulegen, die Spannungswerte mit drei verschiedenen Pegeln aufweist; oder
 (iii) der erste Spannungsquellentreiber (170) und der zweite Spannungsquellentreiber (180) sind ausgebildet, während der Perioden eines Frame jeweils die erste und zweite Spannungsquelle (ELVDD, ELVSS) anzulegen, die jeweils Spannungswerte mit zwei verschiedenen Pegeln aufweisen.

2. Verfahren zur Ansteuerung einer organischen lichtemittierenden Anzeige nach Anspruch 1, wobei das Verfahren aufweist:

- (a) Initialisieren von Spannungen jeweiliger Knoten einer Vielzahl von Pixelschaltungen (142, 242), die in jeweiligen Pixeln (140, 240) enthalten sind, durch gleichzeitiges Anlegen einer ersten Spannungsquelle (ELVDD), einer zweiten Spannungsquelle (ELVSS), von Ansteuersignalen, Steuersignalen und Datensignalen, die Spannungswerte mit jeweiligen Pegeln aufweisen, an alle Pixel (140, 240) in einer Anzeigeeinheit (130);
- (b) Verringern einer Spannung einer Anodenelektrode einer organischen lichtemittierenden Diode (OLED), die in den jeweiligen Pixeln (140, 240) enthalten ist, unter eine Spannung einer Kathodenelektrode der organischen lichtemittierenden Diode (OLED) durch gleichzeitiges Anlegen der ersten Spannungsquelle (ELVDD), der zweiten Spannungsquelle (ELVSS), der Ansteuersignale, der Steuersignale und der Datensignale, die die Spannungswerte mit jeweiligen Pegeln aufweisen, an alle der Pixel (140, 240);
- (c) Speichern einer Schwellenspannung eines Ansteuertransistors (M2, NM2), der in den jeweiligen Pixeln (140, 240) enthalten ist, durch gleichzeitiges Anlegen der ersten Spannungsquelle (ELVDD), der zweiten Spannungsquelle (ELVSS), der Ansteuersignale, der Steuersignale und der Datensignale, die die Spannungswerte mit jeweiligen Pegeln aufweisen, an alle der Pixel (140, 240);
- (d) nacheinander erfolgendes Anlegen der Ansteuersignale an die Pixel (140, 240), die mit Ansteuerleitungen (S1, S2, S3, Sn) der Anzeigeeinheit (130) gekoppelt sind, und Anlegen der Datensignale an die Pixel (140, 240) über die Datenleitungen (D1, D2, Dm) entsprechend den nacheinander angelegten Ansteuersignalen;
- (e) Steuern von allen der Pixel (140, 240) zur

gleichzeitigen Emission von Licht mit einer Helligkeit, die den in den jeweiligen Pixeln (140, 240) gespeicherten Datensignalen entspricht, durch gleichzeitiges Anlegen der ersten Spannungsquelle (ELVDD), der zweiten Spannungsquelle (ELVSS), der Ansteuersignale, der Steuersignale und der Datensignale, die die Spannungswerte mit jeweiligen Pegeln aufweisen, an alle der Pixel (140, 240); und
 (f) Abschalten der Emission der Pixel (140, 240) durch gleichzeitiges Anlegen der ersten Spannungsquelle (ELVDD), der zweiten Spannungsquelle (ELVSS), der Ansteuersignale, der Steuersignale und der Datensignale, die die Spannungswerte mit jeweiligen Pegeln aufweisen, an alle der Pixel (140, 240) und dadurch bewirktes Senken der Spannung der Anodenelektrode der organischen lichtemittierenden Diode (OLED), die in den jeweiligen Pixeln (140, 240) enthalten ist.

3. Ansteuerverfahren nach Anspruch 2, wobei jeder der Pixel (140) aufweist:

einen ersten PMOS-Transistor (M1), der eine Gate-Elektrode, die mit einer Ansteuerleitung (S) der Ansteuerleitungen (S1, S2, S3, Sn) gekoppelt ist, eine erste Elektrode, die mit einer Datenleitung (D) gekoppelt ist, und eine zweite Elektrode, die mit einem ersten Knoten (N1) gekoppelt ist, aufweist;
 einen zweiten PMOS-Transistor (M2), der eine Gate-Elektrode, die mit einem zweiten Knoten (N2) gekoppelt ist, eine erste Elektrode, die mit der ersten Spannungsquelle (ELVDD) gekoppelt ist, und eine zweite Elektrode aufweist;
 einen ersten Kondensator (C1), der zwischen den ersten Knoten (N1) und die erste Elektrode des zweiten Transistors (M2) gekoppelt ist;
 einen zweiten Kondensator (C2), der zwischen den ersten Knoten (N1) und den zweiten Knoten (N2) gekoppelt ist;
 einen dritten PMOS-Transistor (M3), der eine Gate-Elektrode, die mit einer Steuerleitung (GC) gekoppelt ist, eine erste Elektrode, die mit der Gate-Elektrode des zweiten Transistors (M2) gekoppelt ist, und eine zweite Elektrode, die mit der zweiten Elektrode des zweiten Transistors (M2) gekoppelt ist, aufweist; und
 eine organische lichtemittierende Diode (OLED), die eine Anodenelektrode, die mit der zweiten Elektrode des zweiten Transistors (M2) gekoppelt ist, und eine Kathodenelektrode, die mit der zweiten Spannungsquelle (ELVSS) gekoppelt ist, aufweist.

4. Ansteuerverfahren nach Anspruch 3, wobei gemäß (a) die erste Spannungsquelle

(ELVDD) mit einem mittleren Pegel angelegt wird, die Ansteuersignale mit einem niedrigen Pegel angelegt werden und die Steuersignale mit einem hohen Pegel angelegt werden, und/oder wobei (b) aufweist:

(b1), wobei die erste Spannungsquelle (ELVDD) mit einem niedrigen Pegel angelegt wird, das Ansteuersignal mit einem hohen Pegel oder einem niedrigen Pegel angelegt wird, und die Steuersignale mit einem hohen Pegel angelegt werden;
 (b2), wobei die erste Spannungsquelle (ELVDD) mit einem niedrigen Pegel angelegt wird, die Ansteuersignale mit einem hohen Pegel oder einem niedrigen Pegel angelegt werden und die Steuersignale mit einem hohen Pegel angelegt werden;
 (b3), wobei die erste Spannungsquelle (ELVDD) mit einem mittleren Pegel angelegt wird, die Ansteuersignale mit einem hohen Pegel oder einem niedrigen Pegel angelegt werden, und die Steuersignale mit einem hohen Pegel angelegt werden.

5. Ansteuerverfahren nach Anspruch 4, wobei gemäß (b1) und (b2), wenn die Ansteuersignale mit einem niedrigen Pegel angelegt werden, die ihnen entsprechenden Datensignale mit einem niedrigen Pegel angelegt werden, und/oder wobei gemäß (b), wenn die Ansteuersignale mit einem niedrigen Pegel angelegt werden, die ihnen entsprechenden Datensignale mit einem hohen Pegel angelegt werden.

6. Ansteuerverfahren nach einem der Ansprüche 3-5, wobei (c) aufweist:

(c1), wobei die erste Spannungsquelle (ELVDD) mit einem mittleren Pegel angelegt wird, die Ansteuersignale mit einem hohen Pegel oder einem niedrigen Pegel angelegt werden, und die Steuersignale mit einem hohen Pegel angelegt werden; und
 (c2) und (c3), wobei die erste Spannungsquelle (ELVDD) mit einem mittleren Pegel angelegt wird, die Ansteuersignale mit einem niedrigen Pegel angelegt werden, und die Steuersignale mit einem niedrigen Pegel angelegt werden.

7. Verfahren zur Ansteuerung der organischen lichtemittierenden Anzeige nach Anspruch 6, wobei gemäß (c1), wenn die Ansteuersignale mit einem niedrigen Pegel angelegt werden, die ihnen entsprechenden Datensignale mit einem hohen Pegel angelegt werden.

8. Ansteuerverfahren nach einem der Ansprüche 3-7, wobei gemäß (d) die Steuersignale mit einem nied-

rigen Pegel angelegt werden und/oder Breiten der nacheinander angelegten Ansteuersignale während zwei horizontaler Perioden angelegt werden, wobei benachbart angelegte Ansteuersignale der Ansteuersignale derart angelegt werden, dass sie miteinander um eine horizontale Periode überlappen.

9. Ansteuerverfahren nach einem der Ansprüche 3-8, wobei gemäß (e) die erste Spannungsquelle (ELVDD) mit einem hohen Pegel angelegt wird und die Ansteuersignale und die Steuersignale mit einem hohen Pegel angelegt werden, und/oder wobei gemäß (f) die erste Spannungsquelle (ELVDD) mit einem mittleren Pegel angelegt wird und das Ansteuersignal und das Steuersignal mit einem hohen Pegel angelegt werden.

Revendications

1. Afficheur électroluminescent organique, comprenant :

une unité d'affichage (130) comprenant une pluralité de pixels (140, 240), chaque pixel étant relié à l'une, respective d'une pluralité de lignes de balayage (S1, S2, S3, Sn), à l'une respective d'une pluralité de lignes de commande (GC1, GC2, GC3, GCn), et à l'une respective d'une pluralité de lignes de données (D1, D2, Dm) ;
un circuit d'attaque de ligne de commande (160) destiné à fournir des signaux de commande aux pixels (140, 240) par l'intermédiaire des lignes de commande (GC1, GC2, GC3, GCn) ;
un premier circuit d'attaque d'alimentation (170) destiné à appliquer une première alimentation (ELVDD) aux pixels (140, 240) et un deuxième circuit d'attaque d'alimentation (180) destiné à appliquer une deuxième alimentation (ELVSS) aux pixels (140, 240) ;
dans lequel le premier circuit d'attaque d'alimentation (170) et/ou le deuxième circuit d'attaque d'alimentation (180) sont aptes à appliquer des valeurs de tension se situant à des niveaux différents aux pixels (140, 240) pendant des périodes d'une trame ;
dans lequel le circuit d'attaque de ligne de commande (160) est apte à fournir simultanément des signaux de commande à tous les pixels (140, 240) et le premier circuit d'attaque d'alimentation (170) et le deuxième circuit d'attaque d'alimentation (180) sont aptes à fournir simultanément les première et deuxième alimentations (ELVDD ; ELVSS) à tous les pixels (140, 240) ;
dans lequel les pixels (140, 240) présentent l'une des configurations (i) et (ii) suivantes :

(i) chacun des pixels (140) comprend :

un premier transistor (M1) ayant une électrode de grille reliée à une ligne de balayage (S) parmi les lignes de balayage (S1, S2, S3, Sn), une première électrode reliée à une ligne de données (D) parmi les lignes de données (D1, D2, Dm), et une deuxième électrode reliée à un premier noeud (N1) ;
un deuxième transistor (M2) ayant une électrode de grille reliée à un deuxième noeud (N2), une première électrode reliée à la première alimentation (ELVDD) et une deuxième électrode ;
un premier condensateur (C1) relié entre le premier noeud (N1) et la première électrode du deuxième transistor (M2) ;
un deuxième condensateur (C2) relié entre le premier noeud (N1) et le deuxième noeud (N2) ;
un troisième transistor (M3) ayant une électrode de grille reliée à une ligne de commande (GC) parmi les lignes de commande (GC1, GC2, GC3, GCn), une première électrode reliée à l'électrode de grille du deuxième transistor (M2) et une deuxième électrode reliée à la deuxième électrode du deuxième transistor (M2) ; et
une diode électroluminescente organique (OLED) ayant une électrode d'anode reliée à la deuxième électrode du deuxième transistor (M2) et une électrode de cathode reliée à la deuxième alimentation (ELVSS),
dans lequel les premier à troisième transistors (M1, M2, M3) sont des transistors PMOS ;

(ii) chacun des pixels (240) comprend :

un premier transistor (NM1) ayant une électrode de grille reliée à une ligne de balayage (S) parmi les lignes de balayage (S1, S2, S3, Sn), une première électrode reliée à une ligne de données (D) parmi les lignes de données (D1, D2, Dm), et une deuxième électrode reliée à un premier noeud (N1) ;
un deuxième transistor (NM2) ayant une électrode de grille reliée à un deuxième noeud (N2), une première électrode reliée à une deuxième alimentation (ELVSS) et une deuxième électrode ;
un premier condensateur (C1) relié entre le premier noeud (N1) et la première électrode du deuxième transistor (NM2) ;
un deuxième condensateur (C2) relié entre le premier noeud (N1) et le deuxième noeud (N2) ;
un troisième transistor (NM3) ayant une électrode de grille reliée à une ligne de commande (GC) parmi les lignes de commande (GC1, GC2, GC3, GCn), une première électrode reliée à l'électrode de grille du deuxième transistor (NM2) et une deuxième électrode reliée à la

deuxième électrode du deuxième transistor (NM2) ; et
 une diode électroluminescente organique (OLED) ayant une électrode de cathode reliée à la deuxième électrode du deuxième transistor (NM2) et une électrode d'anode reliée à la première alimentation (ELVDD),
 dans lequel les premier à troisième transistors (NM1, NM2, NM3) sont des transistors NMOS, et
 dans lequel une et une seule des conditions (i) à (iii) est satisfaite :

- (i) le premier circuit d'attaque d'alimentation (170) est apte à appliquer la première alimentation (ELVDD) ayant des valeurs de tension se situant à trois niveaux différents pendant les périodes d'une trame, et le deuxième circuit d'attaque d'alimentation (ELVSS) est apte à appliquer la deuxième alimentation (ELVSS) ayant une valeur de tension se situant à un niveau fixe pendant la totalité des périodes d'une trame ;
- (ii) le premier circuit d'attaque d'alimentation (170) est apte à appliquer la première alimentation (ELVDD) ayant une valeur de tension se situant à un niveau fixe pendant la totalité des périodes d'une trame, et le deuxième circuit d'attaque d'alimentation (180) est apte à appliquer la deuxième alimentation (ELVSS) ayant des valeurs de tension se situant à trois niveaux différents pendant les périodes d'une trame ; ou
- (iii) le premier circuit d'attaque d'alimentation (170) et le deuxième circuit d'attaque d'alimentation (180) sont aptes à appliquer respectivement les première et seconde alimentations (ELVDD, ELVSS) ayant chacune des valeurs de tension se situant à deux niveaux différents pendant les périodes d'une trame.

2. Procédé d'attaque d'un afficheur électroluminescent organique selon la revendication 1, le procédé consistant à :

- (a) initialiser des tensions de noeuds respectifs d'une pluralité de circuits de pixels (142, 242) inclus dans des pixels respectifs (140, 240) en appliquant simultanément une première alimentation (ELVDD), une deuxième alimentation (ELVSS), des signaux de balayage, des signaux de commande et des signaux de données ayant des valeurs de tension se situant à des niveaux respectifs, à tous les pixels (140, 240) d'une unité d'affichage (130) ;
- (b) faire décroître une tension d'une électrode d'anode d'une diode électroluminescente orga-

nique (OLED) incluse dans les pixels respectifs (140, 240) en dessous d'une tension d'une électrode de cathode de la diode électroluminescente organique (OLED) en appliquant simultanément la première alimentation (ELVDD), la deuxième alimentation (ELVSS), les signaux de balayage, les signaux de commande et les signaux de données, ayant les valeurs de tension se situant à des niveaux respectifs, à tous les pixels (140, 240) ;

(c) stocker une tension de seuil d'un transistor d'attaque (M2, NM2) inclus dans les pixels respectifs (140, 240) en appliquant simultanément la première alimentation (ELVDD), la deuxième alimentation (ELVSS), les signaux de balayage, les signaux de commande et les signaux de données, ayant les valeurs de tension se situant à des niveaux respectifs, à tous les pixels (140, 240) ;

(d) appliquer séquentiellement les signaux de balayage aux pixels (140, 240) reliés à des lignes de balayage (S1, S2, S3, Sn) de l'unité d'affichage (130) et appliquer les signaux de données aux pixels (140, 240) par l'intermédiaire des lignes de données (D1, D2, Dn) correspondant aux signaux de balayage appliqués séquentiellement,

(e) commander tous les pixels (140, 240) afin qu'ils émettent simultanément de la lumière ayant une luminosité correspondant aux signaux de données stockés dans les pixels respectifs (140, 240) en appliquant simultanément la première alimentation (ELVDD), la deuxième alimentation (ELVSS), les signaux de balayage, les signaux de commande et les signaux de données, ayant les valeurs de tension se situant à des niveaux respectifs, à tous les pixels (140, 240) ; et

(f) désactiver l'émission des pixels (140, 240) en appliquant simultanément la première alimentation (ELVDD), la deuxième alimentation (ELVSS), les signaux de balayage, les signaux de commande et les signaux de données, ayant les valeurs de tension se situant à des niveaux respectifs, à tous les pixels (140, 240) et en abaissant ainsi la tension de l'électrode d'anode de la diode électroluminescente organique (OLED) incluse dans les pixels respectifs (140, 240).

3. Procédé d'attaque selon la revendication 2, dans lequel chacun des pixels (140) comprend :

un premier transistor PMOS (M1) ayant une électrode de grille reliée à une ligne de balayage (S) parmi les lignes de balayage (S1, S2, S3, Sn), une première électrode reliée à une ligne de données (D), et une deuxième électrode re-

- liée à un premier noeud (N1) ;
 un deuxième transistor PMOS (M2) ayant une électrode de grille reliée à un deuxième noeud (N2), une première électrode reliée à une première alimentation (ELVDD) et une deuxième électrode ;
 un premier condensateur (C1) relié entre le premier noeud (N1) et la première électrode du deuxième transistor (M2) ;
 un deuxième condensateur (C2) relié entre le premier noeud (N1) et le deuxième noeud (N2) ;
 un troisième transistor PMOS (M3) ayant une électrode de grille reliée à une ligne de commande (GC), une première électrode reliée à l'électrode de grille du deuxième transistor (M2) et une deuxième électrode reliée à la deuxième électrode du deuxième transistor (M2) ; et
 une diode électroluminescente organique (OLED) ayant une électrode d'anode reliée à la deuxième électrode du deuxième transistor (M2) et une électrode de cathode reliée à la deuxième alimentation (ELVSS).
4. Procédé d'attaque selon la revendication 3, dans lequel en (a), la première alimentation (ELVDD) est appliquée à un niveau intermédiaire, les signaux de balayage sont appliqués à un niveau bas, et les signaux de commande sont appliqués à un niveau haut, et/ou dans lequel (b) comprend :
- (b1), dans lequel la première alimentation (ELVDD) est appliquée à un niveau bas, le signal de balayage est appliqué à un niveau haut ou à un niveau bas, et les signaux de commande sont appliqués à un niveau haut ;
 (b2), dans lequel la première alimentation (ELVDD) est appliquée à un niveau bas, les signaux de balayage sont appliqués à un niveau haut ou à un niveau bas, et les signaux de commande sont appliqués à un niveau haut ;
 (b3), dans lequel la première alimentation (ELVDD) est appliquée à un niveau intermédiaire, les signaux de balayage sont appliqués à un niveau haut ou à un niveau bas, et les signaux de commande sont appliqués à un niveau haut.
5. Procédé d'attaque selon la revendication 4, dans lequel en (b1) et en (b2), si les signaux de balayage sont appliqués à un niveau bas, les signaux de données qui leur correspondent sont appliqués à un niveau bas, et/ou dans lequel en (b3), si les signaux de balayage sont appliqués à un niveau bas, les signaux de données qui leur correspondent sont appliqués à un niveau haut.
6. Procédé d'attaque selon l'une des revendications 3 à 5, dans lequel (c) comprend :
- (c1), dans lequel la première alimentation (ELVDD) est appliquée à un niveau intermédiaire, les signaux de balayage sont appliqués à un niveau haut ou à un niveau bas, et les signaux de commande sont appliqués à un niveau haut ; et
 (c2) et (c3), dans lesquels la première alimentation (ELVDD) est appliquée à un niveau intermédiaire, les signaux de balayage sont appliqués à un niveau bas et les signaux de commande sont appliqués à un niveau bas.
7. Procédé d'attaque de l'afficheur électroluminescent organique selon la revendication 6, dans lequel en (c1), si les signaux de balayage sont appliqués à un niveau bas, les signaux de données qui leur correspondent sont appliqués à un niveau haut.
8. Procédé d'attaque selon l'une des revendications 3 à 7, dans lequel en (d), les signaux de commande sont appliqués à un niveau bas et/ou les largeurs des signaux de balayage appliqués séquentiellement sont appliqués pendant deux périodes horizontales, ceux des signaux de balayage qui sont appliqués de façon adjacente étant appliqués de façon qu'ils se chevauchent mutuellement d'une période horizontale.
9. Procédé d'attaque selon l'une des revendications 3 à 8, dans lequel en (e), la première alimentation (ELVDD) est appliquée à un niveau haut, et les signaux de balayage et les signaux de commande sont appliqués à un niveau haut, et/ou dans lequel en (f), la première alimentation (ELVDD) est appliquée à un niveau intermédiaire, et les signaux de balayage et les signaux de commande sont appliqués à un niveau haut.

FIG. 1

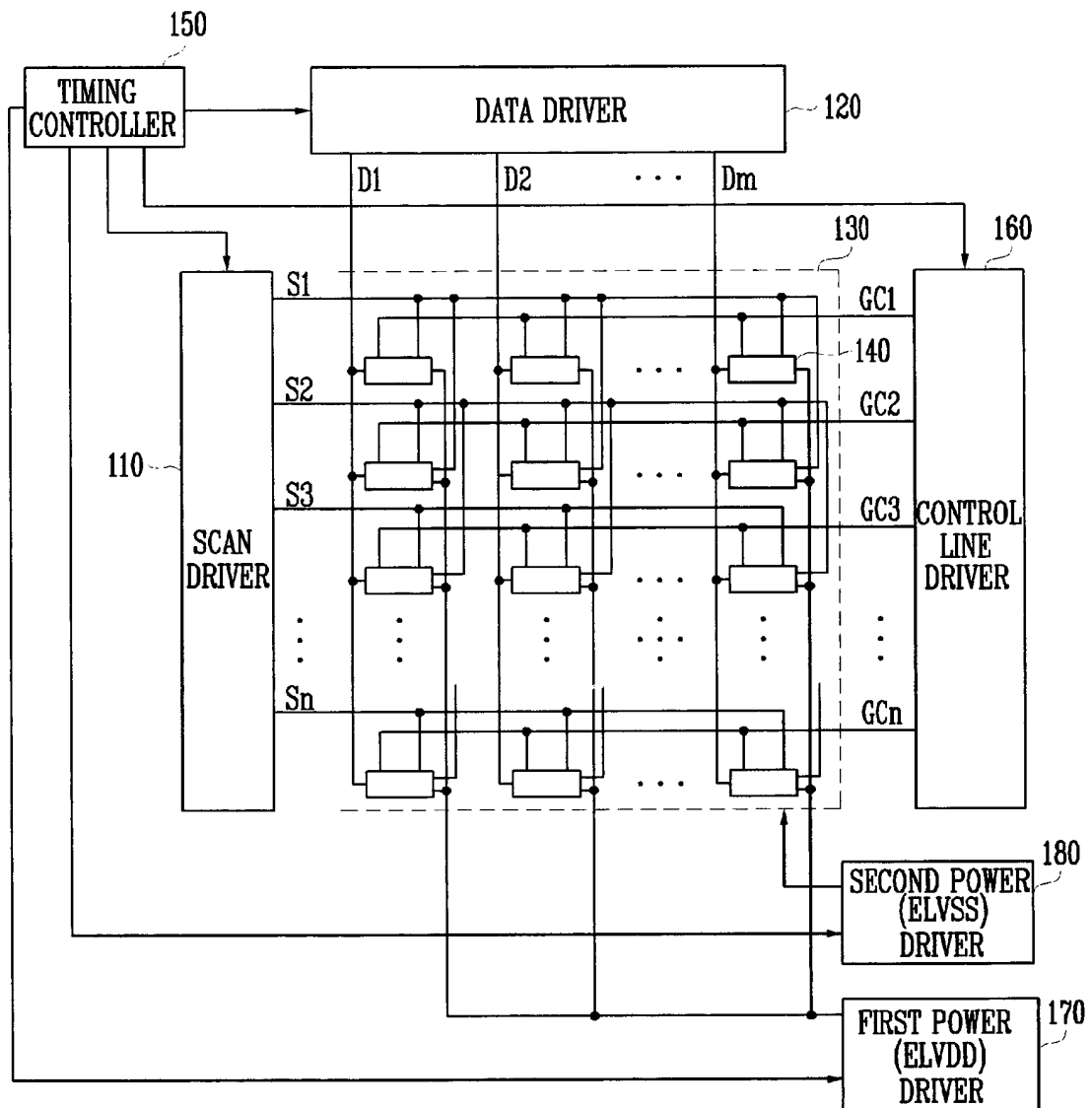


FIG. 2

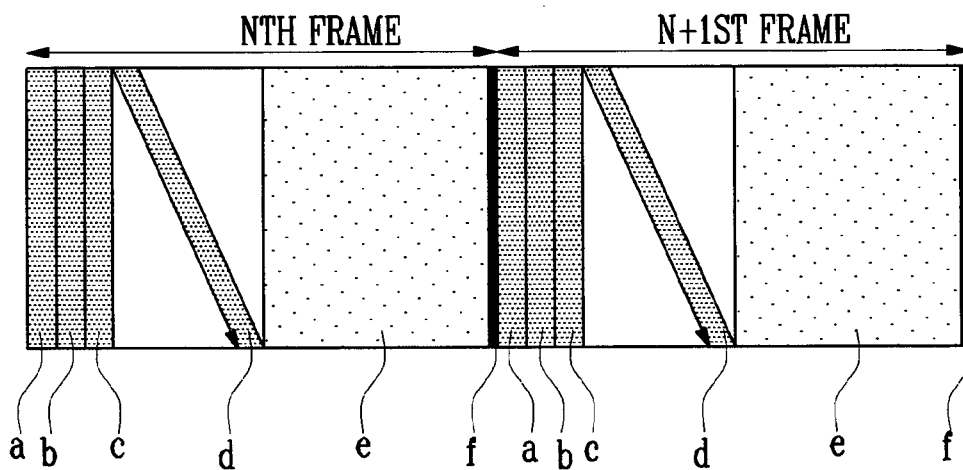


FIG. 3
(Related Art)

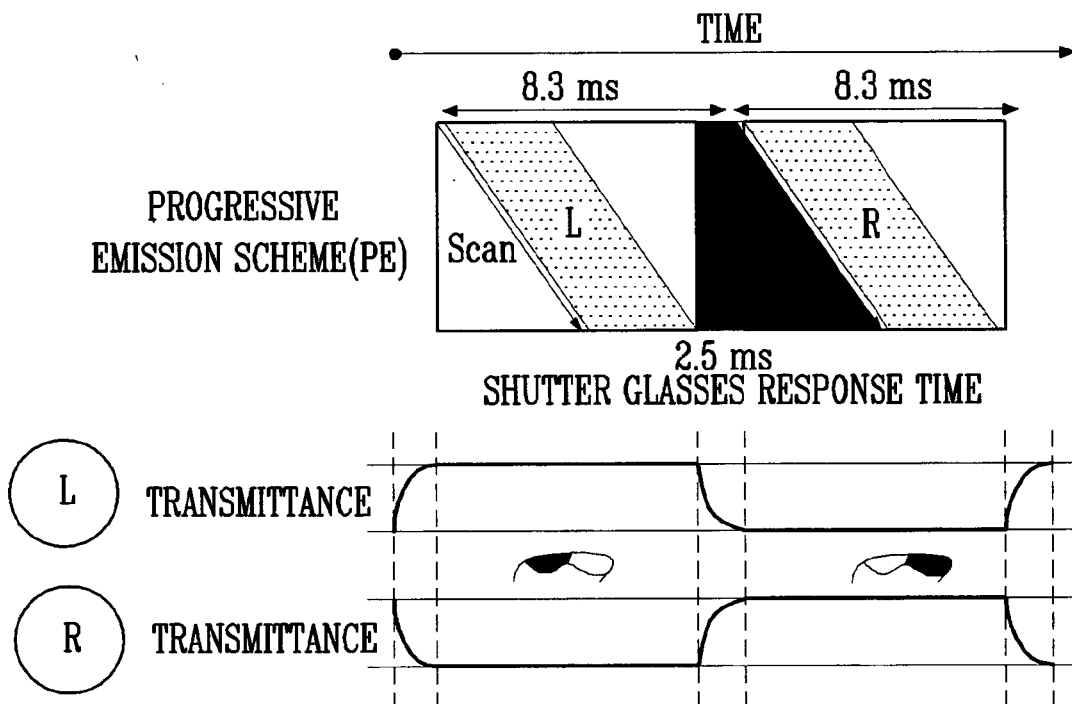


FIG. 4

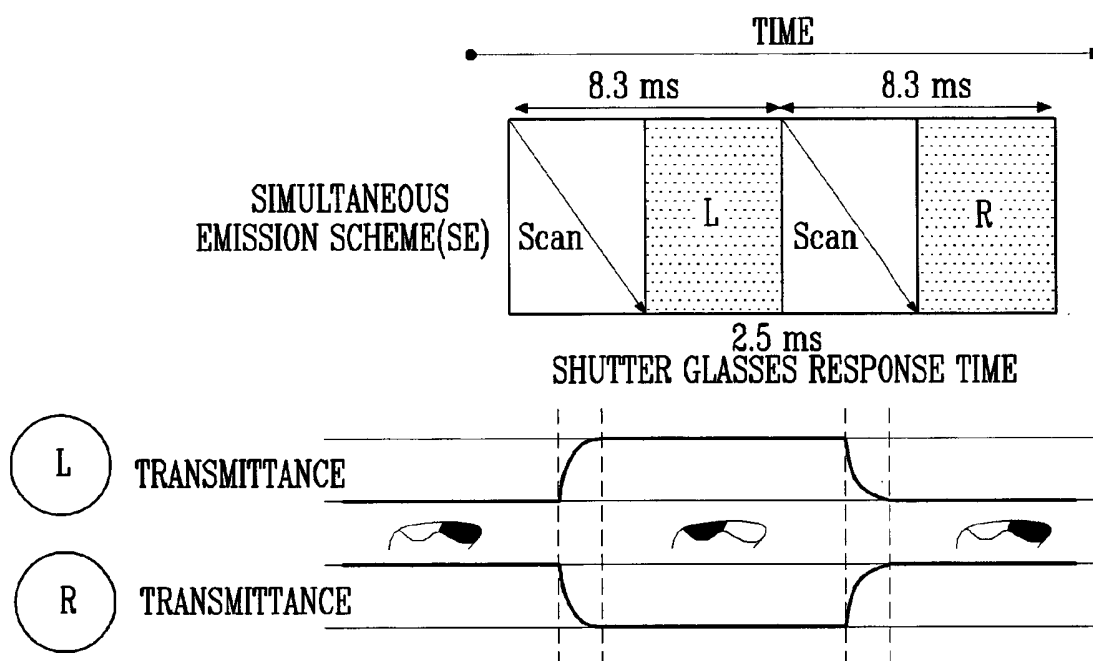


FIG. 5

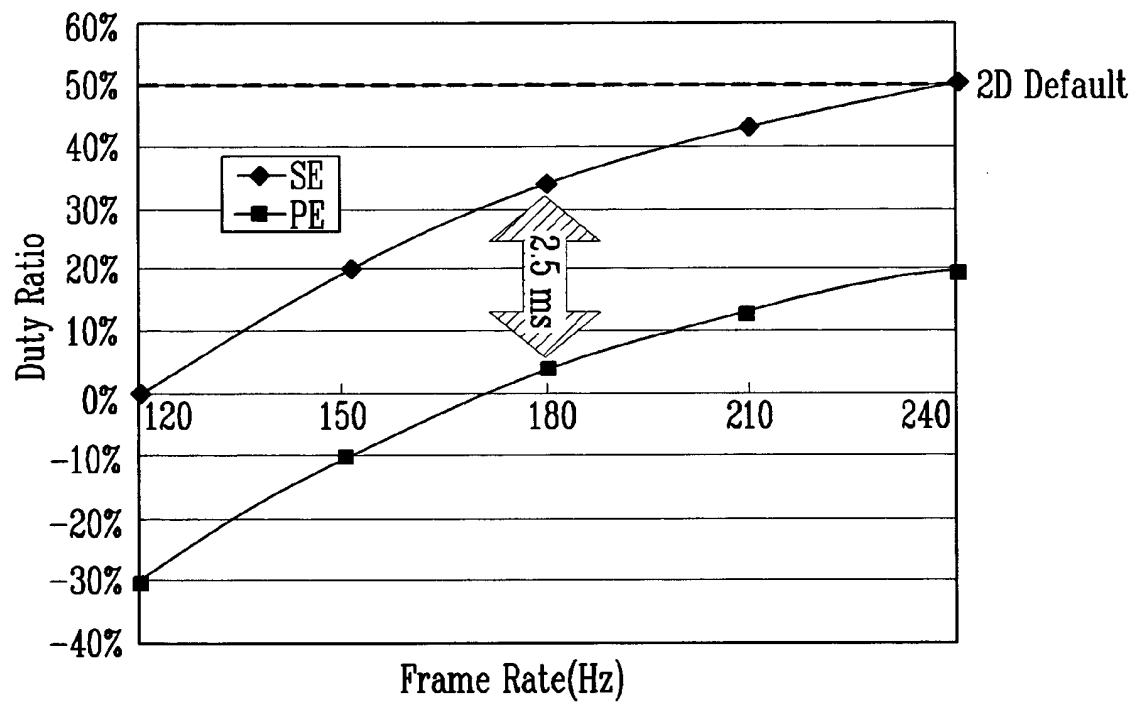


FIG. 6

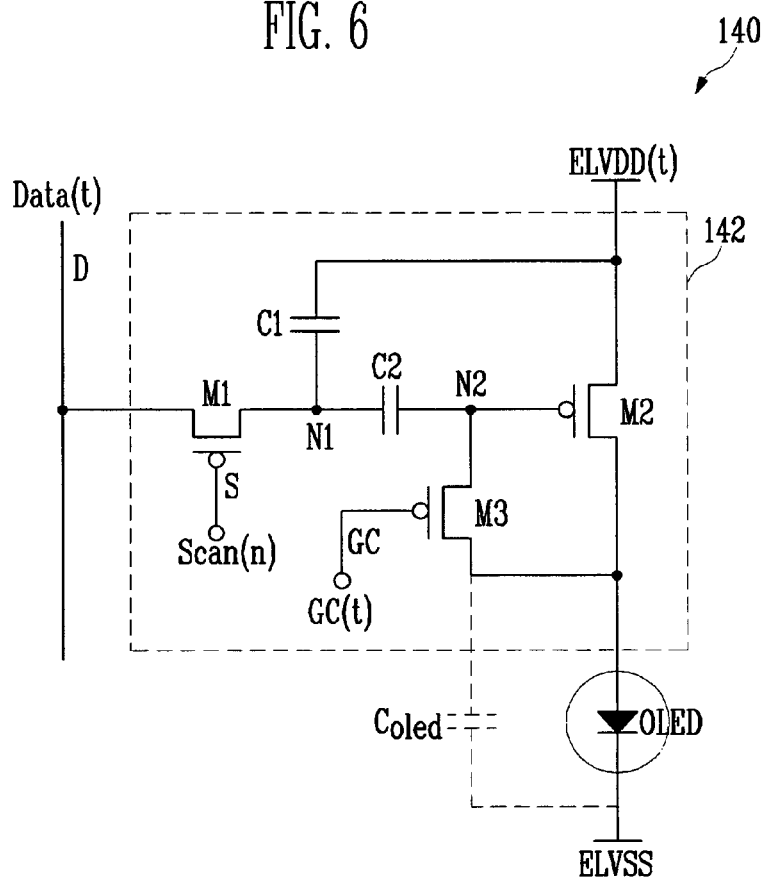


FIG. 7A

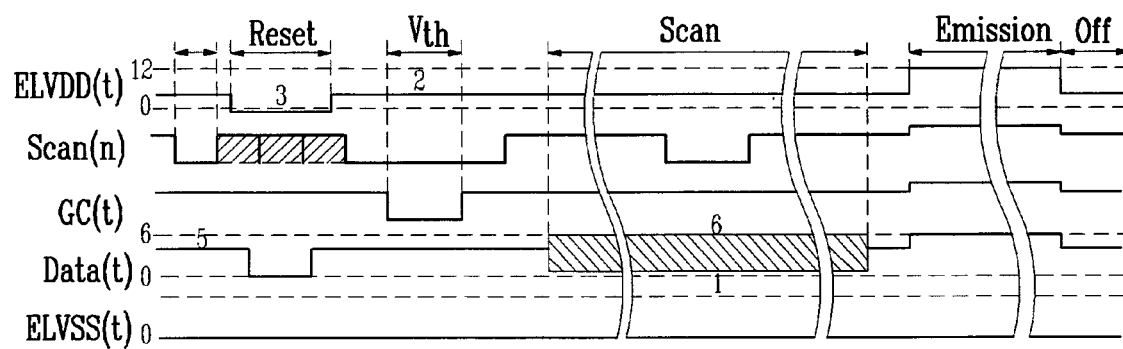


FIG. 7B

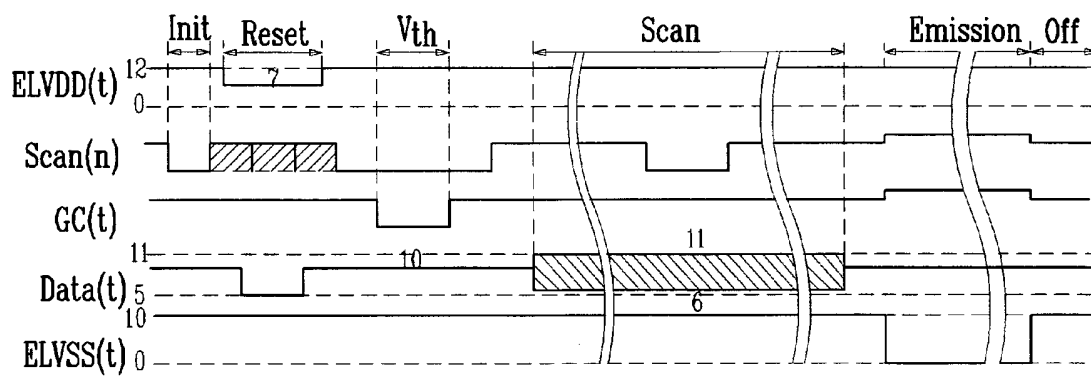


FIG. 7C

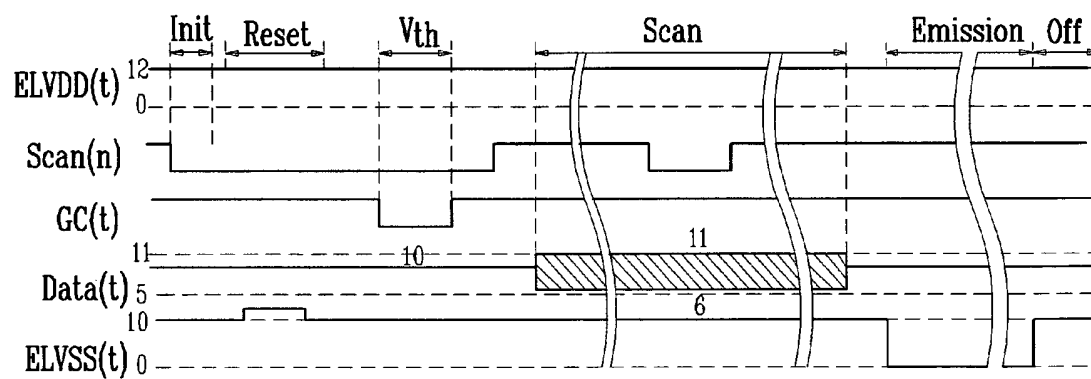


FIG. 8A

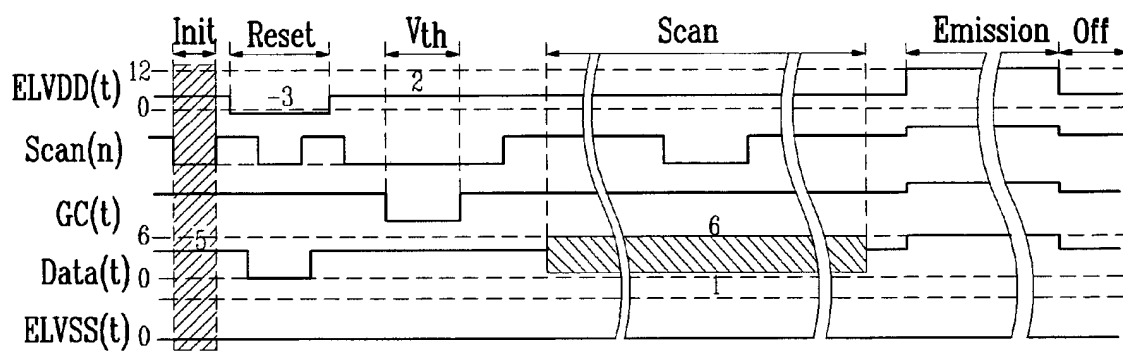
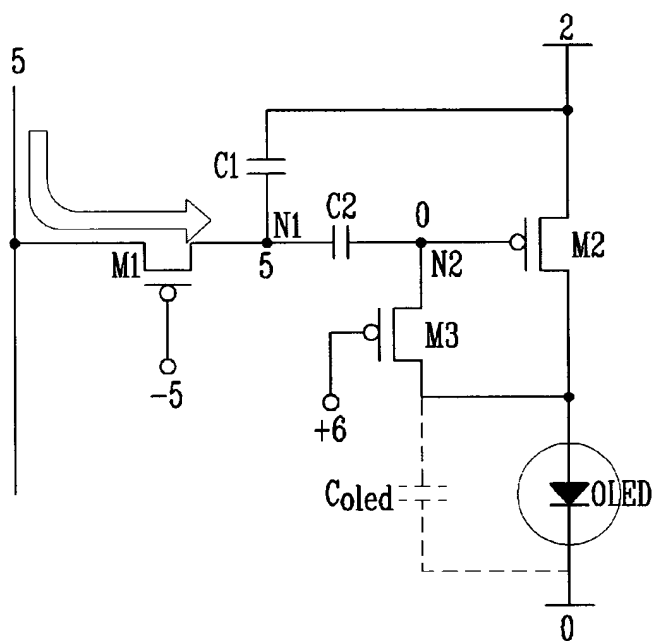


FIG. 8B

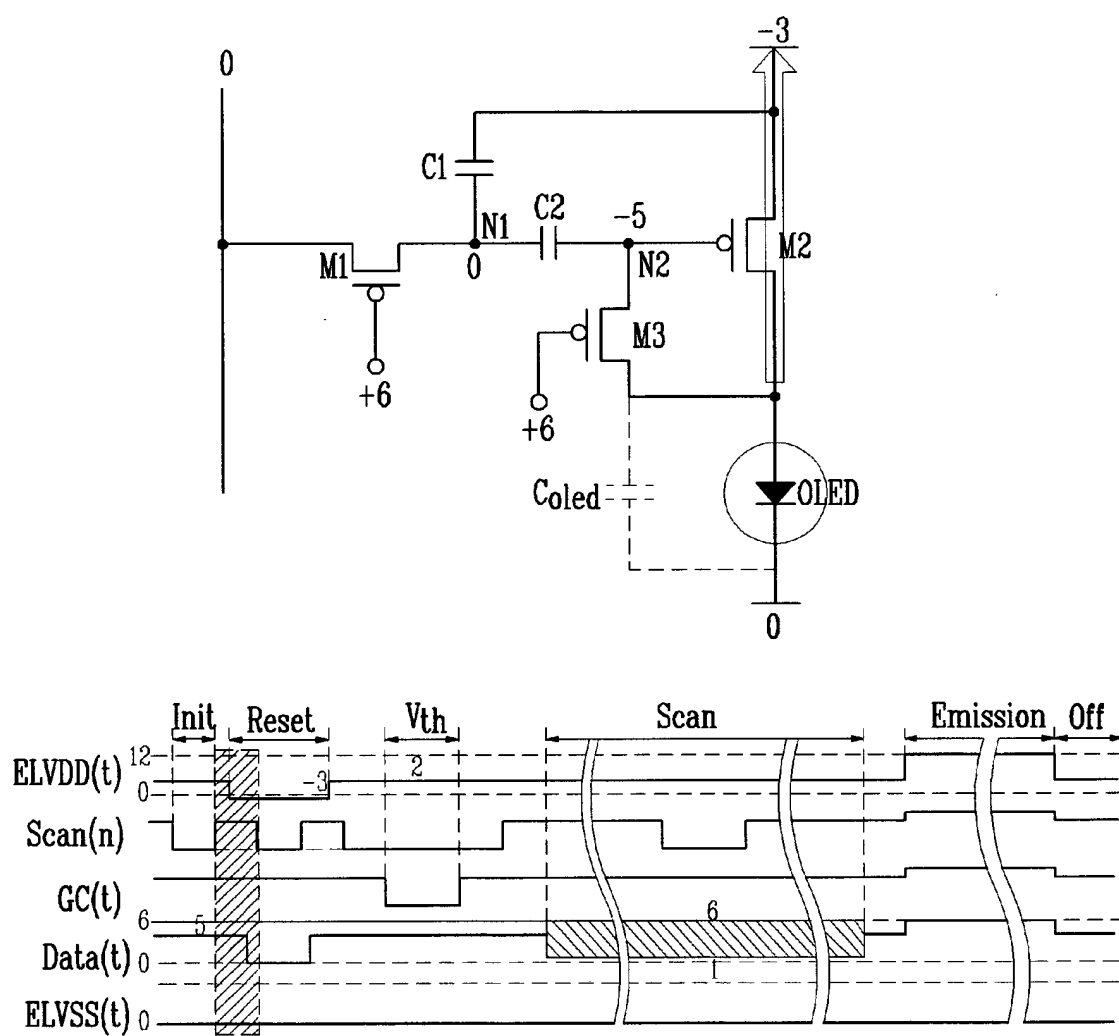


FIG. 8C

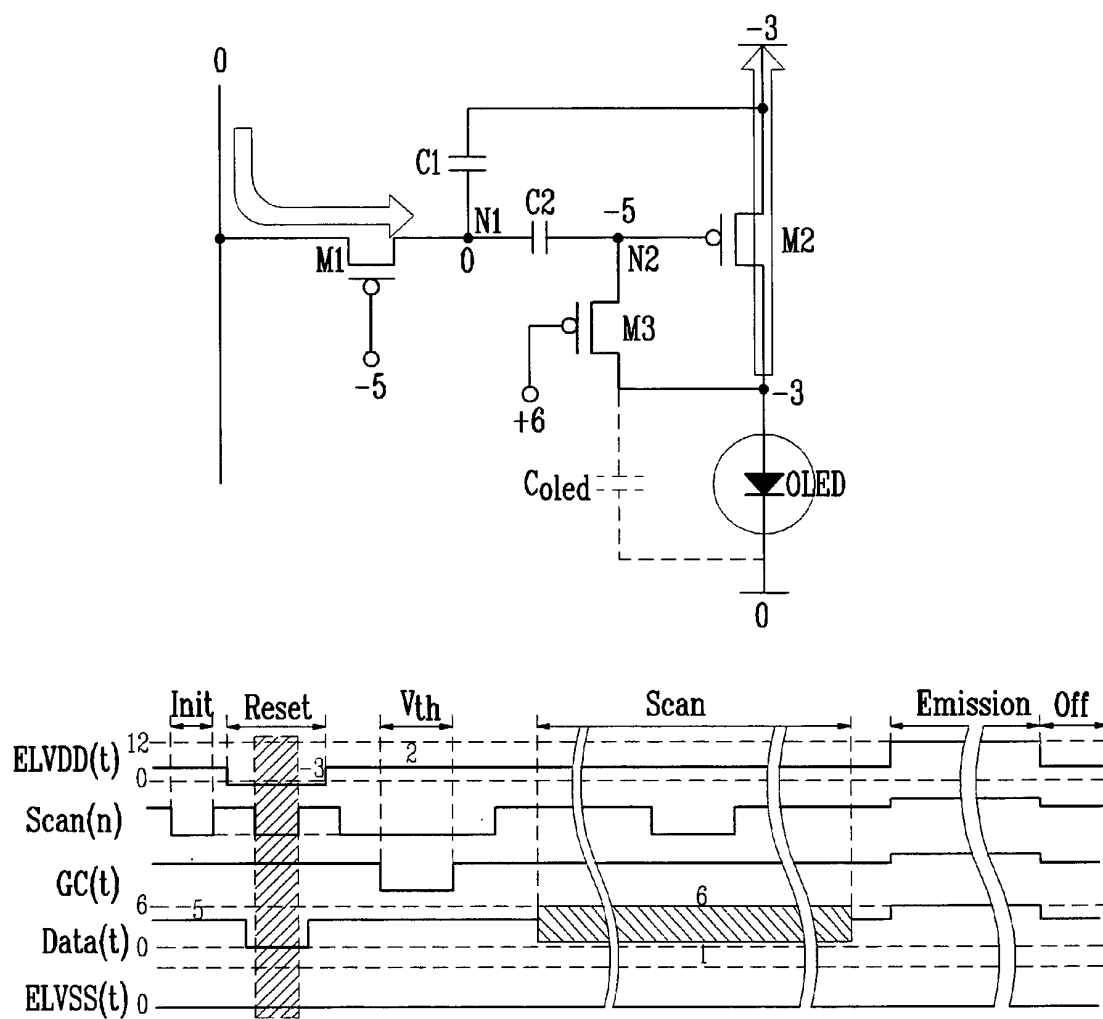


FIG. 8D

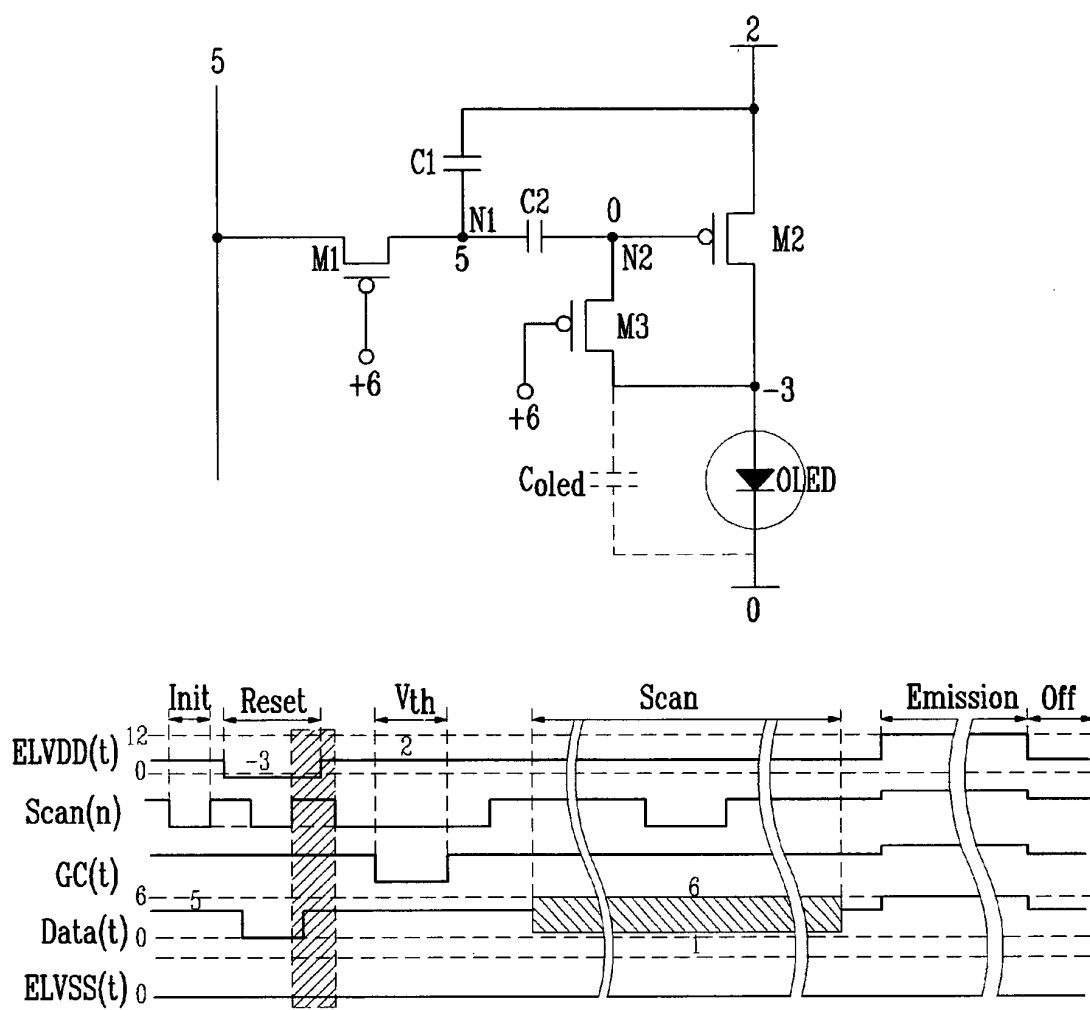


FIG. 8E

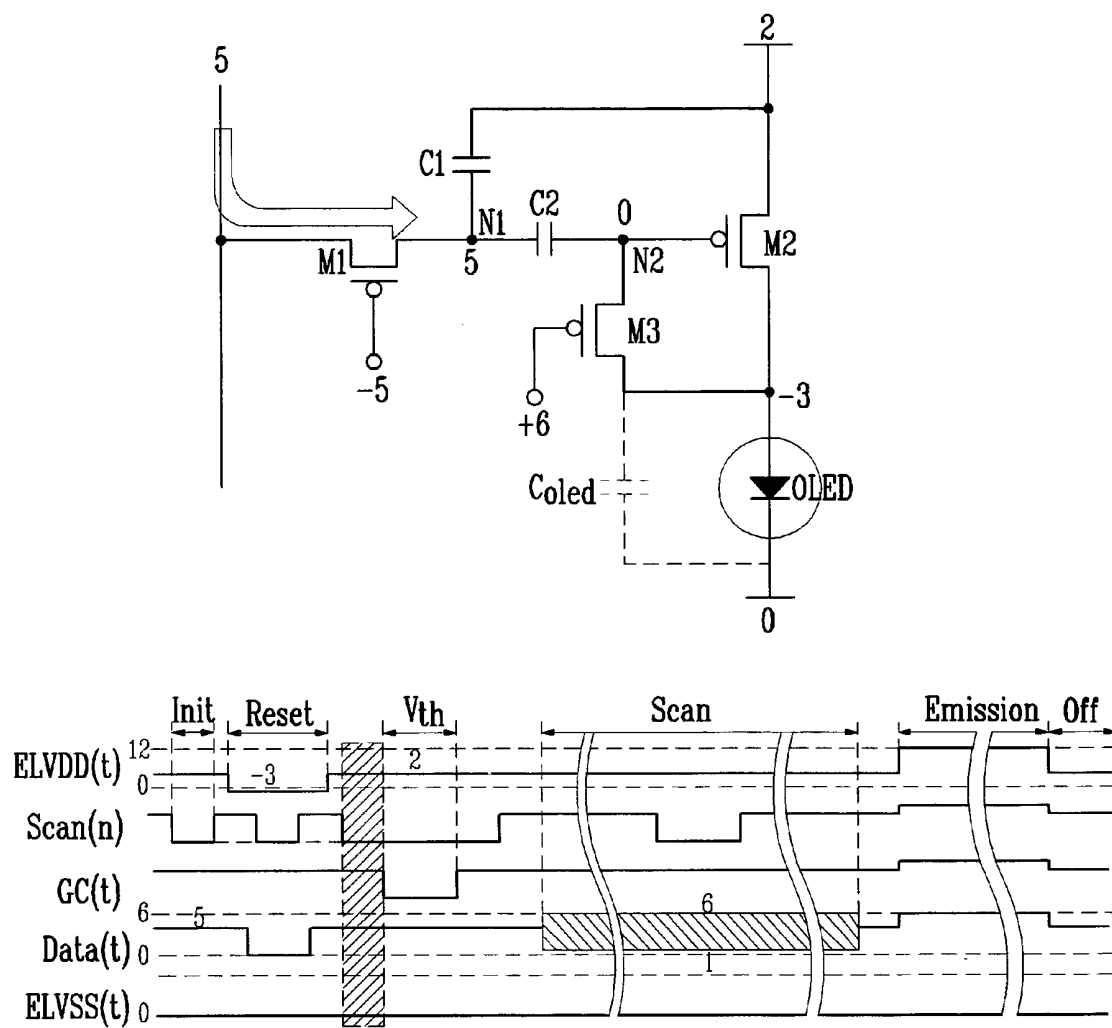


FIG. 8F

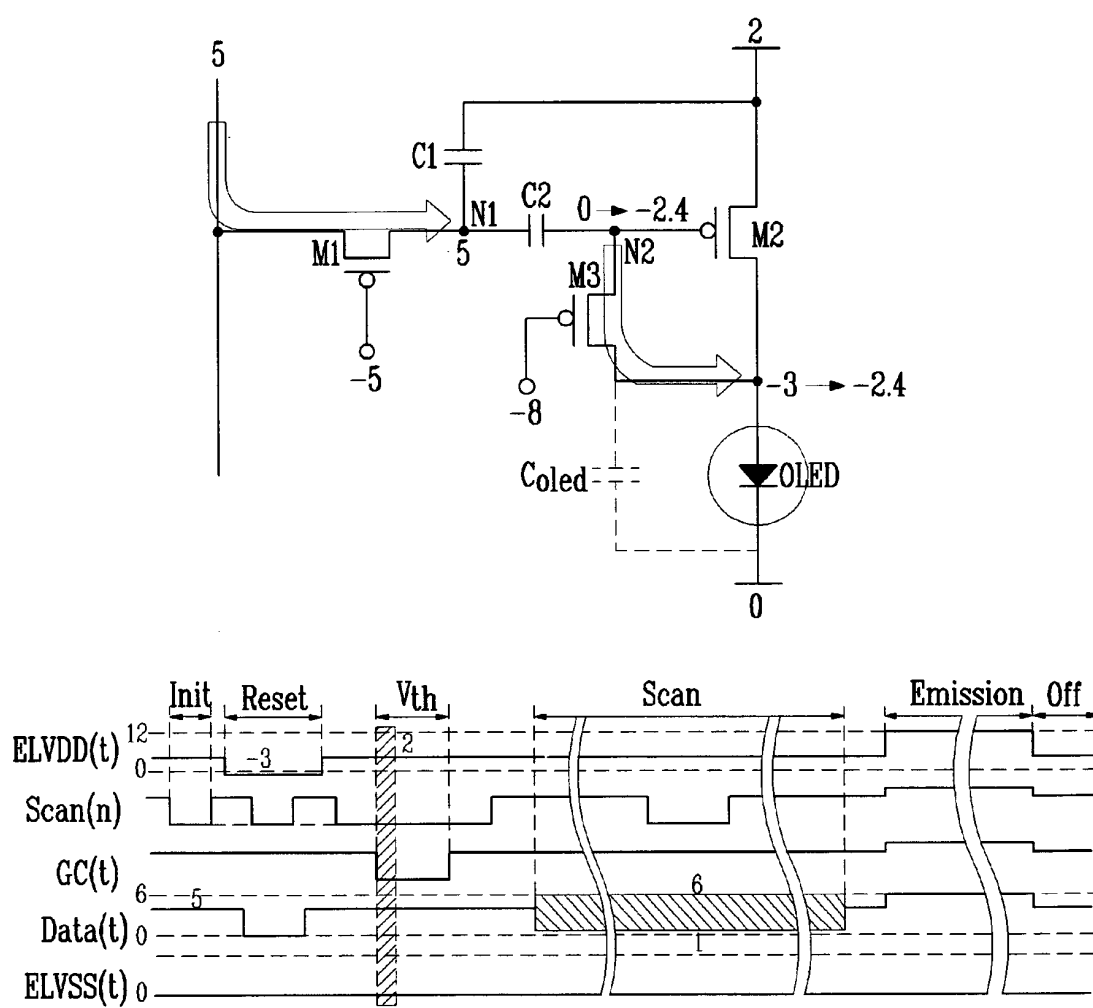


FIG. 8G

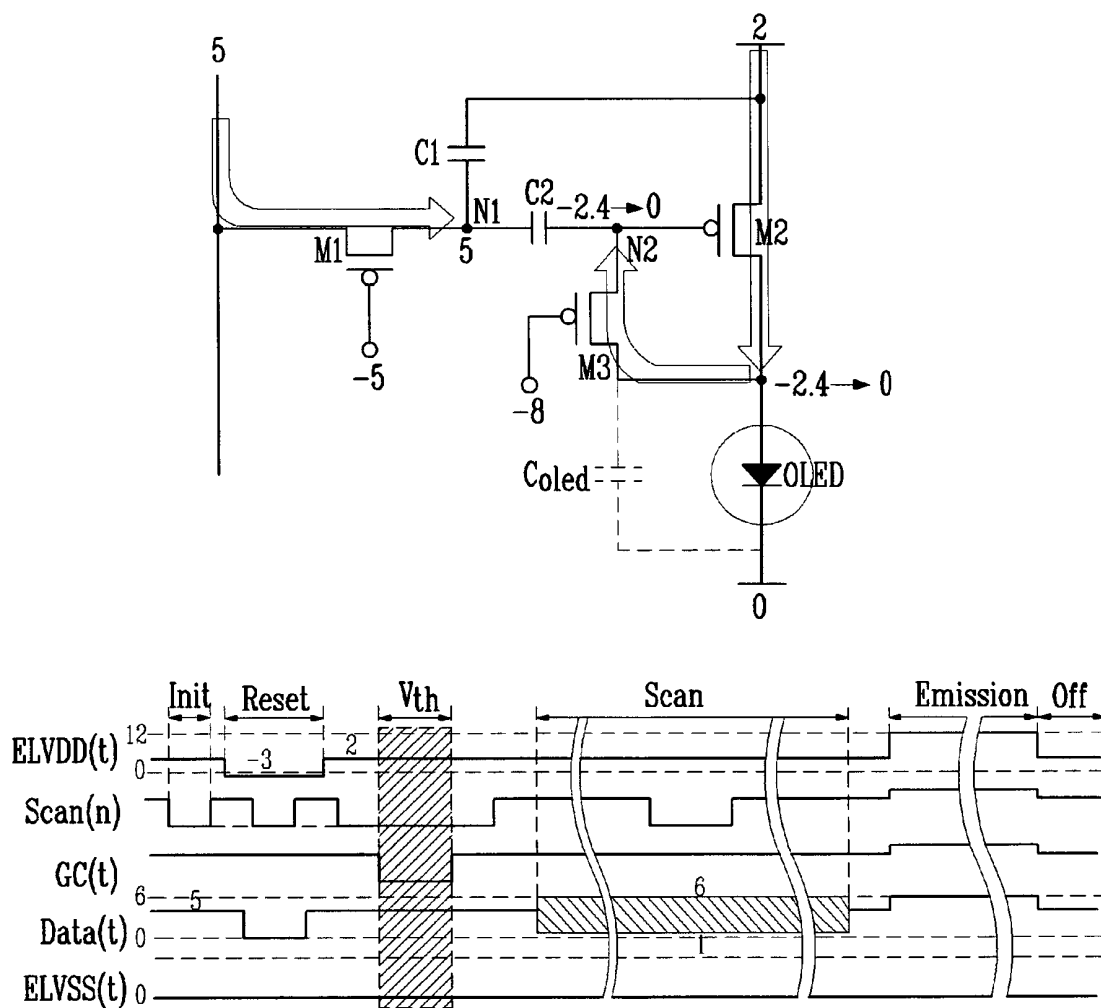


FIG. 8H

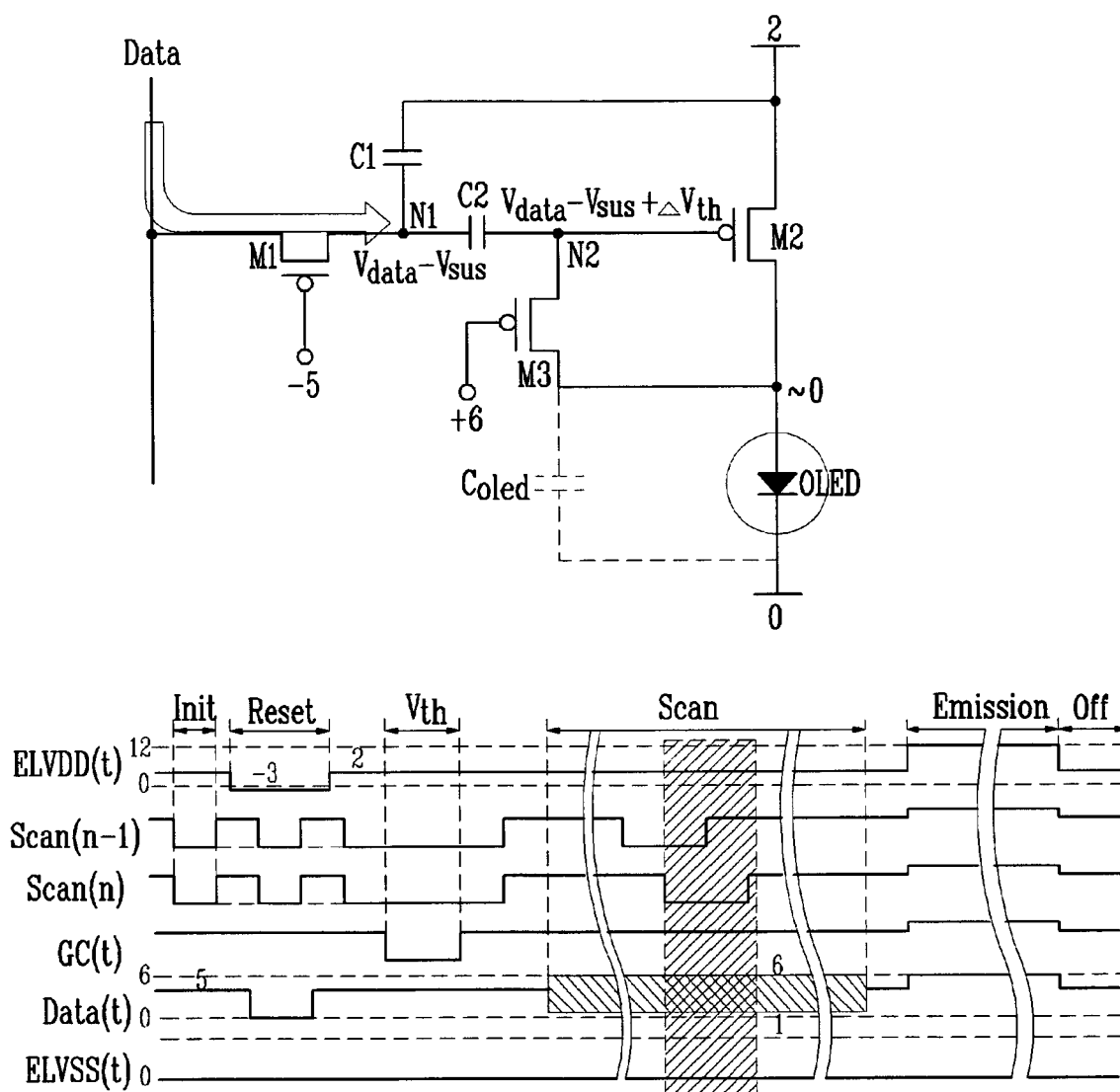


FIG. 8I

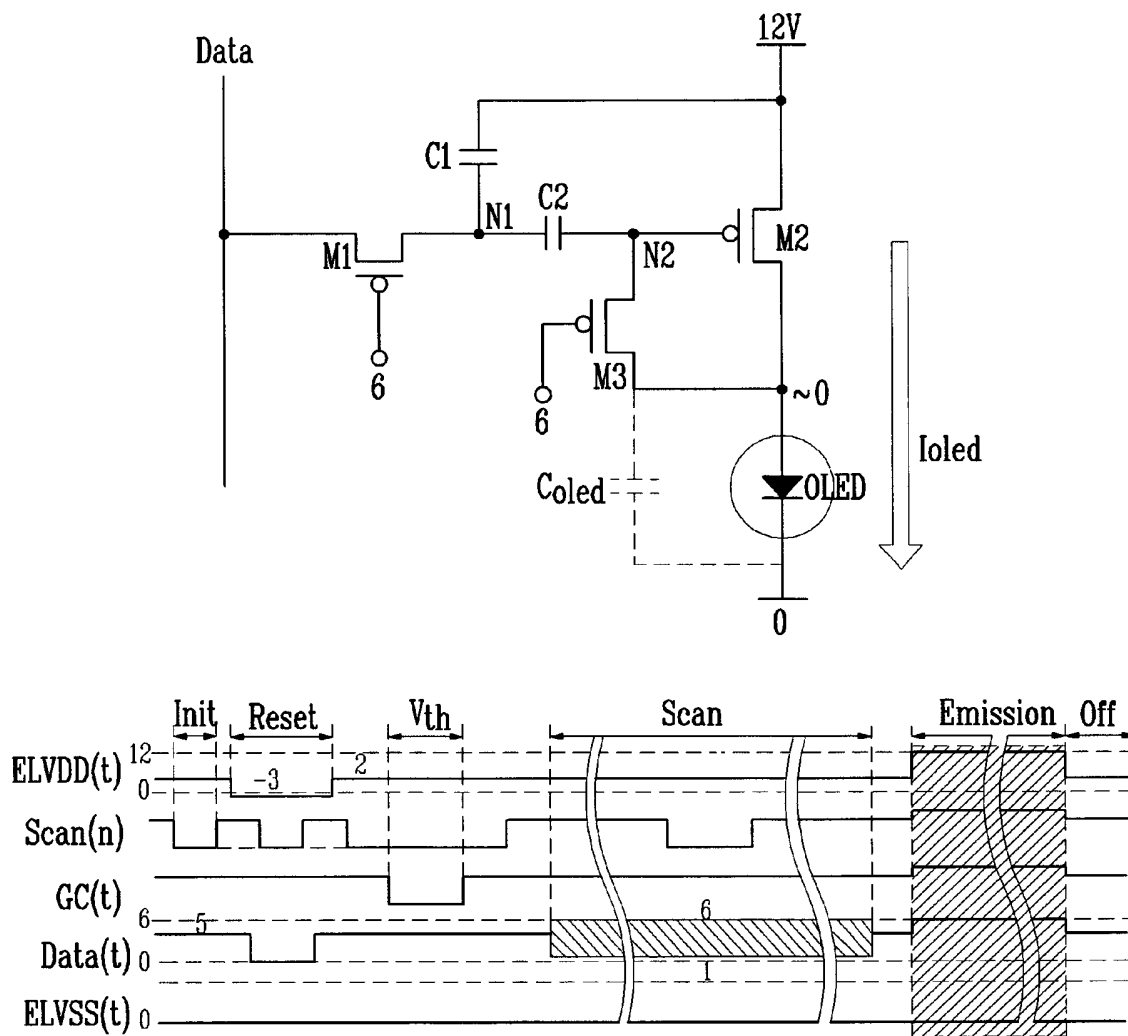


FIG. 8J

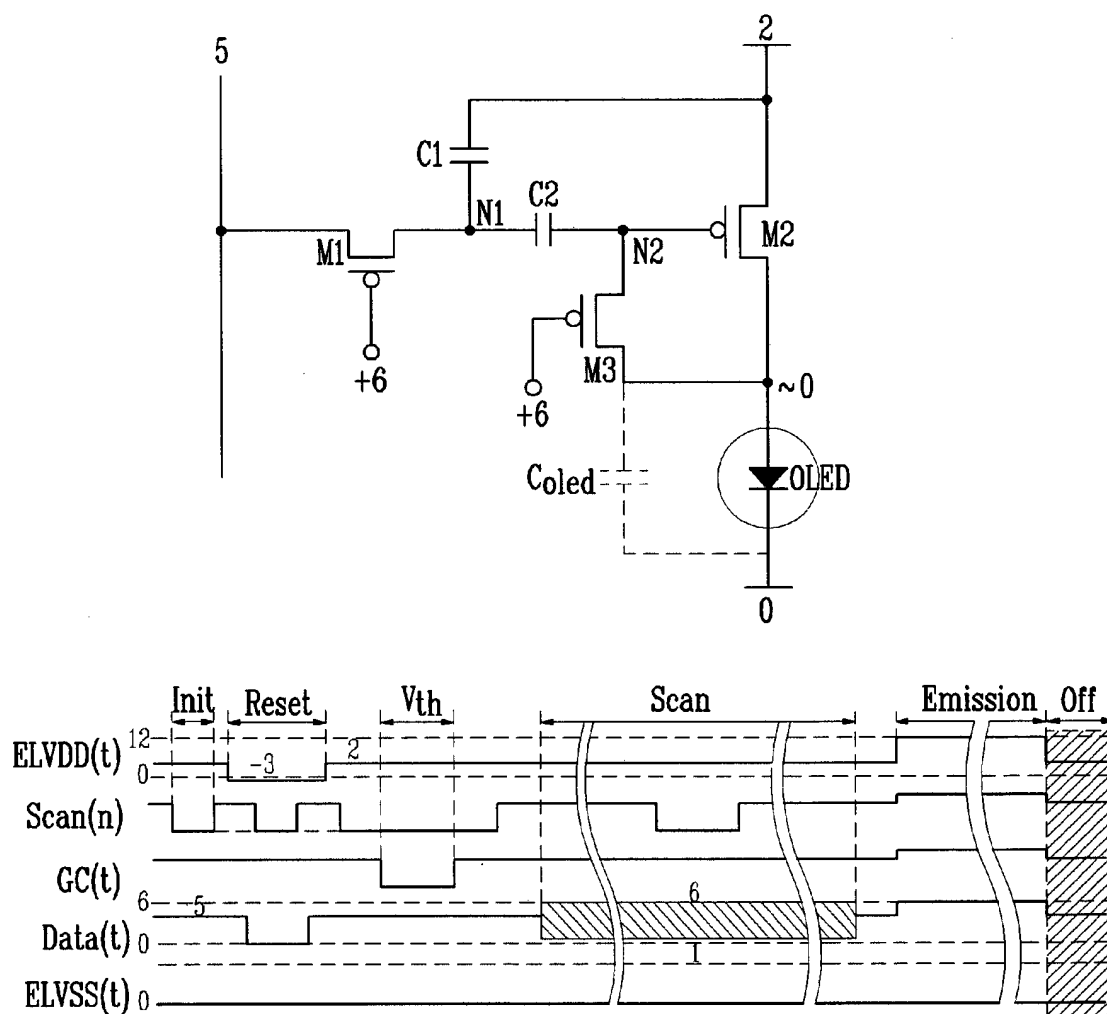
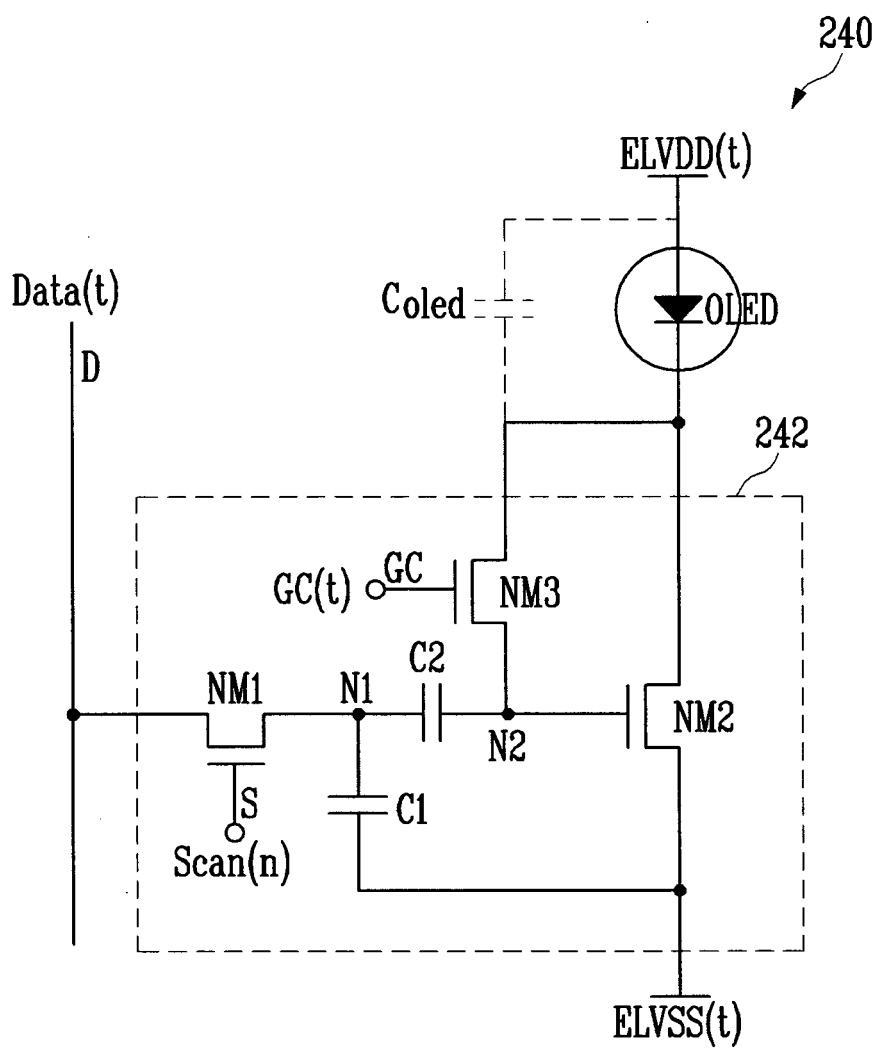


FIG. 9



REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- KR 1020090071280 [0001]
- US 6380689 B1 [0011]
- US 20090058843 A1 [0011]
- US 6229506 B1 [0011]

专利名称(译)	有机发光显示器及其驱动方法		
公开(公告)号	EP2293274B1	公开(公告)日	2013-11-20
申请号	EP2010171396	申请日	2010-07-30
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星移动显示器有限公司.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	LEE BAEK WOON		
发明人	LEE, BAEK-WOON		
IPC分类号	G09G3/00 G09G3/32		
CPC分类号	G09G3/3291 G09G3/003 G09G3/3208 G09G3/3233 G09G3/3258 G09G2300/043 G09G2300/0866 G09G2310/063 G09G2320/043		
优先权	1020090071280 2009-08-03 KR		
其他公开文献	EP2293274A3 EP2293274A2		
外部链接	Espacenet		

摘要(译)

有机发光显示器包括显示单元 (130)，其包括耦合到扫描线 (S1，S2，S3，Sn) 的像素 (140,240)，控制线 (GC1，GC2，GC3，GCn) 和数据线 (D1)，D2，Dm)。用于通过控制线 (GC1，GC2，GC3，GCn) 和第一电源驱动器 (170) 向各个像素 (140,240) 提供控制信号的控制线驱动器 (160) 将第一电源 (ELVDD) 施加到显示单元 (130) 的像素 (140,240)，而第二电源驱动器 (180) 将第二电源 (ELVSS) 施加到显示单元 (130) 的像素 (140,240)。第一功率 (ELVDD) 和/或第二功率 (ELVSS) 被施加到显示单元 (130) 的像素 (140,240)，其在一帧的时段期间具有不同电平的电压值，并且控制信号和在帧的发光时段期间，第一和第二功率 (ELVDD，ELVSS) 被同时提供给所有像素 (140,240)。

