(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 973 162 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
20.09.2017 Bulletin 2017/38

(51) Int Cl.:
H01L 27/32 *(2006.01)*

(21) Application number: **08003998.5**

(22) Date of filing: **04.03.2008**

(54) **ORGANIC LIGHT-EMITTING DISPLAY PANEL AND METHOD OF MANUFACTURING THE SAME**

Organische lichtemittierende Anzeigetafel und Herstellungsverfahren dafür

Panneau d'affichage luminescent organique et son procédé de fabrication

(84) Designated Contracting States:
DE FR GB

(30) Priority: **20.03.2007 KR 20070026889**

(43) Date of publication of application:
24.09.2008 Bulletin 2008/39

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US-A1- 2003 222 589

EP 1 973 162 B1

Printed by Jouve, 75001 PARIS (FR)

Description

Cross-Reference to Related Application

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2007-0026889, filed on March 20, 2007, the disclosure of which is incorporated herein by reference in its entirety.

Background of the Invention

Field of the Invention

[0002] The present invention relates to display panels and, more particularly, to an organic light-emitting display panel and a method of manufacturing the same which prevents formation of a defective storage capacitor.

Description of the Related Art

[0003] Organic light-emitting displays emit light generated when electrons and holes are paired after an electric charge is injected into the organic light-emitting layer. The organic light-emitting display is a next-generation device that can be driven with low voltage and has low power consumption.

[0004] In the organic light-emitting display, a switching transistor is turned on by a scan pulse supplied from a gate line and a data signal applied from a data line. The data signal from the switching transistor is charged to a storage capacitor that drives a driving transistor for one frame period. This allows an electric current from a power line to be supplied to the organic light-emitting diode. A storage electrode connected to a gate electrode of the driving transistor overlaps the power line, thus forming the storage capacitor.

[0005] Misalignment of the mask used for forming the storage electrode may result in a defective storage capacitor. Shifting of the storage electrode to the top, bottom, left or right of the correct position will result in changing the capacity of the storage capacitor at a pixel, causing a brightness difference.

Summary of the Invention

[0006] Accordingly, the present invention provides an organic light-emitting display panel and a method of manufacturing the organic light-emitting display panel in which the overlapping area of a power line and a storage electrode is kept the same and thus the capacity of a storage capacitor provided at each pixel is the same as each other.

[0007] In accordance with an aspect of the present invention, an organic light-emitting display panel comprises: a gate line and a data line formed to cross each other on a substrate; an organic light-emitting diode formed in a pixel area defined by the intersection of the gate line and the data line; a power line formed parallel to the data line and supplying an electric current to the organic light-emitting diode; a switching transistor provided at the intersection of the gate line and the data line; a driving transistor connected to the switching transistor and the power line to control the current supplied from the power line; and a storage capacitor composed of a storage electrode overlapping the power line with a first gate-insulating layer disposed therebetween, wherein the storage capacitor includes a groove portion formed on a lateral side of the power line overlapping the storage electrode so that the overlapping area of the power line and the storage electrode is kept the same.

[0008] The groove portion may be formed on a lateral side adjacent to the data line.

[0009] The groove portion may have a length at least equal to or greater than a length between the top and bottom of the storage electrode.

[0010] The storage electrode may have a width greater than that of an overlapping area of the storage electrode and the power line.

[0011] The organic light-emitting display panel may further include an auxiliary storage electrode extending from the storage electrode to overlap the power line.

[0012] The auxiliary storage electrode may have a width smaller or larger than that of the power line.

[0013] The driving transistor may include: a first semiconductor pattern formed of polysilicon on the substrate; a first source electrode formed on the first semiconductor pattern and connected to the power line; a first drain electrode formed on the first semiconductor pattern to face the first source electrode and connected to the organic light-emitting diode; a second gate-insulating layer formed on the first source electrode and the first drain electrode; and a first gate electrode formed on the second gate-insulating layer to overlap the first semiconductor pattern.

[0014] The first gate electrode may be electrically connected to the storage electrode.

[0015] The switching transistor may include: a second gate electrode formed on the first gate-insulating layer; the second gate-insulating layer formed on the second gate electrode; a second semiconductor pattern formed of amorphous silicon on the substrate; and a second source electrode and a second drain electrode formed on the second semiconductor pattern to face each other.

[0016] The organic light-emitting display panel may further include a bridge electrode connecting the first gate electrode to the second drain electrode.

[0017] In accordance with another aspect of the present invention, there is provided a method of manufacturing an organic light-emitting display panel, the method including: forming a gate line and a data line on a substrate, the gate line and the data line crossing each other with a gate-insulating layer disposed therebetween; forming an organic light-emitting diode in a pixel area defined by the intersection of the gate line and the data line; forming a switching transistor at the intersection of the gate line and the data line; forming a driving tran-

sistor connected to the switching transistor; forming a power line parallel to the data line; and forming a storage electrode overlapping the power line with the gate-insulating layer disposed therebetween to form a storage capacitor and including a projecting portion with respect to a lateral side of the power line.

[0018] The process of forming the power line parallel to the data line may further include forming a groove portion on a lateral side adjacent to the data line in an overlapping area of the storage electrode and the power line.

[0019] The process of forming the groove may further include forming the groove portion to have a length at least equal to or greater than a length between the top and bottom of the storage electrode.

[0020] The process of forming the storage electrode may further include forming an auxiliary storage electrode extending from the storage electrode to overlap the power line.

[0021] The process of forming the auxiliary storage electrode may further include forming the auxiliary storage electrode to have a width smaller or larger than that of the power line.

[0022] The process of forming the switching transistor and the driving transistor may include: forming a first semiconductor pattern with polysilicon on the substrate and a first gate-insulating layer; forming a source electrode on the first semiconductor pattern and connected to the power line, and a first drain electrode facing the first source electrode; forming a second gate-insulating layer on the first source electrode and the first drain electrode; forming a first gate electrode on the second gate-insulating layer to overlap the first semiconductor pattern, and a second gate electrode simultaneously with the first gate electrode; and forming a third gate-insulating layer, a second semiconductor pattern, a second source electrode, and a second drain electrode.

Brief Description of the Drawings

[0023] The above and other features of the present invention will be described in reference to certain exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a plan view of an organic light-emitting display panel in accordance with a first embodiment of the present invention;

FIG. 2 is a cross-sectional view taken along line I - I ' of FIG. 1 ;

FIG. 3 is a plan view of a storage capacitor of the organic light-emitting display panel of FIG. 1;

FIG. 4 is a cross-sectional view taken along line II - II' of FIG. 3;

FIGS. 5A and 5B are plan views of a storage electrode shifted to the left and right, respectively;

FIG. 6 is a plan view of a storage capacitor of an organic light-emitting display panel in accordance with a second embodiment of the present invention;

FIGS. 7A and 7B are plan views of a storage electrode in the storage capacitor of FIG. 6 shifted to the top and bottom, respectively;

FIGS. 8A to 14B are plan views and cross-sectional views illustrating a method of manufacturing an organic light-emitting display panel in accordance with the present invention.

Detailed Description of the Invention

[0024] FIG. 1 is a plan view of an organic light-emitting display panel in accordance with a first embodiment of the present invention, and FIG. 2 is a cross-sectional view taken along line I - I ' of FIG. 1.

[0025] Referring to FIGS. 1 and 2, the organic light-emitting display panel in accordance with the present invention includes a gate line 20, a data line 40, an organic light-emitting diode 100, and a power line 70. Each pixel area includes a switching transistor TFT2, a driving transistor TFT1, and a storage capacitor Cst. The gate line 20 supplies a scan pulse and is connected to a second gate electrode 21 of the switching transistor TFT2. The data line 40 supplies a data signal and is connected to a second source electrode 41 of the switching transistor TFT2. The power line 70 is formed parallel to the data line 40 and crosses the gate line 20 with a first gate-insulating layer 31 disposed therebetween. The power line 70 supplies an electric current to the organic light-emitting diode 100 and is connected to a first source electrode 71 of the driving transistor TFT1.

[0026] The driving transistor TFT1 controls the electric current supplied from the power line 70 to the organic light-emitting diode 100 in response to the data signal applied to a first gate electrode 61 thereof, thus adjusting the light-emitting amount of the organic light-emitting diode 100. The driving transistor TFT1 includes the first gate electrode 61 connected a second drain electrode 42 of the switching transistor TFT2, the first source electrode 71 connected to the power line 70, a first drain electrode 72 facing the first source electrode 71 and connected to an anode electrode 73 of the organic light-emitting diode 100, and a first semiconductor pattern forming a channel portion between the first source electrode 71 and the first drain electrode 72.

[0027] The first semiconductor pattern includes a first semiconductor layer 62 overlapping the first gate electrode 61 with a first gate-insulating layer 31 disposed therebetween, and a first ohmic contact layer 63 formed on the first semiconductor layer 62 except for the channel portion to form ohmic contact with the first source electrode 71 and the first drain electrode 72.

[0028] The first semiconductor layer 62 may be formed of amorphous silicon or polysilicon. The first semiconductor layer 62 may be formed of polysilicon to ensure a longer lifespan in view of the characteristics of the driving transistor TFT1 in which an electric current flows continuously during the light emission period of the organic light-emitting diode 100. If the first semiconductor layer

62 is formed of polysilicon, the driving transistor TFT1 may have a top-gate structure in which the first gate electrode 61 is formed on the first semiconductor layer 62 as shown in FIG. 2.

[0029] When the gate line 20 is supplied with the scan pulse, the switching transistor TFT2 is turned on and the data signal applied to the data line 40 is supplied to the storage capacitor Cst and the first gate electrode 61 of the driving transistor TFT1. For this, the switching transistor TFT2 includes the second gate electrode 21 connected to the gate line 20, the second source electrode 41 connected to the data line 40, the second drain electrode 42 facing the second source electrode 41 and connected to the first gate electrode 61 of the driving transistor TFT1 and the storage capacitor Cst, and a second semiconductor pattern forming a channel portion between the second source electrode 41 and the second drain electrode 42.

[0030] The second semiconductor pattern includes a second semiconductor layer 22 overlapping the second gate electrode 21 with the second gate-insulating layer 32 disposed therebetween, and a second ohmic contact layer 23 formed on the second semiconductor layer 22 except for the channel portion to form ohmic contact with the second source electrode 41 and the second drain electrode 42.

[0031] The second semiconductor layer 22 may be formed of amorphous silicon or polysilicon. Preferably, the second semiconductor layer 22 is formed of amorphous silicon which is advantageous to the on-off operation since the switching transistor TFT2 requires excellent on-off characteristics.

[0032] The second drain electrode 42 and the first gate electrode 61 are connected to each other through a bridge electrode 55. The second drain electrode 42 is exposed by a first contact hole 51, and the first gate electrode 61 is exposed by a second contact hole 52. Accordingly, the second drain electrode 42 and the first gate electrode 61 are connected through the bridge electrode 55 passing through the first and second contact holes 51 and 52. The bridge electrode 55 may be formed of the same material as the anode electrode 73.

[0033] A passivation layer 33 is formed on a substrate 10 on which the driving transistor TFT1, the switching transistor TFT2, and the storage capacitor Cst are formed. The passivation layer 33 may comprise an inorganic insulating layer such as silicon oxide (SiOx), silicon nitride (SiNx), or the like, which does not deteriorate the characteristics of the thin film transistor.

[0034] The organic light-emitting diode 100 includes the anode electrode 73 formed of a transparent conductive material, a cathode electrode 80 formed of an opaque conductive material and facing the anode electrode 73, and an organic light-emitting layer 90 disposed therebetween.

[0035] The organic light-emitting layer 90 emits light in accordance with the amount of the current applied to the anode electrode 73 and the light of the organic light-emitting layer 90 is transmitted toward the anode electrode 73. The organic light-emitting layer 90 may be formed of a low molecular or polymer organic light-emitting material. The organic light-emitting layer 90 may be formed of a low molecular material. In the present embodiment, the organic light-emitting layer 90 is formed independently at each pixel. The organic light-emitting layer 90 may be formed in a triple layer structure in which emissive layers displaying red (R), green (G) and blue (B) are sequentially stacked, in a double layer structure in which emissive layers having a complementary color relationship are stacked, or in a single layer structure composed of an emissive layer emitting white color.

[0036] Moreover, a hole transport layer, an electron transport layer, and an electron injection layer may be further provided on the top and bottom of the organic light-emitting layer 90 to improve the light-emitting efficiency and characteristics of the organic light-emitting layer 90.

[0037] An organic planarization layer 34 may be further provided to compensate for a step height of the organic light-emitting layer 90. The organic planarization layer 34 includes the first contact hole 51 exposing a portion of the second drain electrode 42 of the switching transistor TFT2 and the second contact hole 52 exposing a portion of the first drain electrode 72 of the driving transistor TFT1. The first and second contact holes 51 and 52 are formed to penetrate the first and second gate-insulating layers 31 and 32, the passivation layer 33, and the organic planarization layer 34. Moreover, a barrier layer 35 is formed on the organic planarization layer 34 to form the organic light-emitting layer 90.

[0038] As shown in FIG. 2, the barrier layer 35 is formed on the organic planarization layer 34 to expose the anode electrode 73. The barrier layer 35 brings the organic light-emitting layer 90 into contact with the anode electrode 73.

[0039] The anode electrode 73 connected to the first drain electrode 72 of the driving transistor TFT1 receives a power signal and supplies holes. The anode electrode 73 may be formed of a transparent conductive material such as indium tin oxide (ITO), indium zinc oxide (IZO), and indium tin zinc oxide (ITZO) and connected to the first drain electrode 72 through a pixel contact hole 53.

[0040] The cathode electrode 80 is formed on the organic light-emitting layer 90. The cathode electrode 80 supplies electrons and reflects light emitted from the organic light-emitting layer 90 toward the anode electrode 73. Accordingly, the cathode electrode 80 is formed of aluminum or aluminum alloy having excellent electron transport capability and reflection performance.

[0041] A storage electrode 65 connected to the first gate electrode 61 of the driving transistor TFT1 overlaps the power line 70 with the first gate-insulating layer 31 disposed therebetween, thus forming the storage capacitor Cst. Moreover, as shown in FIG. 3, a groove portion 75 is formed on the power line 70 so that an overlapping area of the storage electrode 65 and the power line 70 is kept the same.

[0042] The groove portion 75 is formed on a lateral side of the power line 70 and, preferably, on a lateral side adjacent to the data line 40. As shown in FIG. 1, the groove portion 75 is recessed toward the inside of the power line 70. The groove portion 75 may be recessed at least 1 to 2 μm toward the inside of the power line 70. Accordingly, the width of an area of the power line 70 overlapping the storage electrode 65 is set to be smaller than that of the power line 70 not overlapping the storage electrode 65.

[0043] FIG. 3 is a plan view showing an area where the storage capacitor in accordance with the first embodiment of the present invention, and FIG. 4 is a cross-sectional view taken along line II - II' of FIG. 3.

[0044] Referring to FIGS. 3 and 4, the storage capacitor Cst is formed by the power line 70 overlapping the storage electrode 65 with the first gate-insulating layer 31 disposed therebetween. The width of the storage electrode 65 is set to be greater than that of the power line 70 by the groove portion 75 formed on the power line 70 in the overlapping area of the storage electrode 65 and the power line 70.

[0045] More specifically, the storage capacitor Cst is formed with a predetermined width W between the right lateral side of the storage electrode 65 and the right lateral side of the power line 70 having the groove portion 75. The width W may be 1 to 2 μm. Accordingly, even if the storage electrode 65 is shifted to the left or right, the capacity of the storage capacitor Cst is the same as the previous state, not shifted. A more detailed description will be given with reference to FIGS. 5A and 5B.

[0046] FIG. 5A is a plan view illustrating an overlapping area of the storage electrode and the power line where the storage electrode is shifted to the left, and FIG. 5B is a plan view illustrating an overlapping area of the storage electrode and the power line where the storage electrode is shifted to the right.

[0047] As shown in FIG. 5A, even if the storage electrode 65 is shifted to the left, the storage electrode 65 formed to protrude more than the lateral side of the groove portion 75 overlaps the power line 70. Accordingly, the overlapping area of the storage electrode 65 and the power line 70 is the same as that where the storage electrode 65 is not shifted as shown in FIG. 3.

[0048] Moreover, the storage electrode 65 is connected to the first gate electrode 61 of the driving transistor TFT1 of FIG. 1. Accordingly, as shown in FIG. 5B, even if the storage electrode 65 is shifted to the right, the first gate electrode 61 overlaps the power line 70 and thus the overlapping area is the same as that where the storage electrode 65 is not shifted.

[0049] FIG. 6 is a plan view of a storage capacitor of an organic light-emitting display panel in accordance with a second embodiment of the present invention.

[0050] The storage capacitor Cst of FIG. 6 is the same as that of FIG. 3, except that the length L1 of the groove portion 76 is greater than that of FIG. 3.

[0051] Referring to FIG. 6, the groove portion 75 may be formed with a length L1 greater than a length L2 between the top and bottom sides of the storage electrode 65. Accordingly, even if the storage electrode 65 is shifted to the top or bottom due to a mask misalignment, the overlapping area of the storage electrode 65 and the power line 70 can be kept the same.

[0052] FIG. 7A is a plan view illustrating an overlapping area of the storage electrode and the power line where the storage electrode is shifted to the top, and FIG. 7B is a plan view illustrating an overlapping area of the storage electrode and the power line where the storage electrode is shifted to the bottom.

[0053] As shown in FIGS. 7A and 7B, even if the storage electrode 65 is shifted to the top or bottom, the overlapping area of the storage electrode 65 and the power line 70 is kept the same. Accordingly, the groove portion 75 formed on the power line 70, the capacity of the storage capacitor Cst formed at each pixel is kept the same, even if at least one of the storage electrode 65 and the power line 70 is shifted to the top, bottom, left or right in a process variation. Moreover, each of a plurality of storage capacitors formed on the organic light-emitting display panels manufactured at different times may have the same capacity.

[0054] Next, a method of manufacturing an organic light-emitting display panel in accordance with the present invention will be described with reference to FIGS. 8A to 14B.

[0055] Referring to FIGS. 8A and 8B, a first semiconductor layer 62 of a driving transistor TFT1 and a first ohmic contact layer 63 are formed on a substrate 10.

[0056] The first semiconductor layer 62 and the first ohmic contact layer 63 are formed of polysilicon in view of the characteristics of the driving transistor TFT1. The process of forming the first semiconductor layer 62 and the first ohmic contact layer 63 will be described in more detail below.

[0057] First, amorphous silicon and impurity-doped amorphous silicon are deposited on the overall surface of the substrate 10 in a uniform thickness. Subsequently, the amorphous silicon is crystallized by laser irradiation or solid phase crystallization using heat and magnetic field. Next, the crystallized silicon layer is patterned by photolithography and etching processes to form the first semiconductor layer 62 and the first ohmic contact layer 63 shown in FIG. 8B.

[0058] Referring to FIGS. 9A to 9C, a first source electrode 71 and a first drain electrode 72 of the driving transistor TFT1 are formed.

[0059] More specifically, a conductive metal is deposited on the overall surface of the substrate 10 by a sputtering method and then patterned by photolithography and etching processes, thus forming the first source electrode 71 and the first drain electrode 72. The first ohmic contact layer 63 not covered but exposed by the first source electrode 71 and the first drain electrode 72 is removed by an etching process to form a channel formed of polysilicon only. A power line 70 is formed simultane-

ously with the formation of the first source electrode 71. A groove portion 75 is formed on an area of the power line 70 overlapping a storage electrode to be formed later.

[0060] The groove portion 75 is formed on a lateral side of the power line 70. Especially, the groove portion 75 is formed on the lateral side of the power line 70 adjacent to a data line 40. Accordingly, it is possible to ensure a left and right margin required when the storage electrode is formed.

[0061] Moreover, as shown in FIG. 9C, the groove portion 75 has a length L1 greater than a length of the storage electrode. Accordingly, it is possible to ensure a misalignment margin by setting the length L1 of the groove portion 75 of the power line 70 greater than the length of the storage electrode such that the storage electrode has the same capacity, even if it is shifted to the top or bottom during the formation thereof.

[0062] Next, a first gate-insulating layer 31 is formed on the overall surface of the substrate 10.

[0063] The first gate-insulating layer 31 is formed by depositing an inorganic insulating material such as silicon oxide (SiOx), silicon nitride (SiNx), or the like on the overall surface of the substrate 10 by a deposition method such as plasma enhanced chemical vapor deposition (PECVD).

[0064] Referring to FIGS. 10A to 10C, a gate line 20, first and second gate electrodes 61 and 21, and the storage electrode 65 are formed on the first gate-insulating layer 31.

[0065] In particular, a conductive metal is deposited on the overall surface of the substrate 10 by a sputtering method and then patterned by photolithography and etching processes, thus forming the gate line 20, the first and second gate electrodes 61 and 21 and the storage electrode 65. The second gate electrode 21 is connected to the gate line 20. The power line 70 overlaps the storage electrode 65 with the first gate-insulating layer 31 disposed therebetween to form a storage capacitor Cst.

[0066] During the formation of the storage electrode 65, an auxiliary storage electrode 66, which extends from the storage electrode 65 to overlap the power line 70, may be further formed.

[0067] As shown in FIGS. 10D and 10E, the auxiliary storage electrode 66 is formed to overlap the power line 70. The width of the auxiliary storage electrode 66 is set to be smaller or greater than that of the power line 70. The auxiliary storage electrode 66 is formed symmetrically with respect to the center of the power line 70 to have a mask misalignment margin for the left and right direction. The auxiliary storage electrode 66 has a width W on both sides thereof the same as the width of the groove portion 75. Accordingly, even if the storage electrode 65 and the auxiliary storage electrode 66 are shifted to the left or right due to a mask misalignment, the area overlapping the power line 70 is kept the same. Moreover, even when the auxiliary storage electrode 66 has a width greater than that of the power line 70, the auxiliary storage electrode 66 may have a margin as wide as the width W of the groove portion 75.

[0068] The width of the auxiliary storage electrode 66 is set to be smaller or larger than that of the power line 70 so that the width W between a lateral side of the auxiliary storage electrode 66 and a lateral side of the power line 70 may be 1 to 2 μm. Where the width of the auxiliary storage electrode 66 is set to be greater than that of the power line 70, the auxiliary storage electrode 66 may be formed to have a size that does not overlap an anode electrode 73 or the adjacent data line 40 to be formed later, even if the auxiliary storage electrode 66 is shifted to the left or right.

[0069] Next, a second gate-insulating layer 32 is deposited on the overall surface of the substrate 10 including the first and second gate electrodes 61 and 21. Since the second gate-insulating layer 32 is formed by the same method as the first gate-insulating layer 31, a description thereof will be omitted.

[0070] As shown in FIGS. 11A and 11B, a second semiconductor layer 22 and a second ohmic contact layer 23 are formed on the substrate 10 including the second gate-insulating layer 32.

[0071] A second semiconductor pattern including the second semiconductor layer 22 and the second ohmic contact layer 23 is formed of amorphous silicon in view of the characteristics of a switching transistor TFT2. That is, amorphous silicon and impurity-doped amorphous silicon are sequentially deposited on the second insulating layer 32 and then patterned by photolithography and etching processes, not subjected to a crystallization process, thus forming the second semiconductor layer 22 and the second ohmic contact layer 23.

[0072] Subsequently, as shown in FIGS. 12A and 12B, a second source electrode 41 and a second drain electrode 42 are formed on the second semiconductor pattern. The data line 40 connected to the second source electrode 41 is formed. Since the process of forming the second source electrode 41, the second drain electrode 42 and the data line 40 is substantially the same as the process of forming the first and second gate electrodes 61 and 21, a description thereof will be omitted.

[0073] Next, as shown in FIGS. 13A and 13B, a passivation layer 33, an organic planarization layer 34, a bridge electrode 55, and an anode electrode 73 are formed.

[0074] The passivation layer 33 is formed by depositing an inorganic insulating layer such as silicon oxide (SiOx) or silicon nitride (SiNx) on the overall surface of the substrate 10. Then, the organic planarization layer 34 is formed on the passivation layer 33. The organic planarization layer 34 is formed by coating an organic material on the overall surface of the passivation layer 33 by a spin coating method, and curing the coated organic material. Subsequently, the organic planarization layer 34 is patterned to form first and second contact holes 51 and 52 and a pixel contact hole 53. The first contact hole 51 is formed to penetrate the organic planarization layer 34 and the passivation layer 33, thus exposing a portion

of the second drain electrode 42. The second contact hole 52 is formed to penetrate the organic planarization layer 34, the passivation layer 33, and the second gate-insulating layer 32, thus exposing a portion of the first gate electrode 61. The pixel contact hole 53 is formed to penetrate the organic planarization layer 34, the passivation layer 33, and the first and second gate-insulating layers 31 and 32 sequentially, thus exposing a portion of the first drain electrode 72.

[0075] A color filter 95 may be further formed during the formation of the organic planarization layer 34 as shown in FIG. 13C.

[0076] Any one of red, green, and color filters 95 is formed at each pixel area prior to the formation of the organic planarization layer 34 and then the organic planarization layer 34 is formed on the color filter 95. Here, the color filter 95 may be formed of an organic material displaying color.

[0077] The organic planarization layer 34 may comprise the color filter. That is, it is possible to form the organic planarization layer 34 at each pixel area as the color filter displaying color.

[0078] Next, the bridge electrode 55 and the anode electrode 73 are formed of a transparent conductive layer. The bridge electrode 55 and the anode electrode 73 are formed in such a manner that a transparent conductive material such as indium tin oxide (ITO), indium zinc oxide (IZO), and indium tin zinc oxide (ITZO) is deposited on the organic planarization layer 34, on which the first and second contact holes 51 and 52 and the pixel contact hole 53 are formed, by a sputtering method, and patterned by photolithography and etching processes. The bridge electrode 55 connects the first gate electrode 61 to the second drain electrode 42. The anode electrode 73 is connected to the first drain electrode 72 of the driving transistor TFT1.

[0079] Referring to FIGS. 14A and 14B, a barrier layer 35, an organic light-emitting layer 90, and a cathode electrode 80 are formed on the substrate 10 including the bridge electrode 55 and the anode electrode 73.

[0080] At least one material of acrylic-based resin, benzocyclobutene (BCB), and polyimide is deposited on the overall surface on the substrate 10 including the bridge electrode 55 and the anode electrode 73. Subsequently, the anode electrode 73 is exposed by photolithography and etching processes. Accordingly, a step height is formed between an area where the anode electrode 73 is formed and the other area which is not etched. Next, the organic light-emitting layer 90 is formed on the anode electrode 73 in the barrier layer 35, and the cathode electrode 80 is formed on the barrier layer 35 and the organic light-emitting layer 90.

[0081] As described above, the power line and the storage electrode which form the storage capacitor are formed taking into account variations in processing. It is thus possible to form the storage capacitor at each pixel area of the organic light-emitting panel having the same capacity, even if mask misalignment should occur during the manufacturing process.

[0082] Although the present invention has been described with reference to certain exemplary embodiments thereof, it will be understood by those skilled in the art that a variety of modifications and variations may be made to the present invention without departing from the scope of the present invention defined in the appended claims.

Claims

1. An organic light-emitting display panel comprising:

a gate line (20) and a data line (40) formed to cross each other on a substrate (10);
an organic light-emitting diode (100) formed in a pixel area defined by the intersection of the gate line (20) and the data line (40);
a power line (70) formed parallel to the data line (40) for supplying an electric current to the organic light-emitting diode (100);
a switching transistor (TFT2) provided at the intersection of the gate line (20) and the data line (40);
a driving transistor (TFT1) connected to the switching transistor (TFT2) and the power line (70) to control the current supplied from the power line (70); and
a storage capacitor (Cst) composed of a storage electrode (65) overlapping the power line (70) with a first gate-insulating layer (31) disposed therebetween,
wherein the storage capacitor (Cst) includes a groove portion (75) formed on a lateral side of the power line (70) in an overlapping area of the power line (70) and the storage electrode (65), wherein the groove portion (75) is recessed toward the inside of the power line (70),
characterized in that
the width of the storage electrode (65) is greater than that of the power line (70) by the groove portion (75) in the overlapping area of the storage electrode (65) and the power line (70), and
in that the groove portion (75) has a length at least equal to or greater than the length of the storage electrode (65) in a direction parallel to the data line (40), such that the overlapping area between the power line (70) and the storage electrode (65) is kept constant.

2. The organic light-emitting display panel of claim 1, wherein the groove portion (75) is formed on a lateral side adjacent to the data line (40).

3. The organic light-emitting display panel of claim 1, wherein the driving transistor (TFT1) comprises:

a first semiconductor pattern (62, 63) formed of polysilicon on the substrate (10);
a first source electrode (71) formed on the first semiconductor pattern (62, 63) and connected to the power line (70);
a first drain electrode (72) formed on the first semiconductor pattern (62, 63) to face the first source electrode (71) and connected to the organic light-emitting diode (100);
first gate-insulating layer (31) formed on the first source electrode (71) and the first drain electrode (72); and
a first gate electrode (61) formed on the first gate-insulating layer (31) to overlap the first semiconductor pattern (62, 63).

4. The organic light-emitting display panel of claim 3, wherein the first gate electrode (61) is electrically connected to the storage electrode (65).

5. The organic light-emitting display panel of claim 1, wherein the switching transistor (TFT2) comprises:

a second gate electrode (21) formed on the first gate-insulating layer (31);
a second gate-insulating layer (32) formed on the second gate electrode (21);
a second semiconductor pattern (22, 23) formed of amorphous silicon on the substrate (10); and
a second source electrode (41) and a second drain electrode (42) formed on the second semiconductor pattern (22, 23) to face each other.

6. The organic light-emitting display panel of claim 5, further comprising a bridge electrode (55) connecting the first gate electrode (61) to the second drain electrode (42).

7. A method of manufacturing an organic light-emitting display panel in accordance with claim 1, the method comprising:

forming a gate line (20) and a data line (40) on a substrate (10), the gate line (20) and the data line (40) crossing each other with a second gate-insulating layer (32) disposed therebetween;
forming an organic light-emitting diode (100) in a pixel area defined by the intersection of the gate line (20) and the data line (40);
forming a switching transistor (TFT2) at the intersection of the gate line (20) and the data line (40);
forming a driving transistor (TFT1) connected to the switching transistor (TFT2); and
forming a power line (70) parallel to the data line (40);
forming a storage electrode (65) overlapping the power line (70) with the first gate-insulating layer (31) disposed therebetween to form a storage capacitor (Cst) and including a projecting portion with respect to a lateral side of the power line (70),
wherein forming the power line (70) parallel to the data line (40) further comprises forming a groove portion (75) on a lateral side of the power line (70) in an overlapping area of the storage electrode (65) and the power line (70), wherein the groove portion (75) is recessed toward the inside of the power line (70),
characterized by
forming the storage electrode (65) with a width which is greater than that of the power line (70) by the groove portion (75) in the overlapping area of the storage electrode (65) and the power line (70) and forming the groove portion (75) to have a length at least equal to or greater than a length of the storage electrode (65) in a direction parallel to the data line (40), such that the overlapping area between the power line (70) and the storage electrode (65) is kept constant.

8. The method of claim 7, wherein forming the power line (70) parallel to the data line (40) further comprises forming the groove portion (75) on a lateral side adjacent to the data line (40).

9. The method of claim 8, wherein forming the switching transistor (TFT2) and the driving transistor (TFT1) comprises:

forming a first semiconductor pattern (62, 63) with polysilicon on the substrate (10) and a first gate-insulating layer;
forming a first source electrode (71) on the first semiconductor pattern (62, 63) and connected to the power line (70), and a first drain electrode (72) facing the first source electrode (70);
forming a first gate-insulating layer (31) on the first source electrode (71) and the first drain electrode (72);
forming a first gate electrode (61) on the first gate-insulating layer (31) to overlap the first semiconductor pattern (62, 63), and a second gate electrode (21) simultaneously with the first gate electrode (61); and
forming a second gate-insulating layer (32), a second semiconductor pattern (22, 23), a second source electrode (241, and a second drain electrode (42).

Patentansprüche

1. Organische lichtemittierende Anzeigetafel, umfassend:

eine Gateleitung (20) und eine Datenleitung (40), die derart ausgebildet sind, dass sie einander auf einem Substrat (10) kreuzen;
eine organische lichtemittierende Diode (100), die in einem Pixelbereich ausgebildet ist, der durch den Schnittpunkt der Gateleitung (20) und der Datenleitung (40) definiert ist;
eine Stromleitung (70), die parallel zu der Datenleitung (40) ausgebildet ist, um der organischen lichtemittierenden Diode (100) einen elektrischen Strom zuzuführen;
einen Schalttransistor (TFT2), der an dem Schnittpunkt der Gateleitung (20) und der Datenleitung (40) bereitgestellt ist;
einen Treibertransistor (TFT1), der mit dem Schalttransistor (TFT2) und der Stromleitung (70) verbunden ist, um den von der Stromleitung (70) zugeführten Strom zu steuern; und
einen Speicherkondensator (Cst), der aus einer Speicherelektrode (65) besteht, die die Stromleitung (70) überlappt, wobei eine erste Gate-Isolierschicht (31) dazwischen angeordnet ist,
wobei der Speicherkondensator (Cst) einen Rillenabschnitt (75) beinhaltet, der an einer lateralen Seite der Stromleitung (70) in einem überlappenden Bereich der Stromleitung (70) und der Speicherelektrode (65) ausgebildet ist, wobei der Rillenabschnitt (75) in Richtung des Inneren der Stromleitung (70) zurückgesetzt ist,
dadurch gekennzeichnet, dass
die Breite der Speicherelektrode (65) in dem überlappenden Bereich der Speicherelektrode (65) und der Stromleitung (70) um den Rillenabschnitt (75) größer ist als die der Stromleitung (70), und dadurch, dass der Rillenabschnitt (75) eine Länge aufweist, die in einer Richtung parallel zu der Datenleitung (40) mindestens gleich der oder größer als die Länge der Speicherelektrode (65) ist, sodass der überlappende Bereich zwischen der Stromleitung (70) und der Speicherelektrode (65) konstant gehalten wird.

2. Organische lichtemittierende Anzeigetafel nach Anspruch 1, wobei der Rillenabschnitt (75) an einer lateralen Seite benachbart zu der Datenleitung (40) ausgebildet ist.

3. Organische lichtemittierende Anzeigetafel nach Anspruch 1, wobei der Treibertransistor (TFT1) Folgendes umfasst:

ein erstes Halbleitermuster (62, 63), das aus Polysilicium auf dem Substrat (10) ausgebildet ist;
eine erste Source-Elektrode (71), die auf dem ersten Halbleitermuster (62, 63) ausgebildet ist und mit der Stromleitung (70) verbunden ist;
eine erste Drain-Elektrode (72), die derart auf dem ersten Halbleitermuster (62, 63) ausgebildet ist, dass sie der Source-Elektrode (71) zugewandt ist, und mit der organischen lichtemittierenden Diode (100) verbunden ist;
die erste Gate-Isolierschicht (31), die auf der ersten Source-Elektrode (71) und der ersten Drain-Elektrode (72) ausgebildet ist; und
eine erste Gate-Elektrode (61), die derart auf der ersten Gate-Isolierschicht (31) ausgebildet ist, dass sie das erste Halbleitermuster (62, 63) überlappt.

4. Organische lichtemittierende Anzeigetafel nach Anspruch 3, wobei die erste Gate-Elektrode (61) elektrisch mit der Speicherelektrode (65) verbunden ist.

5. Organische lichtemittierende Anzeigetafel nach Anspruch 1, wobei der Schalttransistor (TFT2) Folgendes umfasst:

eine zweite Gate-Elektrode (21), die auf der ersten Gate-Isolierschicht (31) ausgebildet ist;
eine zweite Gate-Isolierschicht (32), die auf der zweiten Gate-Elektrode (21) ausgebildet ist;
ein zweites Halbleitermuster (22, 23), das aus amorphem Silicium auf dem Substrat (10) ausgebildet ist; und
eine zweite Source-Elektrode (41) und eine zweite Drain-Elektrode (42), die derart auf dem zweiten Halbleitermuster (22, 23) ausgebildet sind, dass sie einander zugewandt sind.

6. Organische lichtemittierende Anzeigetafel nach Anspruch 5, ferner umfassend eine Brückenelektrode (55), die die erste Gate-Elektrode (61) mit der zweiten Drain-Elektrode (42) verbindet.

7. Verfahren zum Herstellen einer organischen lichtemittierenden Anzeigetafel nach Anspruch 1, wobei das Verfahren Folgendes umfasst:

Ausbilden einer Gateleitung (20) und einer Datenleitung (40) auf einem Substrat (10), wobei die Gateleitung (20) und die Datenleitung (40) einander kreuzen, wobei eine zweite Gate-Isolierschicht (32) dazwischen angeordnet ist;
Ausbilden einer organischen lichtemittierenden Diode (100) in einem Pixelbereich, der durch den Schnittpunkt der Gateleitung (20) und der Datenleitung (40) definiert ist;
Ausbilden eines Schalttransistors (TFT2) an dem Schnittpunkt der Gateleitung (20) und der Datenleitung (40);
Ausbilden eines Treibertransistors (TFT1), der mit dem Schalttransistor (TFT2) verbunden ist; und
Ausbilden einer Stromleitung (70) parallel zu der Datenleitung (40);
Ausbilden einer Speicherelektrode (65), die die

Stromleitung (70) überlappt, wobei die erste Gate-Isolierschicht (31) dazwischen angeordnet ist, um einen Speicherkondensator (Cst) auszubilden, und einen hervorstehenden Abschnitt in Bezug auf eine laterale Seite der Stromleitung (70) beinhaltet,
wobei das Ausbilden der Stromleitung (70) parallel zu der Datenleitung (40) ferner Ausbilden eines Rillenabschnitts (75) an einer lateralen Seite der Stromleitung (70) in einem überlappenden Bereich der Speicherelektrode (65) und der Stromleitung (70) beinhaltet, wobei der Rillenabschnitt (75) in Richtung des Inneren der Stromleitung (70) zurückgesetzt ist,
gekennzeichnet durch
Ausbilden der Speicherelektrode (65) mit einer Breite, die in dem überlappenden Bereich der Speicherelektrode (65) und der Stromleitung (70) um den Rillenabschnitt (75) größer ist als die der Stromleitung (70), und Ausbilden des Rillenabschnitts (75) derart, dass er eine Länge aufweist, die in einer Richtung parallel zu der Datenleitung (40) mindestens gleich der oder größer als eine Länge der Speicherelektrode (65) ist, sodass der überlappende Bereich zwischen der Stromleitung (70) und der Speicherelektrode (65) konstant gehalten wird.

8. Verfahren nach Anspruch 7, wobei das Ausbilden der Stromleitung (70) parallel zu der Datenleitung (40) ferner Ausbilden des Rillenabschnitts (75) an einer lateralen Seite benachbart zu der Datenleitung (40) umfasst.

9. Verfahren nach Anspruch 8, wobei das Ausbilden des Schalttransistors (TFT2) und des Treibertransistors (TFT1) Folgendes umfasst:

Ausbilden eines ersten Halbleitermusters (62, 63) mit Polysilicium auf dem Substrat (10) und einer ersten Gate-Isolierschicht;
Ausbilden einer ersten Source-Elektrode (71) auf dem ersten Halbleitermuster (62, 63) und verbunden mit der Stromleitung (70) und einer ersten Drain-Elektrode (72), die der ersten Source-Elektrode (70) zugewandt ist;
Ausbilden einer ersten Gate-Isolierschicht (31) auf der ersten Source-Elektrode (71) und der ersten Drain-Elektrode (72);
Ausbilden einer ersten Gate-Elektrode (61) auf der ersten Gate-Isolierschicht (31) derart, dass sie das erste Halbleitermuster (62, 63) überlappt, und einer zweiten Gate-Elektrode (21) gleichzeitig mit der ersten Gate-Elektrode (61); und
Ausbilden einer zweiten Gate-Isolierschicht (32), eines zweiten Halbleitermusters (22, 23), einer zweiten Source-Elektrode (41) und einer zweiten Drain-Elektrode (42).

Revendications

1. Panneau d'affichage électroluminescent organique, comprenant :

une ligne de grille (20) et une ligne de données (40) formées de façon à se croiser sur un substrat (10) ;
une diode électroluminescente organique (100) formée dans une zone de pixel définie par l'intersection de la ligne de grille (20) et de la ligne de données (40) ;
une ligne d'alimentation (70) formée parallèlement à la ligne de données (40) pour fournir un courant électrique à la diode électroluminescente organique (100) ;
un transistor de commutation (TFT2) prévu à l'intersection de la ligne de grille (20) et de la ligne de données (40) ;
un transistor de commande (TFT1) connecté au transistor de commutation (TFT2) et à la ligne d'alimentation (70) pour commander le courant fourni par la ligne d'alimentation (70) ; et
un condensateur de stockage (Cst) composé d'une électrode de stockage (65) chevauchant la ligne d'alimentation (70) avec une première couche isolante de grille (31) disposée entre elles,
dans lequel le condensateur de stockage (Cst) inclut une partie rainure (75) formée sur un côté latéral de la ligne d'alimentation (70) dans une zone de chevauchement de la ligne d'alimentation (70) et de l'électrode de stockage (65), la partie rainure (75) étant en retrait vers l'intérieur de la ligne d'alimentation (70),
caractérisé en ce que
la largeur de l'électrode de stockage (65) est supérieure à celle de la ligne d'alimentation (70) de la partie rainure (75) dans la zone de chevauchement de l'électrode de stockage (65) et de la ligne d'alimentation (70), et **en ce que** la partie rainure (75) a une longueur au moins égale ou supérieure à la longueur de l'électrode de stockage (65) dans une direction parallèle à la ligne de données (40), de sorte que la zone de chevauchement entre la ligne d'alimentation (70) et de l'électrode de stockage (65) est maintenue constante.

2. Panneau d'affichage électroluminescent organique selon la revendication 1, dans lequel la partie rainure (75) est formée sur un côté latéral adjacent à la ligne de données (40).

3. Panneau d'affichage électroluminescent organique

selon la revendication 1, dans lequel le transistor de commande (TFT1) comprend :

un premier motif semi-conducteur (62, 63) formé de polysilicium sur le substrat (10) ;
une première électrode de source (71) formée sur le premier motif semi-conducteur (62, 63) et connectée à la ligne d'alimentation (70) ;
une première électrode de drain (72) formée sur le premier motif semi-conducteur (62, 63) de façon à faire face à la première électrode de source (71) et connectée à la diode électroluminescente organique (100) ;
la première couche isolante de grille (31) formée sur la première électrode de source (71) et la première électrode de drain (72) ; et
une première électrode de grille (61) formée sur la première couche isolante de grille (31) de façon à chevaucher le premier motif semi-conducteur (62, 63).

4. Panneau d'affichage électroluminescent organique selon la revendication 3, dans lequel la première électrode de grille (61) est connectée électriquement à l'électrode de stockage (65).

5. Panneau d'affichage électroluminescent organique selon la revendication 1, dans lequel le transistor de commutation (TFT2) comprend :

une seconde électrode de grille (21) formée sur la première couche isolante de grille (31) ;
une seconde couche isolante de grille (32) formée sur la seconde électrode de grille (21) ;
un second motif semi-conducteur (22, 23) formé de silicium amorphe sur le substrat (10) ; et
une seconde électrode de source (41) et une seconde électrode de drain (42) formées sur le second motif semi-conducteur (22, 23) de façon à se faire face.

6. Panneau d'affichage électroluminescent organique selon la revendication 5, comprenant en outre une électrode de pont (55) connectant la première électrode de grille (61) à la seconde électrode de drain (42).

7. Procédé de fabrication d'un panneau d'affichage électroluminescent organique selon la revendication 1, lequel procédé consiste à :

former une ligne de grille (20) et une ligne de données (40) sur un substrat (10), la ligne de grille (20) et la ligne de données (40) se croisant avec une seconde couche isolante de grille (32) disposée entre elles ;
former une diode électroluminescente organique (100) dans une zone de pixel définie par l'intersection de la ligne de grille (20) et de la ligne de données (40) ;
former un transistor de commutation (TFT2) à l'intersection de la ligne de grille (20) et de la ligne de données (40) ;
former un transistor de commande (TFT1) connecté au transistor de commutation (TFT2) ; et
former une ligne d'alimentation (70) parallèle à la ligne de données (40) ;
former une électrode de stockage (65) chevauchant la ligne d'alimentation (70) avec la première couche isolante de grille (31) disposée entre elles pour former un condensateur de stockage (Cst) et incluant une partie en saillie par rapport à un côté latéral de la ligne d'alimentation (70),
dans lequel former la ligne d'alimentation (70) parallèle à la ligne de données (40) consiste en outre à former une partie rainure (75) sur un côté latéral de la ligne d'alimentation (70) dans une zone de chevauchement de l'électrode de stockage (65) et la ligne d'alimentation (70), la partie rainure (75) étant en retrait vers l'intérieur de la ligne d'alimentation (70),
caractérisé par les étapes consistant à
former l'électrode de stockage (65) avec une largeur qui est supérieure à celle de la ligne d'alimentation (70) de la partie rainure (75) dans la zone de chevauchement de l'électrode de stockage (65) et de la ligne d'alimentation (70), et à former la partie rainure (75) de façon qu'elle ait une longueur au moins égale ou supérieure à une longueur de l'électrode de stockage (65) dans une direction parallèle à la ligne de données (40), de sorte que la zone de chevauchement entre la ligne d'alimentation (70) et de l'électrode de stockage (65) est maintenue constante.

8. Procédé selon la revendication 7, dans lequel former la ligne d'alimentation (70) parallèle à la ligne de données (40) consiste en outre à former une partie rainure (75) sur un côté latéral adjacent à la ligne de données (40).

9. Procédé selon la revendication 8, dans lequel former le transistor de commutation (TFT2) et le transistor de commande (TFT1) consiste à :

former un premier motif semi-conducteur (62, 63) avec du polysilicium sur le substrat (10) et une première couche isolante de grille ;
former une première électrode de source (71) sur le premier motif semi-conducteur (62, 63) et connectée à la ligne d'alimentation (70), et une première électrode de drain (72) faisant face à la première électrode de source (70) ;
former une première couche isolante de grille

(31) sur la première électrode de source (71) et la première électrode de drain (72) ;
former une première électrode de grille (61) sur la première couche isolante de grille (31) de façon à chevaucher le premier motif semi-conducteur (62, 63), et une seconde électrode de grille (21) simultanément à la première électrode de grille (61) ; et
former une seconde couche isolante de grille (32), un second motif semi-conducteur (22, 23), une seconde électrode de source (41) et une seconde électrode de drain (42).

FIG. 1

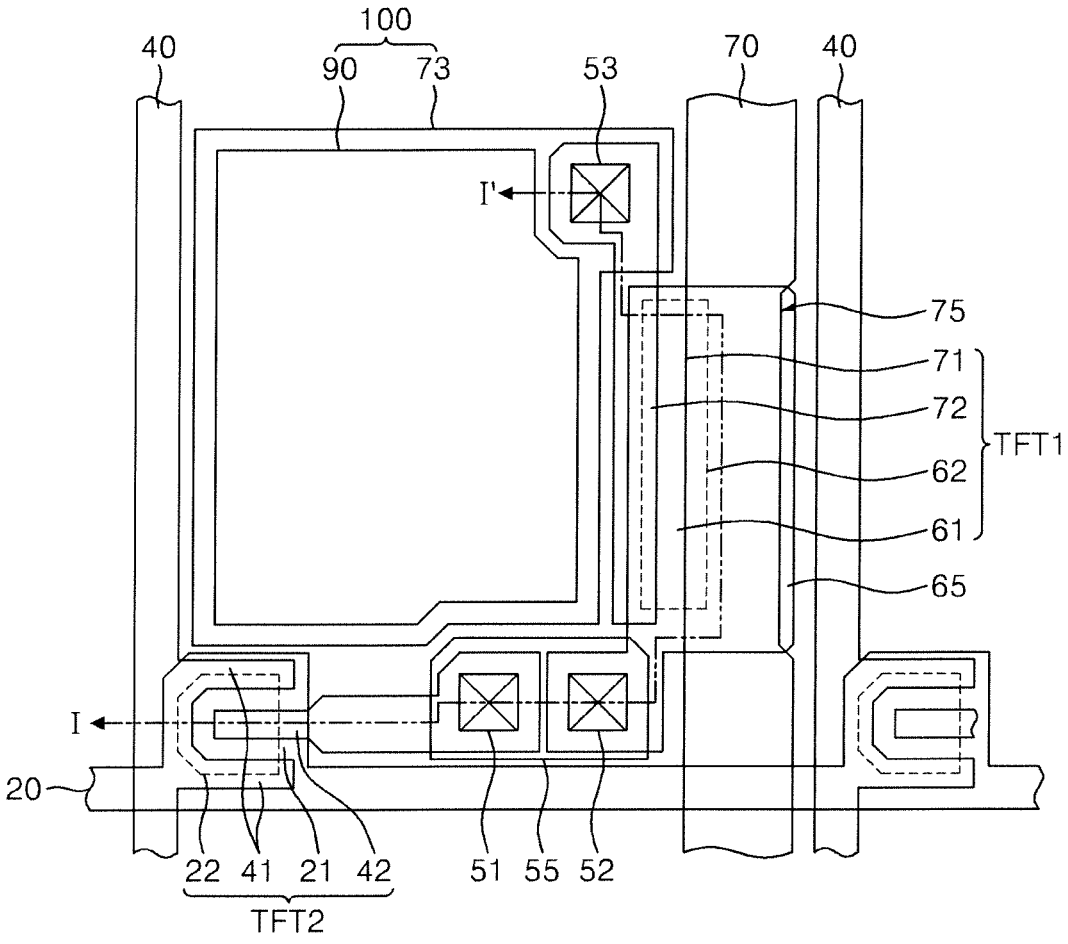

100
40
90
73
53
70
40
I'
75
71
72
TFT1
62
61
65
I
20
22
41
21
42
51
55
52
TFT2

FIG. 2

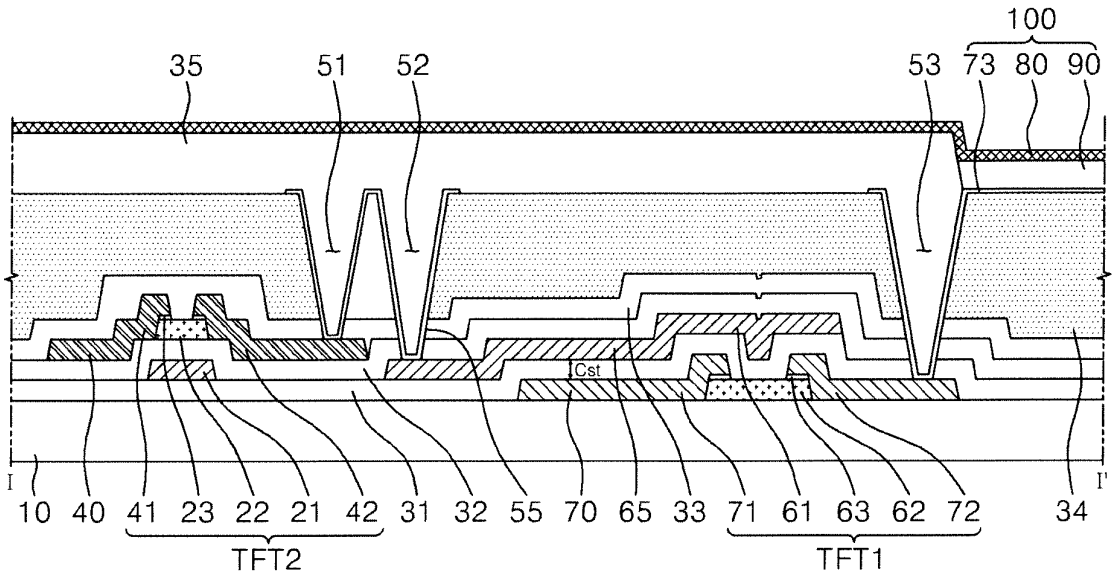

100
35
51
52
53
73
80
90
Cst
I
I'
10
40
41
23
22
21
42
31
32
55
70
65
33
71
61
63
62
72
34
TFT2
TFT1

FIG. 3

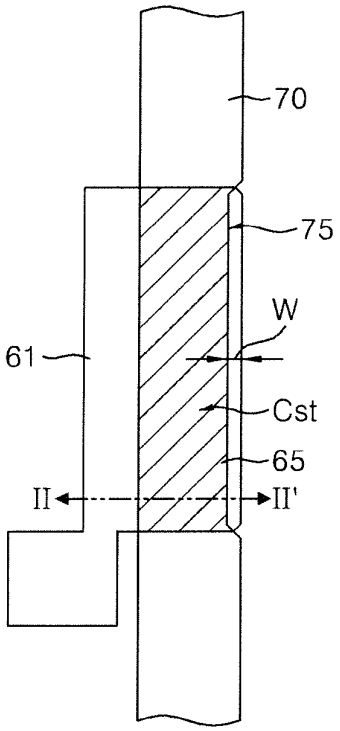

70
75
W
61
Cst
65
II
II'

FIG. 4

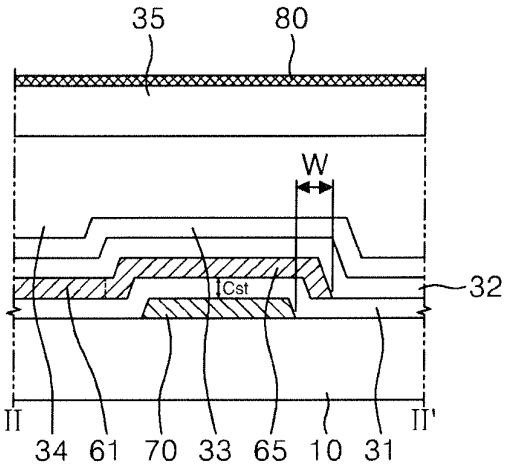


FIG. 5A

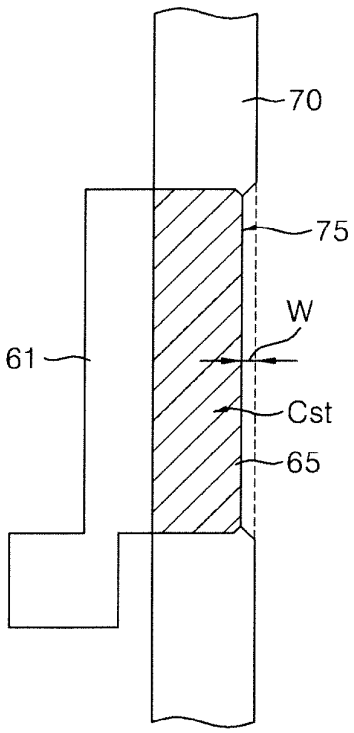


FIG. 5B

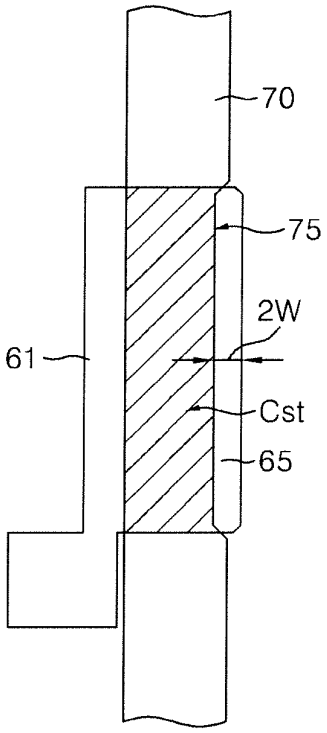


FIG. 6

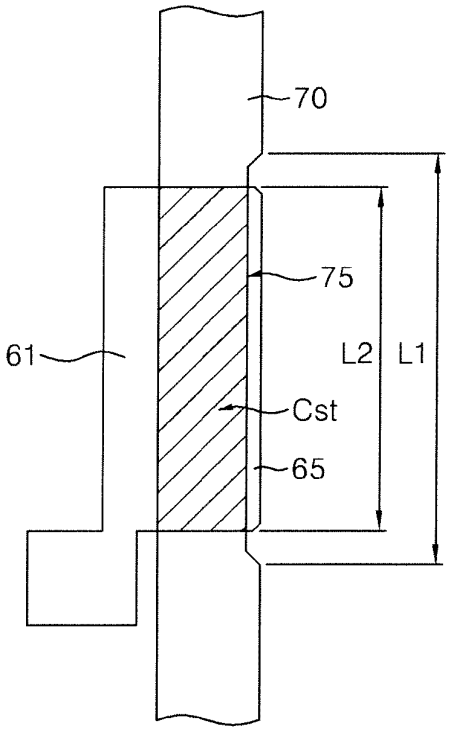


FIG. 7A

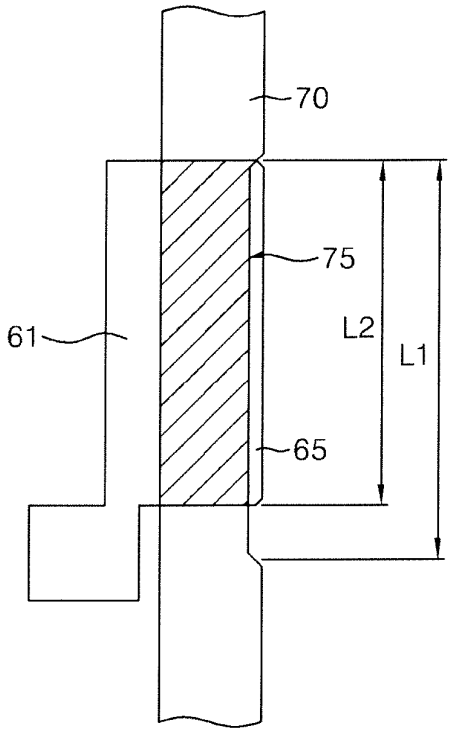


FIG. 7B

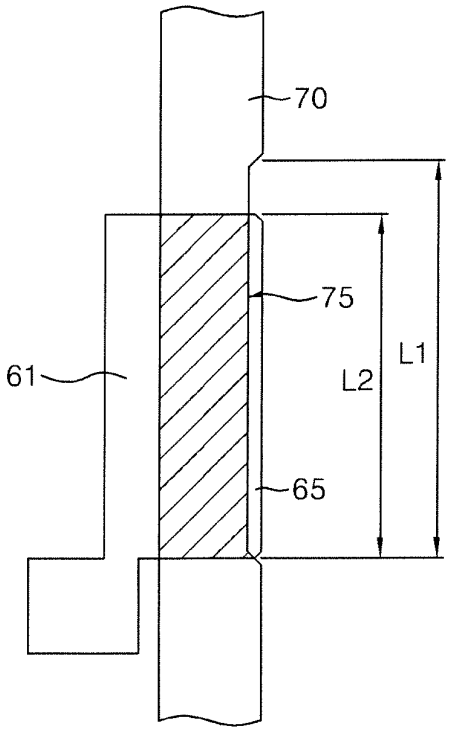


FIG. 8 A

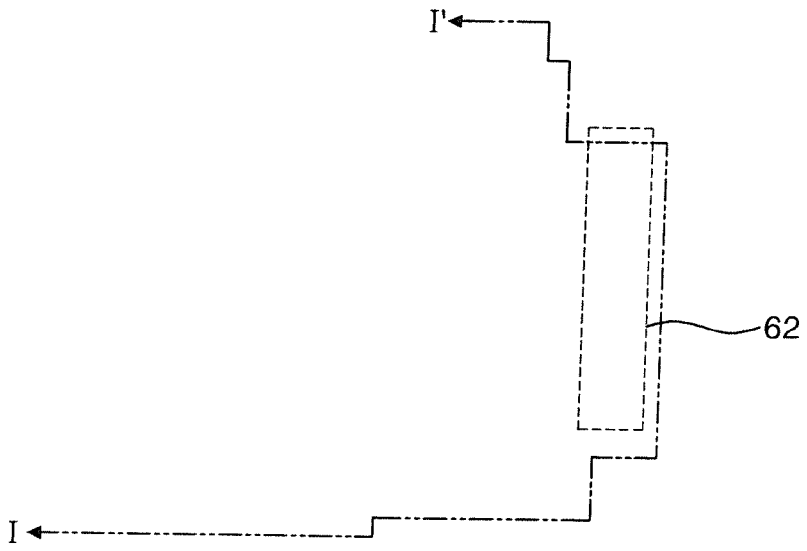


FIG. 8 B

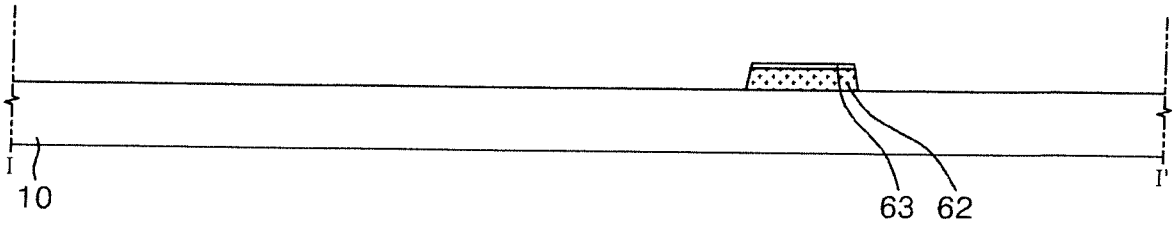


FIG. 9 A

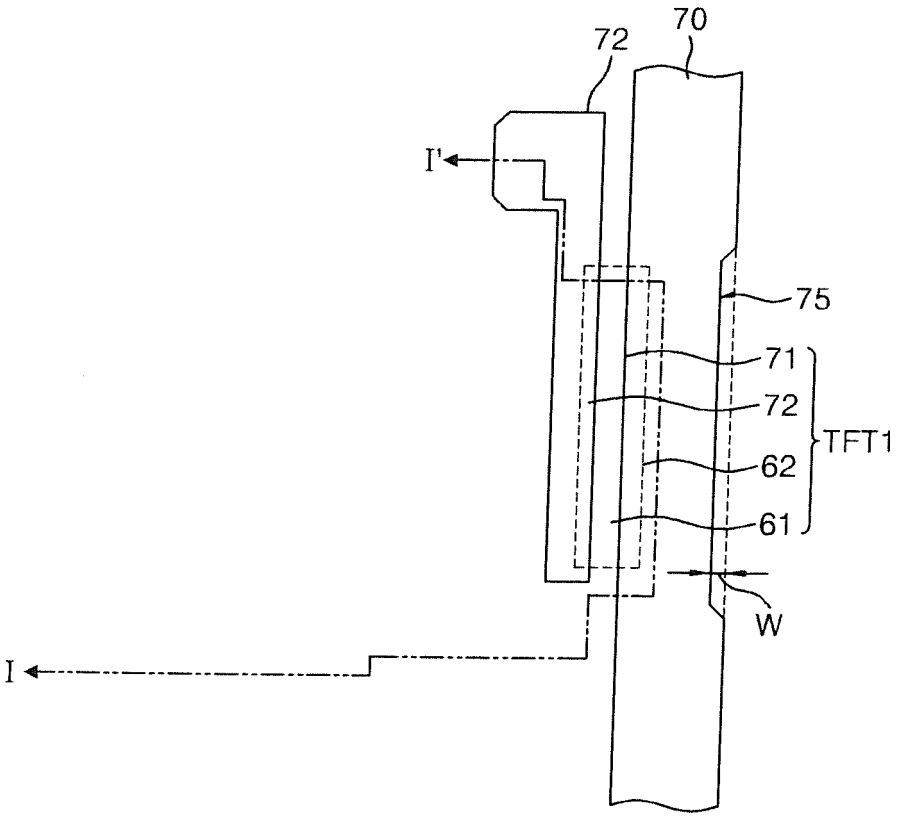


FIG. 9 B

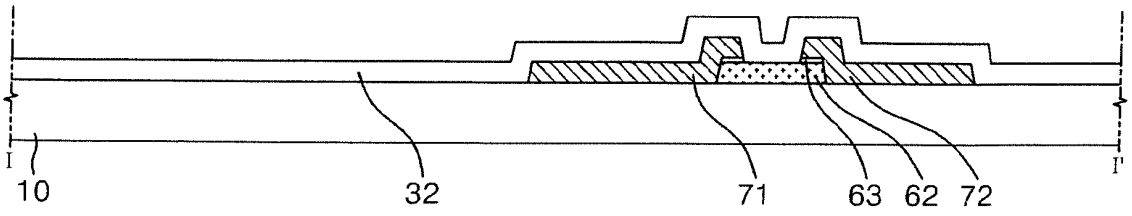


FIG. 9 C

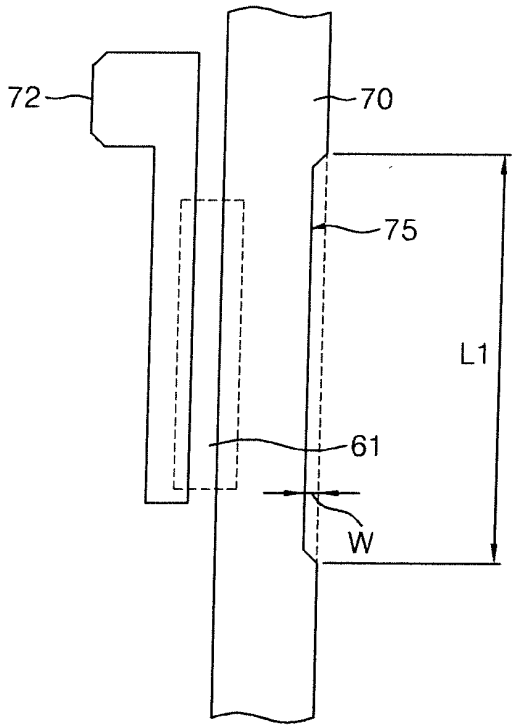


FIG. 10A

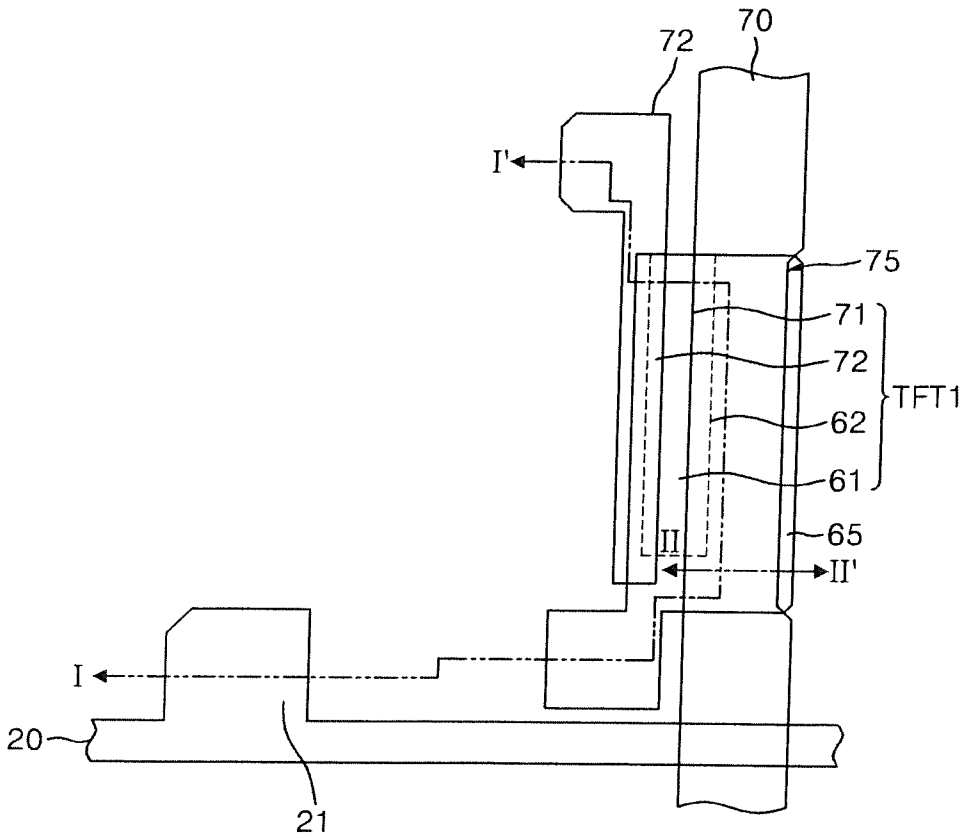


FIG .10B

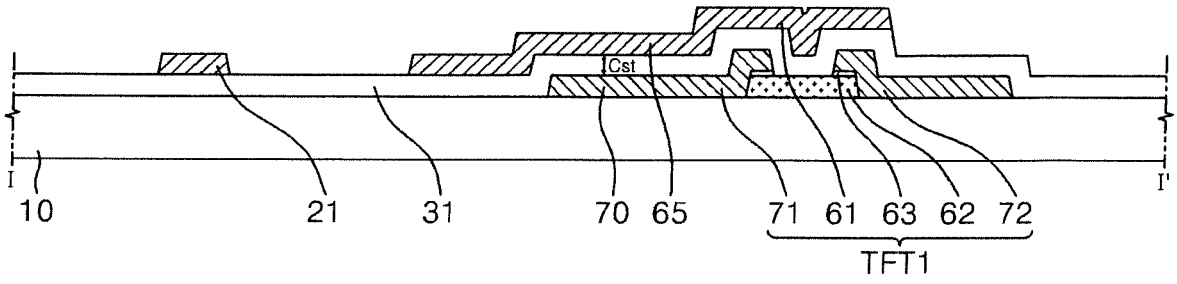


FIG .10C

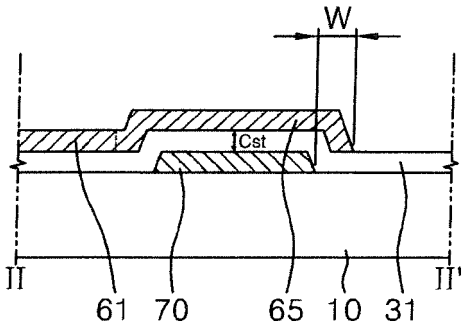


FIG. 10D

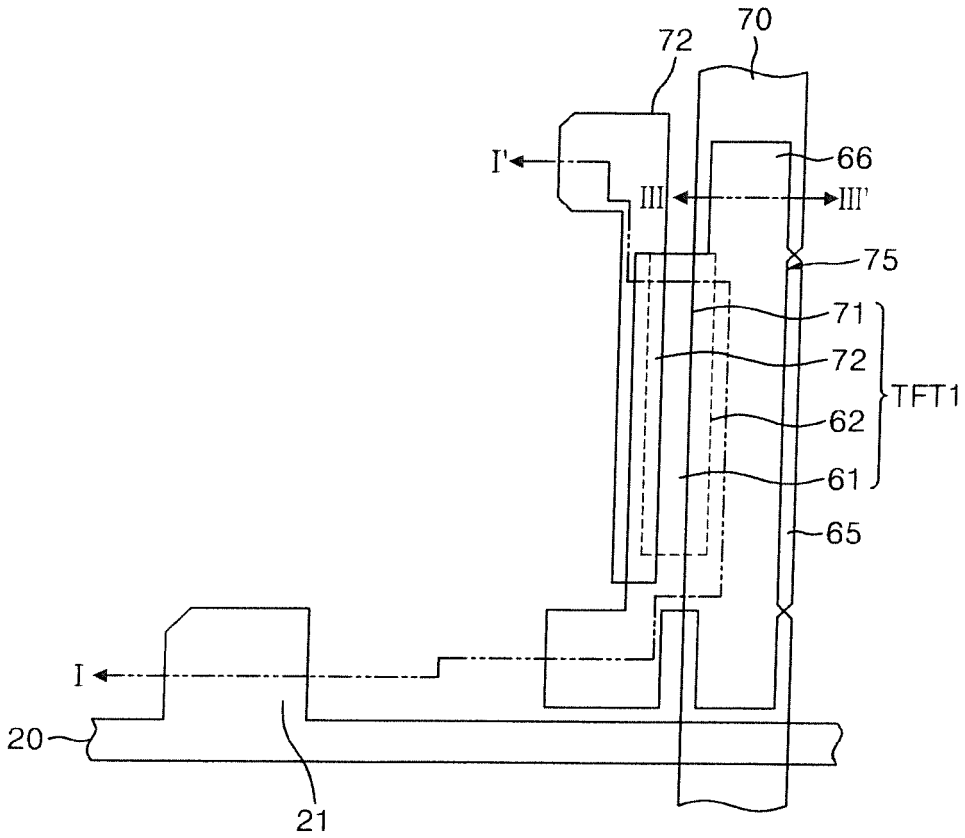


FIG. 10 E

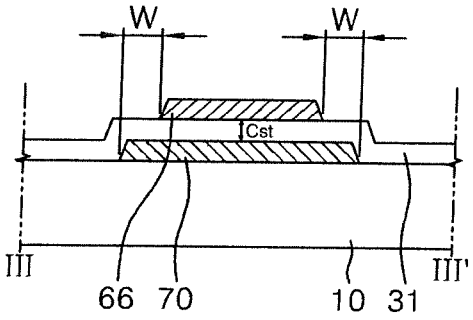


FIG. 11 A

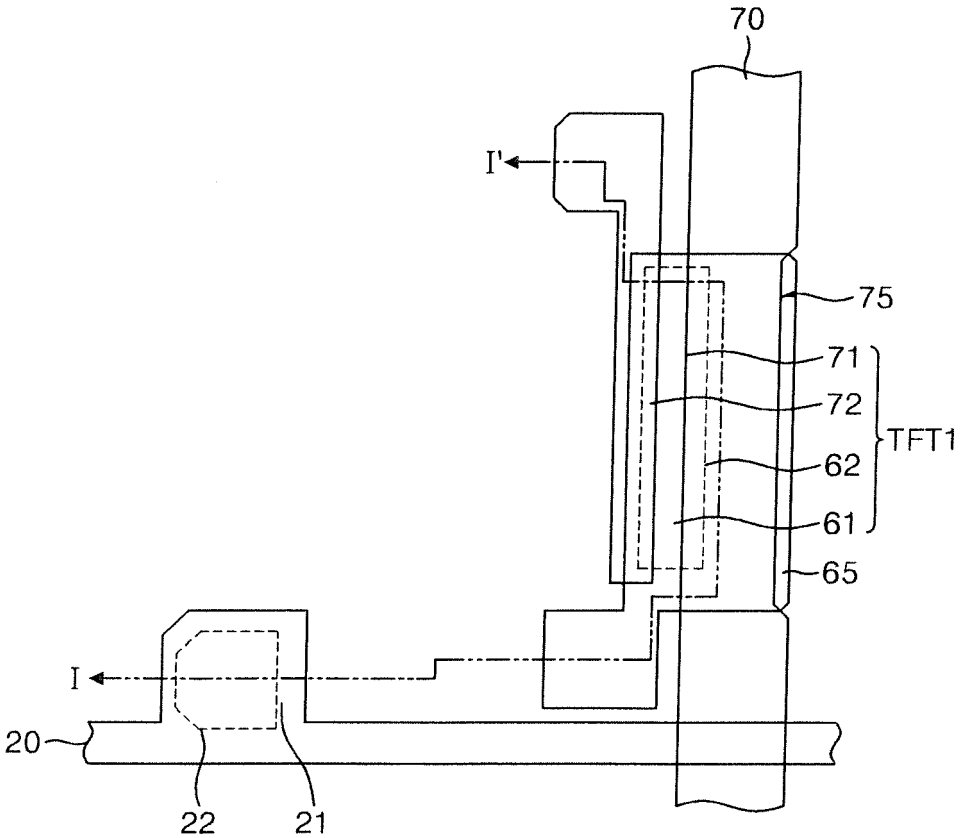


FIG. 11 B

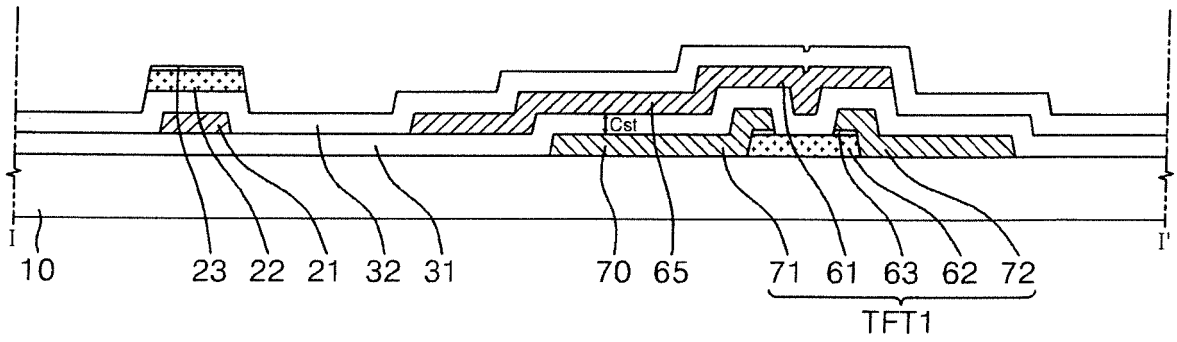


FIG. 12A

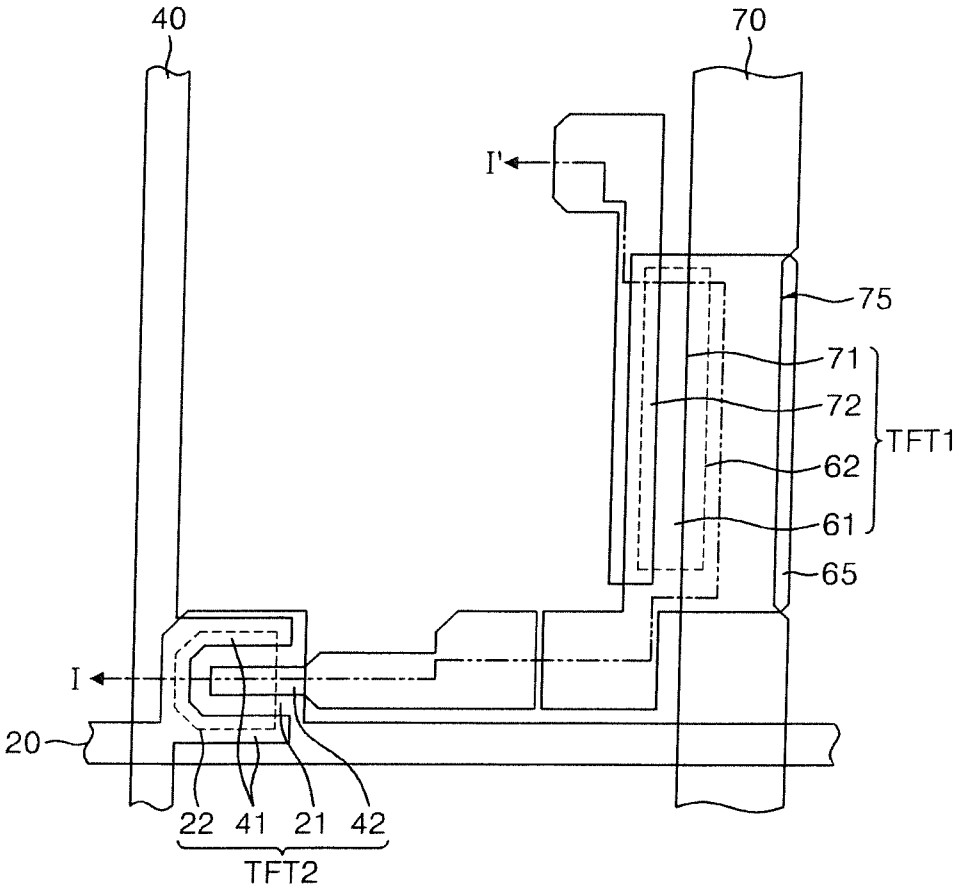


FIG. 12B

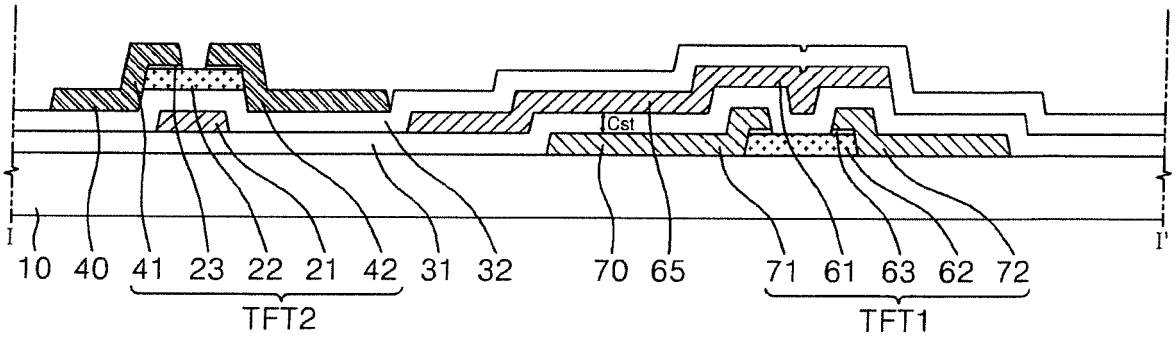


FIG. 13A

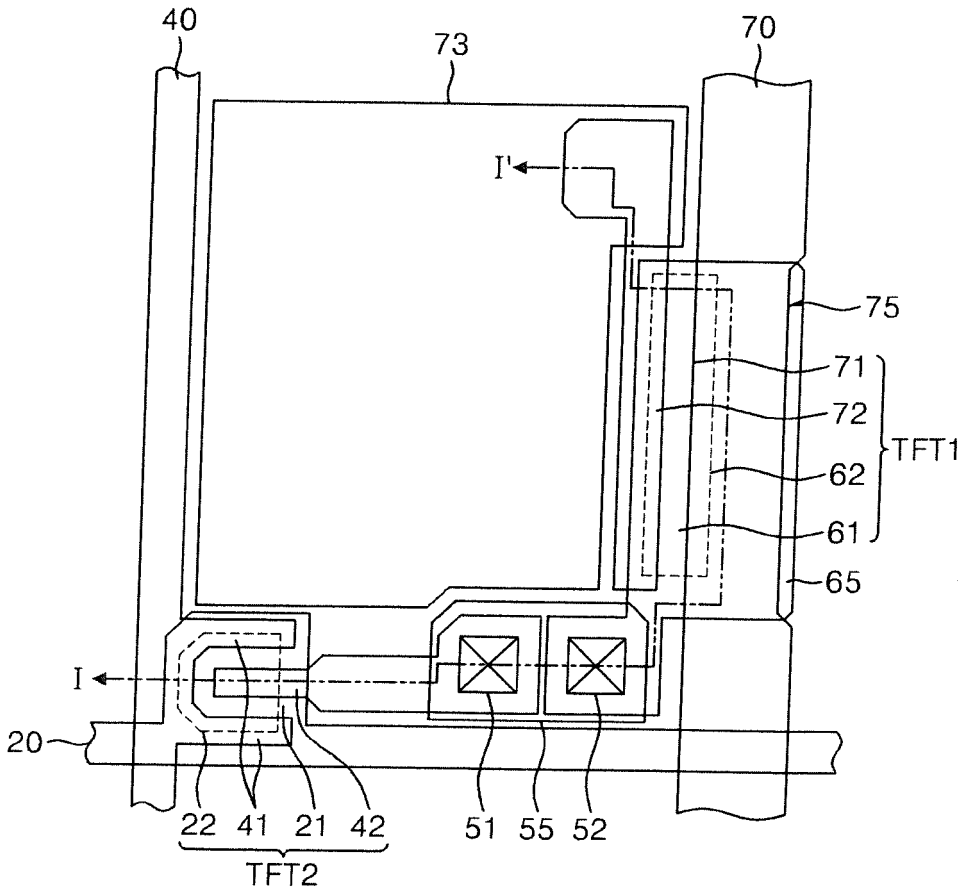


FIG. 13 B

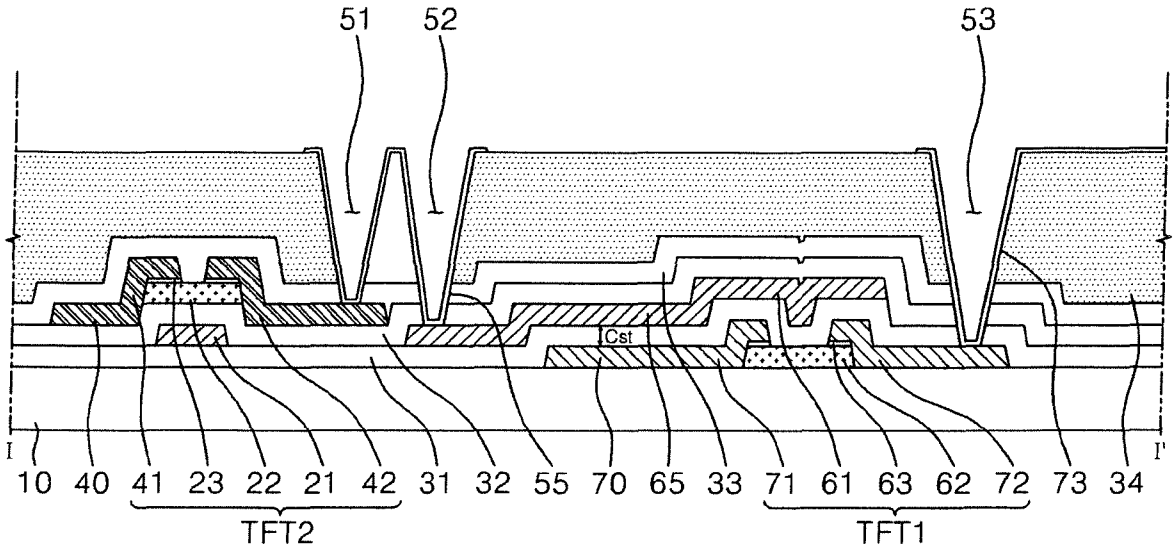


FIG. 13.C

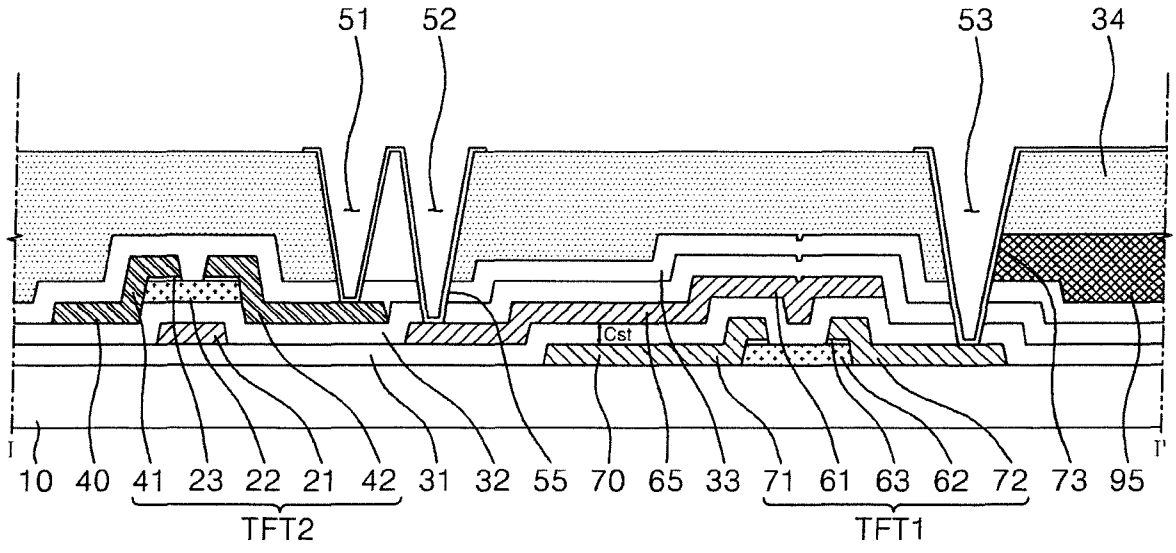


FIG. 14 A

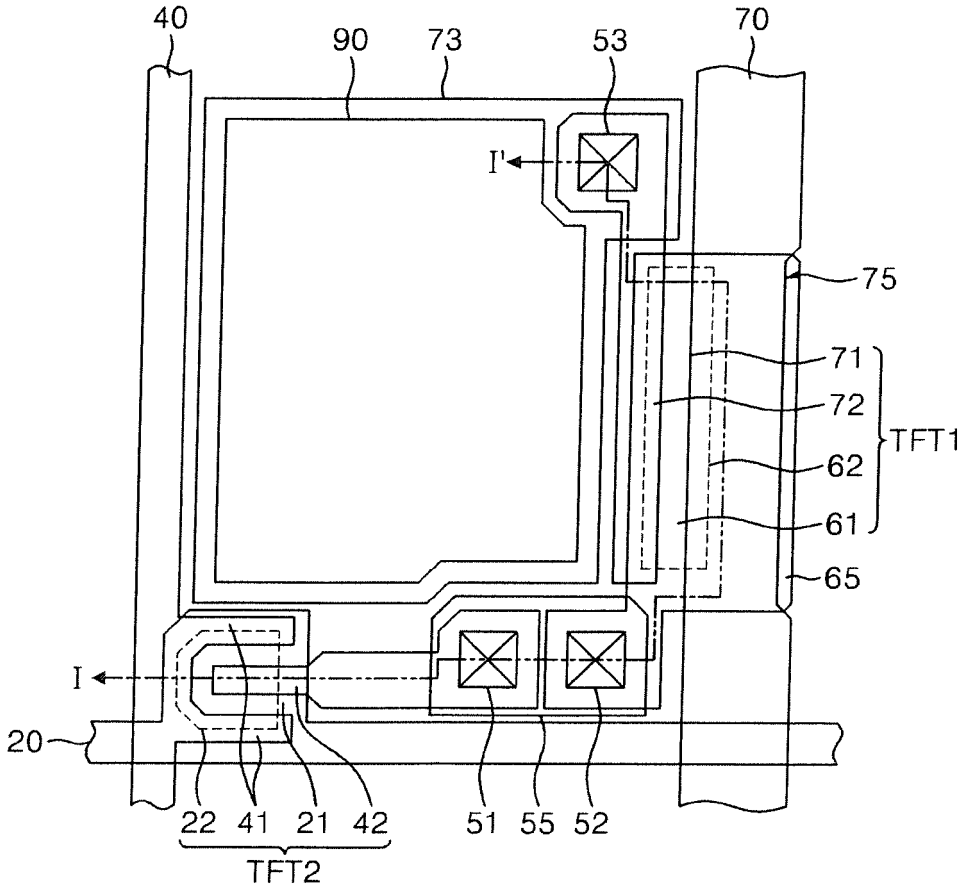
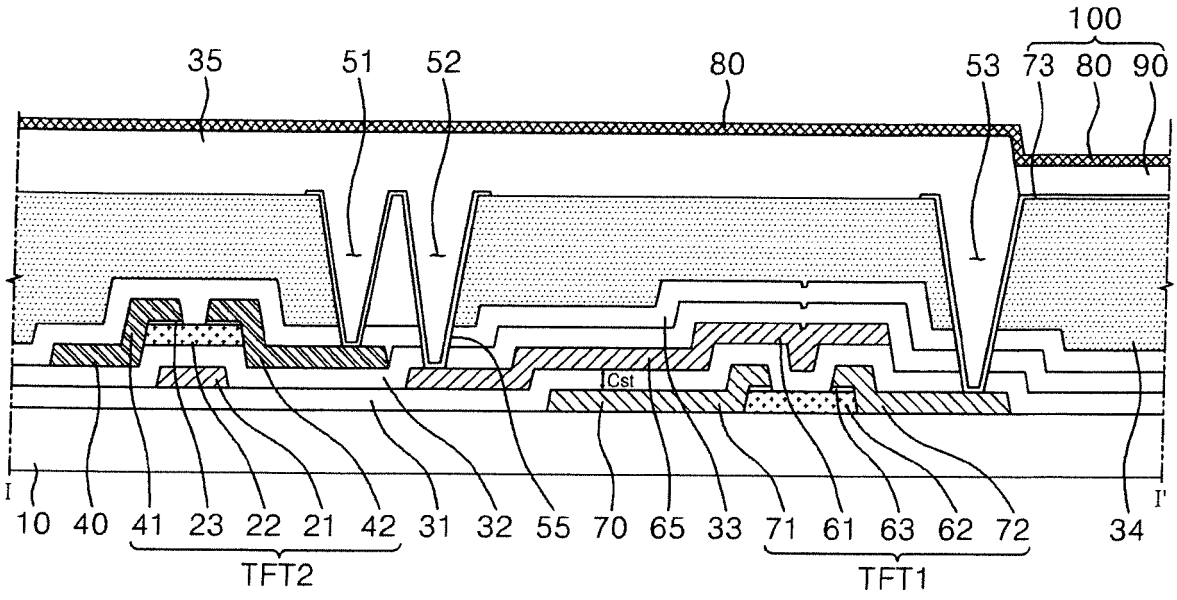


FIG. 14B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TFT1

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 1020070026889 **[0001]**

专利名称(译)	有机发光显示面板及其制造方法		
公开(公告)号	EP1973162B1	公开(公告)日	2017-09-20
申请号	EP2008003998	申请日	2008-03-04
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
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IPC分类号	H01L27/32		
CPC分类号	H01L27/3265 H01L27/3276		
代理机构(译)	DR.威猛和合作伙伴		
优先权	1020070026889 2007-03-20 KR		
其他公开文献	EP1973162A2 EP1973162A3		
外部链接	Espacenet		

摘要(译)

一种有机发光显示面板，具有存储电容器，所述存储电容器包括与电源线重叠的存储电极，其间设置有第一栅极绝缘层，其中所述存储电容器包括形成在所述电源线的侧面上的与所述存储器重叠的凹槽部分电极使得电源线和存储电极的重叠区域保持恒定，以及制造该电极的方法。

FIG. 1