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(54) **Light emitting display**

Lichtemittierende Anzeige

Affichage électroluminescent

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Description

[0001] An aspect of the present invention relates to a light emitting display device, and more particularly, relates to a light emitting display device having a dummy pixel in which the bias is controlled.

[0002] In general, an organic light emitting diode (OLED) display is a display device using an organic material that emits light, and an image is displayed by voltage-driving or current-driving organic light emitting cells arranged in an $N \times M$ matrix. The organic light emitting cell is also called an organic light emitting diode (OLED) since it has diode characteristics, and has a structure having an anode, an organic thin film, and a cathode layer.

[0003] A display panel of a conventional OLED includes a plurality of dummy pixels in left and right sides of an area in which a plurality of pixels for emitting light are included. A selection signal is transmitted to the light emitting pixels through the dummy pixel. As a result, a load of a scan line that transmits the selection signal increases. Therefore, it is necessary to prevent a short circuit and current leakage of a transistor that forms the dummy pixel.

[0004] In particular, the load of the scan line increases because of the biased dummy pixel, thereby causing a scan signal delay. In addition, an insulator breakdown phenomenon may occur in the transistor and the capacitor of the dummy pixel, resulting in a short circuit due to a current leakage.

[0005] The above information disclosed in this Background section is only for enhancement of understanding of the background of the invention and therefore it may contain information that does not form the prior art that is already known to a person of ordinary skill in the art.

[0006] US Patent Application 2004/0100463 describes a display device and controlling method thereof. The display device has a signal line driving circuit, a signal line driving circuit, a scanning line driving circuit, a plurality of dummy pixels, a plurality of pixels and a monitoring element.

[0007] US Patent Application 2005/0258769 describes an electro-optical device, method of checking the same and electronic apparatus. The electro-optical device has an effective region. A plurality of dummy elements is formed in the vicinity of the effective region. The dummy elements are not electrically connected to other elements such as scan lines or data lines.

[0008] US Patent Application 2005/0017672 describes a light emitting device and electronic apparatus. The device has unit circuits and dummy unit circuits. The dummy unit circuit has the same elements as included in the unit circuit except that it does not have an organic EL element.

[0009] An aspect of the present invention sets out to provide an organic light emitting diode (OLED) display eliminating short-circuits and current leakage in a dummy pixel by changing a bias condition of the dummy pixel to thereby prevent a scan signal delay.

[0010] A light emission display according to a first aspect of the present invention is set out in claim 1. Preferred features are set out in claim 2.

[0011] Additional aspects and/or advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

[0012] These and/or other aspects and advantages of the invention will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 schematically shows an organic light emitting diode (OLED) display according to an embodiment of the present invention;

FIG. 2 shows a pixel circuit of according to an embodiment of the present invention;

FIG. 3 shows a signal waveform applied to a pixel circuit;

FIG. 4 shows a random pixel circuit of a first dummy pixel group; and

FIG. 5 shows a random pixel circuit of a second dummy pixel group.

[0013] Reference will now be made in detail to the present embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

[0014] In the following detailed description, only certain embodiments of the present invention have been shown and described, simply by way of illustration. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the scope of the present invention. To clarify the present invention, parts that are not described in the specification are omitted, and parts for which similar descriptions are provided have the same reference numerals.

[0015] Throughout this specification and the claims that follow, when it is described that an element is coupled to

another element, the element may be directly coupled to the other element or electrically coupled to the other element through a third element. Throughout this specification and claims which follow, unless explicitly described to the contrary, the word "comprise/include" or variations such as "comprises/includes" or "comprising/including" will be understood to imply the inclusion of stated elements but not the exclusion of any other elements.

5 [0016] An organic light emitting diode (OLED) display and a pixel circuit according to an embodiment of the present invention will now be described in detail with reference to the accompanying drawings.

[0017] FIG. 1 schematically shows an OLED display according to an embodiment of the present invention.

[0018] As shown in FIG. 1, the OLED display includes a display 100, a scan driver 200, a data driver 300, and a light emission control driver 400.

10 [0019] The display 100 includes a plurality of data lines D_1 to D_m extending in a column direction, and a plurality of scan lines S_1 to S_n and light emission control lines E_1 to E_n extending in a row direction. The display 100 further includes a plurality of pixels formed at crossing parts of the data lines D_1 to D_m and the scan lines S_1 to S_n , and each pixel is connected to the plurality of data lines D_1 to D_m , the plurality of scan lines S_1 to S_n , and the plurality of light emission control lines E_1 to E_n , respectively. Each pixel includes a pixel circuit 110. In addition, the display 100 includes a first dummy pixel group 120 and a second dummy pixel group 130, wherein the first dummy pixel group 120 is formed of a plurality of pixels formed in an upper portion of the display 100, between the display 100 and the scan driver 200 and between the display 100 and the light emission control driver 400, and the second dummy pixel group 130 is formed of a plurality of pixels formed between the data driver 300 and the display 100. The data lines D_1 to D_m transmit data signals representing video signals to the pixel circuit 110, the scan lines S_1 to S_n transmit selection signals to the pixel circuit 110, and the light emission control lines E_1 to E_k transmit a light emission control signal to the pixel circuit 110.

15 [0020] In order to express colors, each pixel represents a unique color among primary colors or alternately represents a primary color with respect to time, and thus a desired color is expressed by temporally or spatially combining the primary colors. The primary colors, for example, include red (R), green (G), and blue (B). When a color is expressed by temporally combining colors, a pixel alternately displays R, G, and B with respect to time. When a color is expressed by spatially combining colors, a color is expressed by three pixels, which are an R pixel, a G pixel, and a B pixel. Herein, each pixel is called a sub-pixel, and one pixel is formed of these three sub-pixels. In addition, when the color is expressed by spatially combining colors, the R pixel, G pixel, and B pixel may be alternately arranged in a row direction or a column direction, or the three pixels may be located at respective angular points of a triangle.

20 [0021] The scan driver 200 generates selection signals and sequentially applies the selection signals to the scan lines S_1 to S_n . Herein, a scan line applied with a current selection signal is called a current scan line, and a scan line applied with a previous selection signal is called a previous scan line.

[0022] The data driver 300 generates a data voltage corresponding to the image signal and transmits the data voltage to the data lines D_1 to D_m .

25 [0023] The light emission control driver 400 sequentially applies the light emission control signal to the light emission control lines E_1 to E_k so as to control light emission of organic light emitting diodes.

30 [0024] The scan driver 200, the data driver 300, and/or the light emission control driver 400 may be electrically connected to the display panel 100, and may also be mounted as a chip on a tape carrier package (TCP), a flexible printed circuit (FPC), or a film attached and electrically coupled to the substrate of the display panel 100. On the other hand, the scan driver 200, the data driver 300, and/or the light emission control driver 400 may be directly attached to a substrate of the display panel 100, and they may be realized as a driving circuit formed on a substrate and having a layer structure similar to scan lines, data lines, light emission control lines, and a thin film transistor.

35 [0025] FIG. 2 shows a circuit of the pixel 110 according to the embodiment of the present invention.

[0026] As shown in FIG. 2, the pixel circuit 110 includes six transistors M1 to M6, two capacitors C1 and C2, and an organic light emitting element (OLED). Herein, the six transistors M1 to M6 are provided as p-channel metal oxide semiconductor (PMOS) transistors. The transistors M1 to M6 each have two electrodes respectively forming a source electrode and a drain electrode, and a control electrode. The organic light emitting element is called an organic light emitting diode since it has diode characteristics, and has a structure having an anode, an organic thin film, and a cathode.

40 [0027] As a driving transistor for driving the OLED, the transistor M1 is coupled between a power source ELVDD and the OLED, and a voltage difference between a gate electrode and a source electrode of the transistor M1 generates current flowing to the OLED. The power source ELVDD supplies a voltage of ELVDD. The transistor M4 is coupled between the power source ELVDD and a power source Vinit that supplies an initial voltage of Vinit, and is turned on/off in response to the selection signal from a previous scan line S_{n-1} .

45 [0028] When the transistor M4 is turned on, the initial voltage Vinit is transmitted to a gate of the transistor M1. The transistor M2 is turned on/off in response to the selection signal from a current scan line S_n , and is coupled between the gate electrode and the source electrode of the transistor M1. The transistor M3 is turned on/off in response to the selection signal from the current scan line S_n , and is coupled between a data line and a drain electrode of the transistor M1. The transistor M3 transmits a data voltage VDATA to the drain electrode of the transistor M1 in response to the selection signal from the current scan line S_n . The transistor M5 couples the transistor M1 and the power source ELVDD in

response to the light emission control signal from the light emission control line E_k . The transistor M6 is coupled between the transistor M1 and the OLED, and transmits current to the OLED through the transistor M1 in response to the light emission control signal from the light emission control line E_k .

[0029] The capacitor C1 is coupled between the transistor M4 and the power source ELVDD supplying the voltage ELVDD. When the transistor M4 is turned on, the capacitor C1 is charged with a voltage (ELVDD - Vinit) that corresponds to a voltage difference between the voltage ELVDD and the initial voltage Vinit, and the voltage between the gate electrode of the transistor M1 and the power source supplying the voltage ELVDD is consistently maintained. The capacitor C2 has a first electrode coupled to the current scan line S_n and a second electrode coupled to the gate electrode of the transistor M1. The capacitor C2 maintains a voltage difference between the selection signal from the current scan line S_n and the gate of the transistor M1. The OLED is coupled between a drain of the transistor M6 and the power source VSS.

[0030] In the pixel circuit 110 according to the embodiment of the present invention, a voltage level of the power source ELVDD is greater than that of the power source VSS.

[0031] An operation of the pixel circuit 110 will now be described with reference to FIG. 3.

[0032] FIG. 3 shows a signal waveform applied to the pixel circuit 110.

[0033] When a scan voltage of a selection signal of a low level (i.e., an enable level) is applied from the previous scan line S_{n-1} during a period D1, the transistor M4 is turned on and an end of the capacitor C1 is initialized with the initial voltage Vinit and charged with a voltage (ELVDD - Vinit) that corresponds to a voltage difference between the voltage ELVDD of the power source and the initial voltage Vinit.

[0034] Subsequently, during a period D2, a selection signal from the current scan line S_n becomes a low level (e.g., an enable level, Vlow), and thus the transistors M2 and M3 are turned on. When the transistor M2 is turned on, the transistor M1 is diode-connected and a data voltage VDATA is applied to the transistor M1 through the transistor M3. Then, a voltage is applied to a gate of the diode-connected transistor M1. The voltage corresponds to a sum of the data voltage VDATA and a threshold voltage VTH. Accordingly, both ends of the capacitor C2 are respectively applied with the gate voltage (VDATA+VTH) and the voltage Vlow, and thus the capacitor C2 is charged with a voltage of (VDATA + VTH - Vlow).

[0035] After a point of time D3, the selection signal from the current scan line S_n becomes a high level (i.e., a disable level, Vhigh) and the light emission signal from the light emission control line E_k becomes the enable level Vlow, and thus the transistors M5 and M6 are turned on in response to the light emission control signal. The source electrode of the transistor M1 is applied with the voltage ELVDD, and the voltage (VDATA+VTH) being applied to the gate electrode during the period D2 is changed as the selection signal from the current scan line S_n becomes the high level Vhigh.

[0036] When the selection signal from the current scan line S_n is changed from the low level Vlow to the high level Vhigh, a voltage at a node of the capacitor C2 and the current scan line S_n is increased by an increased amount ΔV_S of the selection signal level. Therefore, a gate voltage V_G of the transistor M1 is increased compared to the voltage during the period D2 due to the coupling of the capacitors C1 and C2, and an increased amount ΔV_G of the gate voltage V_G is calculated by Equation 1.

[Equation 1]

$$\Delta V_G = \frac{\Delta V_S C_1}{C_1 + C_2}$$

[0037] Since the gate voltage V_G of the transistor M1 is increased by ΔV_G , current I_{OLED} flowing to the transistor M1 can be calculated by Equation 2. That is, a voltage level of a gate-source voltage V_{GS} of the transistor M1 is changed as much as a voltage level of the gate voltage V_G of the transistor M1 is changed, and the drain current I_{OLED} is also changed accordingly.

[Equation 2]

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$$I_{OLED} = \frac{\beta}{2} (V_{GS} + \Delta V_G - V_{TH})^2 = \frac{\beta}{2} (V_{DATA} - ELVDD + \Delta V_G)^2$$

10 **[0038]** Pixels of the first dummy group 120 and the second dummy group 130 according to the embodiment of the present invention will now be respectively described with reference to FIG. 4 and FIG. 5. One portion of a plurality of dummy pixels and the other portion of a plurality of dummy pixels in the display 100 are respectively grouped into the first dummy pixel group 120 and the second dummy pixel group 130 according to the present embodiment, which is not restrictive.

15 **[0039]** FIG. 4 shows a random pixel circuit in the first dummy pixel group 120.

[0040] In contrast to the pixel circuit 110 of the display 100, the pixel circuit of the first dummy pixel group 120 has a selection signal, a light emission control signal, a data signal line, and a power source coupled to power sources that supply the same voltage.

20 **[0041]** In more detail, a power source ELVSS rather than the power source ELVDD is coupled to an end of a first capacitor C1, and thus a voltage ELVSS of the power source ELVSS rather than the data voltage VDATA is applied thereto. In addition, the voltage of the power source ELVSS replaces the selection signal from the current scan line S_n , the selection signal from the previous scan line S_{n-1} , and the light emission control signal from the light emission control line E_k .

[0042] In addition, the voltage of the power source ELVSS replaces the initial voltage V_{init} .

25 **[0043]** A cathode electrode of an OLED is coupled to the power source ELVSS.

[0044] A gate electrode and a source electrode of a transistor M'5 are applied with the same level of voltage, and thus the transistor M'5 is maintained at the turn-off state. A gate electrode and a source electrode of a transistor M'3 are applied with the same level of voltage, and thus the transistor M'3 is maintained at the turn-off state. In addition, although a transistor M'4 is turned on by the power voltage ELVSS, both ends of a first capacitor C'1 are applied with the same level of voltage and thus the first capacitor C'1 is not charged. At this time, although a transistor M'2 is turned on by the voltage ELVSS and thus the transistor M'1 is diode-connected, a short-circuit due to current leakage does not occur because current does not flow toward an anode of the OLED.

30 **[0045]** As described, the pixel circuit of the first dummy pixel group is not coupled to a scan line that transmits a selection signal and is applied with the same level of voltage, and therefore a load of each scan line due to the dummy pixel can be eliminated. Therefore, a selection signal can be transmitted to each scan line without causing a delay. In addition, unexpected light emission of the OLED due to the current leakage in the dummy pixel can be prevented.

35 **[0046]** FIG. 5 shows a pixel circuit of the second dummy pixel group 130.

40 **[0047]** Compared to the pixel 110 of the display 100, a current selection signal, a light emission control signal, an initial voltage OLED transmitted to a pixel circuit of the second dummy pixel group 130 and a cathode electrode of an OLED of the pixel circuit are coupled to a power source that supplies the same level of voltage. A power source ELVDD, a data voltage VDATA, and a selection signal from a previous scan line S_{n-1} are transmitted to the pixel circuit of the second dummy pixel group 130. In addition, a contact hole coupling the power source ELVDD and a source electrode of a transistor M'5, a contact hole coupling the power source ELVDD and an end of a first capacitor C'1, and a contact hole coupling the data lines D1 to Dm and a source electrode of the transistor M'3 are not formed. That is, the source electrode of the transistor M'5, a first electrode of the transistor M'3, and an end of the capacitor C'1 are floating.

45 **[0048]** Therefore, a voltage of the power source ELVDD is not applied to the source electrode of the transistor M'1, or the data voltage VDATA is not applied to the drain electrode of the transistor M'1. Since one end of the first capacitor C'1 is floating, a voltage difference at both ends of the first capacitor C'1 cannot be consistently maintained and accordingly the first capacitor C'1 cannot be charged.

50 **[0049]** In addition, instead of a selection signal from a current scan line (not shown) and a light emission control signal from a light emission control line E_k , a voltage of the power source ELVSS is applied to the pixel circuit of the second dummy pixel group. The voltage of the power source ELVSS replaces the initial voltage V_{init} , and a cathode of the OLED is coupled to the power source ELVSS.

55 **[0050]** When a selection signal of the enable level from a scan line S_n is applied to the transistor M'4 and thus the transistor M'4 is turned on, the other end of the first capacitor C'1 is applied with the voltage of the power source ELVSS. At this time, although the transistor M'2 is turned on by the voltage of the power source ELVSS and thus the transistor M'1 is diode-connected, current does not flow toward the anode of the OLED and thus an occurrence of a short-circuit due to the current leakage can be prevented.

[0051] The second dummy pixel group 130 according to the embodiment of the present invention is provided between the data driver 300 and the display 100, and the second dummy pixel group 130 is applied with the selection signal S_n rather than the voltage of the power source ELVSS so as to balance loads between the scan line S_n that transmits the selection signal to the second dummy pixel group 130 and the plurality of scan lines that transmit the selection signals to the plurality of scan lines S_1 to S_{n-1} in the light emitting state.

[0052] As described, although the pixel circuits of the second dummy pixel group are coupled to the scan line that transmits the selection signal for load balance, the pixel circuits do not emit light because they are applied with the same voltage.

[0053] Light emission of the OLED due to current leakage in the dummy pixel can also be avoided.

[0054] That is, a load of the scan line caused by the plurality of dummy pixels in the non-light emission state can be eliminated according to an aspect of the present embodiment. Therefore, the OLED display according to the embodiment of the present invention can transmit the selection signals to the plurality of pixels without causing a delay. In addition, there is no change of light emission in the OLED of the dummy pixel since no current leakage that causes a short-circuit occurs in the dummy pixel.

[0055] Although it has been described that the pixel circuit according to the embodiment of the present invention includes six transistors and two capacitors, a pixel circuit with a different configuration may also be applied to the present invention in a similar way as described above.

[0056] According to the embodiment of the present invention, a load of a scan line caused by a dummy pixel is eliminated and thus an OLED display can transmit a selection signal without a delay.

[0057] In addition, light emission of the dummy pixel due to current leakage in the OLED display can also be prevented according to the embodiment of the present invention.

[0058] Although the embodiment of the present invention has been shown and described, it would be appreciated by those skilled in the art that changes may be made in this embodiment without departing from the principles of the invention, the scope of which is defined in the claims.

Claims

1. A light emitting display comprising:

a data driver (300) for generating data signals and for transmitting the data signals to a plurality of data lines;
 a scan driver (200) for generating selection signals and for transmitting the selection signals to a plurality of scan lines crossing the plurality of data lines;
 a light emission control driver (400) for generating light emission control signals and for transmitting the light emission control signals to a plurality of light emission control lines crossing the plurality of data lines; and
 a display (100) including:

the plurality of data lines;

the plurality of scan lines;

the plurality of light emission control lines;

a rectangular first area comprising a plurality of first pixels respectively formed at crossing points of data lines and scan lines, each said pixel including a pixel circuit connected to a said data line to receive a said data signal said selection signals and to a said light emission control line to receive a said light emission control signal,

wherein the scan driver (200) and the light emission control driver (400) are, in a top plan view, located outside of opposing respective first and second sides of the display (100) and wherein the data driver (300) is located, in the top plan view, outside of a third side of the display (100);

wherein the display (100) further comprises:

a first dummy pixel group (120) formed of a plurality of dummy pixels, each dummy pixel including a pixel circuit, the first dummy pixel group located in:

i) a rectangular second area that, in the top plan view, is contiguous with the first area, extending along the entire first side of the first area;

ii) a rectangular third area that, in the top plan view, is contiguous with the first area, extending along the entire second side of the first area; and

iii) a rectangular fourth area that, in the top plan view, is contiguous with and on a side of the first area opposite to the third side, the rectangular fourth area extending from an edge of the rectangular

second area that is closest to the scan driver (200) to an edge of the rectangular third area that is closest to the light emission control driver (400); and

5 a second dummy pixel group (130) formed of a plurality of dummy pixels, each dummy pixel including a pixel circuit, the second dummy pixel group provided in a fifth rectangular area that, in the top plan view, is contiguous with the first area, extending along the third edge of the first area from an edge of the rectangular second area that is closest to the scan driver (200) to an edge of the rectangular third area that is closest to the light emission control driver (400);

10 wherein each of the pixel circuits of the first and second dummy pixel groups comprises; first and second capacitors (C'1, C'2; C''1, C''2;) having respective first and second electrodes; a light emitting diode having an anode and a cathode; and first to sixth transistors (M'1 - M'6; M''1 - M''6;), each having a gate electrode and first and second electrodes; wherein the gate electrode of the second transistor (M'1, M''1) is coupled to the first electrode of the first capacitor (C'1, C''1) and wherein the second electrode of the second transistor (M'1, M''1) is coupled to a second electrode of the first transistor (M'3, M''3);

15 wherein the first and second electrodes of the third transistor (M'6, M''6) are respectively coupled to second electrode of the second transistor (M'1, M''1) and to the anode of the light emitting diode; wherein the second electrode of the fourth transistor (M'5, M''5) is coupled to the first electrode of the second transistor (M'1, M''1);

20 wherein the second electrode of the fifth transistor (M'4, M''4) is coupled to the first electrode of the first capacitor (C'1, C''1); wherein the first and second electrodes of the sixth transistor (M'2, M''2) are respectively coupled to the first electrode and the gate electrode of the second transistor (M'1, M''1);

25 wherein the first and second electrodes of the second capacitor (C'2, C''2) are respectively coupled to the gate electrodes of the first (M'3, M''3) and second (M'1, M''1) transistors;

the gate electrodes of the first (M'3, M''3) and sixth (M'2, M''2) transistors are connected to receive a voltage of a first power supply;

30 wherein the gate electrodes of the third (M'6, M''6) and fourth (M'5, M''5) transistors, the first electrode of the fifth transistor (M'4, M''4) and the cathode of the light emitting diode are connected to receive the voltage of the first power supply;

wherein in the pixel circuits of the first dummy pixel group:

35 the first electrode of the fourth transistor (M5, M'5) is coupled to the second electrode of the first capacitor (C1, C'1);

the first electrode of the first transistor (M''1), the gate electrode of the fifth transistor (M'4) and the second electrode of the first capacitor (C'1) are coupled to receive the voltage of the first power supply;

40 wherein in the pixel circuits of the second dummy pixel group:

the first electrode of the first transistor (M''3), the first electrode of the fourth transistor (M''5) and the second electrode of the first capacitor (C''1) are floating; and

45 the gate electrode of the fifth transistor (M''4) is connected to a said scan line.

2. A light emitting display according to claim 1, wherein the scan driver (200), the data driver (300) and the light emission control driver (400) are mounted as a chip on a tape carrier package, a flexible printed circuit, or a film attached and electrically coupled to a substrate of the light emitting display (100).

50 Patentansprüche

1. Lichtemittierende Anzeige, umfassend:

55 einen Datentreiber (300) zum Generieren von Datensignalen und zum Übertragen der Datensignale an eine Mehrzahl von Datenzeilen;

einen Abtasttreiber (200) zum Generieren von Auswahlsignalen und zum Übertragen der Auswahlsignale an eine Mehrzahl von Abtastzeilen, welche die Mehrzahl von Datenzeilen kreuzen;

einen Lichtemissionssteuerungstreiber (400) zum Generieren von Lichtemissionssteuerungssignalen und zum Übertragen der Lichtemissionssteuerungssignale an eine Mehrzahl von Lichtemissionssteuerungszeilen, welche die Mehrzahl von Datenzeilen kreuzen; und eine Anzeige (100), enthaltend:

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die Mehrzahl von Datenzeilen;
die Mehrzahl von Abtastzeilen;
die Mehrzahl von Lichtemissionssteuerungszeilen;

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einen rechteckigen ersten Bereich, der eine Mehrzahl erster Pixel umfasst, die jeweils an Kreuzungspunkten von Datenzeilen und Abtastzeilen ausgebildet sind, wobei jedes Pixel eine Pixelschaltung enthält, die mit einer Datenzeile verbunden ist, um ein Datensignal Auswahlsignale zu empfangen, und mit einer Lichtemissionssteuerungszeile verbunden ist, um ein Lichtemissionssteuerungssignal zu empfangen, wobei der Abtasttreiber (200) und der Lichtemissionssteuerungstreiber (400) in einer Draufsicht außerhalb von einander gegenüberliegenden ersten und zweiten Seiten der Anzeige (100) angeordnet sind und wobei der Datentreiber (300) in der Draufsicht außerhalb einer dritten Seite der Anzeige (100) angeordnet ist; wobei die Anzeige (100) ferner Folgendes umfasst:

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eine erste Dummypixelgruppe (120), die aus einer Mehrzahl von Dummypixeln ausgebildet ist, wobei jedes Dummypixel eine Pixelschaltung enthält, wobei die erste Dummypixelgruppe angeordnet ist in:

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- i) einem rechteckigen zweiten Bereich, der in der Draufsicht an den ersten Bereich angrenzt und sich entlang der gesamten ersten Seite des ersten Bereichs erstreckt;
- ii) einem rechteckigen dritten Bereich, der in der Draufsicht an den ersten Bereich angrenzt und sich entlang der gesamten zweiten Seite des ersten Bereichs erstreckt; und
- iii) einem rechteckigen vierten Bereich, der in der Draufsicht an eine und auf einer Seite des ersten Bereichs, die der dritten Seite gegenüberliegt, angrenzt, wobei sich der rechteckige vierte Bereich von einer Kante des rechteckigen zweiten Bereichs, die dem Abtasttreiber (200) am nächsten ist, zu einer Kante des rechteckigen dritten Bereichs, die dem Lichtemissionssteuerungstreiber (400) am nächsten ist, erstreckt; und

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eine zweite Dummypixelgruppe (130), die aus einer Mehrzahl von Dummypixeln ausgebildet ist, wobei jedes Dummypixel eine Pixelschaltung enthält, wobei die zweite Dummypixelgruppe in einem fünften rechteckigen Bereich bereitgestellt ist, der in der Draufsicht an den ersten Bereich angrenzt und sich entlang der dritten Kante des ersten Bereichs von einer Kante des rechteckigen zweiten Bereichs, die dem Abtasttreiber (200) am nächsten ist, zu einer Kante des rechteckigen dritten Bereichs, die dem Lichtemissionssteuerungstreiber (400) am nächsten ist, erstreckt;

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wobei jede der Pixelschaltungen der ersten und zweiten Dummypixelgruppe Folgendes umfasst:

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erste und zweite Kondensatoren (C'1, C'2; C"1, C"2) mit jeweils einer ersten und einer zweiten Elektrode;
eine lichtemittierende Diode mit einer Anode und einer Kathode und
erste bis sechste Transistoren (M'1 - M'6; M"1 - M"6) mit jeweils einer Gate-Elektrode, einer ersten und einer zweiten Elektrode;

45

wobei die Gate-Elektrode des zweiten Transistors (M'1, M"1) mit der ersten Elektrode des ersten Kondensators (C'1, C"1) gekoppelt ist und wobei die zweite Elektrode des zweiten Transistors (M'1, M"1) mit einer zweiten Elektrode des ersten Transistors (M'3, M"3) gekoppelt ist;

50

wobei die erste und die zweite Elektrode des dritten Transistors (M'6, M"6) mit der zweiten Elektrode des zweiten Transistors (M'1, M"1) bzw. mit der Anode der lichtemittierenden Diode gekoppelt sind;

50

wobei die zweite Elektrode des vierten Transistors (M'5, M"5) mit der ersten Elektrode des zweiten Transistors (M'1, M"1) gekoppelt ist;

55

wobei die zweite Elektrode des fünften Transistors (M'4, M"4) mit der ersten Elektrode des ersten Kondensators (C'1, C"1) gekoppelt ist;

wobei die erste und die zweite Elektrode des sechsten Transistors (M'2, M"2) mit der ersten Elektrode bzw. der Gate-Elektrode des zweiten Transistors (M'1, M"1) gekoppelt sind;

wobei die erste und die zweite Elektrode des zweiten Kondensators (C'2, C"2) mit der Gate-Elektrode des ersten Transistors (M'3, M"3) bzw. des zweiten Transistors (M'1, M"1) gekoppelt sind;

die Gate-Elektroden des ersten Transistors (M'3, M"3) und des sechsten Transistors (M'2, M"2) verbunden

sind, um eine Spannung von einer ersten Spannungsversorgung zu empfangen;
wobei die Gate-Elektroden des dritten Transistors (M'6, M''6) und des vierten Transistors (M'5, M''5), die erste Elektrode des fünften Transistors (M'4, M''4) und die Kathode der lichtemittierenden Diode verbunden sind, um die Spannung von der ersten Spannungsversorgung zu empfangen;
5 wobei in den Pixelschaltungen der ersten Dummypixelgruppe:

die erste Elektrode des vierten Transistors (M5, M'5) mit der zweiten Elektrode des ersten Kondensators (C1, C'1) gekoppelt ist;
10 die erste Elektrode des ersten Transistors (M'1), die Gate-Elektrode des fünften Transistors (M'4) und die zweite Elektrode des ersten Kondensators (C'1) gekoppelt sind, um die Spannung der ersten Spannungsversorgung zu empfangen;

wobei in den Pixelschaltungen der zweiten Dummypixelgruppe:

15 die erste Elektrode des ersten Transistors (M'3), die erste Elektrode des vierten Transistors (M''5) und die zweite Elektrode des ersten Kondensators (C'1) potentialfrei sind und die Gate-Elektrode des fünften Transistors (M''4) mit einer Abtastzeile verbunden ist.

2. Lichtemittierende Anzeige nach Anspruch 1, wobei der Abtasttreiber (200), der Datentreiber (300) und der Lichtemissionssteuerungstreiber (400) als ein Chip auf einem Tape Carrier Package, einer flexiblen Leiterplatte oder einer Folie angebracht sind, das bzw. die an einem Träger der lichtemittierenden Anzeige (100) befestigt und mit dieser elektrisch gekoppelt ist.

25 Revendications

1. Dispositif d'affichage électroluminescent comprenant:

30 un pilote de données (300) destiné à générer des signaux de données et à transmettre les signaux de données à une pluralité de lignes de données ;
un pilote de balayage (200) destiné à générer des signaux de sélection et à transmettre les signaux de sélection à une pluralité de lignes de balayage croisant la pluralité de lignes de données ;
un pilote de commande d'émission de lumière (400) destiné à générer des signaux de commande d'émission de lumière et à transmettre les signaux de commande d'émission de lumière à une pluralité de lignes de
35 commande d'émission de lumière croisant la pluralité de lignes de données ; et
un dispositif d'affichage (100) comportant :

la pluralité de lignes de données ;
la pluralité de lignes de balayage ;
40 la pluralité de lignes de commande d'émission de lumière ;
une première zone rectangulaire comprenant une pluralité de premiers pixels formés respectivement à des points de croisement des lignes de données et des lignes de balayage, chacun desdits pixels comportant un circuit de pixel relié à ladite ligne de données pour recevoir ledit signal de données, lesdits signaux de sélection et à ladite ligne de commande d'émission de lumière pour recevoir ledit signal de commande
45 d'émission de lumière,
le pilote de balayage (200) et le pilote de commande d'émission de lumière (400) étant, en vue de dessus, situés à l'extérieur des premier et deuxième côtés respectifs opposés du dispositif d'affichage (100) et le pilote de données (300) étant situé, en vue de dessus, à l'extérieur d'un troisième côté du dispositif d'affichage (100) ;
50 le dispositif d'affichage (100) comprend en outre :

un premier groupe de pixels factices (120) formé d'une pluralité de pixels factices, chaque pixel factice comportant un circuit de pixel, le premier groupe de pixels factices étant situé dans :

- 55 i) une deuxième zone rectangulaire qui, en vue de dessus, est contiguë à la première zone, s'étendant le long de la totalité du deuxième côté de la première zone ;
ii) une troisième zone rectangulaire qui, en vue de dessus, est contiguë à la première zone, s'étendant le long de la totalité du deuxième côté de la première zone ; et

iii) une quatrième zone rectangulaire qui, en vue de dessus, est contiguë à et située sur un côté de la première zone opposée au troisième côté, la quatrième zone rectangulaire s'étendant à partir d'un bord de la deuxième zone rectangulaire qui est la plus proche du pilote de balayage (200) jusqu'à un bord de la troisième zone rectangulaire qui est la plus proche du pilote de commande d'émission de lumière (400) ; et

un deuxième groupe de pixels factices (130) formé d'une pluralité de pixels factices, chaque pixel factice comportant un circuit de pixel, le deuxième groupe de pixels factices étant prévu dans une cinquième zone rectangulaire qui, en vue de dessus, est contiguë à la première zone, s'étendant le long du troisième bord de la première zone à partir d'un bord de la deuxième zone rectangulaire qui est la plus proche du pilote de balayage (200) jusqu'à un bord de la troisième zone rectangulaire qui est la plus proche du pilote de commande d'émission de lumière (400) ;

chacun des circuits de pixels des premier et deuxième groupes de pixels factices comprenant :

des premier et deuxième condensateurs (C'1, C'2 ; C"1, C"2) ayant des première et deuxième électrodes respectives ;

une diode électroluminescente comportant une anode et une cathode ; et

des premier à sixième transistors (M'1 à M'6 ; M"1 à M"6), ayant chacun une électrode de grille et des première et deuxième électrodes ;

l'électrode de grille du deuxième transistor (M'1, M"1) étant couplée à la première électrode du premier condensateur (C'1, C"1) et la deuxième électrode du deuxième transistor (M'1, M"1) étant couplée à une deuxième électrode du premier transistor (M'3, M"3) ;

les première et deuxième électrodes du troisième transistor (M'6, M"6) étant respectivement couplées à une deuxième électrode du deuxième transistor (M'1, M"1) et à l'anode de la diode électroluminescente ;

la deuxième électrode du quatrième transistor (M'5, M"5) étant couplée à la première électrode du deuxième transistor (M'1, M"1) ;

la deuxième électrode du cinquième transistor (M'4, M"4) étant couplée à la première électrode du premier condensateur (C'1, C"1) ;

les première et deuxième électrodes du sixième transistor (M'2, M"2) étant respectivement couplées à la première électrode et à l'électrode de grille du deuxième transistor (M'1, M"1) ;

les première et deuxième électrodes du deuxième condensateur (C'2, C"2) étant respectivement couplées aux électrodes de grille des premier (M'3, M"3) et deuxième (M'1, M"1) transistors ;

les électrodes de grille des premier (M'3, M"3) et sixième (M'2, M"2) transistors étant reliées pour recevoir une tension d'une première alimentation électrique ;

les électrodes de grille des troisième (M'6, M"6) et quatrième (M'5, M"5) transistors, la première électrode du cinquième transistor (M'4, M"4) et la cathode de la diode électroluminescente étant reliées pour recevoir la tension de la première alimentation électrique ;

dans lequel, dans les circuits de pixels du premier groupe de pixels factices :

la première électrode du quatrième transistor (M'5, M"5) est couplée à la deuxième électrode du premier condensateur (C'1, C"1) ;

la première électrode du premier transistor (M'1), l'électrode de grille du cinquième transistor (M'4) et la deuxième électrode du premier condensateur (C'1) sont couplées pour recevoir la tension de la première alimentation électrique ;

dans lequel, dans les circuits de pixels du deuxième groupe de pixels factices :

la première électrode du premier transistor (M"3), la première électrode du quatrième transistor (M"5) et la deuxième électrode du premier condensateur (C"1) sont flottantes ; et

l'électrode de grille du cinquième transistor (M"4) est reliée à ladite ligne de balayage.

2. Dispositif d'affichage électroluminescent selon la revendication 1, dans lequel le pilote de balayage (200), le pilote de données (300) et le pilote de commande d'émission de lumière (400) sont montés sous forme de puce sur un ensemble de support de bande, un circuit imprimé souple, ou un film fixé et couplé électriquement à un substrat du dispositif d'affichage électroluminescent (100).

FIG. 2

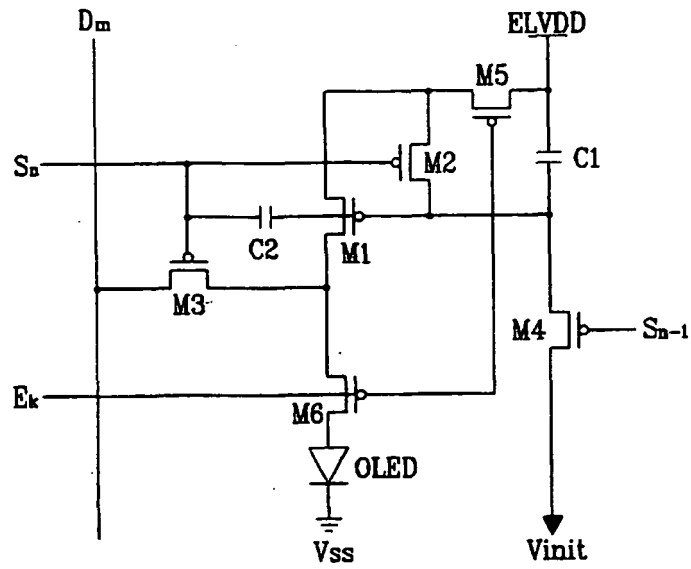


FIG. 3

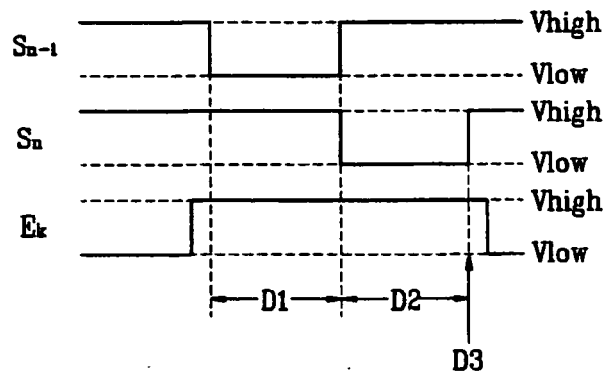


FIG. 4

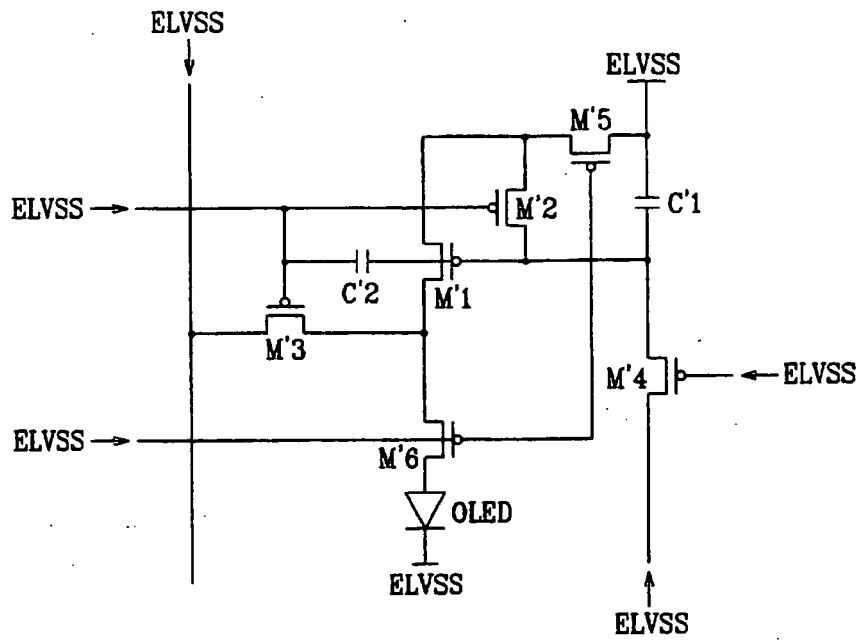
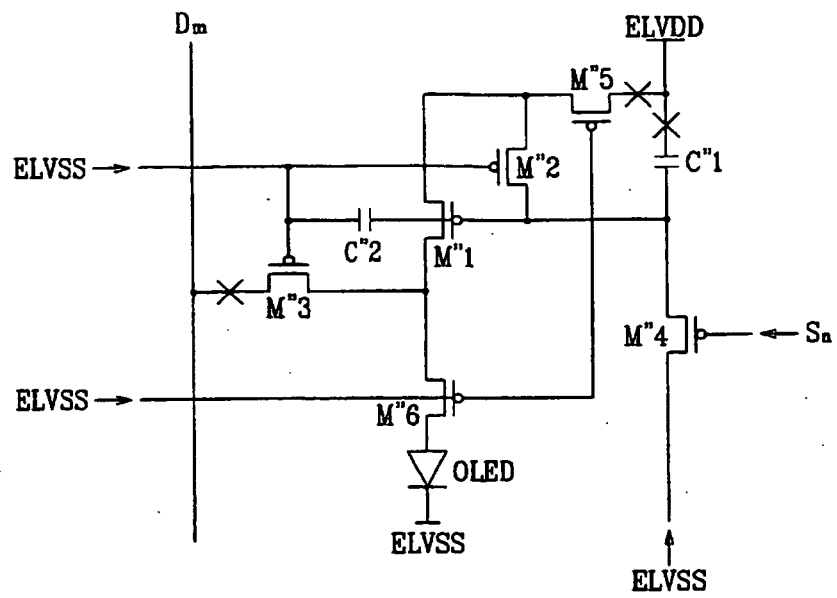


FIG. 5



REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	发光显示器		
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摘要(译)

发光显示器包括数据驱动器 (300) , 扫描驱动器 (200) 和显示器 (100) 。数据驱动器 (300) 产生数据信号并将数据信号发送到数据线。扫描驱动器 (200) 产生第一选择信号并将第一选择信号发送到第一扫描线。显示器 (100) 包括数据线和第一扫描线, 第一像素, 第一虚设像素组 (120) 和第二虚设像素组 (130) 。第一像素由数据线和第一扫描线限定。第一和第二虚设像素组分别由包括像素电路的虚设像素形成, 设置在扫描驱动器 (200) 和数据驱动器 (300) 附近。向第一虚设像素组的每个像素电路施加第一电源的电压。向第二虚设像素组的每个像素电路施加第一电源的电压。

[Equation 1]

$$\Delta V_G = \frac{\Delta V_S C_1}{C_1 + C_2}$$