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(54) **Pixel circuit and display apparatus**

Pixelschaltung und Bildanzeigevorrichtung

Circuit de pixel et appareil d'affichage

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a pixel circuit for current-driving light-emitting devices disposed at respective pixels. The present invention is also concerned with an active-matrix display apparatus having a matrix of such pixel circuits, for controlling currents supplied to light-emitting devices such as organic EL devices with insulated-gate field-effect transistors disposed in the respective pixel circuits.

2. Description of the Related Art

[0002] Image display apparatus such as liquid-crystal display apparatus have a matrix of liquid-crystal pixels, and control the intensity of light passing through or reflected by the pixels depending on image information to display an image represented by the image information. Organic EL display apparatus having organic EL devices as pixels also operate similarly. Unlike liquid-crystal devices, the organic EL devices are self-luminous devices. Therefore, the organic EL devices display more visible images than the liquid-crystal devices, do not require backlight, and have a high response speed. The luminance level (gradation) of each light-emitting device can be controlled by a current flowing therethrough, and hence the organic EL display apparatus are current-controlled whereas the liquid-crystal display apparatus are voltage-controlled.

[0003] Like the liquid-crystal display apparatus, the organic EL display apparatus are classified into a passive-matrix drive type and an active-matrix matrix drive type. Though the passive-matrix drive configuration is simple in structure, it poses difficulty in producing large-size, high-definition display apparatus. Consequently, efforts are mainly directed to develop active-matrix display apparatus. According to the active-matrix drive scheme, a current flowing through a light-emitting device in each pixel circuit is controlled by an active device (generally, a thin-film transistor or TFT) disposed in the pixel circuit. Active-matrix drive systems are disclosed in the following patent documents: Japanese Patent Laid-Open No. 2003-255856; Japanese Patent Laid-Open No. 2003-271095; Japanese Patent Laid-Open No. 2004-133240; Japanese Patent Laid-Open No. 2004-029791; Japanese Patent Laid-Open No. 2004-093682; and Japanese Patent Laid-Open No. Hei 10-214042.

[0004] Some other examples of active-matrix drive systems are given by the prior art documents US2006061560, US2005269959 and EP1496495.

SUMMARY OF THE INVENTION

[0005] A pixel circuit in the past is positioned at a point of intersection between a row scanning line for supplying a control signal and a column signal line for supplying a video signal. The pixel circuit comprises at least a sampling transistor, a pixel capacitance, a drive transistor, and a light-emitting device. The sampling transistor is turned on by a control signal supplied from the scanning line, sampling a video signal supplied from the signal line. The pixel capacitance holds an input voltage depending on the sampled video signal. The drive transistor supplies an output current during a predetermined light-emission period depending on an input voltage held by the pixel capacitance. Generally, the output current is dependent on the carrier mobility and the threshold voltage in a channel region of the drive transistor. In response to the output current supplied from the drive transistor, the light-emitting device emits light at a luminance level depending on the video signal.

[0006] When the input voltage held by the pixel capacitance is applied to the gate of the drive transistor, the output current flows between the source and drain of the drive transistor, energizing the light-emitting device. Generally, the luminance of light emitted from the light-emitting device is proportional to the amount of current flowing therethrough. The amount of output current supplied from the drive transistor is controlled by the gate voltage thereof, i.e., the input voltage written in the pixel capacitance. The pixel circuit in the past controls the amount of current supplied to the light-emitting device by changing the input voltage applied to the gate of the drive transistor depending on the video signal.

[0007] The drive transistor has an operating characteristic expressed by the following equation (1):

$$Ids = (1/2)\mu(W/L)Cox(Vgs - Vth)^2 \quad \cdots(1)$$

where Ids represents the drain current flowing between the source and drain, the drain current serving as the output current supplied to the light-emitting device, Vgs represents the gate voltage that is applied to the gate with respect to

the source, the gate voltage serving as the input voltage referred to above in the pixel circuit, Vth represents the threshold voltage of the transistor, μ represents the mobility in a thin semiconductor film serving as the channel of the transistor. Further W represents the channel width, L represents the channel length, and Cox represents the gate capacitance. As can be seen from the transistor characteristic equation (1), since the thin-film transistor operates in a saturated region, when the gate voltage Vgs increases in excess of the threshold voltage Vth, the transistor is turned on, causing the drain current Ids to flow. In principle, as indicated by the transistor characteristic equation (1), if the gate voltage Vgs is constant, then the drain current Ids is supplied at constant rate to the light-emitting device at all times. Therefore, if the pixels that make up the screen are supplied with respective video signals of the same level, then all the pixels should emit light at the same luminance level, providing image uniformity over the screen.

[0008] Actually, however, thin-film transistors (TFTs) made of thin transistor films such as of polysilicon have individual device characteristic variations. Particularly, the threshold voltage Vth is not constant, but varies from pixel to pixel. As can be understood from the transistor characteristic equation (1), if the threshold voltage Vth varies from drive transistor to drive transistor, then even when the gate voltage Vgs is constant, the drain voltage Ids also varies from drive transistor to drive transistor, resulting in different luminance levels at the pixels and losing the image uniformity over the screen. There have heretofore been developed pixel circuits incorporating a function to cancel threshold voltage variations of the drive transistors, as disclosed in Japanese Patent Laid-Open No. 2004-133240.

[0009] The pixel circuits incorporating a function to cancel threshold voltage variations are capable, to a certain extent, of improving the image uniformity over the screen. However, the characteristics of the polysilicon thin-film transistors indicate that not only the threshold voltage but also the mobility μ vary from device to device. As can be seen from the transistor characteristic equation (1), if the mobility μ varies, then, the drain current Ids also varies though the gate voltage Vgs is constant. As a result, the light-emission luminance varies from device to device, impairing the image uniformity over the screen.

[0010] It is desirable to provide a pixel circuit and a display apparatus for canceling the effect of a carrier mobility in a drive transistor to compensate for a variation of a drain current (output current) supplied from the drive transistor.

[0011] It is also desirable to provide a pixel circuit and a display apparatus which maintain a margin for a corrective action requisite to cancel the effect of a carrier mobility in a drive transistor, for thereby stabilizing the operation of the pixel circuit and the display apparatus.

[0012] To meet the above needs, there is provided in accordance with the appended set of claims of the present invention a pixel circuit for being positioned at a point of intersection between a row scanning line for supplying a control signal and a column signal line for supplying a video signal, including at least a sampling transistor, a pixel capacitance connected to the sampling transistor, a drive transistor connected to the pixel capacitance, a light-emitting device connected to the drive transistor. In the pixel circuit, the sampling transistor is turned on in response to the control signal supplied from the scanning line to sample the video signal supplied from the signal line into the pixel capacitance. The pixel capacitance applies an input voltage to a gate of the drive transistor depending on the sampled video signal. The drive transistor supplies an output current depending on the input voltage to the light-emitting device, the output current having dependency on a carrier mobility in a channel region of the drive transistor. The light-emitting device emits light at a luminance level depending on the video signal in response to the output current supplied from the drive transistor. The pixel circuit further includes a correcting section configured to correct the input voltage sampled in the pixel capacitance in order to cancel out the dependency of the output current on the carrier mobility. The correcting section operates depending on the control signal supplied from the scanning line to extract the output current from the drive transistor and introduce the extracted output current into a capacitance of the light-emitting device and the pixel capacitance for thereby correcting the input voltage. The pixel circuit still further includes an additional capacitance added to the capacitance of the light-emitting device. A portion of the output current extracted from the drive transistor flows into the additional capacitance to give a time margin to operation of the correcting section.

[0013] Preferably, in the pixel circuit, the sampling transistor, the drive transistor, and the correcting section include thin-film transistors formed on an insulating substrate, and the pixel capacitance and the additional capacitance include thin-film capacitors formed on the insulating substrate. The output current of the drive transistor has dependency on a threshold voltage as well as the carrier mobility in the carrier region, and the correcting section detects a threshold voltage of the drive transistor and adds the detected threshold voltage to the input voltage in advance in order to cancel out the dependency of the output current on the threshold voltage. The light-emitting device includes a diode-type light-emitting device having an anode connected to a source of the drive transistor and a cathode connected to ground, the additional capacitance having a terminal connected to the anode of the light-emitting device and another terminal connected to a predetermined fixed potential. The predetermined fixed potential to which another terminal of the additional capacitance is connected is selected from a ground potential on the cathode of the light-emitting device, and a positive power supply potential and a negative power supply potential of the pixel circuit. In an array of pixel circuits each as described above, each of the pixel circuits has either one of a red light-emitting device, a green light-emitting device, and a blue light-emitting device, and the additional capacitances in the respective pixel circuits have different capacitance values for the respective light-emitting devices for thereby uniformizing times requisite to operate the correcting section

in the respective pixel circuits. In the array of pixel circuits, a shortage of the capacitance value of the additional capacitance in one of the pixel circuits is made up for by a portion of the additional capacitance in an adjacent one of the pixel circuits. The correcting section extracts the output current from the drive transistor and supplies the extract output current to the pixel capacitance through a negative feedback loop to correct the input voltage while the video signal is being sampled in the pixel capacitance.

[0014] According to an embodiment of the present invention, there is also provided a display apparatus including a pixel array having a matrix of pixels each positioned at a point of intersection between a row scanning line for supplying a control signal and a column signal line for supplying a video signal, a signal unit for supplying a video signal to the signal line, and a scanner unit for supplying a control signal to the scanning line to successively scan rows of the pixels, each of the pixels including at least a sampling transistor, a pixel capacitance connected to the sampling transistor, a drive transistor connected to the pixel capacitance, a light-emitting device connected to the drive transistor. In the display apparatus, the sampling transistor is turned on in response to the control signal supplied from the scanning line to sample the video signal supplied from the signal line into the pixel capacitance. The pixel capacitance applies an input voltage to a gate of the drive transistor depending on the sampled video signal. The drive transistor supplies an output current depending on the input voltage to the light-emitting device, the output current having dependency on a carrier mobility in a channel region of the drive transistor. The light-emitting device emits light at a luminance level depending on the video signal in response to the output current supplied from the drive transistor. Each of the pixels further includes a correcting section configured to correct the input voltage sampled in the pixel capacitance in order to cancel out the dependency of the output current on the carrier mobility. The correcting section operates depending on the control signal supplied from the scanning line to extract the output current from the drive transistor and introduce the extracted output current into a capacitance of the light-emitting device and the pixel capacitance for thereby correcting the input voltage. Each of the pixels still further includes an additional capacitance added to the capacitance of the light-emitting device. A portion of the output current extracted from the drive transistor flows into the additional capacitance to give a time margin to operation of the correcting section.

[0015] Preferably, in the display apparatus, the sampling transistor, the drive transistor, and the correcting section include thin-film transistors formed on an insulating substrate, and the pixel capacitance and the additional capacitance include thin-film capacitors formed on the insulating substrate. The output current of the drive transistor has dependency on a threshold voltage as well as the carrier mobility in the carrier region, and the correcting section detects a threshold voltage of the drive transistor and adds the detected threshold voltage to the input voltage in advance in order to cancel out the dependency of the output current on the threshold voltage. The light-emitting device includes a diode-type light-emitting device having an anode connected to a source of the drive transistor and a cathode connected to ground, the additional capacitance having a terminal connected to the anode of the light-emitting device and another terminal connected to a predetermined fixed potential. The predetermined fixed potential to which another terminal of the additional capacitance is connected is selected from a ground potential on the cathode of the light-emitting device, and a positive power supply potential and a negative power supply potential of the pixel circuit. Each of the pixels has either one of a red light-emitting device, a green light-emitting device, and a blue light-emitting device, and the additional capacitances in the respective pixels have different capacitance values for the respective light-emitting devices for thereby uniformizing times requisite to operate the correcting section in the respective pixels. A shortage of the capacitance value of the additional capacitance in one of the pixels is made up for by a portion of the additional capacitance in an adjacent one of the pixels. The correcting section extracts the output current from the drive transistor and supplies the extract output current to the pixel capacitance through a negative feedback loop to correct the input voltage while the video signal is being sampled in the pixel capacitance.

[0016] According to an embodiment of the present invention, the pixel circuit and the display apparatus with an integrated array of such pixel circuits have the correcting section for correcting variations of the threshold voltage and the mobility according to a voltage drive system. The pixel circuit with the correcting section includes a plurality of thin-film transistors (TFTs) integrated on an insulating substrate of glass or the like. According to an embodiment of the present invention, the additional capacitance is provided by a thin-film capacitor on the insulating substrate. The additional capacitance is connected parallel to the capacitance of the light-emitting device. With this arrangement, the total capacitance that is used to correct the mobility is of a large value. As a result, an operating time requisite to correct mobility variations can be set to a long time. Specifically, a setting margin for a mobility correcting period can be increased to stabilize the corrective action of the pixel circuit.

[0017] If the display apparatus is a color display apparatus, then each of the pixel circuits has either one of a red light-emitting device, a green light-emitting device, and a blue light-emitting device. Generally, the light-emitting devices have different light-emitting areas and different light-emitting materials for the respective colors, and also have different capacitive components correspondingly. The additional capacitances in the light-emitting devices may be varied to set the mobility correcting period to the same value for different color pixels. As a common time requisite for correcting the mobility is provided for all the pixels, operation of the pixel array can easily be controlled.

[0018] If a white balance is to be achieved among the red (R) pixel, the green (G) pixel, and the blue (B) pixel or the

light-emitting devices in the R, G, B pixels have widely different characteristics, the additional capacitances requisite in the respective R, G, B pixels may differ largely from each other. In such a case, it is possible to assign portions of the additional capacitances among the R, G, B pixels. Specifically, if the capacitance value of the additional capacitance in the pixel circuit of a certain color suffers a shortage, then a portion of the capacitance value of the additional capacitance in an adjacent pixel circuit of another color is assigned to make up for the shortage. The display apparatus including the R, G, B pixel circuits can thus have a common mobility correcting period for the color pixels.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019]

Fig. 1 is a block diagram showing a basic arrangement of a display apparatus according to an embodiment of the present invention;
Fig. 2 is a circuit diagram, partly in block form, of a display apparatus according to a first embodiment of the present invention;
Figs. 3A and 3B are plan views showing pixels of the display apparatus according to the first embodiment;
Fig. 4 is a circuit diagram of a pixel circuit of the display apparatus shown in Fig. 2;
Fig. 5 is a timing chart illustrative of operation of the pixel circuit shown in Fig. 4;
Fig. 6 is a circuit diagram illustrative of operation of the pixel circuit shown in Fig. 4;
Fig. 7 is a graph illustrative of operation of the pixel circuit shown in Fig. 4;
Fig. 8 is a circuit diagram illustrative of operation of the pixel circuit shown in Fig. 4;
Fig. 9 is a graph showing operating characteristics of a drive transistor included in the pixel circuit shown in Fig. 4;
Fig. 10 is a circuit diagram, partly in block form, of a modification of the display apparatus according to the first embodiment shown in Fig. 2;
Fig. 11 is a circuit diagram, partly in block form, of a display apparatus according to a second embodiment of the present invention;
Fig. 12 is a timing chart illustrative of operation of a pixel circuit included in the display apparatus shown in Fig. 11;
Fig. 13 is a circuit diagram illustrative of operation of the pixel circuit included in the display apparatus shown in Fig. 11;
Fig. 14 is a fragmentary plan view of a display apparatus according to a third embodiment of the present invention;
Fig. 15 is a fragmentary plan view of a display apparatus according to a fourth embodiment of the present invention;
Fig. 16 is a circuit diagram, partly in block form, of the display apparatus according to the fourth embodiment shown in Fig. 15; and
Fig. 17 is a circuit diagram, partly in block form, of a modification of the display apparatus according to the fourth embodiment shown in Fig. 16.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] Fig. 1 shows in block form a basic arrangement of a display apparatus according to an embodiment of the present invention. As shown in Fig. 1, the display apparatus, which includes an active-matrix display apparatus, has a pixel array 1 serving as a main unit and surrounding circuits. The surrounding circuits include a horizontal selector 3, a write scanner 4, a driver scanner 5, and a correcting scanner 7. The pixel array 1 includes a matrix of pixels R, G, B positioned at points of intersection between row scanning lines WS and column signal lines SL. For displaying color images, the pixel array 1 is made up of pixels R, G, B in three primaries. However, the present invention is not limited to using such pixels. Each of the pixels R, G, B includes a pixel circuit 2. The signal lines SL are driven by the horizontal selector 3. The horizontal selector 3 serves as a signal unit for supplying a video signal to the signal lines SL. The scanning lines WS are scanned by the write scanner 4. The display apparatus also has other scanning lines DS, AZ extending parallel to the scanning lines WS. The scanning lines DS are scanned by the drive scanner 5. The scanning lines AZ are scanned by the correcting scanner 7. The write scanner 4, the drive scanner 5, and the correcting scanner 7 jointly make up a scanning unit for successively scanning rows of pixels in each horizontal period. When each of the pixel circuits 2 is selected by one of the scanning lines WS, it samples a video signal from the corresponding signal line SL. When each of the pixel circuits 2 is selected by one of the scanning lines DS, it energizes a light-emitting device incorporated in the pixel circuit 2 depending on the sampled video signal. In addition, when each of the pixel circuits 2 is selected by one of the scanning lines AZ, it performs a predetermined correcting process.

[0021] The pixel array 1 is usually formed on an insulating substrate such as of glass in the form of a flat panel. Each of the pixel circuits 2 includes amorphous silicon thin-film transistors (TFTs) or low-temperature polysilicon TFTs. If each of the pixel circuits 2 includes amorphous silicon TFTs, then the scanner unit is constructed as a TAB separate from the flat panel and is connected to the flat panel by flexible cables. If each of the pixel circuits 2 includes low-temperature polysilicon TFTs, then since the signal unit and the scanner unit can also be constructed of low-temperature polysilicon

TFTs, the pixel array, the signal unit, and the scanner unit can integrally be formed on the flat panel.

[0022] Fig. 2 is a circuit diagram, partly in block form, of an active-matrix display apparatus according to a first embodiment of the present invention. As shown in Fig. 2, the active-matrix display apparatus has a pixel array 1 serving as a main unit and surrounding circuits. The surrounding circuits include a horizontal selector 3, a write scanner 4, a driver scanner 5, a first correcting scanner 71, and a second correcting scanner 72. The pixel array 1 includes a matrix of pixel circuits 2 positioned at points of intersection between row scanning lines WS and column signal lines SL. For an easier understanding of the first embodiment, only one pixel circuit 2 is shown at an enlarged scale. The signal lines SL are driven by the horizontal selector 3. The horizontal selector 3 serves as a signal unit for supplying a video signal to the signal lines SL. The scanning lines WS are scanned by the write scanner 4. The display apparatus also has other scanning lines DS, AZ1, AZ2 extending parallel to the scanning lines WS. The scanning lines DS are scanned by the drive scanner 5. The scanning lines AZ1 are scanned by the first correcting scanner 71. The scanning lines AZ2 are scanned by the second correcting scanner 72. The write scanner 4, the drive scanner 5, the first correcting scanner 71, and the second correcting scanner 72 jointly make up a scanning unit for successively scanning rows of pixels in each horizontal period. When each of the pixel circuits 2 is selected by one of the scanning lines WS, it samples a video signal from the corresponding signal line SL. When each of the pixel circuits 2 is selected by one of the scanning lines DS, it energizes a light-emitting device EL incorporated in the pixel circuit 2 depending on the sampled video signal. In addition, when each of the pixel circuits 2 is selected by ones of the scanning lines AZ1, AZ2, it performs a predetermined correcting process.

[0023] The pixel circuit 2 shown in Fig. 2 includes five thin-film transistors Tr1 through Tr4, Trd, two capacitors Cs, Csub, and a light-emitting device EL. The capacitor Cs is a pixel capacitance, and the capacitor Csub is an additional capacitance provided according to an embodiment of the present invention. For a better understanding of the present invention, the capacitor of the light-emitting device EL is illustrated as a capacitor Coled. Each of the transistors Tr1 through Tr3, Trd includes an N-channel polysilicon TFT, and the transistor Tr4 includes a P-channel polysilicon TFT. As described above, the capacitor Cs is the pixel capacitance of the pixel circuit 2. The light-emitting device EL includes a diode-type organic EL device having an anode and a cathode, for example. According to an embodiment of the present invention, however, the light-emitting device EL is not limited to the diode-type organic EL device, but may generally be any of all current-driven devices capable of emitting light.

[0024] The transistor Trd, which is a drive transistor that plays a main role in the pixel circuit 2, has a gate G connected to a terminal of the pixel capacitance Cs and a source S connected to the other terminal of the pixel capacitance Cs. The gate G of the drive transistor Trd is also connected to a reference potential Vss1 through the transistor Tr2, which serves as a switching transistor. The drain of the drive transistor Trd is connected to a power supply potential Vcc through the transistor Tr4, which serves as a switching transistor. The switching transistor Tr2 has a gate connected to the scanning line AZ1. The switching transistor Tr4 has a gate connected to the scanning line DS. The light-emitting device EL has an anode connected to the source S of the drive transistor Trd and a cathode connected to ground, whose ground potential is represented by Vcath. The transistor Tr3, which serves as a switching transistor, is connected between the source S of the drive transistor Trd and a predetermined reference potential Vss2. The switching transistor Tr3 has a gate connected to the scanning line AZ2. The transistor Tr1, which serves as a sampling transistor, is connected between the signal line SL and the gate G of the drive transistor Trd. The sampling transistor Tr1 has a gate connected to the scanning line WS. The additional capacitance Csub has a terminal connected to the anode of the light-emitting device EL and the other terminal connected to ground. According to the present embodiment, the additional capacitance Csub is connected parallel to the capacitor Coled of the light-emitting device EL.

[0025] In response to a control signal WS supplied from the scanning line WS, the sampling transistor Tr1 is turned on and samples a video signal Vsig supplied from the signal line SL into the pixel capacitance Cs. Depending on the sampled video signal Vsig, the pixel capacitance Cs applies an input voltage Vgs to the gate of the drive transistor Trd. The drive transistor Trd supplies an output current Ids depending on the input voltage Vgs to the light-emitting device EL. The output current (drain current) Ids is dependent on the carrier mobility μ in the channel region of the drive transistor Trd. The output current Ids supplied from the drive transistor Trd causes the light-emitting device EL to emit light at a luminance level depending on the video signal Vsig.

[0026] According to a feature of the present invention, the pixel circuit 2 has a correcting section made up of the switching transistors Tr1 through Tr4, for correcting the input voltage Vgs depending on the video signal Vsig sampled in the pixel capacitance Cs in order to cancel out the dependency of the output current Ids on the carrier mobility μ. Specifically, the correcting section (Tr2 through Tr4) operate depending on control signals AZ1, AZ2 supplied from the scanning lines AZ1, AZ2 to extract the output current Ids from the drive transistor Trd and introduce the output current Ids into the capacitance Coled of the light-emitting device EL and the pixel capacitance Cs for thereby correcting the input voltage Vgs. Since the pixel circuit 2 has the additional capacitance Csub added to the capacitance Coled of the light-emitting device EL, part of the output current Ids from the drive transistor Trd flows into the additional capacitance Csub, thus giving a time margin to the operation of the correcting section (Tr2 through Tr4). While the video signal Vsig is being sampled in the pixel capacitance Cs, the correcting section (Tr2 through Tr4) extracts the output current Ids

from the drive transistor Trd and supplies the output current Ids back to the pixel capacitance Cs through a ' negative feedback loop, thereby correcting the input voltage Vgs.

[0027] According to the present embodiment, the output current Ids of the drive transistor Trd is dependent on the threshold voltage Vth as well as the carrier mobility μ in the carrier region. In order to cancel out the dependency of the output current Ids on the carrier mobility μ, the correcting section (Tr2 through Tr4) detects the threshold voltage Vth of the drive transistor Trd in advance and adds the detected threshold voltage Vth to the input voltage Vgs.

[0028] Figs. 3A and 3B show in plan layouts of the thin-film transistors TFTs, the pixel capacitance Cs, and the additional capacitance Csub of each of the pixel circuits 2. Fig. 3A shows the layout that is free of the additional capacitance Csub, and Fig. 3B shows the layout that includes the additional capacitance Csub according to an embodiment of the present invention. The sampling transistor Tr1, the drive transistor Trd, and the correcting section (Tr2 through Tr4) include the thin-film transistors TFTs formed on the insulating substrate, and the pixel capacitance Cs and the additional capacitance Csub include thin-film capacitors also formed on the insulating substrate. In the illustrated layout, the additional capacitance Csub has a terminal connected to the pixel capacitance Cs through an anode contact and the other terminal connected to a given fixed potential. The fixed potential is selected from the ground potential Vcath on the cathode of the light-emitting device EL, or the positive power supply potential Vcc or negative power supply potential of the pixel circuit 2. In the embodiment shown in Fig. 2, the other terminal of the additional capacitance Csub is connected to the ground potential. The pixel circuit 2 shown in Fig. 3B is of a laminated structure including a lower layer which contains the thin-film transistors TFTs, the pixel capacitance Cs, and the additional capacitance Csub and an upper layer connected to the light-emitting device EL. For an easier understanding of the present invention, the light-emitting device EL is omitted from illustration in Figs. 3A and 3B. Actually, the light-emitting device EL is connected to the pixel circuit 2 through an anode contact.

[0029] Fig. 4 shows the pixel circuit 2 of the display apparatus shown in Fig. 2. Fig. 4 also shows the video signal Vsig sampled by the sampling transistor Tr1, the input voltage Vgs and output current Ids of the drive transistor Trd, the capacitor Coled of the light-emitting device EL, and the additional capacitance Csub for an easier understanding of the present invention.

[0030] Fig. 5 is a timing chart illustrative of operation of the pixel circuit shown in Fig. 4. Operation of the pixel circuit shown in Fig. 4 will be described in specific detail below with reference to Fig. 5. Fig. 5 shows the waveforms of control signals that are applied to the scanning lines WS, AZ1, AZ2, DS as the waveforms change along a time axis T. For the sake of brevity, the control signals are denoted by reference characters which are identical to the reference characters of the corresponding scanning lines. Since the transistors Tr1, Tr2, Tr3 are N-channel transistors, they are turned on when the scanning lines WS, AZ1, AZ2 are high in level, and turned off when the scanning lines WS, AZ1, AZ2 are low in level. On the other hand, since the transistor Tr4 is P-channel transistor, it is turned off when the scanning line DS is high in level, and turned on when the scanning line DS is low in level. Fig. 5 also shows potential changes of the gate G and source S of the drive transistor Trd as well as the waveforms of the control signals WS, AZ1, AZ2, DS.

[0031] Fig. 5 shows one field (1f) from times T1 to T8. The rows of the pixel array are successively scanned once during one field. Fig. 5 shows the waveforms of the control signals WS, AZ1, AZ2, DS which are applied to the pixels of one row.

[0032] At time T0 prior to the field (1f), all the control signals WS, AZ1, AZ2, DS are low in level. Therefore, the N-channel transistors Tr1, Tr2, Tr3 are turned off, and only the P-channel transistor Tr4 is turned on. Since the drive transistor Trd is connected to the power supply potential Vcc through the transistor Tr4, the drive transistor Trd supplies the output current Ids depending on the input voltage Vgs to the light-emitting device EL. Accordingly, the light-emitting device EL emits light at time T0. At this time, the input voltage Vgs that is applied to the drive transistor Trd is represented by the difference between the gate potential (G) and the source potential (S).

[0033] At time T1 when the field (1f) begins, the control signal DS goes high, turning off the transistor Tr4. The drive transistor Trd is disconnected from the power supply potential Vcc, whereupon the light-emitting device EL stops emitting light, i.e., enters a non-emission period. At time T1, therefore, all the transistors Tr1 through Tr4 are turned off.

[0034] At time T2, the control signals AZ1, AZ2 go high, turning on the switching transistors Tr2, Tr3. As a result, the gate G of the drive transistor Trd is connected to the reference potential Vss1 and the source S thereof to the reference potential Vss2. By satisfying Vss1 - Vss2 > Vth and Vss1 - Vss2 = Vgs > Vth, the pixel circuit is prepared to correct the threshold voltage Vth at time T3. Stated otherwise, period T2 to T3 corresponds to a reset period of the drive transistor Trd. If the threshold voltage of the light-emitting device EL is represented by VthEL, then VthEL > Vss2 is satisfied. Therefore, a negative bias is applied to the light-emitting device EL, thereby reversely biasing the light-emitting device EL. The reversely biased state of the light-emitting device EL is requisite to properly correct the threshold voltage Vth and correcting the mobility subsequently.

[0035] At time T3, the control signal AZ2 is made low in level and immediately thereafter the control signal DS is also made low in level. The transistor Tr3 is turned off, and the transistor Tr4 is turned on. As a result, the drain current Ids flows into the pixel capacitance Cs to start correcting the threshold voltage Vth. At this time, the gate G of the drive transistor Trd is held at the reference potential Vss1, and the drain current Ids keeps flowing until the drive transistor

Trd is cut off. When the drive transistor Trd is cut off, the source potential (S) of the drive transistor Trd becomes equal to Vss1 - Vth. At time T4 after the drain current Ids is cut off, the control signal DS goes high again, turning off the switching transistor Tr4. The control signal AZ1 then goes low, turning off the switching transistor Tr2. As a consequence, the threshold voltage Vth is held in the pixel capacitance Cs. The period from time T3 to time T4 is thus a period for detecting the threshold voltage Vth of the drive transistor Trd. The period from time T3 to time T4 is referred to as a Vth correcting period.

[0036] After the threshold voltage Vth is corrected, the control signal WS goes high at time T5, turning on the sampling transistor Tr1 to write the video signal Vsig into the pixel capacitance Cs. The pixel capacitance Cs is sufficiently smaller than the equivalent capacitance Coled of the light-emitting device EL. As a result, most of the video signal Vsig is written into the pixel capacitance Cs. Precisely, the difference Vsig - Vss1 between the video signal Vsig and the reference potential Vss1 is written into the pixel capacitance Cs. Therefore, the voltage Vgs between the gate G and source S of the drive transistor Trd reaches a level (Vsig - Vss1 + Vth) which is the sum of the previously detected and held threshold voltage Vth and the presently sampled difference Vsig - Vss1. If it is assumed that Vss1 = 0 V for the sake of brevity, then the gate-to-source voltage Vgs has a level Vsig + Vth as indicated by the timing chart shown in Fig. 5. The video signal Vsig is sampled until T7 when the control signal WS goes low again. The period from time T5 to time T7 corresponds to the sampling period.

[0037] At time T6 prior to time T7 when the sampling period is ended, the control signal DS goes low, turning on the switching transistor Tr4. Since the drive transistor Trd is connected to the power supply potential Vcc, the pixel circuit goes from the non-emission period to an emission period. In the period from time T6 to time T7 in which the sampling transistor Tr1 remains turned on and the switching transistor Tr4 is turned on, the mobility of the drive transistor Trd is corrected. Specifically, according to the present embodiment, the mobility is corrected in the period from time T6 to time T7 where a rear portion of the sampling period and a front portion of the emission period overlap each other. In the front portion of the emission period wherein the mobility is corrected, the light-emitting device EL does not emit light because it is actually reversely biased. In the mobility correcting period from time T6 to time T7, the gate G of the drive transistor Trd is fixed to the level of the video signal Vsig, and the drain current Ids flows through the drive transistor Trd. By setting Vss1 - Vth < VthEL, the light-emitting device EL is reversely biased. Therefore, the light-emitting device EL does not exhibit diode characteristics, but simple capacitance characteristics. Consequently, the drain current Ids flowing through the drive transistor Trd is written into a capacitance C = Cs + Coled + Csub which is the combination of the pixel capacitance Cs, the equivalent capacitance Coled of the light-emitting device EL, and the additional capacitance Csub. The source voltage (S) of the drive transistor Trd rises by an increase ΔV as shown in Fig. 5. The increase ΔV is subtracted from the gate-to-source voltage Vgs that is held by the pixel capacitance Cs, the drive transistor Trd is placed in a negative feedback loop. By thus supplying the output current Ids of the drain transistor Trd across the input voltage Vgs of the drain transistor Trd through the negative feedback loop, the mobility μ can be corrected. The negative feedback quantity ΔV can be optimized by adjusting the time duration of the mobility correcting period (T6 to T7).

[0038] At time T7, the control signal WS goes low, turning off the sampling transistor Tr1. The gate G of the drive transistor Trd is disconnected from the signal line SL. As the video signal Vsig is no longer applied, the gate potential (G) of the drive transistor Trd increases together with the source potential (S) thereof. While the gate potential (G) and the source potential (S) are rising, the gate-to-source voltage Vgs keeps the value (Vsig - ΔV + Vth). As the source potential (S) rises, the light-emitting device EL is no longer reversely biased. When the output current Ids flows into the light-emitting device EL, the light-emitting device EL actually starts emitting light. By substituting Vsig - ΔV + Vth in Vgs of the above transistor characteristic equation (1), the relationship between the drain current Ids and the gate voltage Vgs is given by the following equation (2):

$$Ids = k\mu(Vgs - Vth)^2 = k\mu(Vsig - \Delta V)^2 \quad \cdots(2)$$

where k = (1/2)(W/L)Cox. It can be understood from the characteristic equation (2) that the term of Vth is canceled and the output current Ids supplied to the light-emitting device EL is not dependent on the threshold voltage Vth of the drive transistor Trd. Basically, the drain current Ids is determined by the signal voltage Vsig of the video signal. In other words, the light-emitting device EL emits light at a luminance level depending on the video signal Vsig. The video signal Vsig is corrected by the feedback quantity ΔV. The corrective quantity ΔV acts to cancel the effect of the mobility μ in the coefficient part of the characteristic equation (1). Therefore, the drain current Ids is essentially dependent on only the video signal Vsig.

[0039] Finally at time T8, the control signal DS goes high, turning off the switching transistor Tr4. The light-emitting device EL stops emitting light, and the field (1f) is put to an end. Then, the Vth correcting process, the mobility correcting process, and the light-emitting process are repeated in a next field.

[0040] Fig. 6 is a circuit diagram of the pixel circuit 2 in the mobility correcting period T6 to T7. As shown in Fig. 6, in

the mobility correcting period T6 to T7, the sampling transistor Tr1 and the switching transistor Tr4 are turned on, and the remaining transistors Tr2, Tr3 are turned off. At this time, the source potential (S) of the switching transistor Tr4 is represented by Vss1 - Vth. The source potential (S) is also the anode potential of the light-emitting device EL. As described above, by setting Vss1 - Vth < VthEL, the light-emitting device EL is reversely biased and exhibits simple capacitance characteristics, rather than diode characteristics. Consequently, the drain current Ids flowing through the drive transistor Trd flows into the combined capacitance C = Cs + Coled + Csub which is the combination of the pixel capacitance Cs, the equivalent capacitance Coled of the light-emitting device EL, and the additional capacitance Csub. Stated otherwise, part of the output current Ids flows into the pixel capacitance Cs through a negative feedback loop, correcting the mobility.

[0041] Fig. 7 is a graph illustrating the transistor characteristic equation (2). The vertical axis of the graph represents Ids and the horizontal axis Vsig. Fig. 7 also shows the transistor characteristic equation (2) below the graph. In Fig. 7, characteristic curves of pixels 1, 2 are plotted for comparison. The mobility μ of the drive transistor of the pixel 1 is relatively large. Conversely, the mobility μ of the drive transistor of the pixel 2 is relatively small. With the drive transistors including polysilicon thin-film transistors, the mobility μ inevitably varies from pixel to pixel. For example, when the video signal Vsig of the same level is written into the pixels 1, 2, if no mobility is corrected at all, then an output current Ids1' flowing through the pixel 1 having the larger mobility μ is greatly different from the an output current Ids2' flowing through the pixel 2 having the smaller mobility μ. Since the output currents Ids of the pixels 1, 2 differ greatly from each other due to the different mobilities p, the image uniformity over the screen is greatly impaired.

[0042] According to an embodiment of the present invention, mobility variations are canceled by supplying the output current across the input voltage through a negative feedback loop. As can be seen from the transistor characteristic equations, as the mobility is greater, the drain current Ids becomes larger. Therefore, the negative feedback quantity ΔV is larger as the mobility is greater. As shown in the graph of Fig. 7, the negative feedback quantity $\Delta V1$ of the pixel 1 having the larger mobility μ is greater than the negative feedback quantity $\Delta V2$ of the pixel 2 having the smaller mobility μ. Therefore, the negative feedback is greater as the mobility μ is larger, making it possible to suppress mobility variations. As shown in Fig. 7, if the mobility is corrected by $\Delta V1$ for the pixel 1 having the larger mobility μ, then the output current largely drops from Ids1' to Ids1. On the other hand, since the corrective quantity $\Delta V2$ for the pixel 2 having the smaller mobility μ is smaller, the drop of the output current from Ids2' to Ids2 is not so large. As a result, the output current Ids1 and the output current Ids2 are essentially equal to each other, canceling mobility variations. Because mobility variations are canceled in the full range of Vsig from a black level to a white level, the image uniformity over the screen becomes very high. The above mobility correction is summarized as follows: If there are pixels 1, 2 having different mobilities, then the corrective quantity $\Delta V1$ for the pixel 1 having the larger mobility is larger than the corrective quantity $\Delta V2$ for the pixel 2 having the smaller mobility. In other words, as the mobility is larger, the corrective quantity ΔV is greater, and the reduction in the output current Ids is greater. Thus, currents flowing through pixels having different mobilities are uniformized, thereby correcting mobility variations.

[0043] A numerical analysis of the above mobility correction will be described below with reference to Fig. 8. As shown in Fig. 8, while the transistors Tr1, Tr4 are being turned on, an analysis is performed using the source potential (S) of the drive transistor Trd as a variable V. If the source potential (S) of the drive transistor Trd is represented by V, then the drain current Ids flowing through the drive transistor Trd is expressed by the following equation (3):

$$I_{ds} = k\mu(V_{gs} - V_{th})^2 = k\mu(V_{sig} - V - V_{th})^2 \quad \cdots(3)$$

[0044] Because of the relationship between the drain current Ids and the capacitance C (= Cs + Coled + Csub), the relationship Ids = dQ/dt = CdV/dt is satisfied as indicated by the following equation (4):

$$\text{From } I_{ds} = \frac{dQ}{dt} = C\frac{dV}{dt}, \int \frac{1}{C}dt = \int \frac{1}{I_{ds}}dV \quad \cdots(4)$$

$$\Leftrightarrow \int_0^t \frac{1}{C}dt = \int_{-Vth}^{V} \frac{1}{k\mu(V_{sig} - V_{th} - V)^2}dV$$

$$\Leftrightarrow \frac{k\mu}{C}t = [\frac{1}{V_{sig} - V_{th} - V}]_{-Vth}^{V} = \frac{1}{V_{sig} - V_{th} - V} - \frac{1}{V_{sig}}$$

$$\Leftrightarrow V_{sig} - V_{th} - V = \frac{1}{\frac{1}{V_{sig}} + \frac{k\mu}{C}t} = \frac{V_{sig}}{1 + V_{sig}\frac{k\mu}{C}t}$$

[0045] Then, the equation (3) is substituted in the equation (4), and both sides are integrated. The source voltage V has an initial state represented by - Vth, and the mobility variation correction time (T6 to T7) is represented by t. By solving the differential equation, the pixel current in the mobility variation correction time t is given by the following equation (5):

$$I_{ds} = k\mu(\frac{V_{sig}}{1 + V_{sig}\frac{k\mu}{C}t})^2 \quad \cdots(5)$$

[0046] Fig. 9 shows a graphic representation of the equation (5). The vertical axis of the graph shown in Fig. 9 represents the output current Ids, and the horizontal axis the video signal Vsig. Parameters include mobility correcting periods t = 0 us, 2.5 us, and 5 us and also a relatively large motility 1.2 μ and a relatively small mobility 0.8 μ. The capacitance C is represented by Cs + Coled only, with Csub being zero. It can be seen from Fig. 9 that the mobility variation is sufficiently corrected with t = 2.5 us compared with t = 0 us for essentially no mobility correction. While Ids varies by 40% with no mobility correction, Ids varies by 10% with mobility correction. However, if the correcting period is increased with t = 5 us, then the output current Ids varies greatly due to different mobilities μ. Consequently, the correcting period t needs to be set to an appropriate value in order to perform appropriate mobility correction. In the graph shown in Fig. 9, the optimum correcting period t is in the vicinity of t = 2.5 us. In view of the delay of the control signal (gate pulse) applied to the gate of the transistor, however, correcting period t = 2.5 us is not necessarily pertinent. Judging from the operating characteristics of the transistor, the correcting period t should be as long as possible. In the equation (5) described above, t is included as t/C. In order to increase t without affecting the right side of the equation (5), the value of C may be increased while keeping the value of t/C constant. According to an embodiment of the present invention, the additional capacitance Csub is introduced into the pixel circuit in addition to the pixel capacitance Cs and the light-emitting device capacitance Coled which make up the capacitance C. The additional capacitance Csub makes the total capacitance C greater and increases the correcting period t correspondingly, so that it is possible to increase the time margin of operation of the correcting section which is included in the pixel circuit.

[0047] In the mobility correcting period, as described above and as shown in the timing chart of FIG. 5, while the gate potential is being fixed, the output current Ids is caused to flow through the drive transistor Trd, writing electric charges into the pixel capacitance Cs and the light-emitting device capacitance Coled. The value of the output current Ids is as indicated by the equation (5). As the equation (5) does not contain a term of Vth, the mobility can be corrected without being affected by Vth. Specifically, since the mobility μ is included in a term in the denominator on the right side of the equation (5), as the mobility μ is larger, the output current Ids is smaller, and as the mobility μ is smaller, the output current Ids is larger, thereby correcting mobility variations.

[0048] The mobility correcting term of the equation (5) includes t/C where t represents the mobility correcting period and C the combined capacitance of the pixel capacitance Cs, the light-emitting device capacitance Coled, etc. The relationship between different mobility correcting periods t and output current variations is shown in the graph of Fig. 9. As described above, it is known that the correcting capability is not sufficient if the mobility correcting period t is too short

or too long. In the graph shown in Fig. 9, the mobility correcting period t = 2.5 us is of an essentially optimum level. However, in view of the delay in the gate pulse, the mobility correcting period t = 2.5 us may often be too short. It is practically difficult to control the mobility correcting period t accurately.

[0049] According to an embodiment of the present invention, the capacitance C used to correct the mobility is increased for making the mobility correction easy. The capacitance C may be increased by increasing the light-emitting device capacitance Coled or the pixel capacitance Cs or adding the additional capacitance Csub. The light-emitting device capacitance Coled is determined by the pixel size, the pixel aperture ratio, and the basic properties of the organic EL material of the light-emitting device, and hence it is difficult be increased simply. Increasing the pixel capacitance Cs results in an increase in the anode potential at the time the signal voltage is written. Specifically, the increase in the anode potential is determined by Cs/(Cs + Coled) x ΔV. Therefore, the input signal voltage gain represented by Coled/(Cs + Coled) is lowered. In order to make up for the reduction in the input signal voltage gain, the amplitude level of the video signal has to be increased, putting a burden on the driver accordingly. According to an embodiment of the present invention, in order to increase the capacitance C, the additional capacitance Csub is formed on the insulating substrate on which TFTs are integrated, and connected parallel to the light-emitting device capacitance Coled. In this manner, while increasing the input gain (Coled + Csub)/(Cs + Coled + Csub), the value of the total capacitance C can be increased, and the optimum mobility correcting period t can be set to a long value, making it possible to increase the margin for setting the mobility correcting period. In the pixel circuit according to the first embodiment, the drive transistor Trd is of the N-channel type and the other switching transistors are of both the N-channel type and the P-channel type. However, the transistors may be of either the N-channel type or the P-channel type.

[0050] Fig. 10 is a circuit diagram, partly in block form, of a modification of the display apparatus according to the first embodiment shown in Fig. 2. In the first embodiment, one of the terminals of the additional capacitance Csub is connected to the anode of the light-emitting device EL, and the other terminal to the ground potential Vcath on the cathode of the light-emitting device EL. According to the present modification, the other terminal of the additional capacitance Csub is connected to the power supply potential Vcc. According to an embodiment of the present invention, the other terminal of the additional capacitance Csub may be connected to a fixed potential. The fixed potential may be selected from the ground potential Vcath on the cathode of the light-emitting device EL, or the positive power supply potential Vcc or negative power supply potential of the pixel circuit 2. In some cases, the additional capacitance Csub may be connected parallel to the pixel capacitance Cs to increase the total capacitance Cs. However, since connecting the additional capacitance Csub parallel to the pixel capacitance Cs would reduce the gain of the input signal, it is not desirable to connect the additional capacitance Csub parallel to the pixel capacitance Cs.

[0051] Fig. 11 is a circuit diagram, partly in block form, of a display apparatus according to a second embodiment of the present invention. For an easier understanding of the second embodiment, those parts of the display apparatus according to the second embodiment which correspond to those of the display apparatus according to the first embodiment shown in Fig. 2 are denoted by corresponding reference characters. As shown in Fig. 11, the display apparatus according to the second embodiment has a pixel array 1 and surrounding circuits. The surrounding circuits include a horizontal selector 3, a write scanner 4, a dive scanner 5, a first correcting scanner 71, and a second correcting scanner 72. The pixel array 1 includes a matrix of pixel circuits 2. For an easier understanding of the second embodiment, only one pixel circuit 2 is shown at an enlarged scale. The pixel circuit 2 includes six transistors Tr1, Trd, Tr3 through Tr6, three capacitors Cs1, Cs2, Csub, and a light-emitting device EL. All of the transistors are of the N-channel type. The drive transistor Trd, which plays a mail role in the pixel circuit 2, has a gate G connected to terminals of the capacitors Cs1, Cs2. The capacitor Cs1 serves as a coupling capacitor interconnecting the input and output sides of the pixel circuit 2. The capacitor Cs2 serves as a pixel capacitance into which a video signal is written through the coupling capacitor Cs1. The drive transistor Trd has a source S connected to the other terminal of the pixel capacitance Cs2, and also to the light-emitting device EL. The light-emitting device EL includes a diode-type device having an anode connected to the source S of the drive transistor Trd and a cathode K to the ground potential Vcath. The capacitor Csub is an additional capacitance according to an embodiment of the present invention and is connected between the source S of the drive transistor Trd and the ground potential Vcath. The switching transistor Tr3 is connected between the source S of the drive transistor Trd and the predetermined reference potential Vss2. The switching transistor Tr3 has a gate connected to the scanning line AZ2. The drain of the drive transistor Trd is connected to the power supply Vcc through the switching transistor Tr4. The switching transistor Tr4 has a gate connected to the scanning line DS. In addition, the switching transistor Tr5 is interposed between the gate G and drain of the drive transistor Trd. The switching transistor Tr5 has a gate connected to the scanning line AZ1. The sampling transistor Tr1 on the input side is connected between the signal line SL and the other terminal of the coupling capacitance Cs1. The sampling transistor Tr1 has a gate connected to the scanning line WS. The transistor Tr6 is interposed between the other terminal of the coupling capacitance Cs1 and the predetermined reference potential Vss1. The transistor Tr6 has a gate connected to the scanning line AZ1.

[0052] Fig. 12 is a timing chart illustrative of operation of the pixel circuit shown in Fig. 11. Fig. 11 shows the waveforms of control signals WS, DS, AZ1, AZ2 as the waveforms change along the time axis T, and also shows changes of the gate potential (G) and the source potential (S) of the drive transistor Trd. At time T1 when the field (1f) starts, the control

signals WS, AZ1, AZ2 are low in level, and only the control signal DS is high in level. At time T1, therefore, only the switching transistor Tr4 is turned on, and the remaining transistors Tr1, Tr3, Tr5, Tr6 are turned off. At this time, since the drive transistor Trd is connected to the power supply Vcc through the energized switching transistor Tr4, a predetermined drain current Ids flows into the light-emitting device EL, which emits light.

[0053] At time T2, the control signals AZ1, AZ2 go high, turning on the transistors Tr5, Tr6. As the gate G of the drive transistor Trd is connected to the power supply Vcc through the energized transistor Tr5, the gate potential (G) increases sharply.

[0054] At subsequent time T3, the control signal DS goes low in level, turning off the transistor Tr4. Since the current from the power supply to the drive transistor Trd is not cut off, the drain current Ids is reduced. The source potential (S) and the gate potential (G) are lowered. No drain current flows when the potential difference between the source potential (S) and the gate potential (G) reaches the threshold voltage Vth. At this time, the threshold voltage Vth is held in the pixel capacitance Cs2. The threshold voltage Vth held in the pixel capacitance Cs2 is used to cancel the threshold voltage of the drive transistor Trd. Since the switching transistor Tr3 has been turned on, the source S of the drive transistor Trd is connected to the reference potential Vss2 through the switching transistor Tr3. The reference potential Vss2 is set to a level lower than the threshold voltage of the light-emitting device EL, holding the light-emitting device EL reversely biased.

[0055] Subsequently at time T4, the control signal AZ1 goes low in level, turning off the transistors Tr5, Tr6, fixing the threshold voltage Vth written in the pixel capacitance Cs2. A period from time T2 to time t4 is referred to as a Vth correcting period (T2 to T4). Since the transistor Tr6 is turned on in the Vth correcting period (T2 to T4), the other terminal of the coupling capacitance Cs1 is held at the reference potential Vss1.

[0056] At time T5, the control signals WS, AZ2 go high in level, turning on the sampling transistor Tr1. As a result, the gate G of the drive transistor Trd is connected to the signal line SL through the coupling capacitance Cs1 and the energized sampling transistor Tr1. As a result, the video signal is coupled to the gate G of the drive transistor Trd through the coupling capacitance Cs1, increasing the potential of the gate G. In the timing chart shown in Fig. 13, the voltage representative of the sum of the coupled video signal and the threshold voltage Vth is indicated by Vin. The voltage Vin is held in the pixel capacitance Cs2. Thereafter, at time T7, the control signals WS goes low in level, holding the written potential in the pixel capacitance Cs2. The period in which the video signal is written into the pixel capacitance Cs2 through the coupling capacitance Cs1 is referred to as a sampling period (T5 to T7). The sampling period (T5 to T7) usually corresponds to one horizontal period (1H).

[0057] According to the present embodiment, at time T6 prior to time T7 when the sampling period is finished, the control signal DS goes high and the control signal AZ2 goes low. As a result, the source S of the drive transistor Trd is disconnected from the reference potential Vss2, and a current flows from the drain thereof to the source S thereof. Since the sampling transistor Tr1 remains turned on, the gate potential (G) of the drive transistor Trd is kept as the video signal potential. As the output current flows through the drive transistor Trd, it charges the pixel capacitance Cs2 and the equivalent capacitance of the reversely biased light-emitting device EL. The source potential (S) of the drive transistor Trd is increased by ΔV, and the voltage Vin held in the pixel capacitance Cs2 is reduced accordingly. In other words, the output current from the source (S) is supplied across the input voltage at the gate G through a negative feedback loop during the period T6 to T7. The negative feedback quantity is indicated by ΔV. The mobility of the drive transistor Trd is corrected by the above negative feedback operation.

[0058] At subsequent time T7, the control signal WS goes low. When the video signal is not longer applied, a so-called bootstrap process is performed to increase the gate potential (G) and the source potential (S) while keeping the difference (Vin - ΔV) therebetween. As the source potential (S) rises, the reversely biased state of the light-emitting device EL is canceled, allowing the output current Ids to flow into the light-emitting device EL, which now emits light at a luminance level depending on the video signal. Thereafter, at time T8, the field (1f) is ended, and operation goes on to a next field. In the next field, the threshold voltage Vth is corrected, the signal is written, and the mobility is corrected.

[0059] Fig. 13 is a circuit diagram of the pixel circuit 2 in the mobility correcting period (T6 to T7) shown in Fig. 12. The pixel circuit 2 has a correcting section including the switching transistors Tr3, Tr4, Tr5. The correcting section corrects the input voltage Vin (Vgs) that is held in the pixel capacitance Cs2 prior to or at a beginning end of the light-emission period (T6 to T8) in order to cancel the dependency of the output current Ids on the carrier mobility μ. The correcting section operates in a portion of the sampling period (T5 to T7) depending on the control signals WS, DS that are supplied respectively from the scanning lines WS, DS, to extract the output current Ids from the drive transistor Trd while the video signal Vsig is being sampled, and supply the output current Ids to the pixel capacitance Cs2 through the negative feedback loop to correct the input voltage Vgs. In addition, in order to cancel the dependency of the output current Ids on the threshold voltage Vth, the correcting section (Tr3, Tr4, Tr5) detects the threshold voltage Vth of the drive transistor Trd in the period T2 to T4 prior to the sampling period (T5 to T7) and adds the detected threshold voltage Vth to the input voltage Vgs.

[0060] In the present embodiment, the drive transistor Trd is also an N-channel transistor and has the drain connected to the power supply Vcc and the source S to the light-emitting device EL. With this arrangement, the correcting section

extracts the output current Ids from the drive transistor Trd in the beginning portion (T6 to T7) of the light-emitting period (T6 to T8) which overlaps a rear portion of the sampling period (T5 to T7), and supplies the output current Ids to the pixel capacitance Cs2 through the negative feedback loop. At this time, the correcting section causes the output current Ids extracted from the source S of the drive transistor Trd to flow into the equivalent capacitance Coled of the light-emitting device EL and the additional capacitance Csub during the beginning portion (T6 to T7) of the light-emitting period (T6 to T8). The light-emitting device EL includes a diode-type light-emitting device having an anode connected to the source S of the drive transistor Trd and a cathode to the ground potential Vcath. In the correcting section, the light-emitting device EL is reversely biased between the anode and cathode thereof, and when the output current Ids extracted from the source S of the drive transistor Trd flows into the light-emitting device EL, the diode-type light-emitting device EL functions as the capacitance Coled. The additional capacitance Csub is connected parallel to the capacitance Coled. With this arrangement, the time for which the output current Ids flows is increased, resulting in an increase in the time margin of operation of the mobility correcting section.

[0061] Fig. 14 is a fragmentary plan view of a display apparatus according to a third embodiment of the present invention. Fig. 14 shows a set of red, green, and blue pixels. R, G, B pixel circuits 2 have a red light-emitting device, a green light-emitting device, and a blue light-emitting device, respectively. The additional capacitance Csub in each of the pixel circuits 2 has a capacitance value which is different for each light-emitting device, thereby uniformizing times requisite to operate respective correcting section in the R, G, B pixel circuits 2.

[0062] Generally, for producing R, G, B light-emitting devices, organic EL materials which the light-emitting devices are to be made of are coated differently for the colors R, G, B. Since the organic EL materials and their film thicknesses are different for the colors R, G, B, the light-emitting device capacitances Coled for the colors R, G, B are different from each other. If white organic EL light-emitting devices are colored with R, G, B filters and the R, G, B pixels have different aperture ratios, then the light-emitting device capacitances Coled for the colors R, G, B are also different from each other. Unless some countermeasures are taken, therefore, the capacitances C used to correct the mobility for the colors R, G, B are different from each other. Accordingly, the optimum mobility correcting periods t determined by the equation (5) for the R, G, B pixels are also different from each other. Consequently, it is difficult to adjust the mobility correcting periods for the R, G, B pixels to appropriate values unless some countermeasures are taken.

[0063] According to the present embodiment, the additional capacitances Csub for the respective colors R, G, B are of different values in order to employ a common optimum mobility correcting period among the R, G, B pixels. Since the light-emitting device capacitance Coled is determined by the pixel size, the pixel aperture ratio, and the basic properties of the light-emitting material, it is practically difficult to adjust the light-emitting device capacitances Coled of the respective pixels R, G, B to the same value. Unless some countermeasures are taken, therefore, the capacitances C used to correct the mobility for the colors R, G, B are different from each other, and the optimum mobility correcting periods t for the R, G, B pixels are also different from each other. According to the present embodiment, the additional capacitances Csub added to the respective R, G, B pixels are of different values.

[0064] In order for drain currents requisite for mobility correction to be identical and independent of the mobile correcting period among the different pixels, different two pixels need to satisfy the following equations (6):

$$\begin{cases} \sqrt{\dfrac{k'}{k}} = \dfrac{C'}{C} \\ \dfrac{V_{sig}}{V_{sig}'} = \dfrac{C'}{C} \end{cases} \quad \cdots(6)$$

[0065] In the equations (6), the parameters of one of the pixels are primed to distinguish those from the parameters of the other pixel. The relationship between the output current Ids and the video signal Vsig that flow through one of the pixels is expressed by the following equation (7), which is identical to the equation (5) described above:

$$I_{ds} = k\mu\left(\frac{1}{\dfrac{1}{V_{sig}} + \dfrac{k\mu}{C}t}\right)^2 \quad \cdots(7)$$

[0066] A size k' of the drive transistor, a level Vsig' of the input video signal, and a drain current Ids' flowing through a pixel having a different capacitance C are expressed by the following equation (8):

$$I_{ds}' = k'\mu\left(\frac{1}{\frac{1}{V_{sig}'} + \frac{k'\mu}{C'}t}\right)^2 \quad \cdots(8)$$

[0067] In order that Ids = Ids', the following equation (9) may be satisfied:

$$k\mu\left(\frac{1}{\frac{1}{V_{sig}} + \frac{k\mu}{C}t}\right)^2 = k'\mu\left(\frac{1}{\frac{1}{V_{sig}'} + \frac{k'\mu}{C'}t}\right)^2 \quad \cdots(9)$$

[0068] Both sides of the equation (9) are worked out to obtain the following equation (10):

$$\mu\left(\frac{\sqrt{k'}}{C'} - \frac{\sqrt{k}}{C}\right)t = \frac{1}{\sqrt{kV_{sig}}} - \frac{1}{\sqrt{k'V_{sig}'}} \quad \cdots(10)$$

[0069] In order for the condition expressed by the equation (10) not to depend on the correcting time t, the following relationships need to be satisfied:

$$\frac{\sqrt{k'}}{C'} = \frac{\sqrt{k}}{C} \text{ and } \frac{1}{\sqrt{kV_{sig}}} = \frac{1}{\sqrt{k'V_{sig}'}}$$

[0070] These relationships are rewritten into the equations (6). If C, C' satisfy the conditions given by the equations (6) with respect to different values of Vsig, k, then it is possible to provide a common correcting time t for all the pixels.

[0071] According to the above equations (6), if the dynamic range of the input video signal Vsig and the size factor k of the drive transistor Trd are identical for the R, G, B pixels, then the capacitances C in the respective R, G, B pixels need to be identical in order to provide the common correcting time t for the R, G, B pixels. The capacitance C is represented by C = Cs + Coled + Csub. The capacitance Coled has a different value for each of the R, G, B pixels. It is difficult to change greatly each of the R, G, B pixels because the capacitance Cs has a bootstrap gain. Basically, the capacitance Cs needs to be of a common value for the R, G, B pixels. According to the present embodiment, capacitances Csub having different values for the respective R, G, B pixels are connected parallel to the respective capacitances Coled. The capacitance C used for mobility correction is represented by C = Cs + Coled + Csub. In order to employ the same capacitance C in the R, G, B pixels, the value of the additional capacitance Csub is adjusted for each of the R, G, B pixels. In this manner, the equations (6) are satisfied, and the common mobility correcting time t is provided for the R, G, B pixels. Even if the size factor k of the drive transistor Trd and the dynamic range of the input video signal Vsig are different for the R, G, B pixels, the same time t optimum for mobility correction can be established for the R, G, B pixels by adjusting the additional capacitance Csub for each of the R, G, B pixels so that the equations (6) will be satisfied.

[0072] If it is necessary to adjust the white balance among the R, G, B pixels, the above equations (6) can be modified into the following equations (11):

$$\begin{cases} \sqrt{\frac{k'}{k}}\alpha = \frac{C'}{C} \\ \frac{V_{sig}}{V_{sig}'}\alpha = \frac{C'}{C} \end{cases} \quad \cdots(11)$$

[0073] If the white balance adjustment is requisite, then it is assumed that the output current for each of the R, G, B

pixels differs α times. In order that Ids' = αIds, the following equation (12) needs to be satisfied:

$$\alpha k\mu\left(\frac{1}{\frac{1}{V_{sig}}+\frac{k\mu}{C}t}\right)^2 = k'\mu\left(\frac{1}{\frac{1}{V_{sig}'}+\frac{k'\mu}{C'}t}\right)^2 \quad \cdots(12)$$

[0074] Both sides of the equation (12) are worked out. In order for the condition not to depend on the correcting time t, the following equations (13) need to be satisfied:

$$\frac{\sqrt{k'\alpha}}{C'} = \frac{\sqrt{k}}{C} \text{ and } \frac{1}{\sqrt{k\alpha}V_{sig}} = \frac{1}{\sqrt{k'}V_{sig}'} \quad \cdots(13)$$

[0075] These equations are rewritten into the equations (11). If C, C' satisfy the conditions given by the equations (11) with respect to different values of Vsig, k, then it is possible to provide a common correcting time t for all the pixels.

[0076] Fig. 15 is a fragmentary plan view of a display apparatus according to a fourth embodiment of the present invention. The display apparatus according to the fourth embodiment is basically similar to the display apparatus according to the third embodiment shown in Fig. 14. For an easier understanding of the fourth embodiment, those parts of the display apparatus according to the fourth embodiment which correspond to those of the display apparatus according to the third embodiment are denoted by corresponding reference characters. According to the fourth embodiment, a shortage of the capacitance value of the additional capacitance Csub in one of the R, G, B pixel circuits is made up for by the additional capacitance Csub in an adjacent one of the R, G, B pixel circuits. In Fig. 15, the capacitance value of the additional capacitance Csub in the red (R) pixel suffers a shortage, and such a shortage is made up for by a portion of the additional capacitance Csub in the green (G) pixel that is positioned adjacent to the red (R) pixel. Therefore, the G pixel includes both a portion of the capacitance Csub in the R pixel and the capacitance Csub in the G pixel. The additional capacitance Csub in the blue (B) pixel is sufficient and does not need to be made up for.

[0077] If the output currents of the R, G, B pixels have different level settings in order to achieve a white balance, then the conditions according to the equations (11) need to be satisfied to provide a common mobility correcting time t. Specifically, the difference between C and C' increases for white balance adjustment, and the value of the additional capacitance Csub needs to be greater accordingly. As described above, the additional capacitance Csub is provided by a thin-film capacitor formed on the insulating substrate. Each of the pixels includes thin-film transistors, another capacitor Cs, and interconnections, which pose a limitation on the area taken up by the additional capacitance Csub. Therefore, if the requisite value of the additional capacitance Csub is greater than the maximum capacitance value that one pixel can take, then it may be impossible for the pixels to have the same optimum mobility correcting time t unless some countermeasures are taken. According to the present embodiment, a shortage of the additional capacitance Csub in a pixel (the R pixel in Fig. 15) is made up for by an assigned portion of the additional capacitance Csub in an adjacent pixel (the G pixel in Fig. 15), so that the additional capacitance Csub in the R pixel will be of the requisite value. Since a portion of the additional capacitance Csub in a pixel is assigned to a shortage of additional capacitance Csub in an adjacent pixel, a uniformized optimum motility correcting time t is provided for the R, G, B pixels even if the R, G, B pixels have different white balances and the organic EL materials thereof have widely different characteristics, so that high image uniformity is achieved over the screen.

[0078] Fig. 16 is a circuit diagram, partly in block form, showing a circuit arrangement of the R pixel shown in Fig. 15. As shown in Fig. 16, the red (R) pixel circuit 2 includes an additional capacitance Csub' of an adjacent pixel as well as its own additional capacitance Csub to achieve a desired total capacitance C = Cs + Coled + Csub + Csub'.

[0079] Fig. 17 is a circuit diagram, partly in block form, of a modification of the display apparatus according to the fourth embodiment shown in Fig. 16. For an easier understanding of the present modification, those parts of the display apparatus according to the modification which correspond to those of the display apparatus according to the fourth embodiment are denoted by corresponding reference characters. The display apparatus according to the modification differs from the display apparatus according to the fourth embodiment in that whereas the other terminals of the additional capacitances Csub, Csub' are connected to the ground potential on the ground potential on the cathode of the light-emitting device EL, the other terminals of the additional capacitances Csub, Csub' are connected to the power supply Vcc in the present modification.

[0080] Although certain preferred embodiments of the present invention have been shown and described in detail, it should be understood that various changes and modifications may be made therein without departing from the scope

of the appended claims.

Claims

1. A pixel circuit arranged at a point of intersection between a first row scanning line (WS) for supplying a first control signal and a column signal line (SL) for supplying a video signal, comprising at least:

a sampling transistor (Tr1) connected to said first row scanning line (WS) and to said signal line (SL);
a pixel capacitance (Cs) connected to said sampling transistor (Tr1);
a drive transistor (Trd) having a gate (G) connected to a terminal of said pixel capacitance (Cs) and a source (S) connected to the other terminal of said pixel capacitance (Cs);
a light-emitting device (EL) having an anode terminal connected to the source of said drive transistor (Trd) and a cathode terminal connected to ground (Vcath);
wherein said sampling transistor (Tr1) is arranged to turn on in response to the first control signal supplied from said first row scanning line (WS) to sample the video signal supplied from said signal line (SL) into said pixel capacitance (Cs),
said pixel capacitance (Cs) 15 is arranged to apply an input voltage (Vgs) to the gate of said drive transistor (Trd) depending on the sampled video signal,
said drive transistor (Trd) 15 is arranged to supply an output current (Ids) depending on said input voltage (Vgs) to said light-emitting device (EL), said output current having a dependency on a carrier mobility in a channel region of said drive transistor (Trd),
said light-emitting device (EL) 15 is arranged to emit light at a luminance level depending on said video signal in response to the output current supplied from said drive transistor (Trd),
characterized in that said pixel circuit (2) further comprises:

at least a second row scanning line (AZ2) for supplying a second control signal, and a third row scanning line (DS) for supplying a third control signal,
a correcting means (Tr2-Tr4) comprising at least a first switching transistor (Tr3) and a second switching transistor (Tr4),
wherein a gate terminal of the first switching transistor (Tr3) is connected to said second row scanning line (AZ2), a drain terminal of the first switching transistor (Tr3) is connected to the source (S) of said drive transistor (Tr1), a source terminal of the first switching transistor (Tr3) is connected to a first predetermined fixed potential, a gate terminal of the second switching transistor (Tr4) is connected to said third row scanning line (DS) and the drain of the drive transistor (Trd) is arranged to be connected to a power supply potential (Vcc) through said second switching transistor (Tr4), said correcting means (Tr2-Tr4) being configured to operate in response to the second and third control signals supplied from said second and third row scanning lines (AZ2, DS) for correcting the input voltage (Vgs) sampled in said pixel capacitance (Cs) in order to cancel out the dependency of said output current (Ids) on the carrier mobility,
wherein said third control signal supplied from said third row scanning line (DS) is configured to turn on the said second switching transistor (Tr4) for a predetermined time period immediately before the said sampling transistor (Tr1) is turned off in response to the said first control signal supplied from the said first tow scanning line (WS)
wherein said correcting means (Tr2-Tr4) is arranged to operate depending on the second control signal supplied from said second row scanning line (AZ2) to extract the output current from said drive transistor (Trd) and introduce the extracted output current into a capacitance (Coled) corresponding to an equivalent capacitance of said light-emitting device (EL) when in a reverse-biased mode and into said pixel capacitance (Cs) for thereby correcting the input voltage, and
an additional capacitance (Csub) added in parallel to the equivalent capacitance (Coled) of said light-emitting device (EL), said additional capacitance (Csub) having a terminal connected to the anode terminal of said light-emitting device (EL) and another terminal connected to a second predetermined fixed potential, wherein a portion of the output current extracted from said drive transistor (Trd) flows into said additional capacitance (Csub) to give a time margin to the operation of said correcting means (Tr2-Tr4) during said predetermined time period.

2. The pixel circuit according to claim 1, wherein said sampling (Tr1) transistor, said drive transistor (Trd), and said correcting means (Tr2-Tr4) comprise thin-film transistors formed on an insulating substrate, and said pixel capacitance (Cs) and said additional capacitance (Csub) include thin-film capacitors formed on said insulating substrate.

3. The pixel circuit according to claim 1 or claim 2, wherein the output current of said drive transistor (Trd) has dependency on a threshold voltage as well as the carrier mobility in the carrier region, and said correcting means (Tr2-Tr4) detects a threshold voltage of said drive transistor (Trd) and adds the detected threshold voltage to said input voltage in advance in order to cancel out the dependency of the output current on the threshold voltage.

4. The pixel circuit according to anyone of claims 1 to 3, wherein said light-emitting device (EL) comprises a diode-type light-emitting device having an anode connected to the source of said drive transistor (Trd) and a cathode connected to the ground, said additional capacitance (Csub) having a terminal connected to the anode of said light-emitting device (EL).

5. The pixel circuit according to anyone of claims 1 to 4, wherein said second predetermined fixed potential to which another terminal of said additional capacitance (Csub) is connected is selected from a ground potential on the cathode of said light-emitting device (EL), and a positive power supply potential and a negative power supply potential of the pixel circuit (2).

6. The array of pixel circuits each according to anyone of claims 1 to 5, wherein each of said pixel circuits (2) has either one of a red light-emitting device (R), a green light-emitting device (G), and a blue light-emitting device (B), and the additional capacitances (Csub) in the respective pixel circuits (2) have different capacitance values for the respective light-emitting devices (EL) for thereby uniformizing times requisite to operate the correcting means (Tr2-Tr4) in the respective pixel circuits (2).

7. The array of pixel circuits according to claim 6, wherein a shortage of the capacitance value of the additional capacitance (Csub) in one of said pixel circuits (2) is made up for by a portion of the additional capacitance (Csub) in an adjacent one of said pixel circuits (2).

8. The pixel circuit according to anyone of claims 1 to 5, wherein said correcting means (Tr2-Tr4) extracts the output current from said drive transistor (Trd) and supplies the extracted output current to said pixel capacitance (Cs) through a negative feedback loop to correct said input voltage while the video signal is being sampled in said pixel capacitance (Cs).

9. A display apparatus comprising:

a pixel array having a matrix of pixels (2) each positioned at a point of intersection between row scanning lines (WS, AZ1, AZ2, DS) for supplying control signals and a column signal line (SL) for supplying a video signal;
a signal unit (3) for supplying a video signal to said signal line (SL); and
a scanner unit (4, 5, 71, 72) for supplying control signals to said row scanning lines (WS, AZ1, AZ2, DS) to successively scan rows of the pixels;
each of said pixels comprising a pixel circuit according to anyone of claims 1 to 8.

Patentansprüche

1. Pixelschaltung, die an einem Schnittpunkt zwischen einer ersten Zeilenabtastleitung (WS) zum Zuführen eines ersten Steuersignals und einer Spaltensignalleitung (SL) zum Zuführen eines Videosignals angeordnet ist, welche zumindest Folgendes aufweist:

einen Abtasttransistor (Tr1), der mit der ersten Zeilenabtastleitung (WS) und der Signalleitung (SL) verbunden ist,
eine Pixelkapazität (Cs), die mit dem Abtasttransistor (Tr1) verbunden ist,
einen Treibertransistor (Trd) mit einem Gate (G), das mit einem Anschluss der Pixelkapazität (Cs) verbunden ist, und einer Source (S), die mit dem anderen Anschluss der Pixelkapazität (Cs) verbunden ist,
eine lichtemittierende Vorrichtung (EL) mit einem Anodenanschluss, der mit der Source des Treibertransistors (Trd) verbunden ist, und einem Kathodenanschluss, der an Masse (Vcath) gelegt ist,
wobei der Abtasttransistor (Tr1) dafür eingerichtet ist, ansprechend auf das von der ersten Zeilenabtastleitung (WS) zugeführte erste Steuersignal durchzuschalten, um das von der Signalleitung (SL) der Pixelkapazität (Cs) zugeführte Videosignal abzutasten,
die Pixelkapazität (Cs) dafür eingerichtet ist, eine Eingangsspannung (Vgs), abhängig vom abgetasteten Videosignal, an das Gate des Treibertransistors (Trd) anzulegen,
der Treibertransistor (Trd) dafür eingerichtet ist, der lichtemittierenden Vorrichtung (EL), abhängig von der

Eingangsspannung (Vgs), einen Ausgangsstrom (Ids) zuzuführen, wobei der Ausgangsstrom eine Abhängigkeit von einer Trägerbeweglichkeit in einem Kanalgebiet des Treibertransistors (Trd) hat,
die lichtemittierende Vorrichtung (EL) dafür eingerichtet ist, ansprechend auf den vom Treibertransistor (Trd) zugeführten Ausgangsstrom, Licht bei einem Luminanzpegel auszusenden, der vom Videosignal abhängt,
dadurch gekennzeichnet, dass die Pixelschaltung (2) ferner aufweist:

mindestens eine zweite Zeilenabtastleitung (AZ2) zum Zuführen eines zweiten Steuersignals und eine dritte Zeilenabtastleitung (DS) zum Zuführen eines dritten Steuersignals,
eine Korrektureinrichtung (Tr2-Tr4), die wenigstens einen ersten Schalttransistor (Tr3) und einen zweiten Schalttransistor (Tr4) aufweist,
wobei ein Gateanschluss des ersten Schalttransistors (Tr3) mit der zweiten Zeilenabtastleitung (AZ2) verbunden ist, ein Drainanschluss des ersten Schalttransistors (Tr3) mit der Source (S) des Treibertransistors (Tr1) verbunden ist, ein Sourceanschluss des ersten Schalttransitors (Tr3) mit einem ersten vorgegebenen festen Potential verbunden ist, ein Gateanschluss des zweiten Schalttransistors (Tr4) mit der dritten Zeilenabtastleitung (DS) verbunden ist und der Drain des Treibertransistors (Trd) dafür eingerichtet ist, über den zweiten Schalttransistor (Tr4) mit einem Stromversorgungspotential (Vcc) verbunden zu werden, wobei die Korrektureinrichtung (Tr2-Tr4) dafür ausgelegt ist, ansprechend auf die von der zweiten und der dritten Zeilenabtastleitung (AZ2, DS) zugeführten zweiten und dritten Steuersignale zu arbeiten, um die in der Pixelkapazität (Cs) abgetastete Eingangsspannung (Vgs) zu korrigieren, um die Abhängigkeit des Ausgangsstroms (Ids) von der Trägerbeweglichkeit aufzuheben,
wobei das von der dritten Zeilenabtastleitung (DS) zugeführte dritte Steuersignal dafür ausgelegt ist, den zweiten Schalttransistor (Tr4) für einen vorgegebenen Zeitraum durchzuschalten, unmittelbar bevor der Abtasttransistor (Tr1), ansprechend auf das von der ersten Zeilenabtastleitung (WS) zugeführte erste Steuersignal, gesperrt wird,
wobei die Korrektureinrichtung (Tr2-Tr4) dafür eingerichtet ist, abhängig vom von der zweiten Zeilenabtastleitung (AZ2) zugeführten zweiten Steuersignal zu arbeiten, um den Ausgangsstrom vom Treibertransistor (Trd) zu extrahieren und den extrahierten Ausgangsstrom in eine Kapazität (Coled) einzugeben, die einer äquivalenten Kapazität der lichtemittierenden Vorrichtung (EL) entspricht, wenn sie sich in einem in Sperrrichtung vorgespannten Modus befindet, und in die Pixelkapazität (Cs) einzugeben, um dadurch die Eingangsspannung zu korrigieren, und
eine zusätzliche Kapazität (Csub), die parallel zur äquivalenten Kapazität (Coled) der lichtemittierenden Vorrichtung (EL) hinzugefügt ist, wobei die zusätzliche Kapazität (Csub) einen Anschluss, der mit dem Anodenanschluss der lichtemittierenden Vorrichtung (EL) verbunden ist, und einen anderen Anschluss, der mit einem zweiten vorgegebenen festen Potential verbunden ist, aufweist, wobei ein Teil des vom Treibertransistor (Trd) extrahierten Ausgangsstrom in die zusätzliche Kapazität (Csub) fließt, um einen Zeitspielraum für den Betrieb der Korrektureinrichtung (Tr2-Tr4) während des vorgegebenen Zeitraums zu geben.

2. Pixelschaltung nach Anspruch 1, wobei der Abtasttransistor (Tr1), der Treibertransistor (Trd) und die Korrektureinrichtung (Tr2-Tr4) auf einem isolierenden Substrat gebildete Dünnfilmtransistoren umfassen und die Pixelkapazität (Cs) und die zusätzliche Kapazität (Csub) auf dem isolierenden Subtrat gebildelte Dünnfilmkondensatoren aufweisen.

3. Pixelschaltung nach Anspruch 1 oder 2, wobei der Ausgangsstrom des Treibertransistors (Trd) eine Abhängigkeit von einer Schwellenspannung sowie von der Trägerbeweglichkeit im Trägergebiet aufweist und die Korrektureinrichtung (Tr2-Tr4) eine Schwellenspannung des Treibertransistors (Trd) detektiert und die detektierte Schwellenspannung vorab zur Eingangsspannung addiert, um die Abhängigkeit des Ausgangsstroms von der Schwellenspannung aufzuheben.

4. Pixelschaltung nach einem der Ansprüche 1 bis 3, wobei die lichtemittierende Vorrichtung (EL) eine lichtemittierende Vorrichtung vom Diodentyp umfasst, welche eine Anode, die mit der Source des Treibertransistors (Trd) verbunden ist, und eine Kathode, die mit der Masse verbunden ist, aufweist, wobei die zusätzliche Kapazität (Csub) einen mit der Anode der lichtemittierenden Vorrichtung (EL) verbundenen Anschluss aufweist.

5. Pixelschaltung nach einem der Ansprüche 1 bis 4, wobei das zweite vorgegebene feste Potential, mit dem ein anderer Anschluss der zusätzlichen Kapazität (Csub) verbunden ist, aus einem Massepotential an der Kathode der lichtemittierenden Vorrichtung (EL) und einem positiven Stromversorgungspotential und einem negativen Stromversorgungspotential der Pixelschaltung (2) ausgewählt ist.

6. Array von Pixelschaltungen, jeweils nach einem der Ansprüche 1 bis 5, wobei jede der Pixelschaltungen (2) entweder eine rotes Licht emittierende Vorrichtung (R), eine grünes Licht emittierende Vorrichtung (G) oder eine blaues Licht emittierende Vorrichtung (B) aufweist und die zusätzlichen Kapazitäten (Csub) in den jeweiligen Pixelschaltungen (2) unterschiedliche Kapazitätswerte für die jeweiligen lichtemittierenden Vorrichtungen (EL) haben, um dadurch Zeitanforderungen für das Betreiben der Korrektureinrichtung (Tr2-Tr4) in den jeweiligen Pixelschaltungen (2) zu vergleichmäßigen.

7. Array von Pixelschaltungen nach Anspruch 6, wobei ein Mangel des Kapazitätswerts der zusätzlichen Kapazität (Csub) in einer der Pixelschaltungen (2) durch einen Teil der zusätzlichen Kapazität (Csub) in einer benachbarten der Pixelschaltungen (2) ausgeglichen wird.

8. Pixelschaltung nach einem der Ansprüche 1 bis 5, wobei die Korrektureinrichtung (Tr2-Tr4) den Ausgangsstrom aus dem Treibertransistor (Trd) extrahiert und den extrahierten Ausgangsstrom der Pixelkapazität (Cs) durch eine Gegenkopplungsschleife zuführt, um die Eingangsspannung zu korrigieren, während das Videosignal in der Pixelkapazität (Cs) abgetastet wird.

9. Anzeigevorrichtung, welche aufweist:

ein Pixel-Array mit einer Matrix von Pixeln (2), die jeweils an einem Schnittpunkt zwischen Zeilenabtastleitungen (WS, AZ1, AZ2, DS) zum Zuführen von Steuersignalen und einer Spaltensignalleitung (SL) zum Zuführen eines Videosignals angeordnet sind,
eine Signaleinheit (3) zum Zuführen eines Videosignals zu der Signalleitung (SL) und
eine Abtasteinheit (4, 5, 71, 72) zum Zuführen von Steuersignalen zu den Zeilenabtastleitungen (WS, AZ1, AZ2, DS), um Zeilen der Pixel der Reihe nach abzutasten,
wobei jedes der Pixel eine Pixelschaltung nach einem der Ansprüche 1 bis 8 aufweist.

Revendications

1. Circuit de pixel agencé à un point d'intersection entre une première ligne de balayage de rangée (WS) servant à fournir un premier signal de commande et une ligne de signal de colonne (SL) servant à fournir un signal vidéo, le circuit de pixel comprenant au moins :

un transistor d'échantillonnage (Tr1) relié à ladite première ligne de balayage de rangée (WS) et à ladite ligne de signal (SL) ;
une capacité de pixel (Cs) reliée audit transistor d'échantillonnage (Tr1) ;
un transistor d'attaque (Trd) possédant une grille (G) reliée à une borne de ladite capacité de pixel (Cs) et une source (S) reliée à l'autre borne de ladite capacité de pixel (Cs) ;
un dispositif électroluminescent (EL) possédant une borne d'anode reliée à la source dudit transistor d'attaque (Trd) et une borne de cathode reliée à la terre (Vcath) ;
lequel transistor d'échantillonnage (Tr1) est agencé pour passer à l'état conducteur en réponse au premier signal de commande fourni par ladite première ligne de balayage de rangée (WS) pour échantillonner le signal vidéo fourni par ladite ligne de signal (SL) dans ladite capacité de pixel (Cs),
laquelle capacité de pixel (Cs) est agencée pour appliquer une tension d'entrée (Vgs) à la grille dudit transistor d'attaque (Trd) fonction du signal vidéo échantillonné,
lequel transistor d'attaque (Trd) est agencé pour fournir un courant de sortie (Ids) fonction de ladite tension d'entrée (Vgs) audit dispositif électroluminescent (EL), ledit courant de sortie présentant une dépendance vis-à-vis d'une mobilité des porteurs de charge dans une zone de canal dudit transistor d'attaque (Trd),
lequel dispositif électroluminescent (EL) est agencé pour émettre de la lumière à un niveau de luminance fonction dudit signal vidéo en réponse au courant de sortie fourni par ledit transistor d'attaque (Trd),
ledit circuit de pixel (2) étant **caractérisé en ce qu'**il comprend en outre :

au moins une deuxième ligne de balayage de rangée (AZ2) servant à fournir un deuxième signal de commande, et une troisième ligne de balayage de rangée (DS) servant à fournir un troisième signal de commande,
un moyen de correction (Tr2-Tr4) comprenant au moins un premier transistor de commutation (Tr3) et un deuxième transistor de commutation (Tr4),
une borne de grille duquel premier transistor de commutation (Tr3) est reliée à ladite deuxième ligne de

balayage de rangée (AZ2), une borne de drain duquel premier transistor de commutation (Tr3) est reliée à la source (S) dudit transistor d'attaque (Tr1), une borne de source duquel premier transistor de commutation (Tr3) est reliée à un premier potentiel fixe prédéfini, une borne de grille du deuxième transistor de commutation (Tr4) est reliée à ladite troisième ligne de balayage de rangée (DS) et le drain duquel transistor d'attaque (Trd) est agencé pour être relié à un potentiel d'alimentation (Vcc) via ledit deuxième transistor de commutation (Tr4), ledit moyen de correction (Tr2-Tr4) étant conçu pour fonctionner en réponse aux deuxième et troisième signaux de commande fournis par lesdites deuxième et troisième lignes de balayage de rangée (AZ2, DS) pour corriger la tension d'entrée (Vgs) échantillonnée dans ladite capacité de pixel (Cs) dans le but de neutraliser la dépendance dudit courant de sortie (Ids) vis-à-vis de la mobilité des porteurs de charge,
lequel troisième signal de commande fourni par ladite troisième ligne de balayage de rangée (DS) est conçu pour faire passer à l'état conducteur ledit deuxième transistor de commutation (Tr4) pendant une période de temps prédéfinie immédiatement avant que ledit transistor d'échantillonnage (Tr1) passe à l'état non conducteur en réponse audit premier signal de commande fourni par ladite première ligne de balayage de rangée (WS),
lequel moyen de correction (Tr2-Tr4) est agencé pour fonctionner en fonction dudit deuxième signal de commande fourni par ladite deuxième ligne de balayage de rangée (AZ2) pour extraire le courant de sortie dudit transistor d'attaque (Trd) et introduire le courant de sortie extrait dans une capacité (Coled) correspondant à une capacité équivalente dudit dispositif électroluminescent (EL) lorsqu'il se trouve dans un mode de polarisation inverse et dans ladite capacité de pixel (Cs) pour corriger ainsi la tension d'entrée, et une capacité supplémentaire (Csub) ajoutée en parallèle à la capacité équivalente (Coled) dudit dispositif électroluminescent (EL), ladite capacité supplémentaire (Csub) possédant une borne reliée à la borne d'anode dudit dispositif électroluminescent (EL) et une autre borne reliée à un deuxième potentiel fixe prédéfini, une partie duquel courant de sortie extrait dudit transistor d'attaque (Trd) circule dans ladite capacité supplémentaire (Csub) pour conférer une marge de temps au fonctionnement dudit moyen de correction (Tr2-Tr4) durant ladite période de temps prédéfinie.

2. Circuit de pixel selon la revendication 1, dans lequel ledit transistor d'échantillonnage (Tr1), ledit transistor d'attaque (Trd) et ledit moyen de correction (Tr2-Tr4) comprennent des transistors en couches minces formés sur un substrat isolant, et ladite capacité de pixel (Cs) et ladite capacité supplémentaire (Csub) comportent des condensateurs en couches minces formés sur ledit substrat isolant.

3. Circuit de pixel selon la revendication 1 ou la revendication 2, dans lequel le courant de sortie dudit transistor d'attaque (Trd) présente une dépendance vis-à-vis d'une tension de seuil en plus de la mobilité des porteurs de charge dans la zone des porteurs de charge, et ledit moyen de correction (Tr2-Tr4) détecte une tension de seuil dudit transistor d'attaque (Trd) et ajoute à l'avance la tension de seuil détectée à ladite tension d'entrée dans le but de neutraliser la dépendance du courant de sortie vis-à-vis de la tension de seuil.

4. Circuit de pixel selon l'une quelconque des revendications 1 à 3, dans lequel ledit dispositif électroluminescent (EL) comprend un dispositif électroluminescent du type diode possédant une anode reliée à la source dudit transistor d'attaque (Trd) et une cathode reliée à la terre, ladite capacité supplémentaire (Csub) possédant une borne reliée à l'anode dudit dispositif électroluminescent (EL).

5. Circuit de pixel selon l'une quelconque des revendications 1 à 4, dans lequel ledit deuxième potentiel fixe prédéfini auquel une autre borne de ladite capacité supplémentaire (Csub) est reliée est sélectionné parmi un potentiel à la terre sur la cathode dudit dispositif électroluminescent (EL), et un potentiel d'alimentation positif et un potentiel d'alimentation négatif du circuit de pixel (2).

6. Réseau de circuits de pixel chacun selon l'une quelconque des revendications 1 à 5, dans lequel chacun desdits circuits de pixel (2) possède un dispositif quelconque parmi un dispositif électroluminescent rouge (R), un dispositif électroluminescent vert (G) et un dispositif électroluminescent bleu (B), et les capacités supplémentaires (Csub) dans les circuits de pixel (2) respectifs possèdent des valeurs de capacité différentes pour les dispositifs électroluminescents (EL) respectifs pour uniformiser ainsi des temps nécessaires au fonctionnement du moyen de correction (Tr2-Tr4) dans les circuits de pixel (2) respectifs.

7. Réseau de circuits de pixel selon la revendication 6, dans lequel un déficit de la valeur de capacité de la capacité supplémentaire (Csub) dans l'un desdits circuits de pixel (2) est comblé par une partie de la capacité supplémentaire (Csub) dans un circuit de pixel adjacent parmi lesdits circuits de pixel (2).

8. Circuit de pixel selon l'une quelconque des revendications 1 à 5, dans lequel ledit moyen de correction (Tr2-Tr4) extrait le courant de sortie dudit transistor d'attaque (Trd) et fournit le courant de sortie extrait à ladite capacité de pixel (Cs) via une boucle de contre-réaction pour corriger ladite tension d'entrée pendant l'échantillonnage du signal vidéo dans ladite capacité de pixel (Cs).

9. Appareil d'affichage, comprenant :

un réseau de pixels possédant une matrice de pixels (2) positionnés chacun à un point d'intersection entre des lignes de balayage de rangée (WS, AZ1, AZ2, DS) servant à fournir des signaux de commande et une ligne de signal de colonne (SL) servant à fournir un signal vidéo ;
une unité de signal (3) servant à fournir un signal vidéo à ladite ligne de signal (SL) ; et
une unité de balayage (4, 5, 71, 72) servant à fournir des signaux de commande auxdites lignes de balayage de rangée (WS, AZ1, AZ2, DS) pour balayer successivement des rangées des pixels ;
chacun desdits pixels comprenant un circuit de pixel selon l'une quelconque des revendications 1 à 8.

FIG. 1

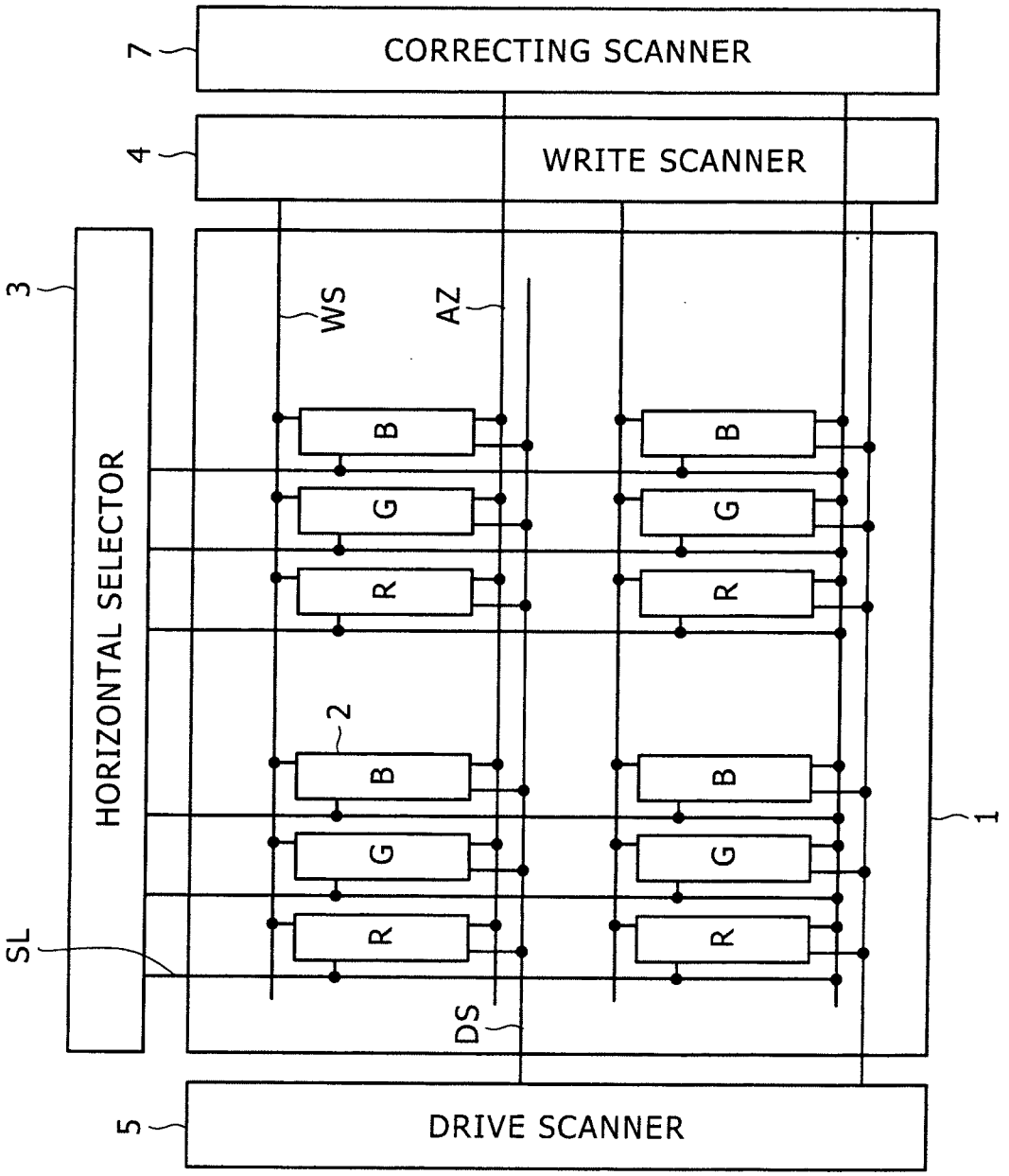

7
CORRECTING SCANNER
4
WRITE SCANNER
3
HORIZONTAL SELECTOR
WS
AZ
B
G
R
2
SL
DS
1
5
DRIVE SCANNER

FIG. 2

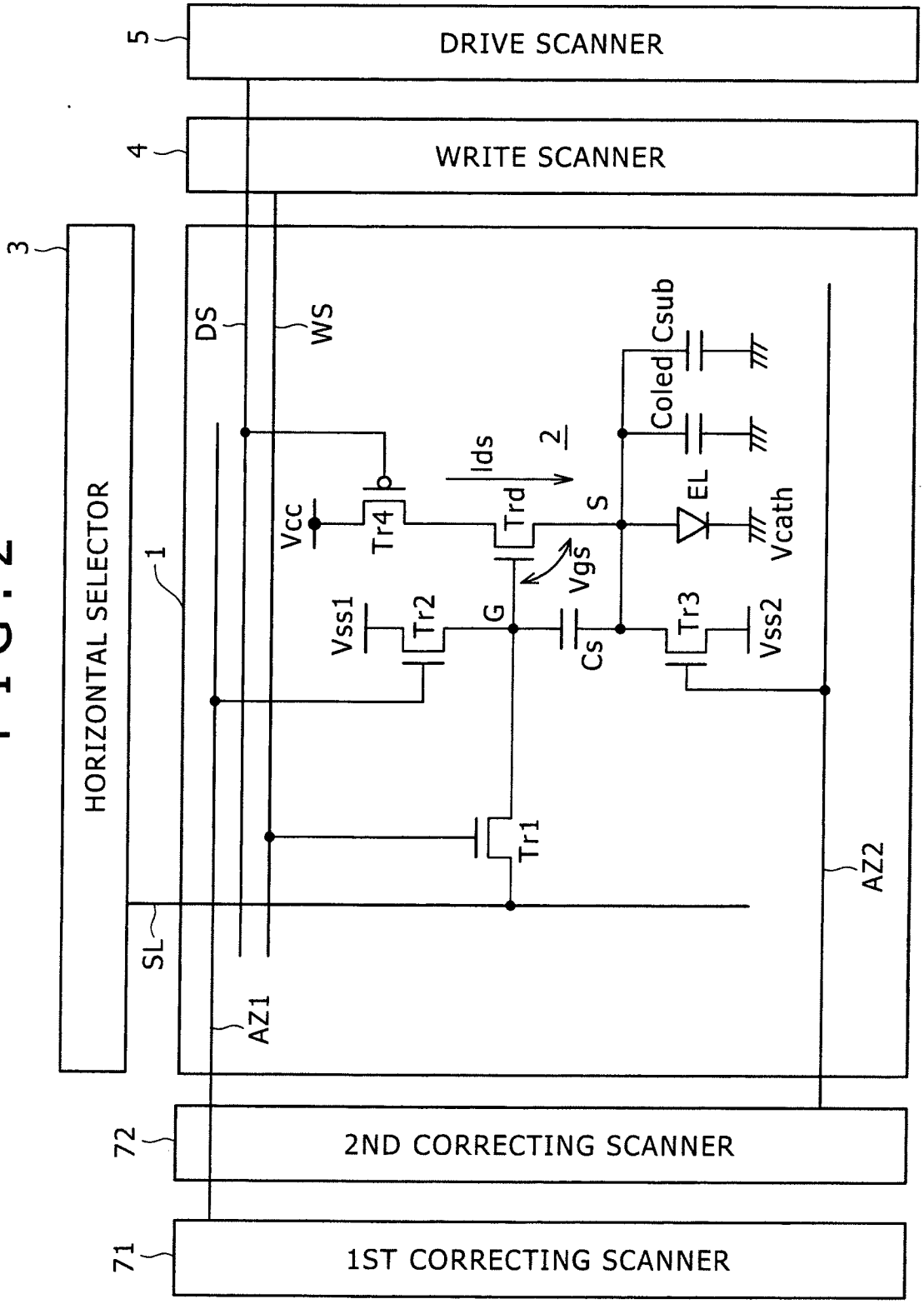

5
DRIVE SCANNER
4
WRITE SCANNER
3
HORIZONTAL SELECTOR
1
DS
WS
Vcc
Tr4
p
Ids
2
Trd
S
Coled
Csub
EL
Vcath
Vgs
Vss1
Tr2
G
Cs
Tr3
Vss2
Tr1
SL
AZ1
AZ2
72
2ND CORRECTING SCANNER
71
1ST CORRECTING SCANNER

FIG. 3B

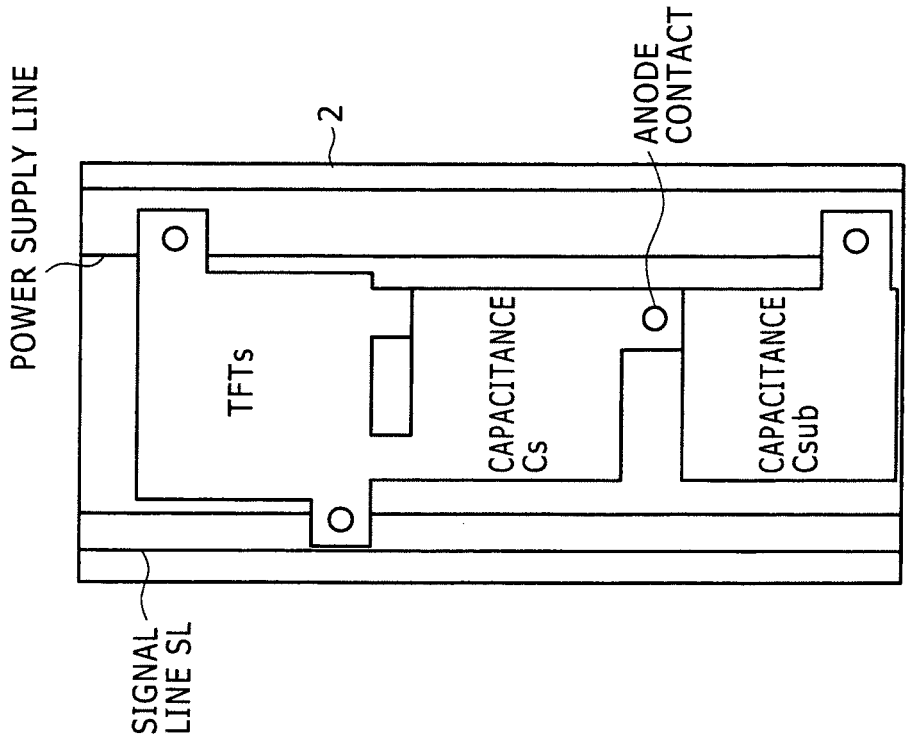

POWER SUPPLY LINE
2
ANODE CONTACT
TFTs
CAPACITANCE Cs
CAPACITANCE Csub
SIGNAL LINE SL

FIG. 3A

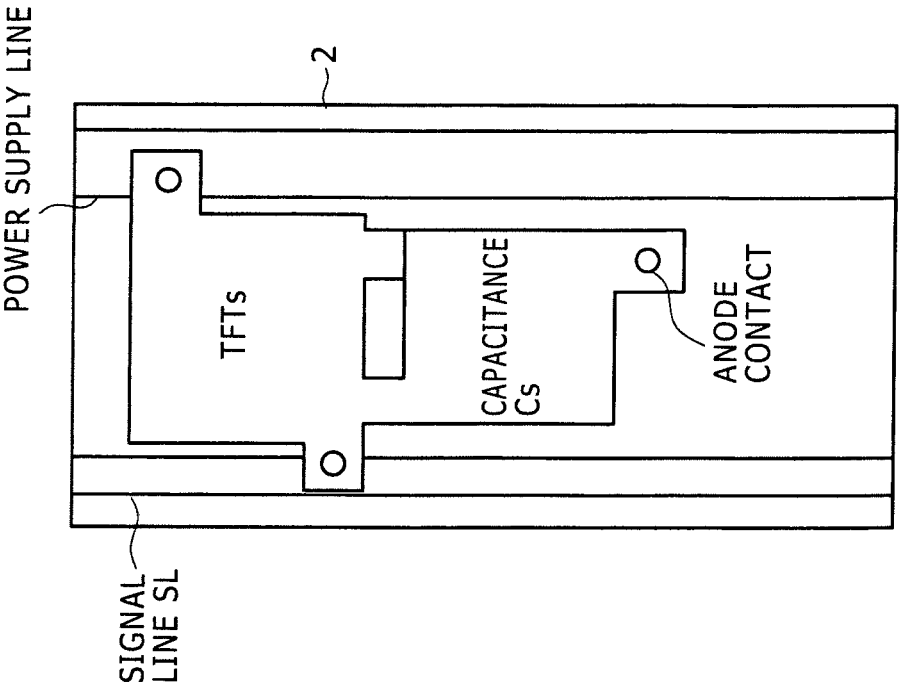

POWER SUPPLY LINE
2
TFTs
CAPACITANCE Cs
ANODE CONTACT
SIGNAL LINE SL

FIG. 4

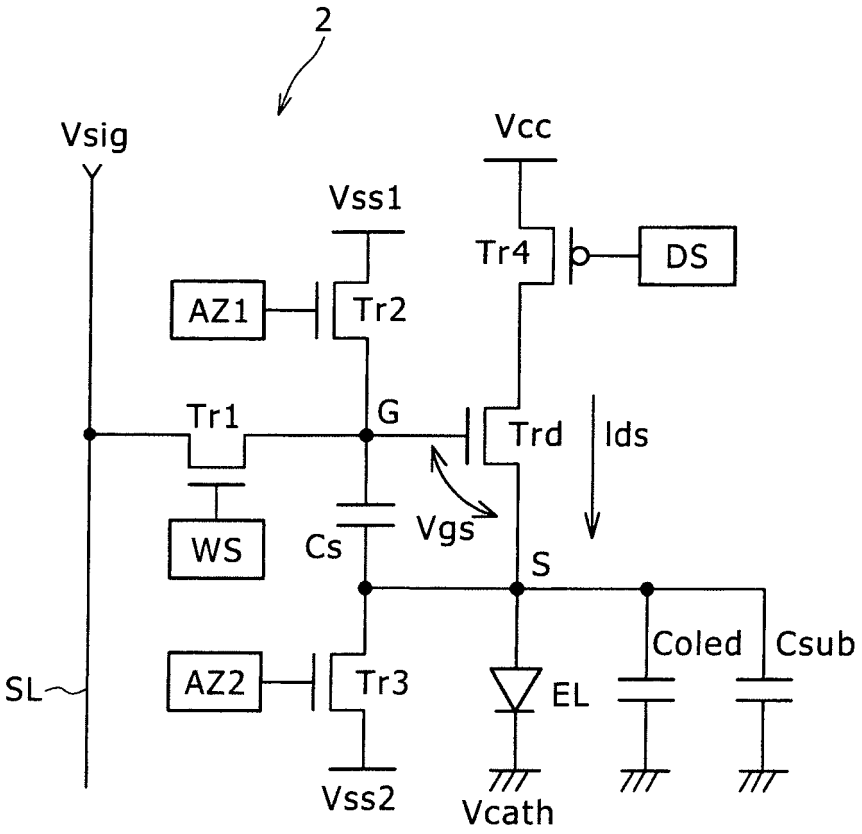

2
Vsig
Vcc
Vss1
Tr4
DS
AZ1
Tr2
Tr1
G
Trd
Ids
Vgs
WS
Cs
S
Coled
Csub
SL
AZ2
Tr3
EL
Vss2
Vcath

FIG. 5

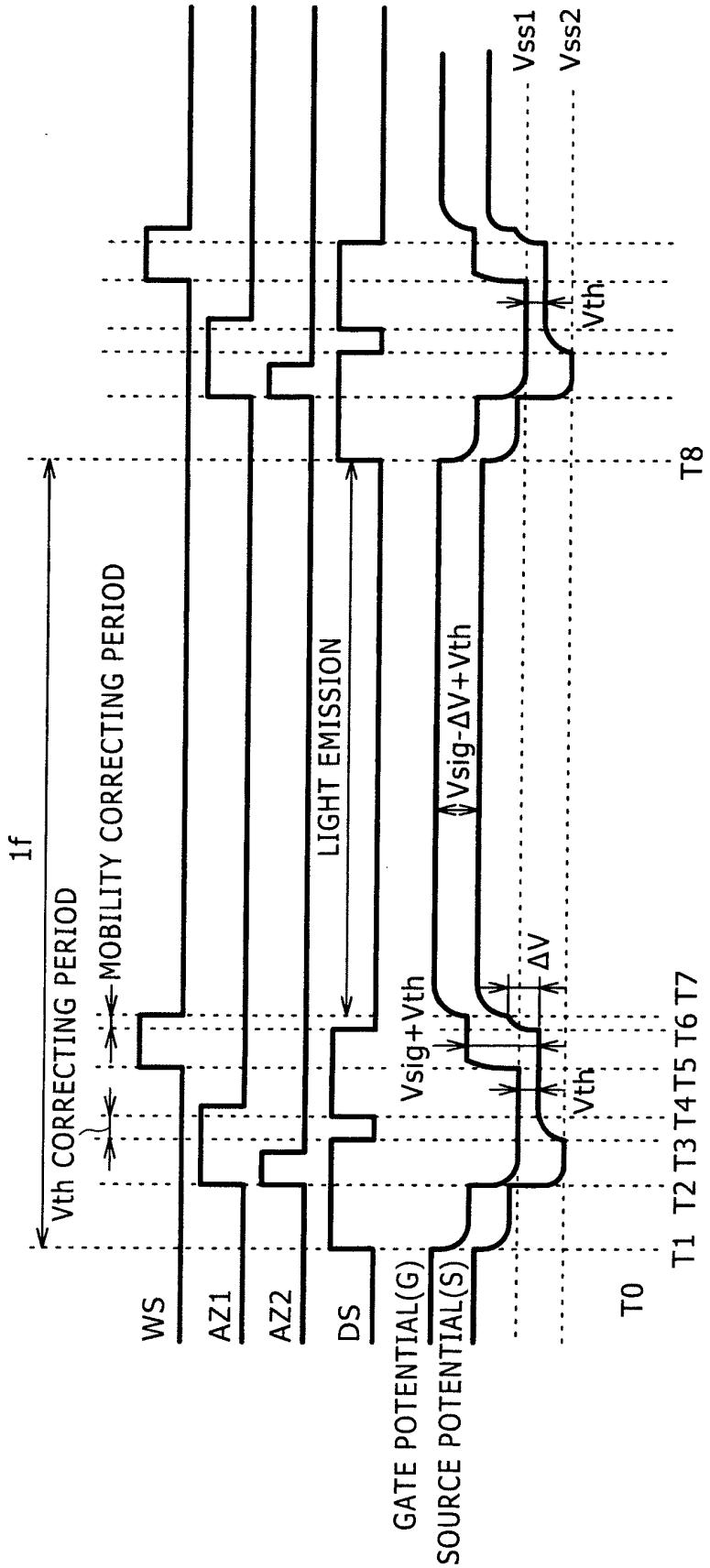

1f
Vth CORRECTING PERIOD
MOBILITY CORRECTING PERIOD
LIGHT EMISSION
WS
AZ1
AZ2
DS
GATE POTENTIAL(G)
SOURCE POTENTIAL(S)
Vsig+Vth
Vsig-ΔV+Vth
ΔV
Vth
Vth
Vss1
Vss2
T0
T1
T2
T3
T4
T5
T6
T7
T8

FIG. 6

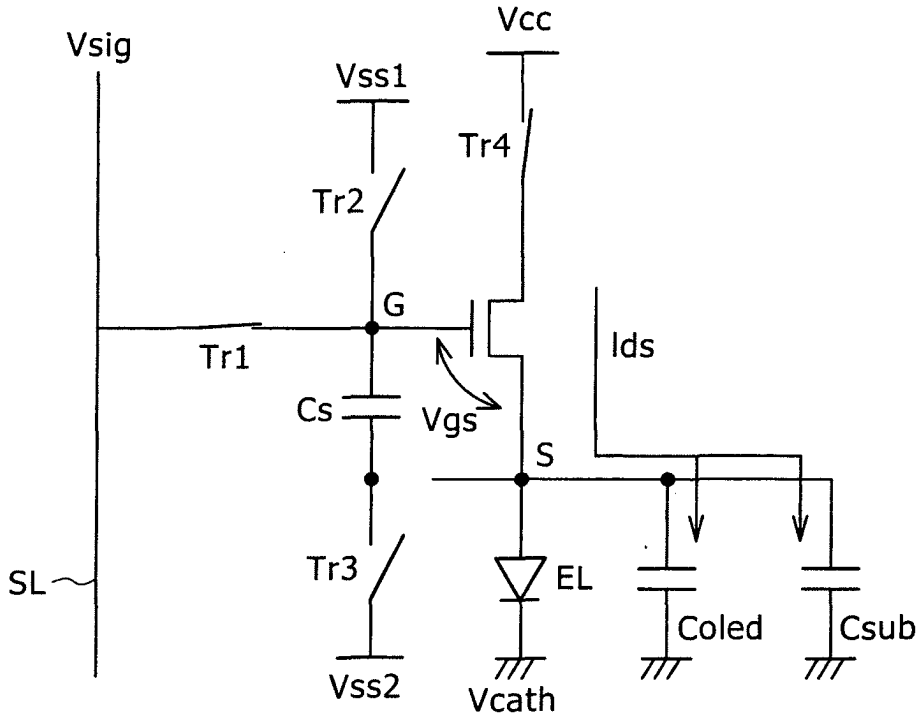
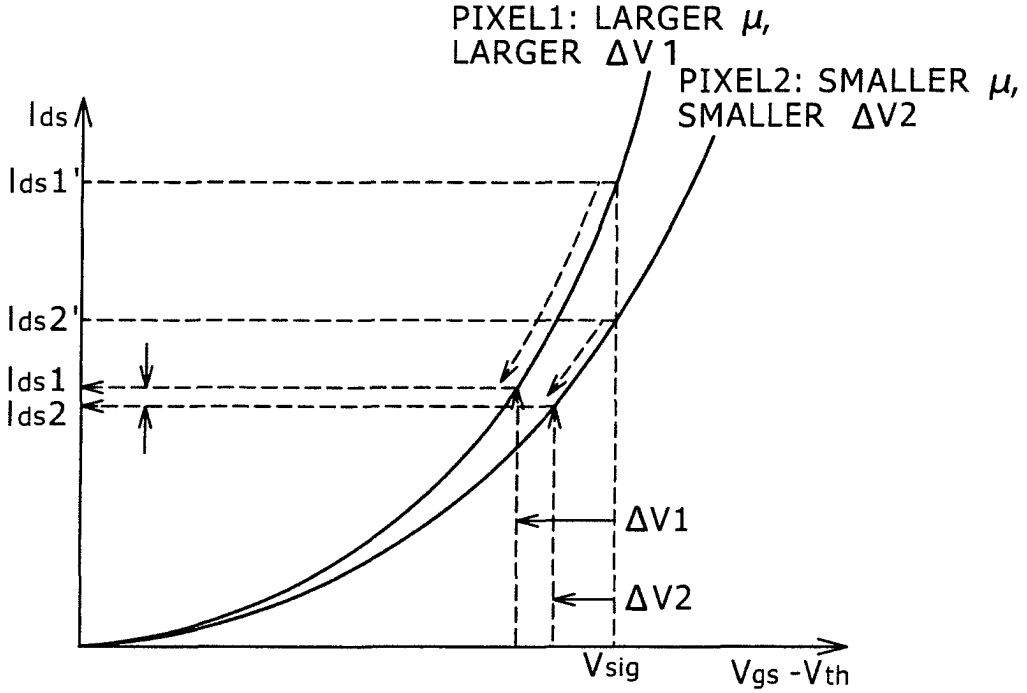


FIG. 7



$$Ids = k\mu(Vgs - Vth)^2 = k\mu(Vsig - \Delta V)^2$$

FIG. 8

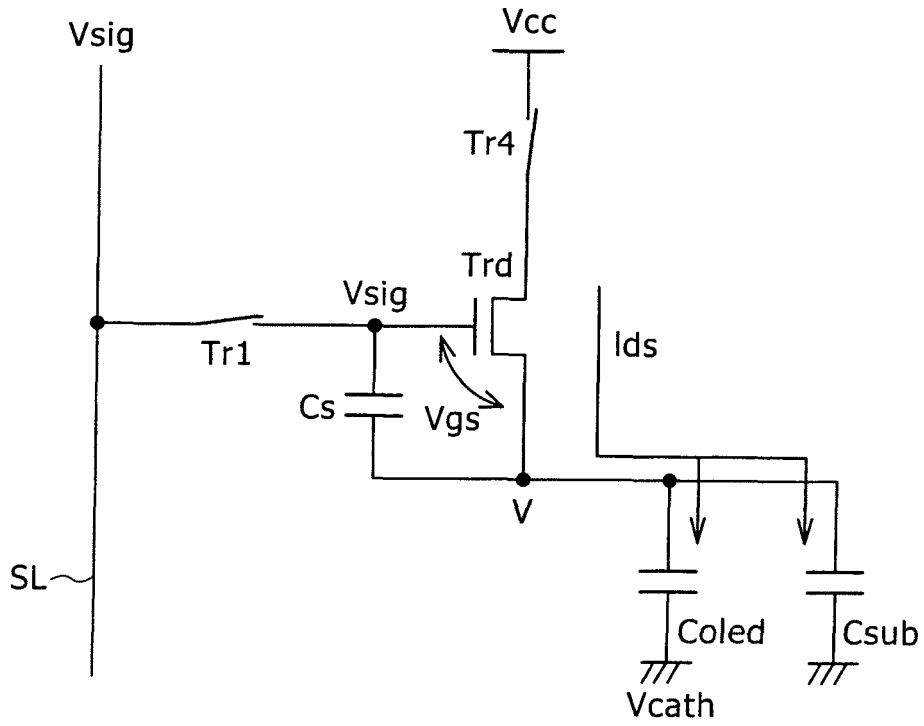


FIG. 9

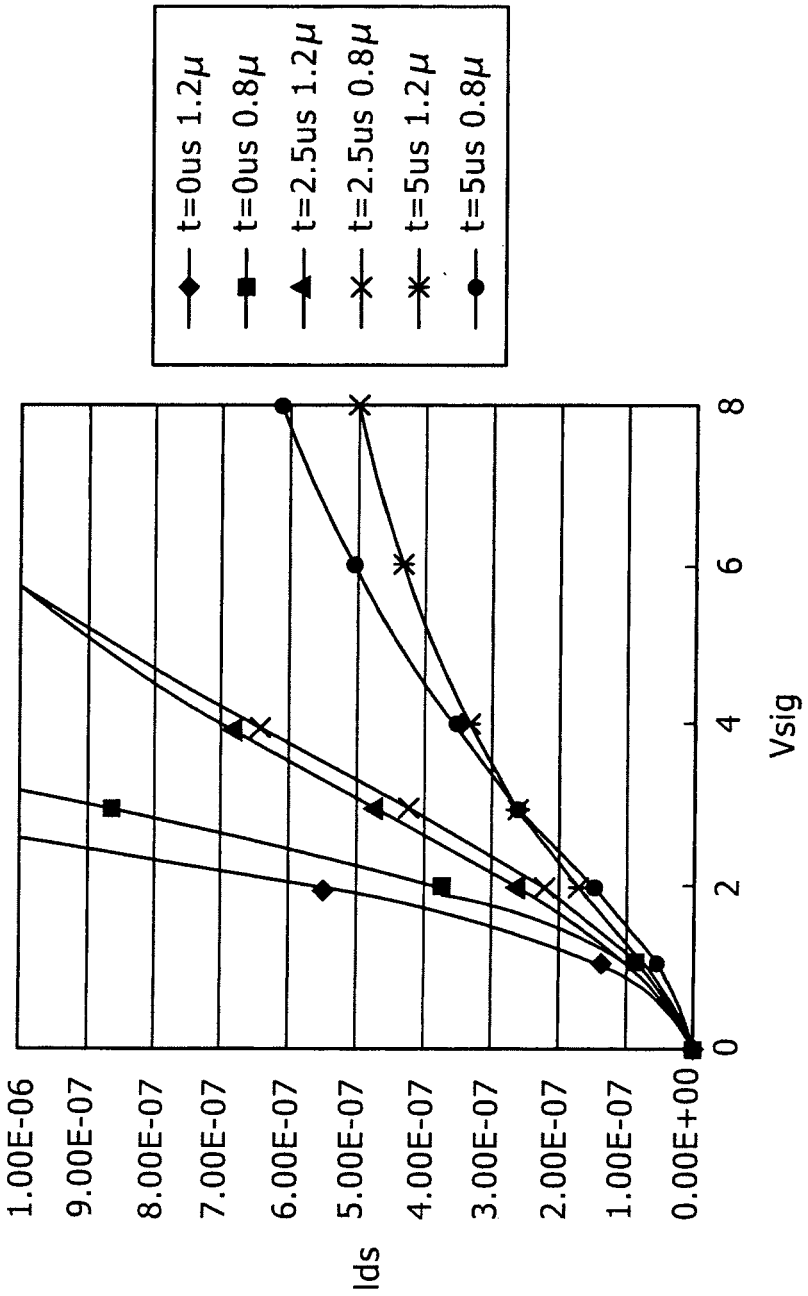

t=0us 1.2μ
t=0us 0.8μ
t=2.5us 1.2μ
t=2.5us 0.8μ
t=5us 1.2μ
t=5us 0.8μ
1.00E-06
9.00E-07
8.00E-07
7.00E-07
6.00E-07
5.00E-07
4.00E-07
3.00E-07
2.00E-07
1.00E-07
0.00E+00
Ids
0
2
4
6
8
Vsig

FIG.10

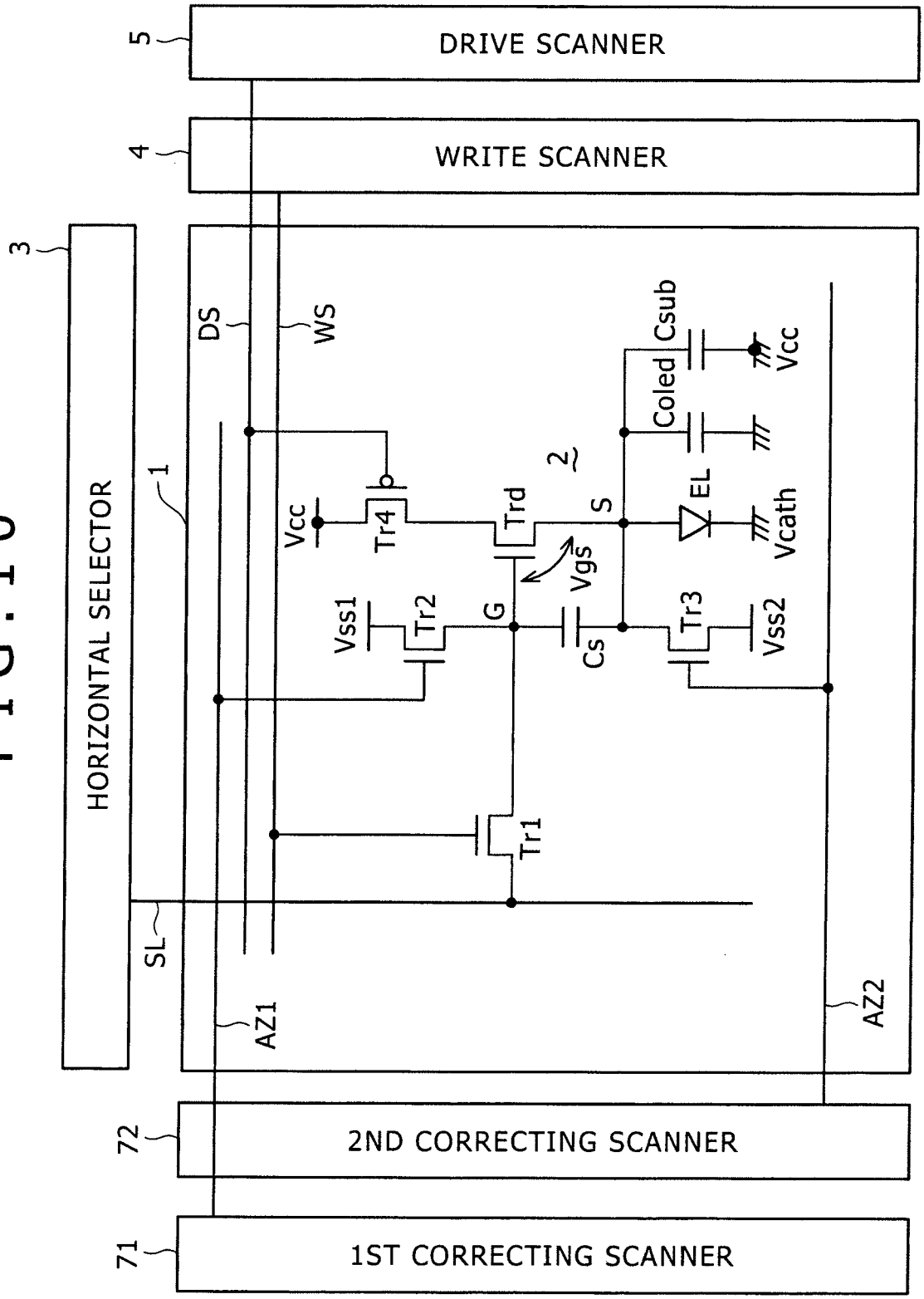

5
DRIVE SCANNER
4
WRITE SCANNER
3
HORIZONTAL SELECTOR
1
DS
WS
Csub
Coled
Vcc
2
Vcc
Tr4
Trd
S
EL
Vcath
Vgs
Vss1
Tr2
G
Cs
Tr3
Vss2
Tr1
SL
AZ1
AZ2
72
2ND CORRECTING SCANNER
71
1ST CORRECTING SCANNER

FIG. 11

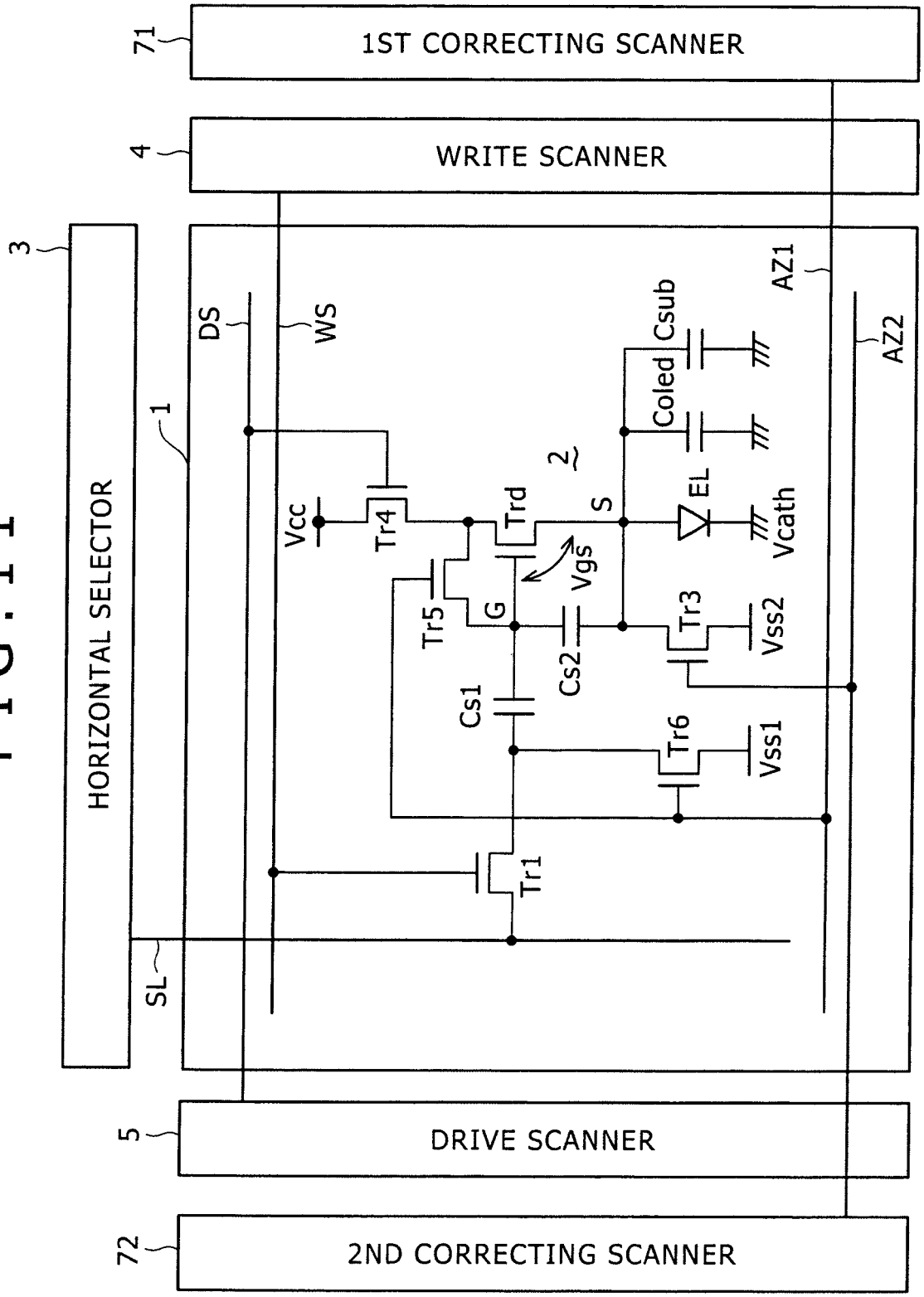

71
1ST CORRECTING SCANNER
4
WRITE SCANNER
3
HORIZONTAL SELECTOR
1
DS
WS
AZ1
AZ2
Csub
Coled
2
Vcc
Tr4
Trd
S
EL
Vcath
Vgs
Tr5
G
Tr3
Vss2
Cs2
Cs1
Tr6
Vss1
Tr1
SL
5
DRIVE SCANNER
72
2ND CORRECTING SCANNER

FIG. 12

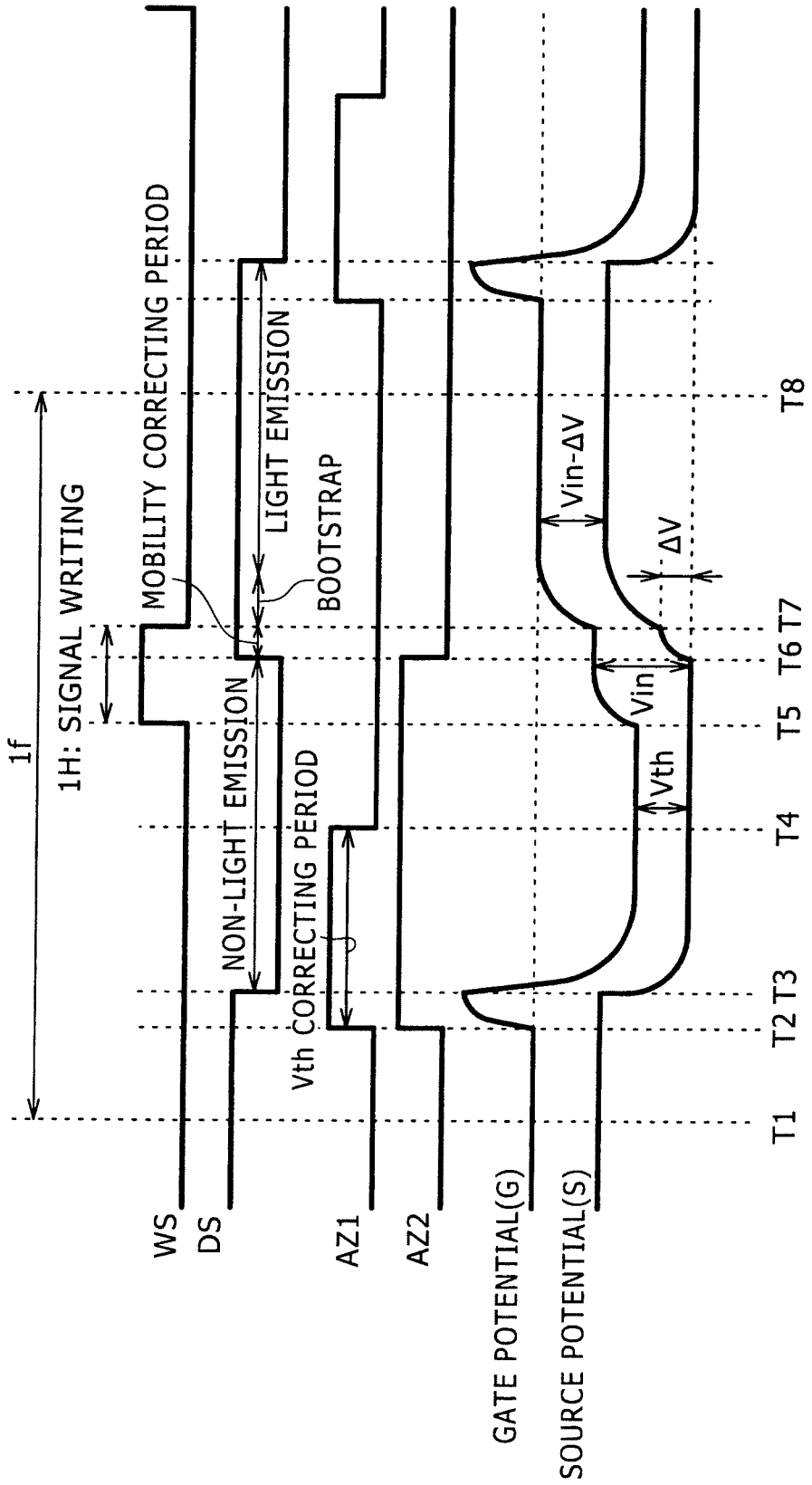

1f
1H: SIGNAL WRITING
MOBILITY CORRECTING PERIOD
LIGHT EMISSION
BOOTSTRAP
NON-LIGHT EMISSION
Vth CORRECTING PERIOD
WS
DS
AZ1
AZ2
GATE POTENTIAL(G)
SOURCE POTENTIAL(S)
Vin-ΔV
ΔV
Vin
Vth
T1
T2 T3
T4
T5
T6 T7
T8

FIG. 13

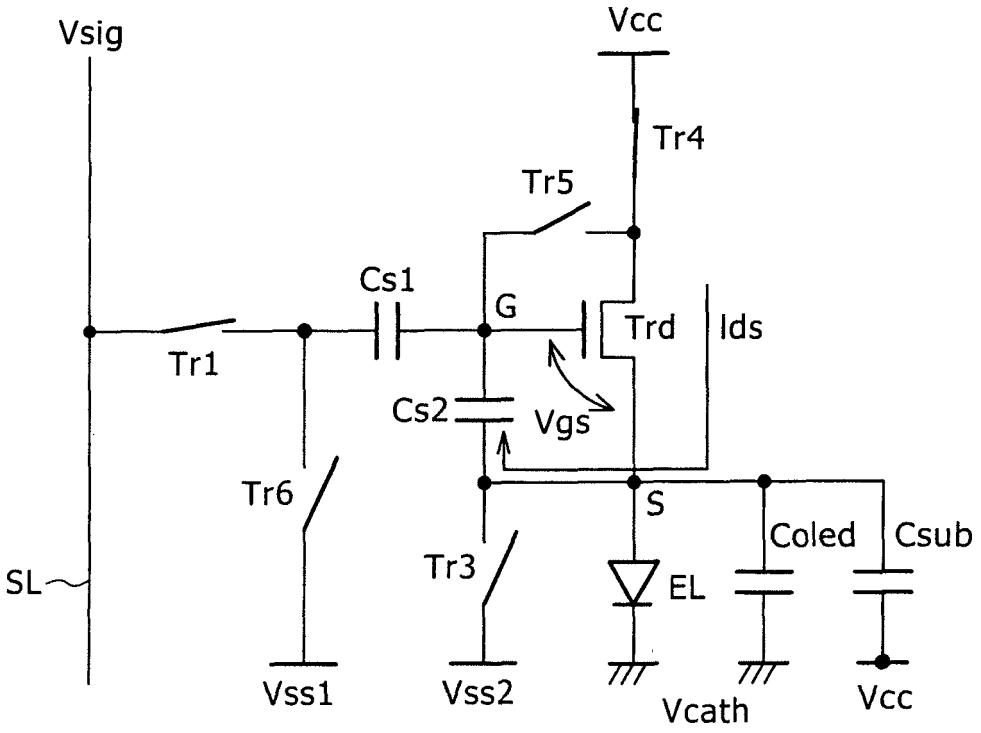

Vsig
Vcc
Tr4
Tr5
Cs1
G
Trd
Ids
Tr1
Cs2
Vgs
Tr6
S
Coled
Csub
Tr3
EL
SL
Vss1
Vss2
Vcath
Vcc

FIG.14

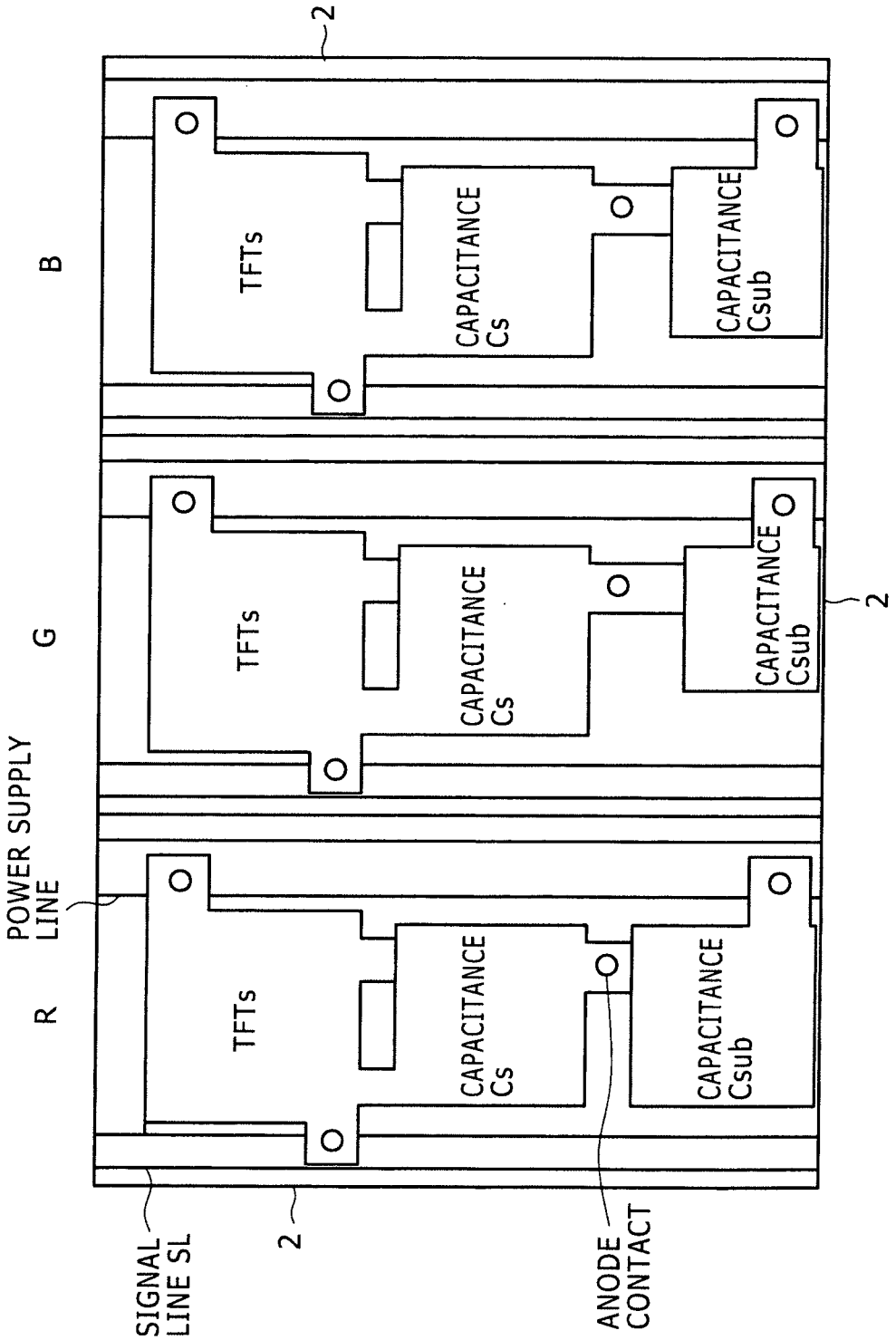

2
B
TFTs
CAPACITANCE Cs
CAPACITANCE Csub
G
TFTs
CAPACITANCE Cs
CAPACITANCE Csub
2
POWER SUPPLY LINE
R
TFTs
CAPACITANCE Cs
CAPACITANCE Csub
SIGNAL LINE SL
2
ANODE CONTACT

FIG. 15

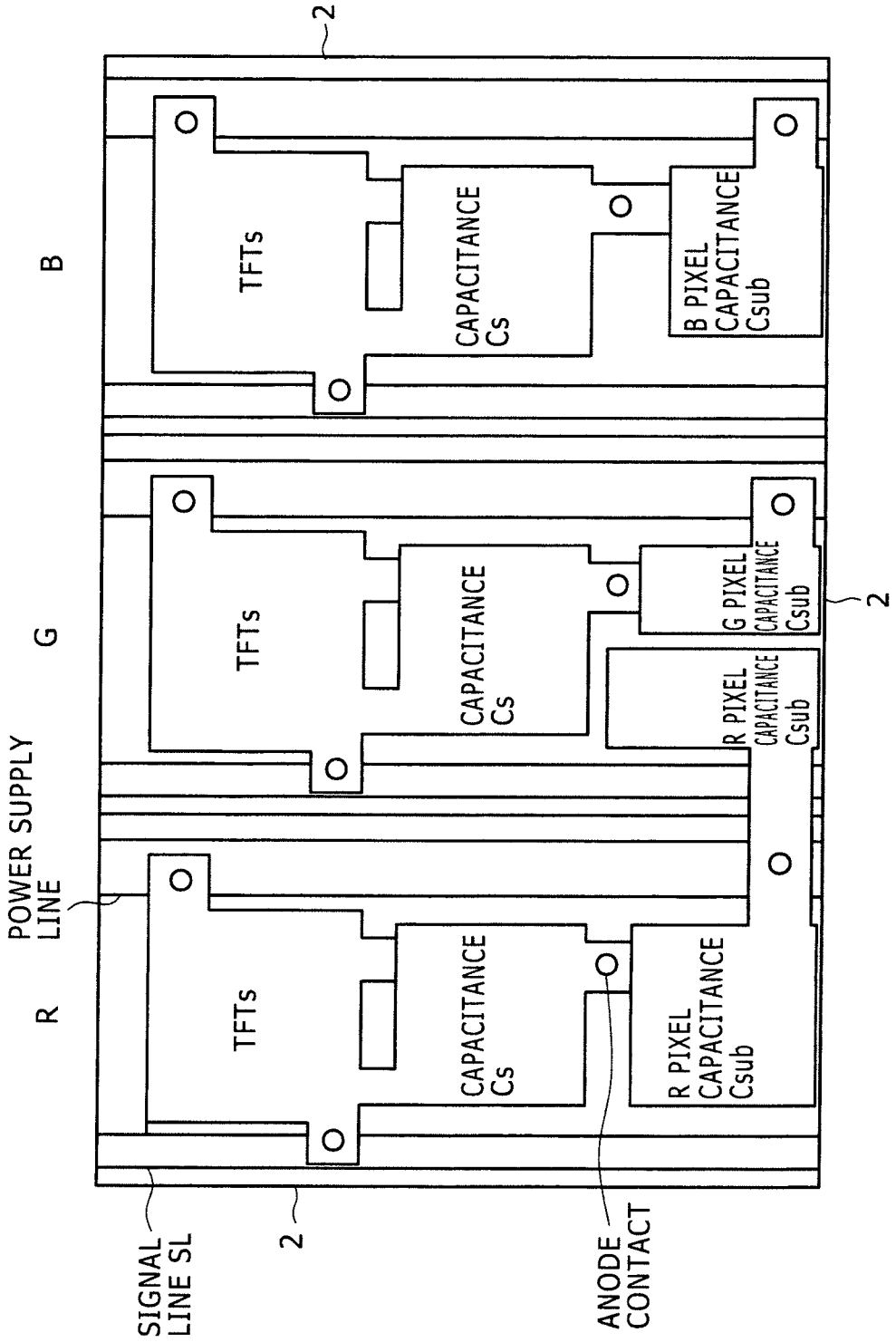

2
B
TFTs
CAPACITANCE Cs
B PIXEL CAPACITANCE Csub
G
TFTs
CAPACITANCE Cs
G PIXEL CAPACITANCE Csub
2
R PIXEL CAPACITANCE Csub
POWER SUPPLY LINE
R
TFTs
CAPACITANCE Cs
R PIXEL CAPACITANCE Csub
SIGNAL LINE SL
2
ANODE CONTACT

FIG. 16

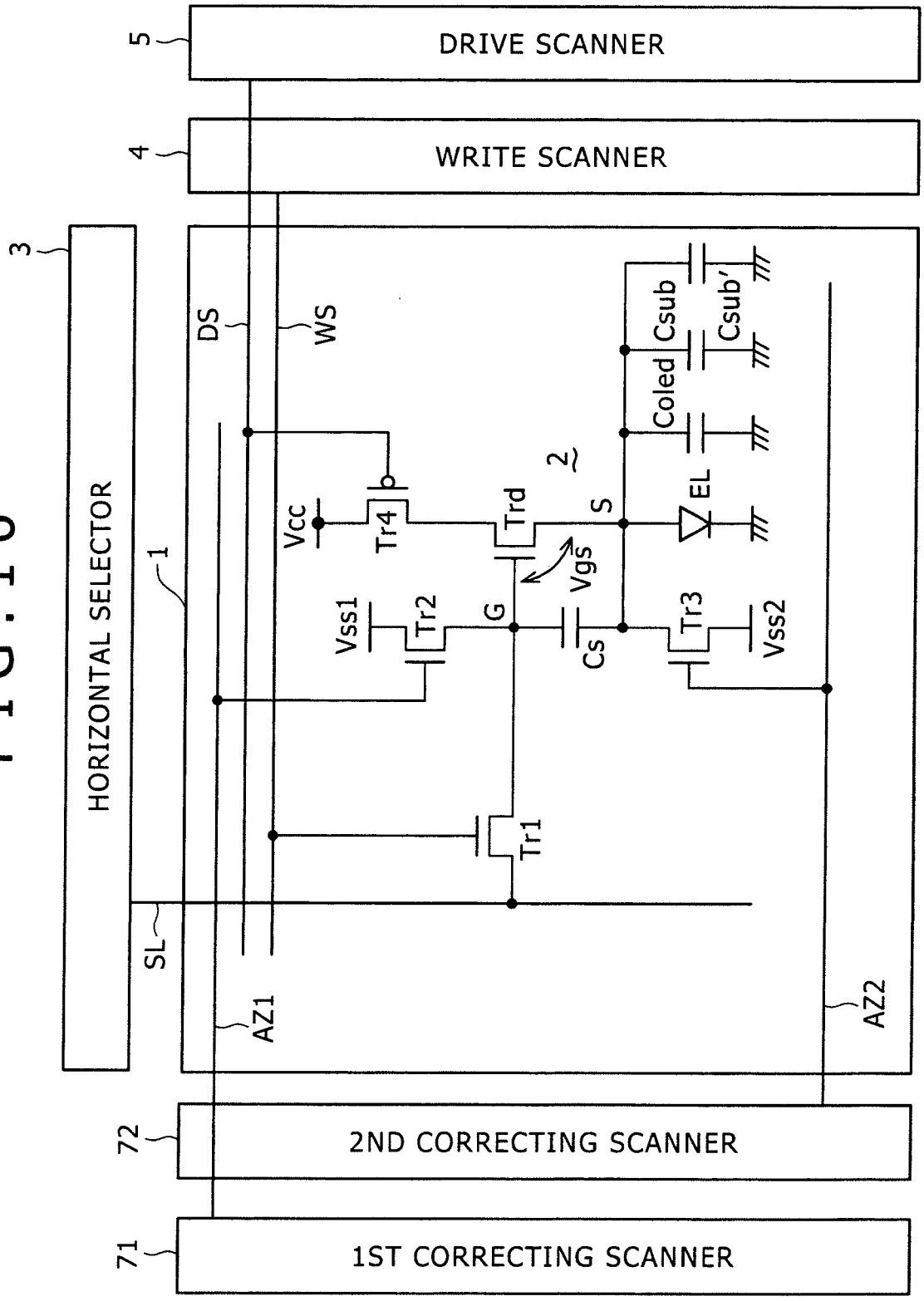
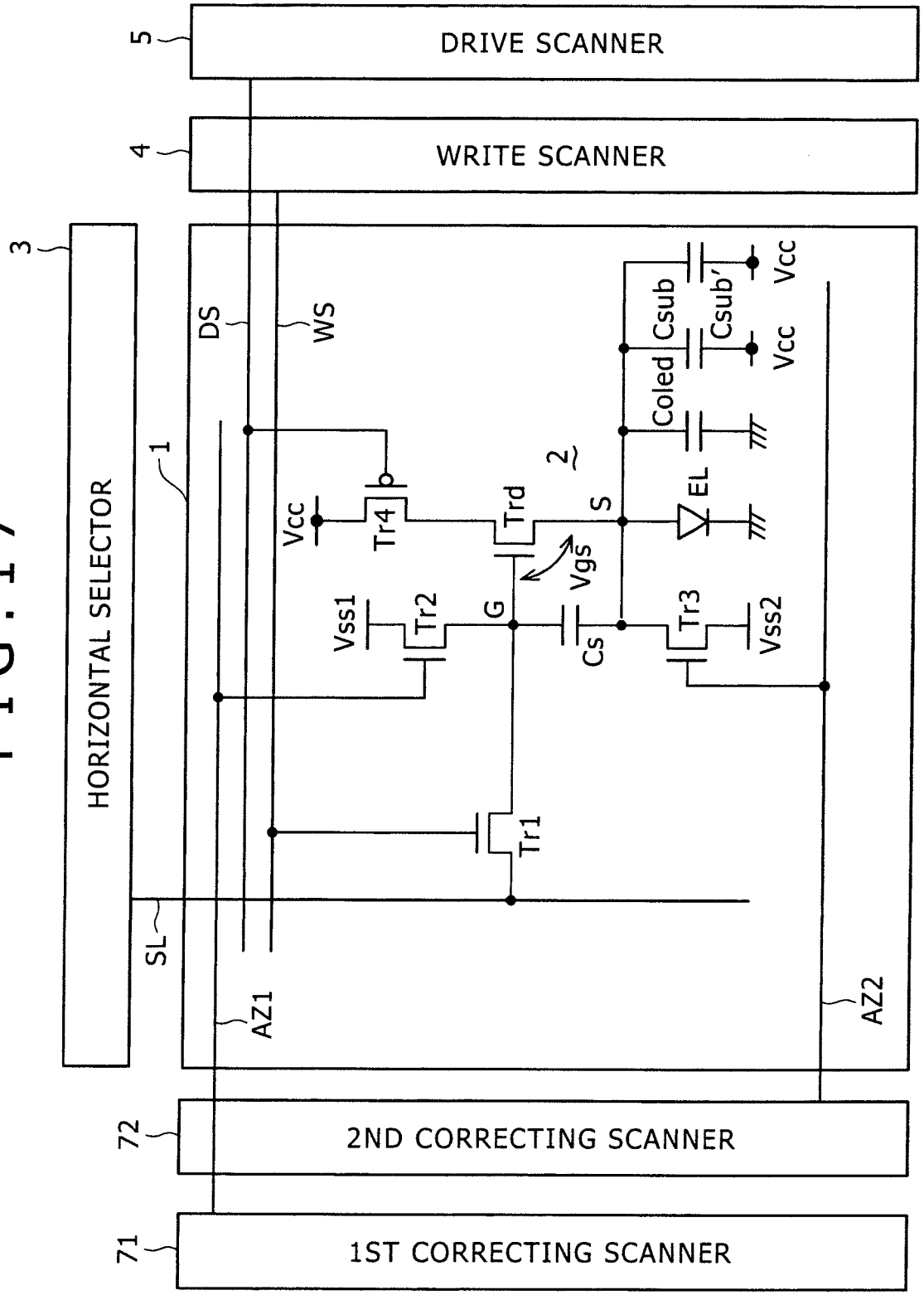

5
DRIVE SCANNER
4
WRITE SCANNER
3
HORIZONTAL SELECTOR
1
DS
WS
Vcc
Tr4
Trd
2
S
Vgs
G
Vss1
Tr2
Cs
Tr3
Vss2
Tr1
Coled
Csub
Csub'
EL
SL
AZ1
AZ2
72
2ND CORRECTING SCANNER
71
1ST CORRECTING SCANNER

FIG. 17


5
DRIVE SCANNER
4
WRITE SCANNER
3
HORIZONTAL SELECTOR
1
DS
WS
2
Vcc
Tr4
Trd
S
Csub
Csub'
Vcc
Coled
EL
Vgs
G
Vss1
Tr2
Cs
Tr3
Vss2
Tr1
SL
AZ1
AZ2
72
2ND CORRECTING SCANNER
71
1ST CORRECTING SCANNER

REFERENCES CITED IN THE DESCRIPTION

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- US 2005269959 A **[0004]**
- EP 1496495 A **[0004]**

专利名称(译)	像素电路和显示装置		
公开(公告)号	EP1772847B1	公开(公告)日	2013-12-04
申请号	EP2006121909	申请日	2006-10-06
[标]申请(专利权)人(译)	索尼公司		
申请(专利权)人(译)	索尼公司		
当前申请(专利权)人(译)	索尼公司		
[标]发明人	YAMASHITA JUNICHI C O SONY CORPORATION UCHINO KATSUHIDE C O SONY CORPORATION		
发明人	YAMASHITA, JUNICHI C/O SONY CORPORATION UCHINO, KATSUHIDE C/O SONY CORPORATION		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0417 G09G2300/0819 G09G2300/0842 G09G2300/0852 G09G2300/0861 G09G2310/0251 G09G2310/0256 G09G2310/0262 G09G2320/0233 G09G2320/043		
优先权	2005294308 2005-10-07 JP		
其他公开文献	EP1772847A1		
外部链接	Espacenet		

摘要(译)

本发明公开了一种像素电路（2），其包括校正部分（Tr1-Tr4），其被配置为校正在像素电容（Cs）中采样的输入电压，以抵消输出电流对载流子迁移率的依赖性。在像素电路（2）中，校正部分（Tr1-Tr4）根据从扫描线（WS）提供的控制信号进行操作，以从驱动晶体管（Trd）提取输出电流，并将提取的输出电流引入到发光器件（EL）的电容（电流）和像素电容（Cs）用于校正输入电压。像素电路（2）还包括添加到发光器件（EL）的电容（Coled）的附加电容（Csub）。在像素电路（2）中，从驱动晶体管（Trd）提取的输出电流的一部分流入附加电容（Csub），以给校正部分（Tr1-Tr4）的操作提供时间余量。