

(19)



(11)

EP 1 653 434 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention
of the grant of the patent:
30.01.2019 Bulletin 2019/05

(51) Int Cl.:
G09G 3/3233 ^(2016.01) **G09G 3/3266** ^(2016.01)

(21) Application number: **05109982.8**

(22) Date of filing: **26.10.2005**

(54) **Scan driver, light emitting display using the same, and driving method thereof**

Zeilentreiber, lichtemittierende Anzeige damit und Ansteuerverfahren dafür

Circuit de commande de lignes, affichage électroluminescent l'utilisant, et son procédé de commande

(84) Designated Contracting States:
DE FR GB

(30) Priority: **28.10.2004 KR 2004086915**

(43) Date of publication of application:
03.05.2006 Bulletin 2006/18

(73) Proprietor: **Samsung Display Co., Ltd.**
Gyeonggi-do (KR)

(72) Inventors:
• **EOM, Ki Myeong**
Kyeonggi-do (KR)
• **OH, Choon Yul**
Kyeonggi-do (KR)

(74) Representative: **Gulde & Partner**
Patent- und Rechtsanwaltskanzlei mbB
Wallstraße 58/59
10179 Berlin (DE)

(56) References cited:
EP-A- 1 424 674 **JP-A- 2004 191 574**
US-A1- 2002 196 389 **US-A1- 2003 107 560**
US-A1- 2003 142 509

• **CHOI S M ET AL: "A SELF-COMPENSATED
VOLTAGE PROGRAMMING PIXEL STRUCTURE
FOR ACTIVE-MATRIX ORGANIC LIGHT
EMITTING DIODES" IDW. PROCEEDINGS OF THE
INTERNATIONAL DISPLAY WORKSHOPS, XX,
XX, 2003, pages 535-538, XP008057381**

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 1 653 434 B1

Description**CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2004-0086915, filed on October 28, 2004, in the Korean Intellectual Property Office.

BACKGROUND**1. Field of the Invention**

[0002] The present invention relates to a scan driver, a light emitting display including the same, a driving method thereof, and more particularly, to a scan driver, a light emitting display including the same, and a driving method thereof, in which the number of wiring lines is decreased, and the number of output lines connected to a scan driver is decreased, thereby enhancing an aperture ratio and reducing power consumption.

2. Discussion of Related Art

[0003] Recently, various flat panel displays have been developed to replace cathode ray tube (CRT) displays because the CRT displays are relatively heavy and bulky. Among the flat panel displays, a light emitting display is notable because it has high emission efficiency, high brightness, a wide viewing angle, and a fast response time.

[0004] The light emitting display includes a plurality of light emitting devices, wherein each light emitting device has a structure in which an emission layer is placed between a cathode electrode and an anode electrode. Here, electrons and holes are injected into the emission layer and recombined to create excitons, and light is emitted when an exciton falls to a lower energy level.

[0005] Such a light emitting display is classified into an inorganic light emitting display including an inorganic emission layer, and an organic light emitting display including an organic emission layer.

[0006] FIG. 1 is a circuit diagram of a pixel provided in a conventional light emitting display. Referring to FIG. 1, four pixels are adjacent to each other, and each pixel includes a light emitting device (e.g., organic light emitting diode (OLED)) and a pixel circuit. The pixel circuit includes a first transistor M1, a second transistor M2, a third transistor M3, and a capacitor Cst. Here, each of the first through third transistors M1, M2 and M3 has a gate, a source and a drain; and the capacitor Cst has a first electrode and a second electrode.

[0007] Every pixel has the same configuration, and thus a top left pixel will be exemplarily described hereinbelow. The first transistor M1 includes the source connected to a power line Vdd, the drain connected to the source of the third transistor M3, and the gate connected to a first node A. The first node A is connected to the drain of the second transistor M2. Here, the first transistor M1 supplies current corresponding to the data signal to the light emitting device OLED.

[0008] The second transistor M2 includes the source connected to a data line D1, the drain connected to the first node A, and the gate connected to a first scan line S1. Here, the second transistor M2 receives a first selection signal through its gate and supplies the data signal to the first node A.

[0009] The third transistor M3 includes the source connected to the drain of the first transistor M1, the drain connected to an anode electrode of the light emitting device OLED, and the gate connected to an emission control line E1 to respond to an emission control signal. Here the third transistor M3 controls the current flowing from the first transistor M1 to the light emitting device OLED in response to the emission control signal, thereby controlling the light emitting device OLED to emit light.

[0010] The capacitor Cst includes the first electrode connected to the power line Vdd, and the second electrode connected to the first node A. Here, the capacitor Cst stores electric charges corresponding to the data signal, and supplies a signal based on the stored electric charges to the gate of the first transistor M1 for one frame, thereby maintaining an operation of the first transistor M1 for one frame.

[0011] However, in the pixel provided in the conventional light emitting display, the emission control lines are connected to pixel rows, respectively. Therefore, the number of wiring lines is proportional to the number of emission control lines, thereby deteriorating an aperture ratio.

[0012] Further, in this case, the scan driver outputs the emission control signal to the plurality of emission control lines, and therefore, the number of output lines connected to the scan driver increases in proportion to the number of emission control lines, thereby increasing the number of components provided in the scan driver. Therefore, the power consumption increases in the scan driver. Further, the size of the scan driver is increased, thereby wastefully occupying much space of the light emitting display.

[0013] EP 1 424 674 A1 discloses an EL display panel whis is supplied with a higher current in order to charge/discharge parasitic devices. Further, the device is fed with the current for only a part of a one-frame period.

[0014] CHOI S MET AL: "A SELF-COMPENSATED VOLTAGE PROGRAMMING PIXEL STRUCTURE FOR ACTIVE-MATRIX ORGANIC LIGHT EMITTING DIODES", IOW. PROCEEDINGS OF THE INTERNATIONAL DISPLAY WORKSHOPS, XX, XX, 2003, pages 535-538, XP008057381, discloses a pixel structure which is programmed with two scan line cycles. The actual current row scan signal and the previous current row scan signal are applied.

[0015] US 2002/196389 A1 discloses an electro-optical device comprising pixels with a scan line and a second gate line shared by adjacent pixel rows for controlling emission of the pixels. The signals on these two lines are not generated by a shift register.

[0016] JP 2004 191574 A discloses an active matrix panel with a pixel having a memory function, wherein the scan driver contains a shift register for generating scan signals.

[0017] US 2003/107560 A1 discloses an OLED device having pixels with a first scan line shared by adjacent pixel rows and a second scan line for controlling emission of a single pixel row.

[0018] US 2003/0142509 A1 is directed to a light emitting display including control circuit for supplying scanning signals and control signals to a pixel circuit.

SUMMARY OF THE INVENTION

[0019] Accordingly, it is an aspect of the present invention to provide a scan driver, a light emitting display including the same, and a driving method thereof, in which the number of emission control lines is decreased to enhance an aperture ratio, and thus the number of signals outputted from the scan driver is also decreased, thereby making fabrication thereof easy and reducing power consumption.

[0020] An exemplary embodiment according to the present invention provides a light emitting display according to claim 1.

[0021] Yet another exemplary embodiment according to the present invention provides a method of driving a light emitting display according to claim 12.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] These and/or other features and aspects of the present invention will become apparent and more readily appreciated from the following description of exemplary embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 is a circuit diagram of pixels provided in a conventional light emitting display;

FIG. 2 illustrates a configuration of a light emitting display according to a first exemplary embodiment of the present invention;

FIG. 3 is a circuit diagram of a pixel portion provided in the light emitting display according to the first exemplary embodiment of the present invention;

FIG. 4 illustrates a configuration of a light emitting display according to a second exemplary embodiment of the present invention;

FIG. 5 is a circuit diagram of a pixel portion provided in the light emitting display according to the second exemplary embodiment of the present invention;

FIG. 6 illustrates a configuration of a light emitting display according to a third exemplary embodiment of the present invention;

FIG. 7 is a circuit diagram of a pixel portion provided in the light emitting display according to the third exemplary embodiment of the present invention;

FIG. 8 illustrates a configuration of a light emitting display according to a fourth exemplary embodiment of the present invention;

FIG. 9 is a circuit diagram of a pixel portion provided in the light emitting display according to the fourth exemplary embodiment of the present invention;

FIG. 10 is a circuit diagram of a first embodiment of a current generator according to an exemplary embodiment of the present invention;

FIG. 11 shows an operational timing diagram of a pixel including the current generator illustrated in FIG. 10;

FIG. 12 is a circuit diagram of a second exemplary embodiment of a current generator according to an exemplary embodiment of the present invention;

FIG. 13 shows an operational timing diagram of a pixel including the current generator illustrated in FIG. 12;

FIG. 14 illustrates a configuration of a scan driver provided in the light emitting display according to an exemplary embodiment of the present invention; and

FIG. 15 shows an operation timing diagram of the scan driver illustrated in FIG. 14.

DETAILED DESCRIPTION

[0023] Hereinafter, certain exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. Herein, when one element is described as being connected to another element, it may mean that the one element is directly connected to another element or that the one element is indirectly connected to another element via a third element. There may be parts shown in the drawings, or parts not shown in the drawings, that are not discussed in the specification as they are not essential to a complete understanding of the invention. Like reference numerals designate like elements throughout the drawings and the specification.

[0024] FIG. 2 illustrates a configuration of a light emitting display according to a first exemplary embodiment of the present invention. Referring to FIG. 2, a light emitting display according to the first exemplary embodiment of the present invention includes a pixel portion 100, a data driver 200, and a scan driver 300.

[0025] The pixel portion 100 includes a plurality of pixels 110 each including light emitting devices; a plurality of first scan lines S1, S2, ..., S2n-1, S2n arranged in a row direction; a plurality of emission control lines E1, E2, ..., En-1, En arranged in the row direction; a plurality of data lines D1, D2, ..., Dm-1, Dm arranged in a column direction; and a plurality of pixel power lines Vdd to supply pixel power. Here, the pixel power lines Vdd are connected to a first power line 130 and receives electric power from an external power source.

[0026] Further, data signals are transmitted through the data lines D1, D2, ..., Dm-1, Dm to the pixels 110 in response to scan signals transmitted through the scan lines S1, S2, ..., S2n-1, S2n, so that driving currents can be generated corresponding to the data signals. Also, a first transistor (not shown) provided in the pixel 110 generates a driving current corresponding to the data signal, and supplies the driving current to the light emitting device in response to the emission control signals transmitted through the emission control lines E1, E2, ..., En-1, En, thereby displaying an image. The number of emission control lines E1, E2, ..., En-1, En is equal to one half of the number of scan lines S1, S2, ..., S2n-1, S2n.

[0027] The data driver 200 is connected to the data lines D1, D2, ..., Dm-1, Dm and supplies the data signals to the pixel portion 100.

[0028] The scan driver 300 is provided on one side of the pixel portion 100, and connected to the plurality of scan lines S1, S2, ..., S2n-1, S2n and the plurality of emission control lines E1, E2, ..., En-1, En, thereby supplying the scan signals and the emission control signals to the pixel portion 100 in sequence. Thus, the rows of the pixel portion 100 are selected in sequence.

[0029] Here, one emission control line for supplying one emission control signal is connected with adjacent pixels respectively connected to two scan lines, so that two scan lines are sequentially selected by the scan signal, and then the pixels provided in two rows corresponding to the two scan lines are controlled to emit light at substantially the same time in response to one emission control signal.

[0030] FIG. 3 is a circuit diagram of a pixel portion provided in the light emitting display according to the first exemplary embodiment of the present invention. As shown in FIG. 3, a plurality of pixels 111, 112 are arranged in the pixel portion. Each pixel includes a current generator 115, a first transistor M1' connected to the current generator 115, and a light emitting device OLED connected to the first transistor M1'. For example, the light emitting device OLED may be an organic light emitting device.

[0031] The current generator 115 periodically generates a current corresponding to the data signal when the scan signal, the data signal, and pixel power are respectively transmitted through the scan lines S1 and S2, the data lines D1 and D2, and the pixel power lines Vdd, thereby allowing the current to flow in a first node N1. Here, the current generator 115 may include a plurality of transistors and a capacitor.

[0032] Then, each first transistor M1' provided in two adjacent pixels connected to the same data line is connected to the same emission control line E1, and receives one emission control signal from the scan driver 300, so that the light emitting device OLED emits light according to operations of the first transistor M1'. At this time, one emission control signal is transmitted to two row lines, so that the light emitting devices OLED placed on two pixel rows emit light at substantially the same time.

[0033] FIG. 4 illustrates a configuration of a light emitting display according to a second exemplary embodiment of the present invention. Referring to FIG. 4, a light emitting display according to the second exemplary embodiment of the present invention includes a pixel portion 100', a data driver 200', and a scan driver 300.

[0034] The pixel portion 100' includes a plurality of pixels 110' each including light emitting devices; a plurality of first scan lines S1, S2, ..., S2n-1, S2n arranged in a row direction; a plurality of emission control lines E1, E2, ..., En-1, En arranged in the row direction; a plurality of data lines D1, D2, ..., Dm-1, Dm arranged in a column direction; and a plurality of pixel power lines Vdd to supply pixel power. Here, the number of emission control lines is equal to one half of the number of scan lines. Further, the pixel power line Vdd is connected to a first power line 130 and receives electric power from an external power source.

[0035] The signals transmitted through the plurality of scan lines S1, S2, ..., S2n-1, S2n are inputted to two rows of pixels. At this time, the pixels on one of the two rows receive the signal as an initialization signal to initialize the pixels, and the pixels on the other row receive the signal to make the data signals be transmitted to the pixels.

[0036] When the signal is used as the scan signal, data signals are transmitted from the data lines D1, D2, ..., Dm-1, Dm to the pixels 110' in response to the scan signals transmitted through the scan lines S1, S2, ..., S2n-1, S2n, so that driving currents can be generated corresponding to the data signals. Also, a first transistor (not shown) provided in the pixel 110' generates a driving current corresponding to the data signal, and supplies the driving current to the light emitting device in response to the emission control signals transmitted through the emission control lines E1, E2, ..., En-1, En, thereby displaying an image.

[0037] The data driver 200' is connected to the data lines D1, D2, ..., Dm-1, Dm and supplies the data signals to the pixel portion 100'.

[0038] The scan driver 300' is provided on one side of the pixel portion 100', and connected to the plurality of scan lines S1, S2, ..., S2n-1, S2n and the plurality of the emission control lines E1, E2, ..., En-1, En, thereby supplying the scan signals and the emission control signals to the pixel portion 100' in sequence. Thus, the rows of the pixel portion 100' are selected in sequence. In the scan driver 300', the number of output terminals to output the scan signals is twice as large as the number of output terminals to output the emission control signals.

[0039] Here, one emission control line for supplying one emission control signal is connected with adjacent pixels respectively connected to two scan lines, so that two scan lines are sequentially selected by the scan signals, and then the pixels provided on two rows are controlled to emit light at substantially the same time in response to one emission control signal.

[0040] FIG. 5 is a circuit diagram of a pixel portion provided in the light emitting display according to the second exemplary embodiment of the present invention. As shown in FIG. 5, a plurality of pixels 111', 112' are arranged in the pixel portion. Each pixel includes a current generator 115', a first transistor M1" connected to the current generator 115', and a light emitting device OLED connected to the first transistor M1". For example, the light emitting device OLED is an organic light emitting device.

[0041] The current generator 115' periodically generates a current corresponding to the data signal when the scan signal, the emission control signal, the data signal, and pixel power are respectively transmitted through the scan lines S1 and S2, the emission control lines E1, the data lines D1 and D2, and the pixel power line Vdd, thereby allowing the current to flow in a first node N2. Here, the current generator 115' may include a plurality of transistors and a capacitor.

[0042] Then, each first transistor M1" provided in two adjacent pixels connected to the same data line is connected to the same emission control line E1, and receives one emission control signal from the scan driver 300', so that the light emitting device OLED emits light according to operations of the first transistor M1". At this time, one emission control signal is transmitted to two rows of pixels, so that the light emitting devices OLED placed on the two rows emit light at substantially the same time.

[0043] FIG. 6 illustrates configuration of a light emitting display according to a third exemplary embodiment of the present invention. Referring to FIG. 6, a light emitting display according to the third exemplary embodiment of the present invention includes a pixel portion 400, a data driver 500, and a scan driver 600.

[0044] The pixel portion 400 includes a plurality of pixels 410 each including light emitting devices; a plurality of first scan lines S1, S2, ..., Sn-1, Sn arranged in a row direction; a plurality of emission control lines E1, E2, ..., En-1, En arranged in the row direction; a plurality of data lines D1, D2, ..., Dm-1, Dm arranged in a column direction; and a plurality of pixel power lines Vdd to supply pixel power. Here, the pixel power line Vdd is connected to a first power line 430 and receives electric power from an external power source.

[0045] Further, data signals are transmitted from the data lines D1, D2, ..., Dm-1, Dm to the pixels 110 in response to scan signals transmitted through the scan lines S1, S2, ..., Sn-1, Sn, so that driving currents can be generated corresponding to the data signals. Also, a first transistor (not shown) provided in the pixel 410 generates a driving current corresponding to the data signal, and supplies the driving current to the light emitting device in response to the emission control signals transmitted through the emission control lines E1, E2, ..., En-1, En, thereby displaying an image.

[0046] The data driver 500 is connected to the data lines D1, D2, ..., Dm-1, Dm and supplies the data signals to the pixel portion 400.

[0047] The scan driver 600 is provided on one side of the pixel portion 400, in which the output terminals to output the scan signals is twice as many as the output terminals to output the emission control signals. Here, one scan line is connected to one scan signal output terminal of the scan driver, and two emission control lines are connected to one emission control signal output terminal, so that the scan signal and the emission control signal are transmitted to the pixel portion 400 in sequence. That is, two adjacent pixels respectively connected to two different scan lines are connected to different emission control lines to which the same emission control signal is transmitted, thereby allowing two pixels to emit light at substantially the same time.

[0048] FIG. 7 is a circuit diagram of a pixel portion provided in the light emitting display according to the third exemplary embodiment of the present invention. The pixel portion includes a plurality of pixels 411, 412. As shown in FIG. 7, a current generator 415 periodically generates a current corresponding to the data signal when the scan signal, the data signal, and pixel power are respectively transmitted through the scan lines S1 and S2, the data lines D1 and D2, and the pixel power line Vdd, thereby allowing the current to flow in a first node N3. Here, the current generator 415 may

include a plurality of transistors and a capacitor.

[0049] Here, one output terminal G01 of the scan driver 600 is connected with a pair of emission control lines E1 and E2. Therefore, the pair of emission control lines receives one emission control signal from the scan driver 600, and transmits the same emission control signal to a first transistor M11 connected with the pair of emission control lines.

[0050] Further, the light emitting device OLED emits light according to operations of the first transistor M11, and thus one emission control signal is transmitted to two rows of pixels, so that the light emitting devices OLED in the two rows of pixels emit light at substantially the same time.

[0051] FIG. 8 illustrates a configuration of a light emitting display according to a fourth exemplary embodiment of the present invention. Referring to FIG. 8, a light emitting display according to the fourth exemplary embodiment of the present invention includes a pixel portion 400', a data driver 500', and a scan driver 600'.

[0052] The pixel portion 400' includes a plurality of pixels 410' each including light emitting devices; a plurality of first scan lines S1, S2, ..., Sn-1, Sn arranged in a row direction; a plurality of emission control lines E1, E2, ..., En-1, En arranged in the row direction; a plurality of data lines D1, D2, ..., Dm-1, Dm arranged in a column direction; and a plurality of pixel power lines Vdd to supply pixel power. Here, the pixel power line Vdd is connected to a first power line 430' and receives electric power from an external power source.

[0053] The signals transmitted through the plurality of scan lines S1, S2, ..., Sn-1, Sn are inputted to two rows of pixels. At this time, pixels on one of the two rows receive the signal as an initialization signal to initialize the pixels, and the pixels on the other row receive the signal to make the data signals be transmitted to the pixels.

[0054] When the signal is used as the scan signal, data signals are transmitted from the data lines D1, D2, ..., Dm-1, Dm to the pixels 410' in response to the scan signals transmitted through the scan lines S1, S2, ..., Sn-1, Sn, so that driving currents can be generated corresponding to the data signals. Also, a first transistor (not shown) provided in the pixel 410' generates a driving current corresponding to the data signal, and supplies the driving current to the light emitting device in response to the emission control signals transmitted to the emission control lines E1, E2, ..., En-1, En, thereby displaying an image.

[0055] The data driver 500' is connected to the data lines D1, D2, ..., Dm-1, Dm and supplies the data signals to the pixel portion 400'.

[0056] The scan driver 600' is provided on one side of the pixel portion 400'. The scan driver 600' has twice as many output terminals to output the scan signals as compared to output terminals to output the emission control signals. Here, one scan line is connected to one scan signal output terminal of the scan driver 600', and two emission control lines are connected to one emission control signal output terminal, so that the scan signal and the emission control signal are transmitted to the pixel portion 400' in sequence. That is, two adjacent pixels respectively connected to two different scan lines are connected to different emission control lines to which the same emission control signal is transmitted, thereby allowing two pixels to emit light at substantially the same time.

[0057] FIG. 9 is a circuit diagram of a pixel portion provided in the light emitting display according to the fourth exemplary embodiment of the present invention. As shown in FIG. 9, a current generator 415' periodically generates a current corresponding to the data signal when the scan signal, the emission control signal, the data signal, and pixel power are respectively transmitted through the scan lines S1 and S2, the emission control lines E1 and E2, the data lines D1 and D2, and the pixel power line Vdd, thereby allowing the current to flow in a first node N4. Here, the current generator 415' may include a plurality of transistors and a capacitor.

[0058] Here, one output terminal G01' of the scan driver 600' is connected to a pair of emission control lines E1 and E2. Therefore, the pair of emission control lines receives one emission control signal from the scan driver 600', and transmits the same emission control signal to a first transistor M11' connected with the pair of emission control lines.

[0059] Further, the light emitting device OLED emits light according to operations of the first transistor M11', and thus one emission control signal is transmitted to two rows of pixels, so that the light emitting devices OLED of the two rows of pixels emit light at substantially the same time.

[0060] FIG. 10 is a circuit diagram of a first embodiment of a current generator according to an exemplary embodiment of the present invention. By way of example, the current generator of FIG. 10 may be used as one or more of the current generators 115, 115', 415 and 415' of FIGs. 3, 5, 7 and 9. Referring to FIG. 10, the current generator includes a second transistor M22, a third transistor M23, and a capacitor Cst'. Here, each of the second transistor M22 and the third transistor M23 includes a gate, a source and a drain. Further, the capacitor Cst' includes a first electrode and a second electrode.

[0061] The second transistor M22 includes the source connected to a power line Vdd, the drain connected to a first node N, and the gate connected to a second node A'. Here, the second node A' is connected to the drain of the third transistor M23. The second transistor M22 supplies a current corresponding to the data signal to a light emitting device OLED.

[0062] The third transistor M23 includes the source connected to a data line Dm, the drain connected to the second node A', and the gate connected to a first scan line Sn. Here, the third transistor M23 supplies the data signal to the second node A' in response to a first selection signal transmitted to its gate. In this embodiment, n and m are arbitrary

integers.

[0063] The capacitor Cst' includes the first electrode connected to the power line Vdd, and the second electrode connected to the first node A'. Here, the capacitor Cst' stores therein an electric charge corresponding to the data signal, and supplies the stored electric charge to the gate of the second transistor M22 for one frame, thereby maintaining an operation of the second transistor M22 for one frame.

[0064] FIG. 11 shows an operational timing diagram of a pixel including the current generator illustrated in FIG. 10. Referring to FIGs. 3, 10 and 11, for example, the pixels are divided into a first (upper) pixel 111, and a second (lower) pixel 112, and every pixel is operated by a first scan signal s2n-1 transmitted to the current generator 115 of the first pixel 111, a second scan signal s2n transmitted to the current generator 115 of the second pixel 112, and an emission control signal en inputted through the first transistor M1'. In this example, the node N of FIG. 10 would correspond to the node N1 of FIG. 3.

[0065] When the first scan signal s2n-1 is changed from a high level signal to a low level signal but the second scan signal s2n and the emission control signal en are maintained at the high signal, the third transistor M23 is turned on, thereby supplying the data signal to the second node A'. At this time, the capacitor Cst' includes the first electrode connected to the pixel power line Vdd to receive the pixel power, and the second electrode connected to the second node A' to receive the voltage corresponding to the data signal. Therefore, the capacitor Cst' is charged with the voltage corresponding to a voltage difference between the pixel power and the data signal, thereby supplying the charged voltage to the gate of the second transistor M22. At this time, a current that can be represented by the following Equation 1 would flow from the source to the drain of the second transistor M22 if the current path is not interrupted.

[Equation 1]

$$I_{OLED} = \frac{\beta}{2} (V_{gs} - V_{th})^2 = \frac{\beta}{2} (V_{data} - V_{dd} - V_{th})^2$$

where I_{OLED} is a current flowing in the light emitting device OLED; V_{gs} is a voltage applied between the source and the gate of the second transistor M22; V_{dd} is a voltage of the pixel power, V_{th} is a threshold voltage of the second transistor M22; and V_{data} is a voltage corresponding to the data signal.

[0066] However, the emission control signal en is a high level signal, so that the first transistor M1' is turned off, thereby interrupting the current. As the current does not flow in the first pixel 111, the first pixel 111 does not emit light.

[0067] Further, when the second scan signal s2n is changed from a high level signal to a low level signal, the third transistor M23 is turned on, thereby supplying the data signal to the second node A'. At this time, the capacitor Cst' includes the first electrode connected to the pixel power line Vdd to receive the pixel power, and the second electrode connected to the second node A' to receive the data signal. Thus, the capacitor Cst' is charged with the voltage corresponding to a difference between the pixel power and the data signal, thereby supplying the charged voltage to the gate of the second transistor M22.

[0068] Therefore, the current that can be represented by the Equation 1 would flow from the source to the drain of the second transistor M22 if the current path is not interrupted.

[0069] However, the emission control signal en is a high level signal, so that the first transistor M1' is turned off, thereby interrupting the current. As the current does not flow in the second pixel 112, the second pixel 112 does not emit light.

[0070] Further, when the emission control signal en supplied through the emission control line En connected to the first pixel 111 and the second pixel 112 is changed to a low level signal, the current that can be represented by the Equation 1 flows in both the first pixel 111 and the second pixel 112, so that both the first and second pixels 111 and 112 emit light.

[0071] FIG. 12 is a circuit diagram of a second embodiment of a current generator according to an exemplary embodiment of the present invention. By way of example, the current generator of FIG. 10 may be used as one or more of the current generators 115, 115', 415 and 415' of FIGs. 3, 5, 7 and 9, respectively. Referring to FIG. 12, the current generator includes second through sixth transistors M32, M33, M34, M35 and M36, and a capacitor Cst". Here, each of the second through sixth transistors M32 through M36 is a p-channel metal oxide semiconductor (PMOS) transistor, and includes a gate, a source and a drain. Further, the capacitor Cst" includes a first electrode and a second electrode. In the described embodiment, there may not be any physical differences between each drain and each source of the second through sixth transistors M32 through M36. Alternatively, the source, the drain and the gate may be referred to as first, second and third electrodes, respectively.

[0072] The current generator of FIG. 12 is connected to the first transistor M1', M1", M11 or M11' respectively of FIGs. 3, 5, 7 and 9 via a first node N'. Further, the emission control line En connected to the first transistor is connected to the current generator, thereby controlling the pixel power Vdd being inputted to the current generator using the emission control signal en.

[0073] The second transistor M32 includes the source connected to a second node A", the drain connected to a third node B, and the gate connected to a fourth node C, so that the current flows from the second node A" to the third node B according to voltages applied to the fourth node C.

[0074] The third transistor M33 includes the source connected to a data line Dm, the drain connected to the second node A", and the gate connected to a second scan line S2n. Here, the third transistor M33 selectively supplies the data signal to the second node A" through the data line Dm in response to a first scan signal s2n transmitted through the first scan line S2n.

[0075] The fourth transistor M34 includes the source connected to the third node B, the drain connected to the fourth node C, and the gate connected to the first scan line S2n. Here, the fourth transistor M34 makes the third node B and the fourth node C be substantially equipotential in response to the first scan signal s2n transmitted through the first scan line S2n, thereby allowing the second transistor M32 to be connected like a diode.

[0076] The fifth transistor M35 includes the source connected to the pixel power line Vdd, the drain connected to the second node A", and the gate connected to the emission control line En. Here, the fifth transistor M35 selectively supplies the pixel power to the second node A" in response to the first emission control signal en supplied through the emission control line En.

[0077] The sixth transistor M36 includes the source and the gate connected to the second scan line S2n-1, and the drain connected to the fourth node C, thereby supplying an initialization signal to the fourth node C. The initialization signal refers to a second scan signal s2n-1 inputted to the row prior to inputting the first scan signal s2n. Further, the second scan line S2n-1 refers to a scan line connected to a row of pixels to provide the second scan signal s2n-1 prior to providing the first scan signal s2n through the first scan line S2n.

[0078] The capacitor Cst" includes the first electrode connected to the pixel power line Vdd, and the second electrode connected to the fourth node C. Here, the capacitor Cst" is initialized by the initialization signal transmitted through the sixth transistor M36.

[0079] FIG. 13 shows an operational timing diagram of a pixel including the current generator illustrated in FIG. 12. Referring to FIGs. 5, 12 and 13, for example, the pixels are divided into a first (upper) pixel 111' and a second (lower) pixel 112', and every pixel is operated by a first scan signal s2n-1, a second scan signal s2n and a third scan signal s2n+1 that are transmitted to the current generators 115', and an emission control signal en inputted through the first transistor M1". Further, each pixel receives two scan signals.

[0080] When the first scan signal s2n-1 is changed from a high level signal to a low level signal but the second scan signal s2n, the third scan signal s2n+1 and the emission control signal en are maintained as the high level signal, the first pixel 111' is selected, and thus operated.

[0081] In the first pixel 111', when the sixth transistor M36 is turned on, the first scan signal s2n-1 is transmitted as the initialization signal to the fourth node C, thereby initializing the capacitor Cst". Then, when the second scan signal s2n is changed from a high level signal to a low level signal, and the emission control signal en is maintained as a high level signal, the third and fourth transistors M33 and M34 are turned on.

[0082] When the third transistor M33 and the fourth transistor M34 are turned on, the data signal is transmitted to the second node A" through the data line Dm, and the third node B and the fourth node C become substantially equipotential, so that the second transistor M32 is connected like a diode, thereby supplying the data signal from the second node A" to the fourth node C.

[0083] Thus, the capacitor Cst" is charged with voltage corresponding to the data signal, so that a voltage based on the following Equation 2 is applied between the gate and the source of the second transistor M32.

[Equation 2]

$$V_{sg} = V_{dd} - (V_{data} - V_{th})$$

Where V_{sg} is a voltage applied the source and the gate of the second transistor M32; V_{dd} is a pixel power voltage; V_{data} is a voltage corresponding to the data signal; and V_{th} is the threshold voltage of the second transistor M32.

[0084] The capacitor Cst" is charged with a voltage corresponding to the data signal, and thus the voltage based on the Equation 2 is applied between the gate and the source of the second transistor M32.

[0085] However, the emission control signal en is maintained as a high level signal, thereby interrupting the current flowing from the source to the drain of the second transistor M32.

[0086] Further, when the second scan signal s2n is changed from a high level signal to a low level signal, the second scan signal s2n is inputted to the sixth transistor M36 of the second pixel 112', thereby initializing the capacitor Cst" of the second pixel 112'.

[0087] Also, when the second pixel 112' is selected by the third scan signal s2n+1, the third transistor M33 and the fourth transistor M34 are turned on. As the third and fourth transistors M33 and M34 are turned on, the data signal is

transmitted to the second node A" through the data line Dm, the third node B and the fourth node C are substantially equipotential, and the second transistor M32 is connected like a diode, thereby transmitting the data signal from the second node A" to the fourth node C.

[0088] Therefore, the capacitor Cst" is charged with a voltage corresponding to the data signal, so that the voltage based on the foregoing Equation 2 is applied between the gate and the source of the second transistor M32.

[0089] Then, the emission control signal en is changed to a low level signal, maintained as the low level signal for a predetermined period, and inputted to the current generator, so that each fifth transistor M35 of the first pixel 111' and the second pixel 112' is turned on, thereby supplying the pixel power to the second node A". At this time, the voltage stored in the capacitor Cst" is transmitted to the gate of the second transistor M32, and the first transistor M31 is turned on by the emission control signal en while the fifth transistor M35 is turned on, so that the second transistor M32 controls the current to flow in both the first pixel 111' and the second pixel 112'. At this time, the current is calculated by the following Equation 3.

[Equation 3]

$$I_{OLED} = \frac{\beta}{2}(V_{gs} - V_{th})^2 = \frac{\beta}{2}(V_{data} - V_{dd} + V_{th} - V_{th})^2 = \frac{\beta}{2}(V_{data} - V_{dd})^2$$

where I_{OLED} is a current flowing in the light emitting device OLED; V_{gs} is a voltage applied between the source and the gate of the second transistor M32; V_{dd} is a voltage of the pixel power, V_{th} is the threshold voltage of the second transistor M32; and V_{data} is a voltage corresponding to the data signal.

[0090] Therefore, the current flows in the light emitting device OLED regardless of the threshold voltage of the second transistor M32.

[0091] FIG. 14 illustrates a configuration of a scan driver provided in a light emitting display according to an exemplary embodiment of the present invention. The scan driver 300 of FIG. 14, for example, may be used as one or more of the scan drivers 300, 300', 600 and 600' of FIGs. 2, 4, 6 and 8, respectively. Referring to FIG. 14, the scan driver includes a shift register 310, an operator 320, and a buffer 330.

[0092] The shift register 310 includes a plurality of flip-flops 311, 312, 313 and 314 (FF[1], FF[2], FF[3], FF[4]) connected in a column line, wherein an output signal is transmitted from a higher flip-flop 311 to a lower flip-flop 312, and the lower flip-flop 312 shifts the output signal of the higher flip-flop 311.

[0093] Hereinbelow, some flip-flops of the shift register 310 will be exemplarily described, and the flip-flops will be called a first flip-flop 311, a second flip-flop 312, a third flip-flop 313, and a fourth flip-flop 314 from the topmost flip-flop to the bottommost flip-flop in order.

[0094] The first flip-flop 311 receives a start pulse sp and shifts the start pulse sp into the shift signal, thereby outputting the shift signal to the second flip-flop 312 and the operator 320. Further, the second flip-flop 312 receives the shift signal from the first flip-flop 311, and outputs it to the third flip-flop 313 and the operator 320. Further, the third flip-flop 313 receives the shift signal from the second flip-flop 312, and outputs it to the fourth flip-flop 314 and the operator 320. Further, the fourth flip-flop 314 receives the signal from the third flip-flop 313 and outputs it to the lower flip-flop (not shown) and the operator 320.

[0095] The operator 320 includes a first operator 321 having a NAND gate, and a second operator 322 having a NAND gate and a NOR gate, wherein the first operator 321 and the second operator 322 are alternately formed. Hereinbelow, each NAND gate and each NOR gate of the first operator 321 and the second operator 322 will be called a first NAND gate 323, a second NAND gate 324, a third NAND gate 325, a fourth NAND gate 326, a first NOR gate 327, and a second NOR gate 328 from the topmost NAND or NOR gate to the bottommost NAND or NOR gate in order.

[0096] The first NAND gate 323 receives the signals from the first flip-flop 311 and the second flip-flop 312 and performs a NAND operation, thereby forming a first scan signal s[1]. The second NAND gate 324 receives the signals from the second flip-flop 312 and the third flip-flop 313 and performs the NAND operation, thereby forming a second scan signal s[2]. The third NAND gate 325 receives the signals from the third flip-flop 313 and the fourth flip-flop 314 and performs the NAND operation, thereby forming a third scan signal s[3]. The fourth NAND gate 326 receives the signals from the fourth flip-flop 314 and a lower flip-flop (not shown) and performs the NAND operation, thereby forming a fourth scan signal s[4].

[0097] Further, the first NOR gate 327 receives the signals from the second flip-flop 312 and the third flip-flop 313 and performs a NOR operation, thereby forming a first emission control signal e[1], and the second NOR gate 328 receives the signals from the fourth flip-flop 314 and the lower flip-flop (not shown) and performs the NOR operation, thereby forming a second emission control signal e[2].

[0098] Therefore, the first operator 321 including the NAND gate generates only the scan signal. Further, the second operator 322 including the NAND gate and the NOR gate generates the scan signal and the emission control signal.

[0099] The buffer 330 includes first through sixth buffers 331, 332, 333, 334, 335 and 336 from the topmost buffer to the bottommost buffer in order. Here, each of the first buffer 331, the second buffer 332, the fourth buffer 334, and the fifth buffer 335 includes two inverters connected in series, thereby enhancing driving efficiency of the scan signal. Further, each of the third buffer 333 and the sixth buffer 336 includes one inverter, thereby enhancing the driving efficiency of the emission control signal.

[0100] In the scan driver with this configuration, the number of output terminals to output the emission control signals decreases as compared with the number of output terminals to output the scan signals, so that the number of the output terminals in the scan driver decreases, thereby reducing the size of the scan driver.

[0101] FIG. 15 shows an operational timing diagram of the scan driver illustrated in FIG. 14. Referring to FIG. 15, in a state where a clock signal is inputted to each flip-flop of the shift register 310, when the start pulse sp is inputted to the first flip-flop 311, the first flip-flop 311 shifts the start pulse sp and outputs a first shift signal sr1 when the clock signal rises. Then, the first shift signal sr1 is inputted to the second flip-flop 312, and the second flip-flop 312 shifts the first shift signal sr1 and outputs a second shift signal sr2 when the clock signal falls.

[0102] At this time, the first NAND gate 323 receives the first and second shift signals sr1 and sr2 and performs the NAND operation, thereby generating the first scan signal s[1]. Further, the second NAND gate 324 receives the second and third shift signals sr2 and sr3 and perform the NAND operation, thereby generating the second scan signal s[2]. Further, the third NAND gate 325 receives the third and fourth shift signals sr3 and sr4 and perform the NAND operation, thereby generating the third scan signal s[3]. Further, the fourth NAND gate 326 receives the fourth shift signal sr4 and the fifth shift signal (not shown), thereby generating the second scan signal s[4].

[0103] Also, the first NOR gate 327 receives the second shift signal sr2 and the third shift signal sr3 and performs the NOR operation, thereby generating the first emission control signal e[1]. Further, the second NOR gate 328 receives the fourth shift signal sr4 and the fifth shift signal and performs the NOR operation, thereby generating the second emission control signal e[2].

[0104] As described above, the described embodiments of the present invention provide a scan driver, a light emitting display including the same, and a driving method thereof, in which one emission control line is shared by pixels provided on two adjacent rows, so that the number of wiring lines provided in a pixel portion is decreased, thereby enhancing an aperture ratio.

[0105] Further, because one emission control signal transmitted through the one emission control line is used for the pixels provided on two adjacent rows, the number of emission control signals outputted from the scan driver is reduced, thereby decreasing the number of components and wiring lines needed for the scan driver, and simplifying the fabrication process. Moreover, the size of the scan driver is decreased, thereby reducing the size of the light emitting display. Also, the scan driver consumes less power, thereby reducing the power consumption of the light emitting display.

[0106] Although a few exemplary embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes might be made in the described embodiments without departing from the principles of the invention, the scope of which is defined in the claims.

Claims

1. A light emitting display comprising:

a plurality of scan lines (S1, ..., S2n) adapted to transmit scan signals (s[1], s[2], s[3], s[4]);
 a plurality of data lines (D1, ..., Dm) adapted to transmit a data signal;
 a plurality of emission control lines (E1, ..., En) adapted to transmit an emission control signal (e[1], e[2]); and
 a plurality of pixels (110) adapted to emit light in response to the scan signals (s[1], s[2], s[3], s[4]), the data signal and the emission control signal (e[1], e[2]), a luminosity of the light being varied to represent different gray scales in accordance with a magnitude of the data signal,
 wherein each pixel (110) comprises a light emitting device (OLED), a current generator (115) connected to a corresponding scan line (SL1), a corresponding data line (DL1) and to a pixel power line Vdd for generating a current corresponding to the data signal, and a first transistor (M1') connected between the light emitting device (OLED) and the current generator (115), and having a gate electrode coupled to a corresponding emission control line (E1) for controlling the light emission of the light emitting device (OLED), and
 a scan driver (300) adapted to supply the scan signals (s[1], s[2], s[3], s[4]) to respective scan lines (S1, S2, S3, S4, S2n-1, S2n) and to supply the emission control signals (e[1], e[2]) to respective emission control lines (E1, E2, En), the scan driver (300) comprising:

a shift register (310) adapted to shift an input starting signal (sp) and output a plurality of shift signals to a plurality of output lines in sequence; and

characterized in that

the number of emission control lines (E1, E2, En) is half the number of scan lines (S1, S2, S3, S4, S2n-1, S2n), and

the scan driver (300) comprises:

a plurality of first operators (321) coupled to the plurality of output lines of the shift register (310) and for using the shift signals to generate only scan signals (s[1], s[3]); and
 a plurality of second operators (322) coupled to the plurality of output lines of the shift register (310) and for using the shift signals to generate scan signals (s[2], s[4]) and emission control signals (e[1], e[2]) for controlling the light emitting display to emit light,
 wherein the number of the emission control signals (e[1], e[2]) is half of the number of the scan signals (s[1], s[2], s[3], s[4]),
 wherein at least two of the plurality of pixels (110) that receive the scan signals through different scan lines (S1, S2) among the plurality of scan lines (S1, ..., S2n) are coupled to one emission control line (E1) among the plurality of emission control lines (E1, ..., En), and wherein:

- each first operator (321) is composed of a NAND gate (323, 325),
- each second operator (322) is composed of a NAND gate (324, 326) and a NOR gate (327, 328),
- the first operators (321) and the second operators (322) are alternately arranged,
- each of the NAND gates (323) of the first operator (321) inputs the output signals from adjacent (2j-1)th and (2j)th flip-flops (311 and 312) of the shift register (310), the output of this NAND gate (323) being coupled to the (2j-1)th scan line (s[1]),
- each of the NAND gates (324) of the second operator (322) inputs the output signals from two adjacent (2j)th and (2j+1)th flip-flops (312 and 313) of the shift register (310), the output of this NAND gate (324) being coupled to the (2j)th scan line (s[2]), and
- each of the NOR gates (327) of the second operator (322) inputs the output signals from two adjacent (2j)th and (2j+1)th flip-flops (312 and 313) of the shift register (310), the output of this NOR gate (327) being coupled to the (j)th light emission control line (e[1]), j being a positive integer.

2. The light emitting display according to claim 1, wherein the first operators (321) and the second operators (322) are alternately arranged.

3. The light emitting display to claim 2,
 wherein the plurality of shift signals comprises at least a first shift signal, a second shift signal and a third shift signal,
 wherein at least one of the first operators (321) has a NAND gate (323, 325) using the first shift signal and the second shift signal as two input signals, and
 wherein at least one of the second operators (322) has a NAND gate (324, 326) using the second shift signal and the third shift signal as two input signals, and a NOR gate (327, 328) using the second shift signal and the third shift signal as two input signals.

4. The light emitting display according to claim 2, wherein at least one of the first operators (321) is coupled to a first buffer (331, 334) to enhance driving efficiency of the scan signals (s[1], s[3]), and at least one of the second operators (322) is coupled to a second buffer (333, 336) to enhance driving efficiency of the emission control signals (e[1], e[2]).

5. The light emitting display according to claim 4, wherein the first buffer (331, 334) comprises an even number of inverters, and the second buffer (333, 336) comprises an odd number of inverters.

6. The light emitting display according to claim 1, wherein at least one of the pixels (110) comprises:

a light emitting device (OLED) adapted to emit light corresponding to a current;
 a first transistor (M1') adapted to selectively transmit the current to the light emitting device (OLED) in response to the emission control signal;
 a second transistor adapted to generate the current corresponding to the data signal;
 a third transistor adapted to selectively transmit the data signal to the second transistor in response to a corresponding one of the scan signals; and
 a capacitor adapted to store a voltage corresponding to the data signal and to apply the stored voltage to the second transistor.

7. The light emitting display according to claim 6, wherein the light emitting device (OLED) comprises an organic light emitting diode.

8. The light emitting display according to claim 1, further comprising a data driver (200) to transmit the data signal to the data lines (D1, ..., Dm).

9. The light emitting display according to claim 1, wherein the plurality of pixels (110) comprise a first pixel (111) for receiving a first scan signal and a second scan signal among the scan signals, and a second pixel (112) for receiving the second scan signal and a third scan signal among the scan signals, wherein the first and second pixels (111, 112) are coupled to a same one of the emission control lines (E1).

10. The light emitting display according to claim 1, wherein the plurality of pixels (110) comprise a first pixel for receiving a first scan signal and a second scan signal among the scan signals, and a second pixel for receiving the second scan signal and a third scan signal among the scan signals, wherein the first and second pixels emit light in response to one of the emission control signals, which is transmitted through different ones of the emission control lines.

11. The light emitting display according to claim 9 or 10, wherein the first pixel (111) comprises:

a light emitting device (OLED) adapted to emit light corresponding to a current;
a first transistor adapted (M1') to selectively transmit the current to the light emitting device (OLED) in response to the emission control signal;
a second transistor adapted to generate the current corresponding to the data signal;
a third transistor adapted to transmit the data signal to the second transistor in response to the second scan signal;
a fourth transistor adapted to selectively connect the second transistor like a diode in response to the second scan signal;
a fifth transistor adapted to selectively apply a first power to the second transistor in response to the emission control signal;
a capacitor adapted to store a voltage corresponding to the data signal and to apply the stored voltage to the second transistor; and
a sixth transistor adapted to transmit an initialization signal to initialize the capacitor in response to the first scan signal.

12. A method of driving the light emitting display of one of the preceding claims, the method comprising:

shifting an input starting signal (sp) and outputting a plurality of shift signals to a plurality of output lines in sequence; and

characterized by the following steps:

using the shift signals with a plurality of first operators (321) coupled to the plurality of output lines of the shift register (310) to generate only scan signals (s[1], s[3]); and
using the shift signals with a plurality of second operators (322) coupled to the plurality of output lines of the shift register (310) to generate scan signals (s[2], s[4]) and emission control signals (e[1], e[2]) for controlling the light emitting display to emit light, wherein the number of the emission control signals (e[1], e[2]) is half of the number of the scan signals (s[1], s[2], s[3], s[4]);
transmitting a first scan signal (s[1]) to a first scan line (S1) coupled to a first pixel row comprising a plurality of pixels (111);
transmitting a second scan signal (s[2]) to a second scan line (S2) adjacent to the first scan line (S1) and coupled to a second pixel row comprising a plurality of pixels (112); and
transmitting a first emission control signal (e[1]) to a first emission control line (E1) coupled to the pixels (111, 112) of the first and second scan lines (S1, S2) for allowing the first pixel row and the second pixel row to emit light at substantially the same time in response to the first emission control signal (e[1]) transmitted to the first and second pixel rows.

13. The method according to claim 12, wherein a luminosity of the light is varied to represent different gray scales in accordance with magnitudes of data signals respectively provided when the scan signal and the another scan signal are transmitted.

14. The method according to claim 12, further comprising:

transmitting the second scan signal to the first pixel row, and
transmitting a third scan signal to the second pixel row.

15. The method according to one of the claims 12-14, wherein the same emission control signal is transmitted through emission control lines that are different from each other.

16. The method according to one of the claims 12-14, wherein the same emission control signal is transmitted through one emission control line.

Patentansprüche

1. Lichtemittierende Anzeige, umfassend:

eine Mehrzahl von Abtastleitungen (S1, ..., S2n), die zum Senden von Abtastsignalen (s[1], s[2], s[3], s[4]) ausgelegt sind;

eine Mehrzahl von Datenleitungen (D1, ..., Dm), die zum Senden eines Datensignals ausgelegt sind;

eine Mehrzahl von Emissionssteuerungsleitungen (E1, ..., En), die zum Senden eines Emissionssteuerungssignals (e[1], e[2]) ausgelegt sind; und

eine Mehrzahl von Pixeln (110), die zum Emittieren von Licht als Reaktion auf die Abtastsignale (s[1], s[2], s[3], s[4]), das Datensignal und das Emissionssteuerungssignal (e[1], e[2]) ausgelegt sind, wobei eine Leuchtkraft des Lichts verändert wird, um entsprechend einer Stärke des Datensignals unterschiedliche Graustufen darzustellen,

wobei jedes Pixel (110) eine lichtemittierende Vorrichtung (OLED), einen mit einer entsprechenden Abtastleitung (SL1), einer entsprechenden Datenleitung (DL1) und einer Pixelstromleitung Vdd verbundenen Stromgenerator (115) zum Erzeugen eines dem Datensignal entsprechenden Stroms und einen zwischen die lichtemittierende Vorrichtung (OLED) und den Stromgenerator (115) geschalteten ersten Transistor (M1') umfasst, wobei der erste Transistor (M1') eine mit einer entsprechenden Emissionssteuerungsleitung (E1) gekoppelte Gate-Elektrode zum Steuern der Lichtemission der lichtemittierenden Vorrichtung (OLED) aufweist, und

einen Abtasttreiber (300), der dazu ausgelegt ist, die Abtastsignale (s[1], s[2], s[3], s[4]) an die jeweiligen Abtastleitungen (S1, S2, S3, S4, S2n-1, S2n) zu liefern und die Emissionssteuerungssignale (e[1], e[2]) an die jeweiligen Emissionssteuerungsleitungen (E1, E2, En) zu liefern, wobei der Abtasttreiber (300) umfasst:

ein Schieberegister (310), das dazu ausgelegt ist, ein Eingangsstartsignal (sp) zu verschieben und eine Mehrzahl von Schiebesignalen an eine Mehrzahl von Ausgangsleitungen der Reihe nach auszugeben; und

dadurch gekennzeichnet, dass

die Anzahl der Emissionssteuerungsleitungen (E1, E2, En) der halben Anzahl der Abtastleitungen (S1, S2, S3, S4, S2n-1, S2n) entspricht und der Abtasttreiber (300) umfasst:

eine Mehrzahl von ersten Operatoren (321), die mit der Mehrzahl von Ausgangsleitungen des Schieberegisters (310) gekoppelt sind und dazu dienen, unter Verwendung der Schiebesignale nur die Abtastsignale (s[1], s[3]) zu erzeugen; und

eine Mehrzahl von zweiten Operatoren (322), die mit der Mehrzahl von Ausgangsleitungen des Schieberegisters (310) gekoppelt sind und dazu dienen, unter Verwendung der Schiebesignale die Abtastsignale (s[2], s[4]) und die Emissionssteuerungssignale (e[1], e[2]) zum Steuern der lichtemittierenden Anzeige zum Emittieren von Licht zu erzeugen,

wobei die Anzahl der Emissionssteuerungssignale (e[1], e[2]) der halben Anzahl der Abtastsignale (s[1], s[2], s[3], s[4]) entspricht,

wobei mindestens zwei aus der Mehrzahl von Pixeln (110), welche die Abtastsignale über unterschiedliche Abtastleitungen (S1, S2) aus der Mehrzahl von Abtastleitungen (S1, ..., S2n) empfangen, mit einer Emissionssteuerungsleitung (E1) aus der Mehrzahl von Emissionssteuerungsleitungen (E1, ..., En) gekoppelt sind und wobei:

- jeder erste Operator (321) aus einem NAND-Gatter (323, 325) gebildet ist,

- jeder zweite Operator (322) aus einem NAND-Gatter (324, 326) und einem NOR-Gatter (327,

328) gebildet ist,

- die ersten Operatoren (321) und die zweiten Operatoren (322) abwechselnd angeordnet sind,
- jedes der NAND-Gatter (323) des ersten Operators (321) die Ausgangssignale von benachbarten $(2j-1)^{\text{ten}}$ und $(2j)^{\text{ten}}$ Flipflops (311 und 312) des Schieberegisters (310) als Eingangssignale aufnimmt, wobei der Ausgang dieses NAND-Gatters (323) mit der $(2j-1)^{\text{ten}}$ Abtastleitung ($s[1]$) gekoppelt ist,
- jedes der NAND-Gatter (324) des zweiten Operators (322) die Ausgangssignale von zwei benachbarten $(2j)^{\text{ten}}$ und $(2j+1)^{\text{ten}}$ Flipflops (312 und 313) des Schieberegisters (310) als Eingangssignale aufnimmt, wobei der Ausgang dieses NAND-Gatters (324) mit der $(2j)^{\text{ten}}$ Abtastleitung ($s[2]$) gekoppelt ist, und
- jedes der NOR-Gatter (327) des zweiten Operators (322) die Ausgangssignale von zwei benachbarten $(2j)^{\text{ten}}$ und $(2j+1)^{\text{ten}}$ Flipflops (312 und 313) des Schieberegisters (310) als Eingangssignale aufnimmt, wobei der Ausgang dieses NOR-Gatters (327) mit der $(j)^{\text{ten}}$ Lichtemissionssteuerungsleitung ($e[1]$) gekoppelt ist, wobei j eine positive ganze Zahl ist.

2. Lichtemittierende Anzeige nach Anspruch 1, wobei die ersten Operatoren (321) und die zweiten Operatoren (322) abwechselnd angeordnet sind.

3. Lichtemittierende Anzeige nach Anspruch 2,

wobei die Mehrzahl von Schiebesignalen mindestens ein erstes Schiebesignal, ein zweites Schiebesignal und ein drittes Schiebesignal umfasst,

wobei mindestens einer der ersten Operatoren (321) ein NAND-Gatter (323, 325) aufweist, welches das erste Schiebesignal und das zweite Schiebesignal als zwei Eingangssignale verwendet, und

wobei mindestens einer der zweiten Operatoren (322) ein NAND-Gatter (324, 326) aufweist, welches das zweite Schiebesignal und das dritte Schiebesignal als zwei Eingangssignale verwendet, und ein NOR-Gatter (327, 328) aufweist, welches das zweite Schiebesignal und das dritte Schiebesignal als zwei Eingangssignale verwendet.

4. Lichtemittierende Anzeige nach Anspruch 2, wobei mindestens einer der ersten Operatoren (321) mit einem ersten Puffer (331, 334) gekoppelt ist, um die Ansteuereffektivität der Abtastsignale ($s[1]$, $s[3]$) zu verbessern, und mindestens einer der zweiten Operatoren (322) mit einem zweiten Puffer (333, 336) gekoppelt ist, um die Ansteuereffektivität der Emissionssteuerungssignale ($e[1]$, $e[2]$) zu verbessern.

5. Lichtemittierende Anzeige nach Anspruch 4, wobei der erste Puffer (331, 334) eine gerade Anzahl von Wechselrichtern umfasst und der zweite Puffer (333, 336) eine ungerade Anzahl von Wechselrichtern umfasst.

6. Lichtemittierende Anzeige nach Anspruch 1, wobei mindestens eines der Pixel (110) umfasst:

eine lichtemittierende Vorrichtung (OLED), die zum Emittieren von Licht, das einem Strom entspricht, ausgelegt ist;

einen ersten Transistor ($M1'$), der zum selektiven Übertragen des Stroms an die lichtemittierende Vorrichtung (OLED) als Reaktion auf das Emissionssteuerungssignal ausgelegt ist;

einen zweiten Transistor, der zum Erzeugen des Stroms, der dem Datensignal entspricht, ausgelegt ist;

einen dritten Transistor, der zum selektiven Senden des Datensignals an den zweiten Transistor als Reaktion auf ein entsprechendes der Abtastsignale ausgelegt ist; und

einen Kondensator, der zum Speichern einer Spannung, die dem Datensignal entspricht, und zum Anlegen der gespeicherten Spannung an den zweiten Transistor ausgelegt ist.

7. Lichtemittierende Anzeige nach Anspruch 6, wobei die lichtemittierende Vorrichtung (OLED) eine organische lichtemittierende Diode umfasst.

8. Lichtemittierende Anzeige nach Anspruch 1, ferner umfassend einen Datentreiber (200) zum Senden des Datensignals an die Datenleitungen ($D1$, ..., Dm).

9. Lichtemittierende Anzeige nach Anspruch 1,

wobei die Mehrzahl von Pixeln (110) ein erstes Pixel (111) zum Empfangen eines ersten Abtastsignals und eines zweiten Abtastsignals aus den Abtastsignalen und ein zweites Pixel (112) zum Empfangen des zweiten Abtastsignals und eines dritten Abtastsignals aus den Abtastsignalen umfasst, wobei das erste und zweite Pixel (111, 112) mit derselben der Emissionssteuerungsleitungen ($E1$) gekoppelt sind.

10. Lichtemittierende Anzeige nach Anspruch 1,
wobei die Mehrzahl von Pixeln (110) ein erstes Pixel zum Empfangen eines ersten Abtastsignals und eines zweiten
Abtastsignals aus den Abtastsignalen und ein zweites Pixel zum Empfangen des zweiten Abtastsignals und eines
dritten Abtastsignals aus den Abtastsignalen umfasst, wobei das erste und zweite Pixel als Reaktion auf eines der
Emissionssteuerungssignale, welches durch verschiedene der Emissionssteuerungsleitungen gesendet werden,
Licht emittieren.

11. Lichtemittierende Anzeige nach Anspruch 9 oder 10, wobei das erste Pixel (111) umfasst:

eine lichtemittierende Vorrichtung (OLED), die zum Emittieren von Licht, das einem Strom entspricht, ausgelegt
ist;
einen ersten Transistor (M1') zum selektiven Übertragen des Stroms an die lichtemittierende Vorrichtung (OLED)
als Reaktion auf das Emissionssteuerungssignal;
einen zweiten Transistor, der zum Erzeugen des Stroms, der dem Datensignal entspricht, ausgelegt ist;
einen dritten Transistor, der zum Senden des Datensignals an den zweiten Transistor als Reaktion auf das
zweite Abtastsignal ausgelegt ist;
einen vierten Transistor, der dazu ausgelegt ist, den zweiten Transistor als Reaktion auf das zweite Abtastsignal
wie eine Diode selektiv zu verbinden;
einen fünften Transistor, der zum selektiven Anlegen eines ersten Stroms an den zweiten Transistor als Reaktion
auf das Emissionssteuerungssignal ausgelegt ist;
einen Kondensator, der zum Speichern einer Spannung, die dem Datensignal entspricht, und zum Anlegen der
gespeicherten Spannung an den zweiten Transistor ausgelegt ist; und
einen sechsten Transistor, der zum Senden eines Initialisierungssignals zum Initialisieren des Kondensators
als Reaktion auf das erste Abtastsignal ausgelegt ist.

12. Verfahren zum Ansteuern der lichtemittierenden Anzeige nach einem der vorangehenden Ansprüche, wobei das
Verfahren umfasst:

Verschieben eines Eingangsstartsignals (sp) und Ausgeben, der Reihe nach, einer Mehrzahl von Schiebesig-
nalen an eine Mehrzahl von Ausgangsleitungen; und
gekennzeichnet durch folgende Schritte:

Verwenden der Schiebesignale mit einer Mehrzahl von ersten Operatoren (321), die mit der Mehrzahl von
Ausgangsleitungen des Schieberegisters (310) gekoppelt sind, zum Erzeugen nur der Abtastsignale (s[1],
s[3]); und

Verwenden der Schiebesignale mit einer Mehrzahl von zweiten Operatoren (322), die mit der Mehrzahl
von Ausgangsleitungen des Schieberegisters (310) gekoppelt sind, zum Erzeugen der Abtastsignale (s[2],
s[4]) und der Emissionssteuerungssignale (e[1], e[2]) zum Steuern der lichtemittierenden Anzeige zum
Emittieren von Licht, wobei die Anzahl der Emissionssteuerungssignale (e[1], e[2]) der halben Anzahl der
Abtastsignale (s[1], s[2], s[3], s[4]) entspricht;

Senden eines ersten Abtastsignals (s[1]) an eine erste Abtastleitung (S1), die mit einer ersten Pixelzeile
gekoppelt ist, die eine Mehrzahl von Pixeln (111) umfasst;

Senden eines zweiten Abtastsignals (s[2]) an eine zweite Abtastleitung (S2), die der ersten Abtastleitung
(S1) benachbart und mit einer zweiten Pixelzeile gekoppelt ist, die eine Mehrzahl von Pixeln (112) umfasst;
und

Senden eines ersten Emissionssteuerungssignals (e[1]) an eine erste Emissionssteuerungsleitung (E1),
die mit den Pixeln (111, 112) der ersten und zweiten Abtastleitung (S1, S2) gekoppelt ist, um als Reaktion
auf das an die erste und zweite Pixelzeile gesendete erste Emissionssteuerungssignal (e[1]) zu ermöglichen,
dass die erste Pixelzeile und die zweite Pixelzeile im Wesentlichen zur selben Zeit Licht emittieren.

13. Verfahren nach Anspruch 12, wobei eine Leuchtkraft des Lichts verändert wird, um entsprechend den Stärken von
Datensignalen, die jeweils geliefert werden, wenn das Abtastsignal und das andere Abtastsignal gesendet werden,
unterschiedliche Graustufen darzustellen.

14. Verfahren nach Anspruch 12, ferner umfassend:

Senden des zweiten Abtastsignals an die erste Pixelzeile und
Senden eines dritten Abtastsignals an die zweite Pixelzeile.

15. Verfahren nach einem der Ansprüche 12-14, wobei dasselbe Emissionssteuerungssignal über voneinander verschiedene Emissionssteuerungsleitungen gesendet wird.

16. Verfahren nach einem der Ansprüche 12-14, wobei dasselbe Emissionssteuerungssignal über eine Emissionssteuerungsleitung gesendet wird.

Revendications

1. Afficheur électroluminescent comprenant :

une pluralité de lignes de balayage (S1, ..., S2n) conçues pour transmettre des signaux de balayage (s[1], s[2], s[3], s[4]) ;

une pluralité de lignes de données (D1, ..., Dm) conçues pour transmettre un signal de donnée ;

une pluralité de lignes de commande d'émission (E1, ..., En) conçues pour transmettre un signal de commande d'émission (e[1], e[2]) ; et

une pluralité de pixels (110) conçus pour émettre une lumière en réponse aux signaux de balayage (s[1], s[2], s[3], s[4]), au signal de donnée et au signal de commande d'émission (e[1], e[2]), une luminosité de la lumière étant modifiée pour représenter des gammes de gris différentes en fonction d'une amplitude du signal de donnée, dans lequel chaque pixel (110) comprend un dispositif électroluminescent (OLED), un générateur de courant (115) raccordé à une ligne de balayage (SL1) correspondante, à une ligne de données (DL1) correspondante et à une ligne d'alimentation de pixel Vdd pour générer un courant correspondant au signal de donnée, et un premier transistor (M1') raccordé entre le dispositif électroluminescent (OLED) et le générateur de courant (115), et présentant une électrode de porte couplée à une ligne de commande d'émission (E1) correspondante pour commander l'émission de lumière du dispositif électroluminescent (OLED), et

un pilote de balayage (300) conçu pour fournir les signaux de balayage (s[1], s[2], s[3], s[4]) à des lignes de balayage (S1, S2, S3, S4, S2n-1, S2n) respectives et pour fournir les signaux de commande d'émission (e[1], e[2]) à des lignes de commande d'émission (E1, E2, En) respectives, le pilote de balayage (300) comprenant :

un registre à décalage (310) conçu pour décaler un signal de lancement (sp) entré et sortir une pluralité de signaux de décalage vers une pluralité de lignes de sortie en séquence ; et

caractérisé en ce que :

le nombre de lignes de commande d'émission (E1, E2, En) est la moitié du nombre de lignes de balayage (S1, S2, S3, S4, S2n-1, S2n), et

le pilote de balayage (300) comprend :

une pluralité de premiers opérateurs (321) couplés à la pluralité de lignes de sortie du registre à décalage (310) et pour utiliser les signaux de décalage afin de générer uniquement des signaux de balayage (s[1], s[3]) ; et

une pluralité de seconds opérateurs (322) couplés à la pluralité de lignes de sortie du registre à décalage (310) et pour utiliser les signaux de décalage afin de générer des signaux de balayage (s[2], s[4]) et des signaux de commande d'émission (e[1], e[2]) en vue de commander l'afficheur électroluminescent pour émettre une lumière,

dans lequel le nombre des signaux de commande d'émission (e[1], e[2]) est la moitié du nombre des signaux de balayage (s[1], s[2], s[3], s[4]),

dans lequel au moins deux de la pluralité de pixels (110) qui reçoivent les signaux de balayage via des lignes de balayage (S1, S2) différentes parmi la pluralité de lignes de balayage (S1, ..., S2n) sont couplés à une ligne de commande d'émission (E1) parmi la pluralité de lignes de commande d'émission (E1, ..., En), et dans lequel :

- chaque premier opérateur (321) est composé d'une porte NON-ET (323, 325),

- chaque second opérateur (322) est composé d'une porte NON-ET (324, 326) et d'une porte NON-OU (327, 328),

- les premiers opérateurs (321) et les seconds opérateurs (322) sont agencés en alternance, - chacune des portes NON-ET (323) du premier opérateur (321) entre les signaux de sortie depuis des (2j-1)^e et (2j)^e bascules bistables (311 et 312) adjacentes du registre à décalage (310), la sortie de cette porte NON-ET (323) étant couplée à la (2j-1)^e ligne de balayage (s[1]),

- chacune des portes NON-ET (324) du second opérateur (322) entre les signaux de sortie depuis deux $(2j)^{\text{e}}$ et $(2j+1)^{\text{e}}$ bascules bistables (312 et 313) adjacentes du registre à décalage (310), la sortie de cette porte NON-ET (324) étant couplée à la $(2j)^{\text{e}}$ ligne de balayage ($s[2j]$), et
 - chacune des portes NON-OU (327) du second opérateur (322) entre les signaux de sortie depuis deux $(2j)^{\text{e}}$ et $(2j+1)^{\text{e}}$ bascules bistables (312 et 313) adjacentes du registre à décalage (310), la sortie de cette porte NON-OU (327) étant couplée à la $(j)^{\text{e}}$ ligne de commande d'émission ($e[1]$) de lumière, j étant un nombre entier positif.

2. Afficheur électroluminescent selon la revendication 1, dans lequel les premiers opérateurs (321) et les seconds opérateurs (322) sont agencés en alternance.

3. Afficheur électroluminescent selon la revendication 2, dans lequel la pluralité de signaux de décalage comprend au moins un premier signal de décalage, un deuxième signal de décalage et un troisième signal de décalage, dans lequel au moins l'un des premiers opérateurs (321) présente une porte NON-ET (323, 325) utilisant le premier signal de décalage et le deuxième signal en tant que deux signaux d'entrée, et dans lequel au moins l'un des seconds opérateurs (322) présente une porte NON-ET (324, 326) utilisant le deuxième signal de décalage et le troisième signal de décalage en tant que deux signaux d'entrée, et une porte NON-OU (327, 328) utilisant le deuxième signal de décalage et le troisième signal en tant que deux signaux d'entrée.

4. Afficheur électroluminescent selon la revendication 2, dans lequel au moins l'un des premiers opérateurs (321) est couplé à un premier tampon (331, 334) pour améliorer une efficacité d'attaque des signaux de balayage ($s[1]$, $s[3]$), et au moins l'un des seconds opérateurs (322) est couplé à un second tampon (333, 336) pour améliorer une efficacité d'attaque des signaux de commande d'émission ($e[1]$, $e[2]$).

5. Afficheur électroluminescent selon la revendication 4, dans lequel le premier tampon (331, 334) comprend un nombre pair d'onduleurs, et le second tampon (333, 336) comprend un nombre impair d'onduleurs.

6. Afficheur électroluminescent selon la revendication 1, dans lequel au moins l'un des pixels (110) comprend :

un dispositif électroluminescent (OLED) conçu pour émettre une lumière correspondant à un courant ;
 un premier transistor ($M1'$) conçu pour transmettre de manière sélective le courant au dispositif électroluminescent (OLED) en réponse au signal de commande d'émission ;
 un deuxième transistor conçu pour générer le courant correspondant au signal de donnée ;
 un troisième transistor conçu pour transmettre de manière sélective le signal de donnée au deuxième transistor en réponse à l'un correspondant des signaux de balayage ; et
 un condensateur conçu pour stocker une tension correspondant au signal de donnée et pour appliquer la tension stockée au deuxième transistor.

7. Afficheur électroluminescent selon la revendication 6, dans lequel le dispositif électroluminescent (OLED) comprend une diode électroluminescente organique.

8. Afficheur électroluminescent selon la revendication 1, comprenant en outre un pilote de données (200) pour transmettre le signal de donnée aux lignes de données ($D1$, ..., Dm).

9. Afficheur électroluminescent selon la revendication 1, dans lequel la pluralité de pixels (110) comprend un premier pixel (111) pour recevoir un premier signal de balayage et un deuxième signal de balayage parmi les signaux de balayage, et un second pixel (112) pour recevoir le deuxième signal de balayage et un troisième signal de balayage parmi les signaux de balayage, dans lequel les premier et second pixels (111, 112) sont couplés à une même ligne des lignes de commande d'émission ($E1$).

10. Afficheur électroluminescent selon la revendication 1, dans lequel la pluralité de pixels (110) comprend un premier pixel pour recevoir un premier signal de balayage et un deuxième signal de balayage parmi les signaux de balayage, et un second pixel pour recevoir le deuxième signal de balayage et un troisième signal de balayage parmi les signaux de balayage, dans lequel les premier et second pixels émettent une lumière en réponse à l'un des signaux de commande d'émission, qui est transmis via des lignes de commande d'émission qui sont différentes.

11. Afficheur électroluminescent selon la revendication 9 ou 10, dans lequel le premier pixel (111) comprend :

un dispositif électroluminescent (OLED) conçu pour émettre une lumière correspondant à un courant ;
 un premier transistor conçu (M1') pour transmettre de manière sélective le courant au dispositif électroluminescent (OLED) en réponse au signal de commande d'émission ;
 un deuxième transistor conçu pour générer le courant correspondant au signal de donnée ;
 5 un troisième transistor conçu pour transmettre le signal de donnée au deuxième transistor en réponse au deuxième signal de balayage ;
 un quatrième transistor conçu pour raccorder de manière sélective le deuxième transistor comme une diode en réponse au deuxième signal de balayage ;
 10 un cinquième transistor conçu pour appliquer de manière sélective une première alimentation au deuxième transistor en réponse au signal de commande d'émission ;
 un condensateur conçu pour stocker une tension correspondant au signal de donnée et pour appliquer la tension stockée au deuxième transistor ; et
 un sixième transistor conçu pour transmettre un signal d'initialisation pour initialiser le condensateur en réponse au premier signal de balayage.

- 15
 12. Procédé d'attaque de l'afficheur électroluminescent selon l'une des revendications précédentes, le procédé comprenant :

20 le décalage d'un signal de lancement (sp) entré et la sortie d'une pluralité de signaux de décalage vers une pluralité de lignes de sortie en séquence ; et
caractérisé par les étapes suivantes :

25 l'utilisation des signaux de décalage avec une pluralité de premiers opérateurs (321) couplés à la pluralité de lignes de sortie du registre à décalage (310) afin de générer uniquement des signaux de balayage (s[1], s[3]); et

30 l'utilisation des signaux de décalage avec une pluralité de seconds opérateurs (322) couplés à la pluralité de lignes de sortie du registre à décalage (310) afin de générer des signaux de balayage (s[2], s[4]) et des signaux de commande d'émission (e[1], e[2]) en vue de commander l'afficheur électroluminescent pour émettre une lumière, où le nombre de signaux de commande d'émission (e[1], e[2]) est la moitié du nombre des signaux de balayage (s[1], s[2], s[3], s[4]) ;

la transmission d'un premier signal de balayage (s[1]) à une première ligne de balayage (S1) couplée à une première rangée de pixels comprenant une pluralité de pixels (111) ;

35 la transmission d'un deuxième signal de balayage (s[2]) à une deuxième ligne de balayage (S2) adjacente à la première ligne de balayage (S1) et couplée à une seconde rangée de pixels comprenant une pluralité de pixels (112) ; et

40 la transmission d'un premier signal de commande d'émission (e[1]) à une première ligne de commande d'émission (E1) couplée aux pixels (111, 112) des première et deuxième lignes de balayage (S1, S2) pour permettre à la première rangée de pixels et à la seconde rangée de pixels d'émettre une lumière sensiblement au même moment en réponse au premier signal de commande d'émission (e[1]) transmis aux première et seconde rangées de pixels.

- 45 13. Procédé selon la revendication 12, dans lequel une luminosité de la lumière est modifiée pour représenter des gammes de gris différentes en fonction d'amplitudes de signaux de donnée respectivement fournis lorsque le signal de balayage et l'autre signal de balayage sont transmis.

- 50 14. Procédé selon la revendication 12, comprenant en outre :

la transmission du deuxième signal de balayage à la première rangée de pixels, et
 la transmission d'un troisième signal de balayage à la seconde rangée de pixels.

- 55 15. Procédé selon l'une quelconque des revendications 12 à 14, dans lequel le même signal de commande d'émission est transmis via des lignes de commande d'émission qui sont différentes les unes des autres.

16. Procédé selon l'une quelconque des revendications 12 à 14, dans lequel le même signal de commande d'émission est transmis via une ligne de commande d'émission.

FIG. 1
(PRIOR ART)

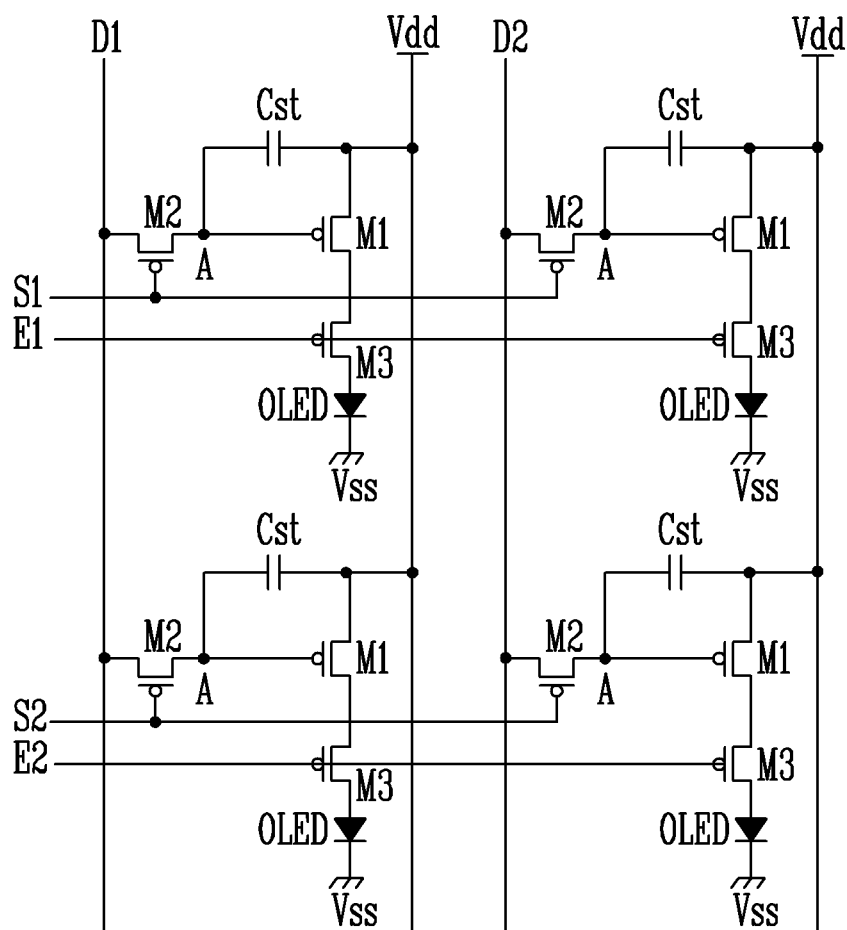


FIG. 2

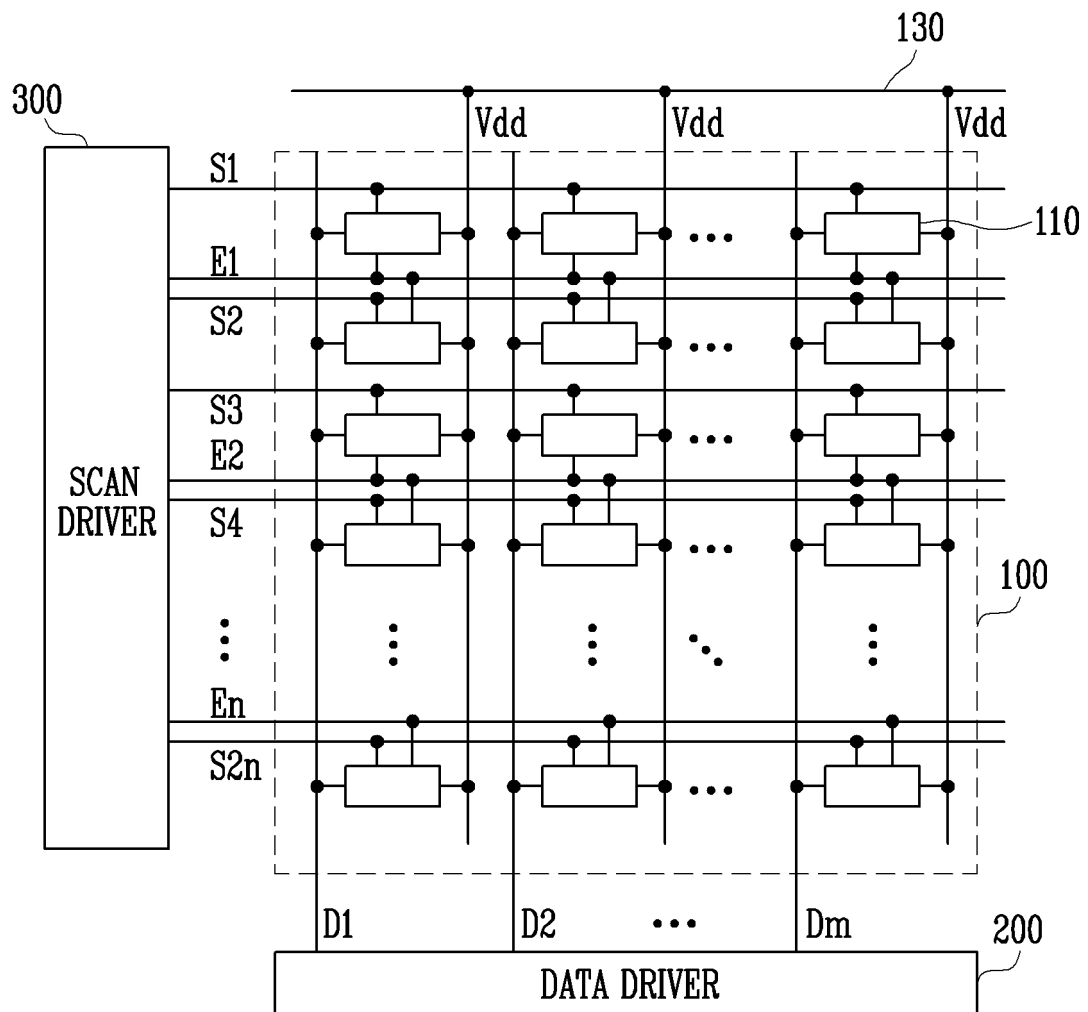


FIG. 3

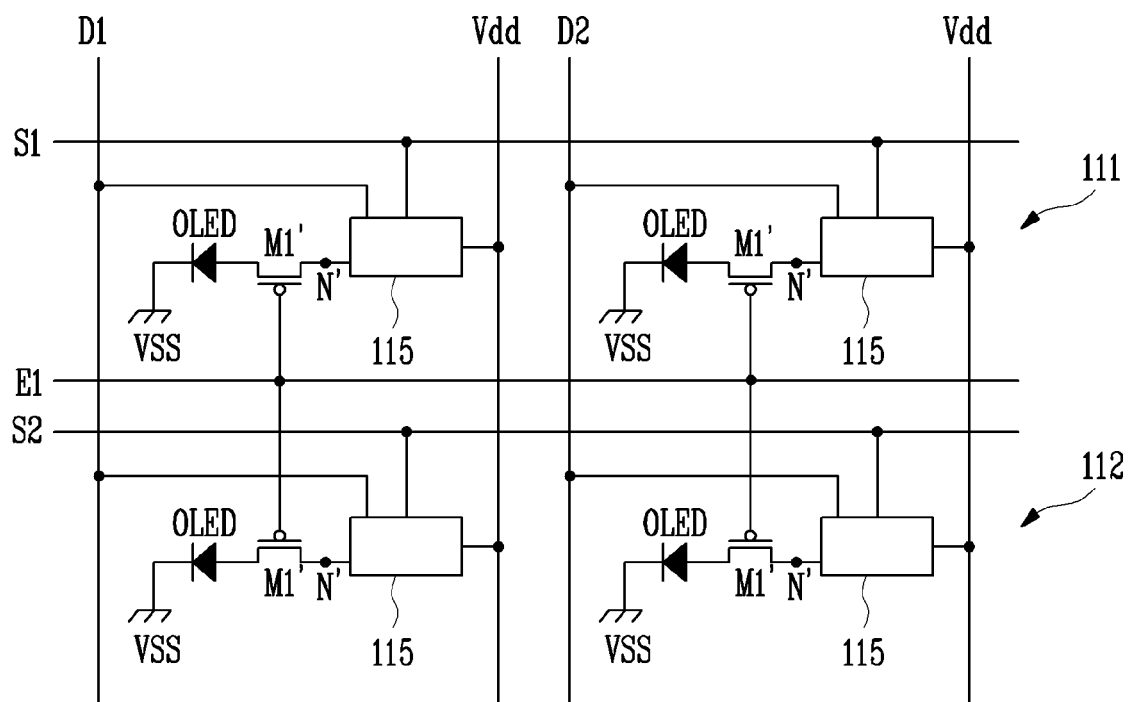


FIG. 4

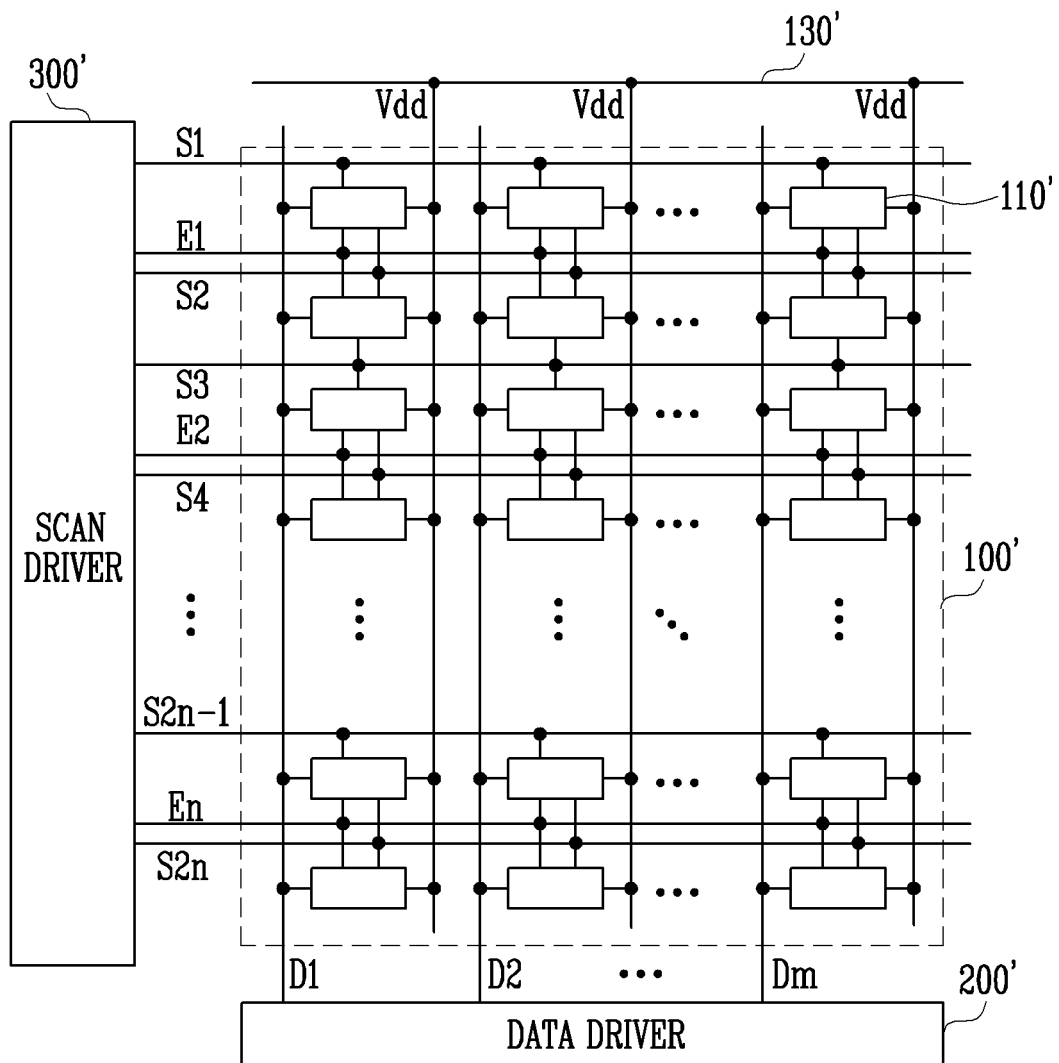


FIG. 5

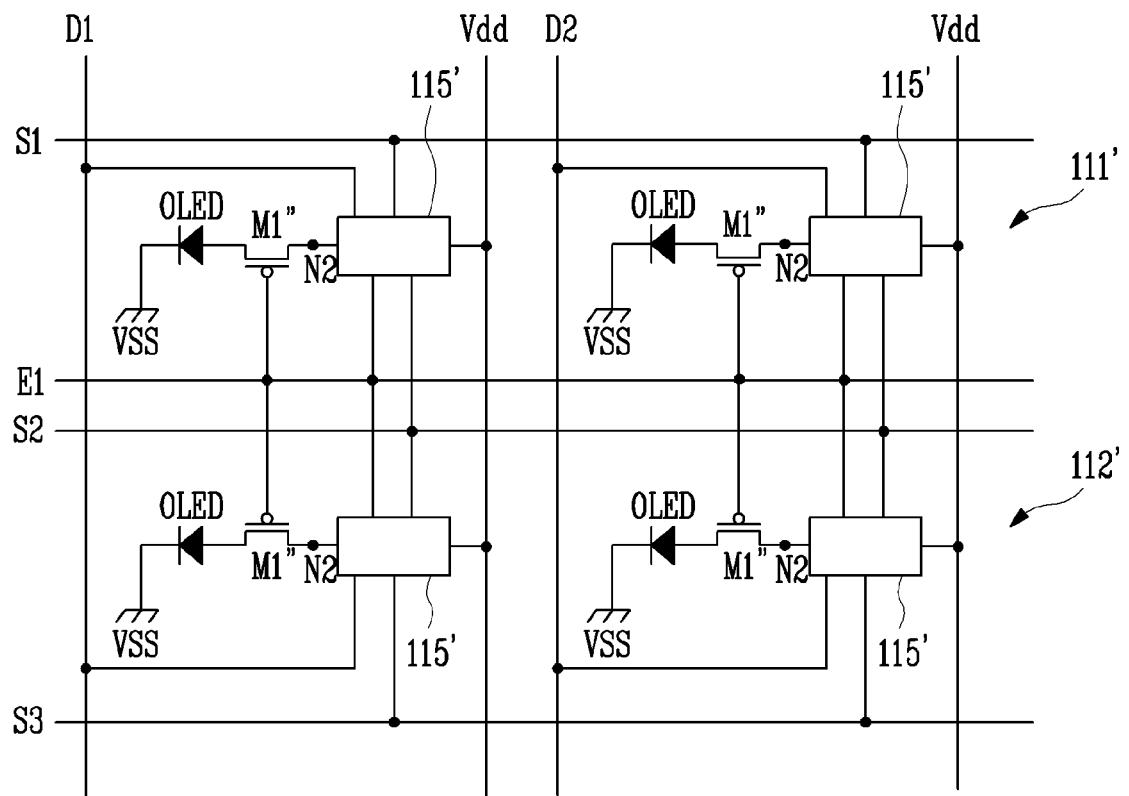


FIG. 6

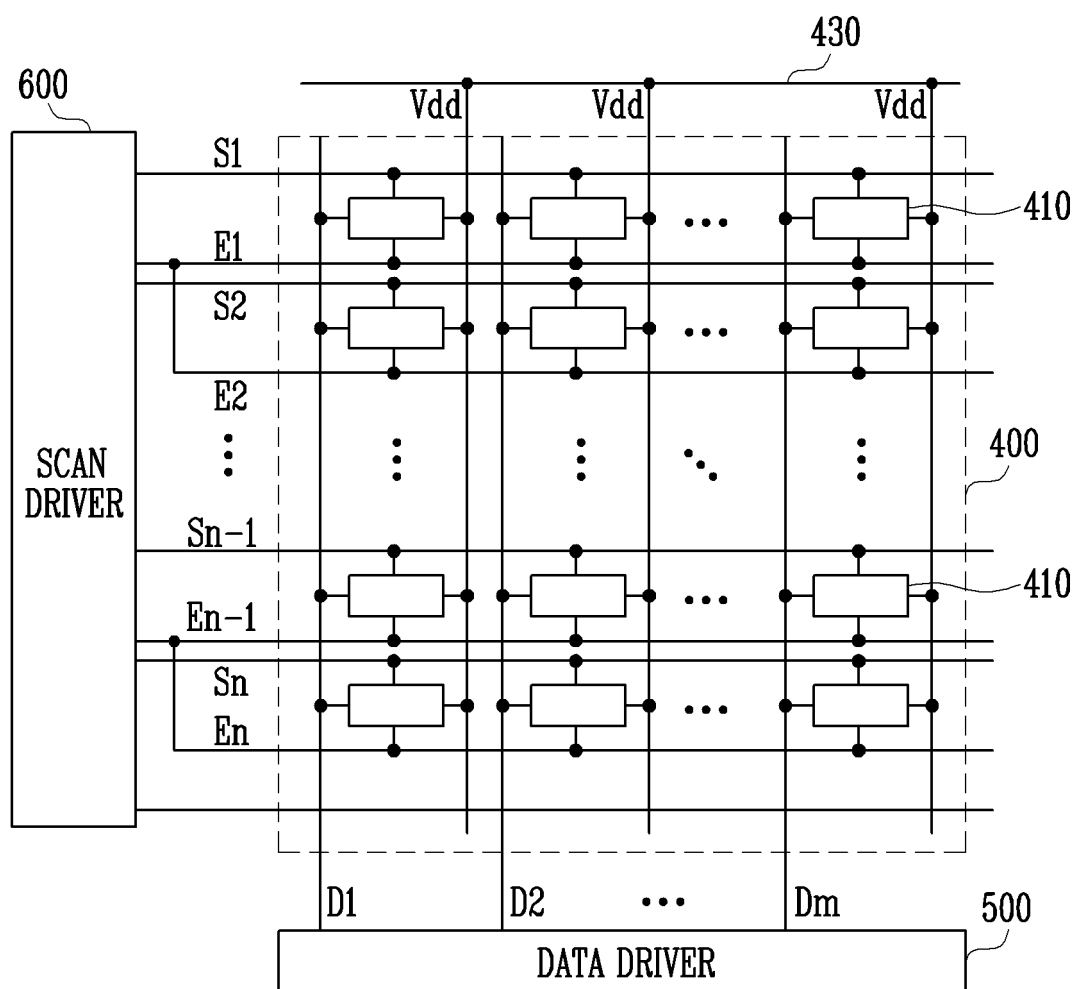


FIG. 7

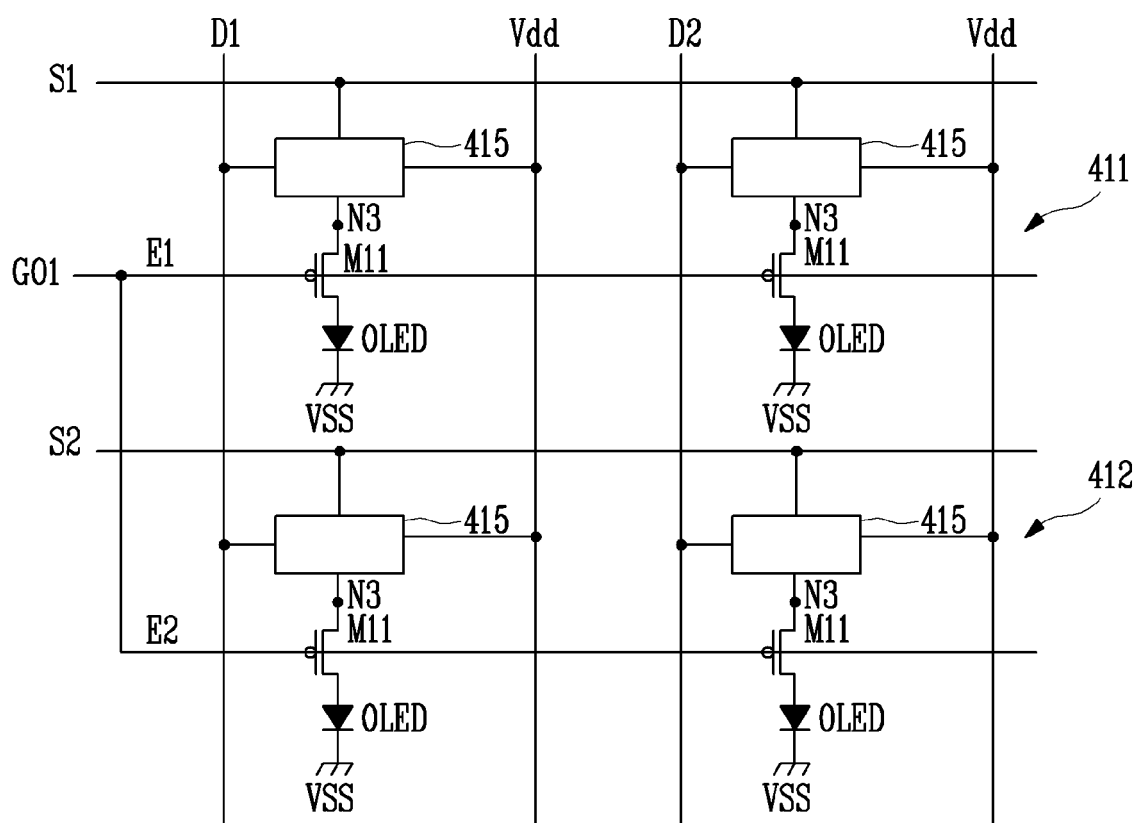


FIG. 8

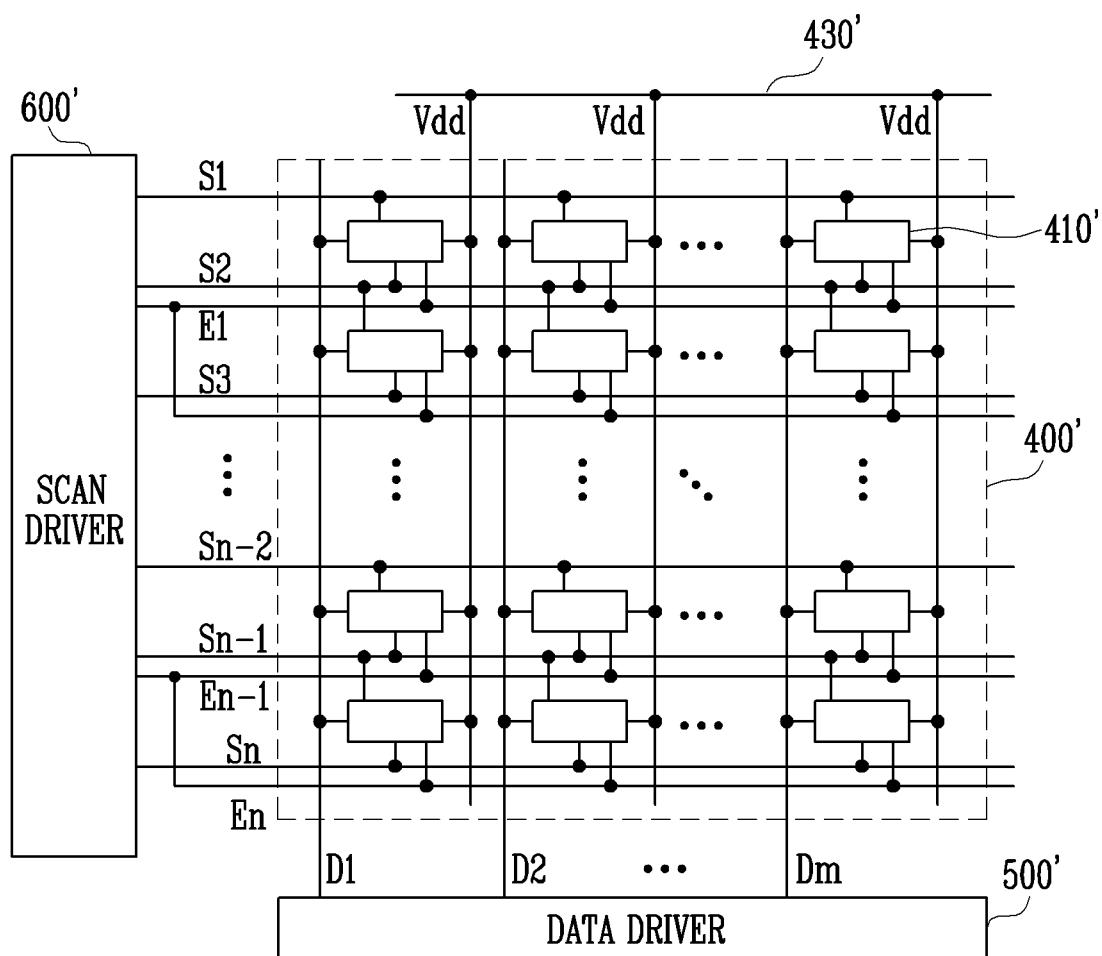


FIG. 9

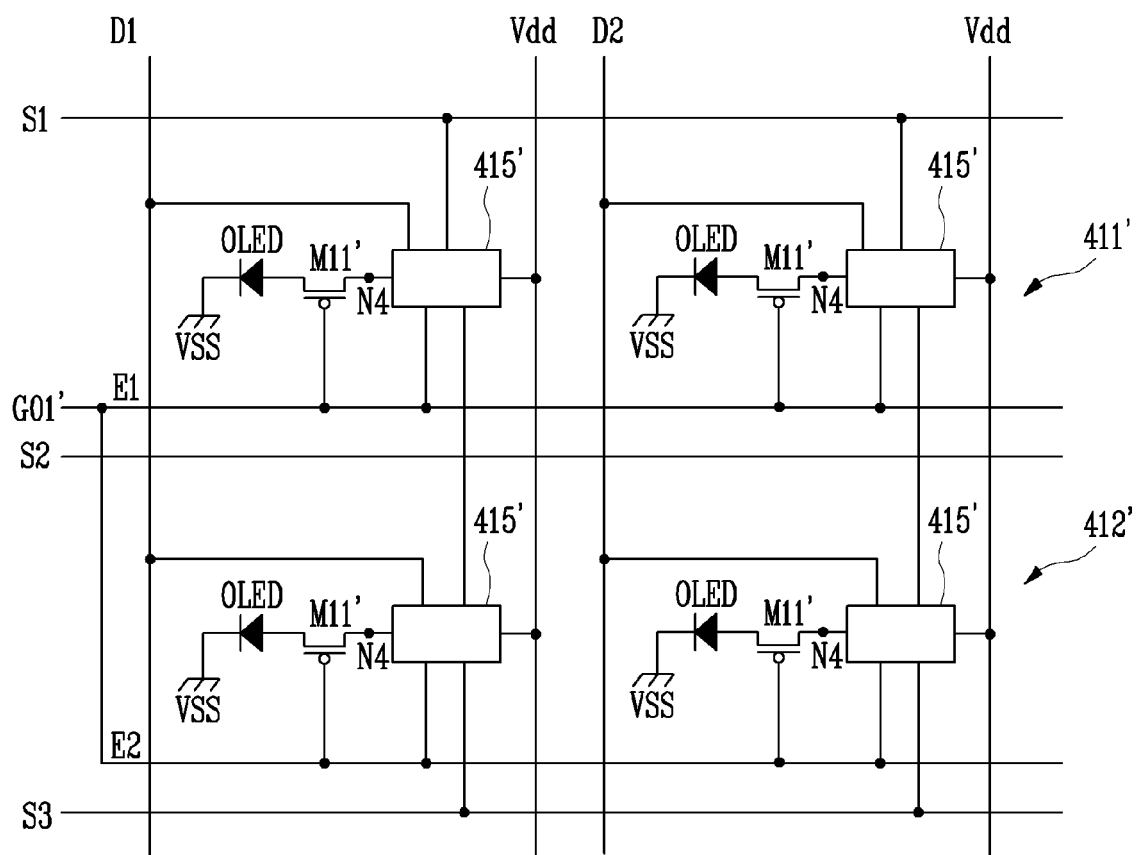


FIG. 10

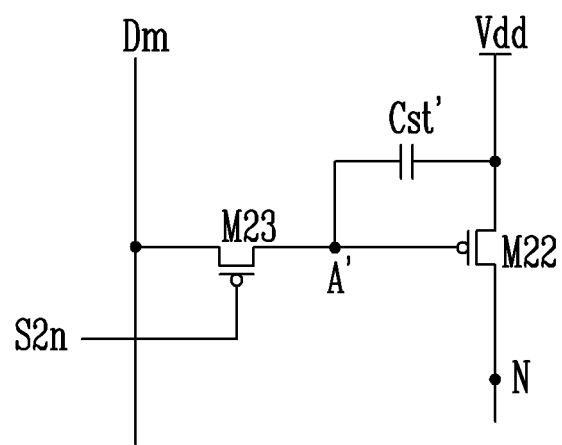


FIG. 11

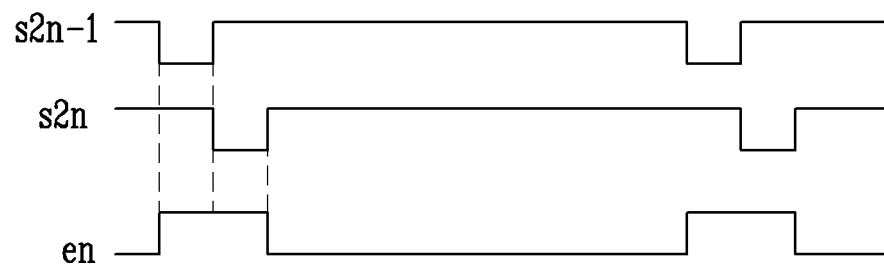


FIG. 12

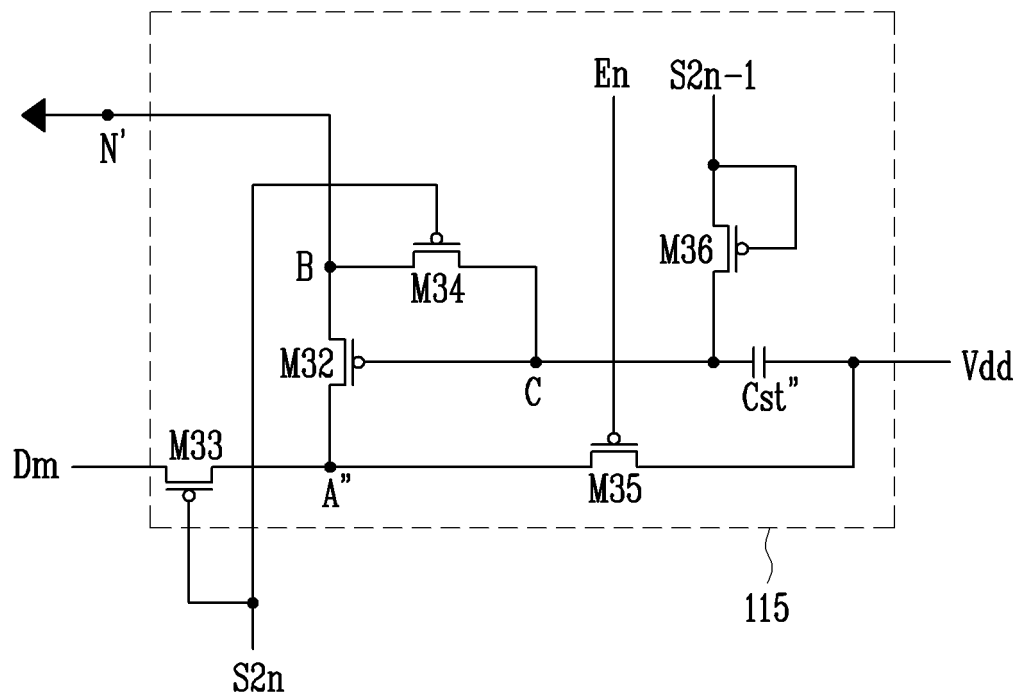


FIG. 13

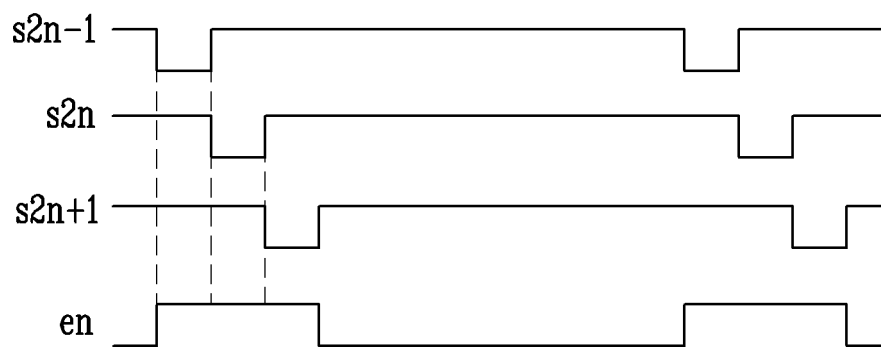


FIG. 14

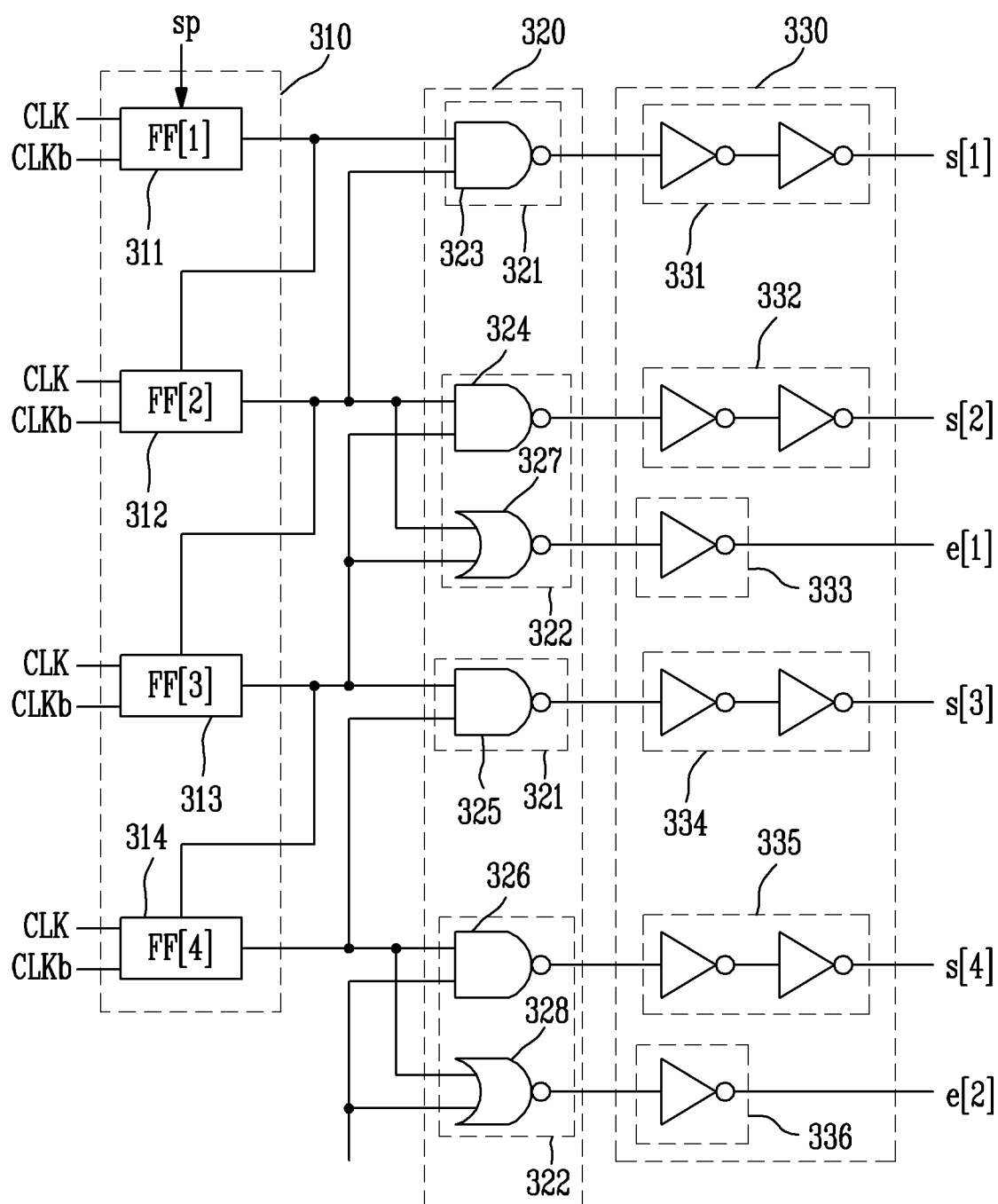
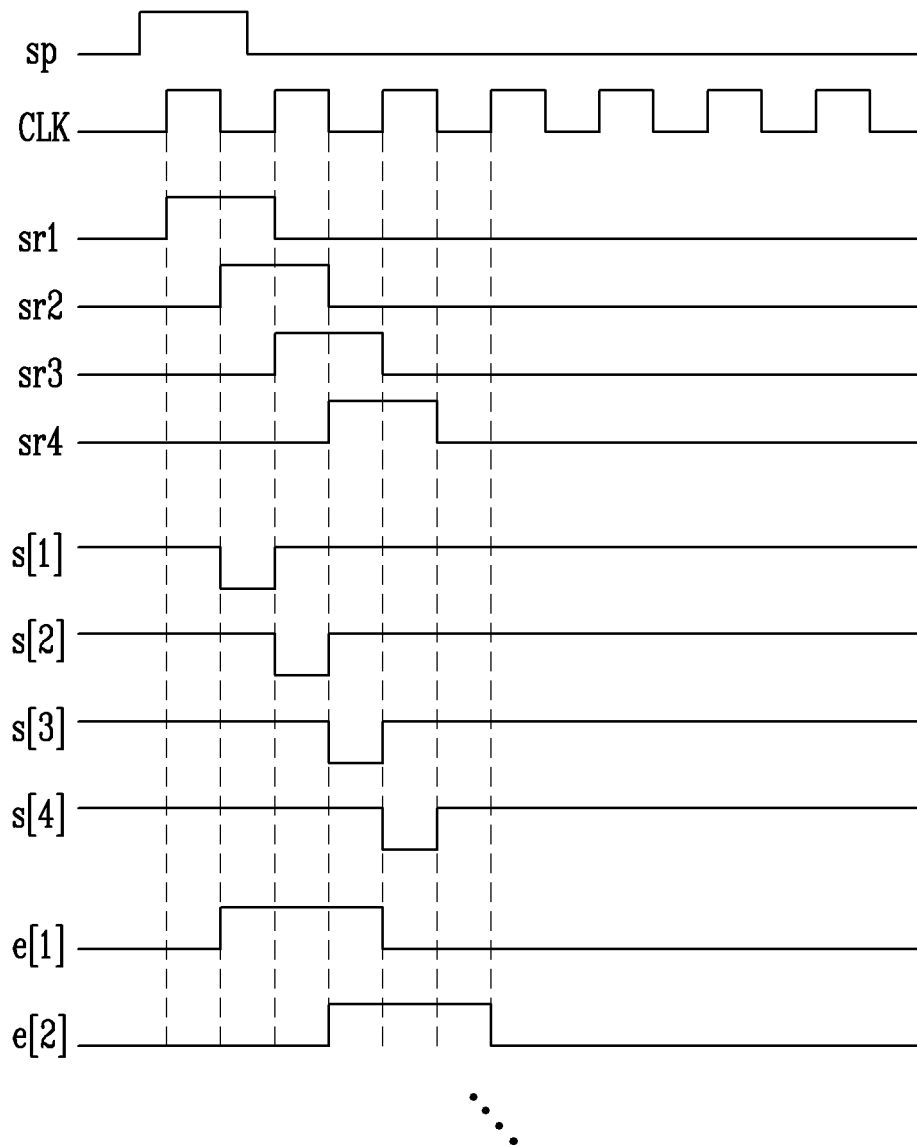


FIG. 15



REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- KR 1020040086915 [0001]
- EP 1424674 A1 [0013]
- US 2002196389 A1 [0015]
- JP 2004191574 A [0016]
- US 2003107560 A1 [0017]
- US 20030142509 A1 [0018]

Non-patent literature cited in the description

- **CHOI S M et al.** A SELF-COMPENSATED VOLT-AGE PROGRAMMING PIXEL STRUCTURE FOR ACTIVE-MATRIX ORGANIC LIGHT EMITTING DIODES. *10W. PROCEEDINGS OF THE INTERNATIONAL DISPLAY WORKSHOPS*, XX, XX, 2003, 535-538 [0014]

专利名称(译)	扫描驱动器，使用其的发光显示器及其驱动方法		
公开(公告)号	EP1653434B1	公开(公告)日	2019-01-30
申请号	EP2005109982	申请日	2005-10-26
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	EOM KI MYEONG OH CHOON YUL		
发明人	EOM, KI MYEONG OH, CHOON YUL		
IPC分类号	G09G3/3233 G09G3/3266		
CPC分类号	G09G3/3233 G09G3/3266 G09G2300/0465 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2320/043		
优先权	1020040086915 2004-10-28 KR		
其他公开文献	EP1653434A1		
外部链接	Espacenet		

摘要(译)

一种发光显示器，包括：多条扫描线，适于传输扫描信号;多条数据线，适于传输数据信号;多个发射控制线，适于发射发射控制信号;多个像素适于响应扫描信号，数据信号和发射控制信号发光。通过不同扫描线接收扫描信号的至少两个像素连接到一个发射控制线。利用这种配置，扫描驱动器和包括该扫描驱动器的发光显示器在像素部分中设置的布线数量减少，从而提高了孔径比，减少了发射控制信号的数量，减少了部件和布线的数量。扫描驱动器需要，简化制造工艺，并降低发光显示器的功耗。

[Equation 1]

$$I_{OLED} = \frac{\beta}{2} (V_{gs} - V_{th})^2 = \frac{\beta}{2} (V_{data} - V_{dd} - V_{th})^2$$