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(54) **Organic light emitting display with circuit measuring pad and method of fabricating the same**

Organische elektrolumineszierende Anzeigevorrichtung mit Schaltungsmesskontakt und Verfahren zur Herstellung.

Dispositif d'affichage organique électroluminescent avec un contact pour mesure du circuit et sa méthode de fabrication.

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Description

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 2004-70087, filed September 2, 2004, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to an organic light emitting display with a circuit measuring pad and method of fabricating the same and, more particularly, to an organic light emitting display with a circuit measuring pad which may prevent a short circuit between the circuit measuring pad and an opposite electrode and method of fabricating the same.

2. Description of the Related Art

[0003] Among flat panel displays, an organic light emitting display (OLED) has a fast response speed of 1ms or less, low power consumption, and a wide viewing angle due to an emissive display, and thus it has an advantage as a medium displaying a moving picture regardless of its size. Also, the OLED may be fabricated at low temperature and has a simplified manufacturing process since it employs the existing semiconductor manufacturing process technologies, and thus it attracts public attention as the next flat panel display.

[0004] The OLED is fabricated by forming a thin film transistor (TFT) array having a plurality of TFTs and capacitors on a substrate using a semiconductor manufacturing process, and depositing an organic layer having an emission layer on an emission region of the substrate on which the TFT array is formed.

[0005] In the OLED, a silicon semiconductor and metal electrodes are organically connected to each other through contact holes, and a pixel electrode which is patterned corresponding to each unit pixel is supplied with an electrical current for driving a light emitting element by the TFT connected thereto through a via hole.

[0006] Driving circuit measuring pads are arranged at the periphery of a display region in which the unit pixels of the OLED are formed. The driving circuit measuring pads are formed to check if circuit operation of the OLED is normally performed, during a manufacturing process.

[0007] However, the driving circuit measuring pad may cause a short circuit with an opposite electrode formed on the display region of the OLED, leading to failure of the OLED and low reliability of the OLED.

SUMMARY OF THE INVENTION

[0008] The present invention, therefore, solves aforementioned problems associated with conventional devices by providing a circuit measuring pad which may prevent a short circuit between the circuit measuring pad and an opposite electrode to thereby improve reliability of a display, an OLED with the circuit measuring pad, and method of fabricating the same.

[0009] The present invention also provides a method of improving a manufacturing process of the OLED by implementing the OLED having a thin pixel defining layer.

[0010] In an exemplary embodiment of the present invention, an organic light emitting display includes the technical features of claim 1.

[0011] In another exemplary embodiment according to the present invention, a method of fabricating an organic light emitting display includes the technical features of claim 10.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The above and other features of the present invention will be described in reference to certain exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a plan view of an OLED according to the present invention;

FIGS. 2 to 5 are cross-sectional views taken along the line I - I ' in FIG. 1, which illustrate a method of fabricating an OLED according to a first embodiment of the present invention; and

FIGS. 6 to 8 are cross-sectional views illustrating a method of fabricating an OLED according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

[0014] FIG. 1 is a plan view of an organic light emitting display (OLED) according to the present invention.

[0015] Referring to FIG. 1, the OLED includes a display region 5 having unit pixels and circuit portions 3a and 3b for driving the display region 5. The circuit portions 3a and 3b include a data driver region 3a and a scan driver region 3b. Each of the circuit portions 3a and 3b includes thin film transistors (TFTs) corresponding to the respective pixels, and is connected to the display region 5 via an interconnection line. Scan lines and data lines are arranged in the display region 5 to transfer signals from the data driver region 3a and the scan driver region 3b of the circuit portions 3a and 3b, and each signal is applied to a designated pixel to operate the OLED.

[0016] A circuit measuring pad 15 may be arranged on

a region 15a between an emission region and the data driver region 3a or on one side 15b of an edge of the OLED. The circuit measuring pad 15 is formed at the same time as the TFTs in the OLED. The circuit measuring pad 15 is connected to the data lines, and thus it is possible to determine if circuit operation is normally performed by checking electrical characteristics through the circuit measuring pad 15.

[0017] FIG. 5 is a cross-sectional view of an OLED according to a first embodiment of the present invention, taken along the line - ' in FIG. 1.

[0018] Referring to FIG. 5, a substrate 200 includes a display region A and a circuit measuring pad region B.

[0019] A buffer layer 205 is arranged on the display region A and the circuit measuring pad region B, and a TFT is arranged on the buffer layer 205 of the display region A. The TFT includes a semiconductor layer 210, a gate insulating layer 215, a gate electrode 220, an inter insulating layer 220, and source and drain electrodes 230a and 230b.

[0020] Insulating layers which are deposited at the same time as the gate insulating layer 215 and the interlayer insulating layer 225 are arranged on the buffer layer 205 of the circuit measuring pad region B.

[0021] A first conductive layer 230c is arranged on the interlayer insulating layer 225 of the circuit measuring pad region B.

[0022] A first insulating layer is arranged on the source and drain electrodes 230a and 230b and the first conductive layer 230c. The first insulating layer may be a passivation layer 235. The first insulating layer may further include a planarization layer 240.

[0023] A first via hole 245a which exposes the source electrode 230a or the drain electrode 230b and a second via hole 245b which exposes the conductive layer 230c are arranged in the first insulating layer. A pixel electrode 250a which is in contact with the source electrode 230a or drain electrode 230b through the first via hole 245a and a second conductive layer 250b which is in contact with the first conductive layer 230c through the second via hole 245b are arranged.

[0024] A taper angle $\theta 1$ of the second via hole 245b may be 50° or less.

[0025] Thickness of the second conductive layer 250b may be in a range of 100 to 1,000 Å.

[0026] A taper angle $\theta 2$ of an edge of the second conductive layer 250b may be 50° or less.

[0027] A pixel defining layer 260a which exposes the pixel electrode 250a is arranged, an organic layer 270 having an emission layer is arranged on the exposed pixel electrode 260b. A pixel defining layer 260b is also arranged on the second conductive layer 250b. The pixel defining layers 260a and 26b are formed of thin layers and preferably have a thickness of 3,000 Å or less.

[0028] An opposite electrode 280 is arranged on the pixel defining layers 260a and 260b.

[0029] Even though the pixel defining layers 260a and 260b are formed of thin layers, since the taper angles $\theta 1$ and $\theta 2$ are 50° or less, an insulating layer may be formed to a uniform thickness even on a tapered portion, thereby preventing a short circuit between the circuit measuring pad and the opposite electrode.

[0030] Therefore, the OLED having the thin pixel defining layer may be implemented, and such a structure may improve characteristics of a laser induced thermal imaging process of the OLED.

[0031] Also, reliability of the OLED may be improved by preventing the short circuit.

[0032] FIGS. 2 to 5 are cross-sectional views illustrating a method of fabricating an OLED according to the present invention.

[0033] Referring to FIG. 2, a buffer layer 205 is formed on a substrate 200 having a display region A and a circuit measuring pad region B. Forming the buffer layer 205 is not necessary, but since it serves to prevent impurities from being come into a TFT element from the substrate 200, it is preferable that the buffer layer 205 is formed. The buffer layer 205 may be formed of silicon nitride (SiNx), silicon oxide (SiO_2) or silicon oxynitride (SiO_xN_y).

[0034] A semiconductor layer 210 is formed on a portion of the buffer layer 205 corresponding to the display region A. The semiconductor layer 210 may be formed of amorphous silicon or crystalline silicon.

[0035] A gate insulating layer 215 is formed over the substrate 200 having the semiconductor layer 210. The gate insulating layer 215 is formed of a typical insulating layer such as a silicon oxide (SiO_2) layer. A gate electrode 220 is formed over the substrate 200 having the gate insulating layer 215.

[0036] Referring to FIG. 3, an inter insulating layer 225 is formed over the substrate 200 having the gate electrode 220. Contact holes are formed in the inter insulating layer 225 to expose source and drain regions of the semiconductor layer 210, respectively. A conductive layer is deposited and patterned on the interlayer insulating layer 225 to form source and drain electrodes 230a and 230b which are in contact with the exposed source and drain regions respectively while forming a first conductive layer 230c above the circuit measuring pad region B.

[0037] A first insulating layer is formed over the substrate 200 having the source and drain electrodes 230a and 230b and the first conductive layer 230c.

[0038] The first insulating layer may be a passivation layer 235. The passivation layer 235 may be formed of a silicon nitride (SiNx) layer or silicon oxide (SiO_2) layer. The passivation layer 235 is preferably formed of a silicon nitride (SiNx) layer for passivation effect and light blocking effect of the semiconductor layer 210.

[0039] A planarization layer 240 may be formed on the passivation layer 235. The planarization layer 240 may be formed of a material selected from a group consisting of polyacrylates resin, epoxy resin, phenolic resin, polyamides resin, polyimides resin, unsaturated polyesters resin, polyphenylenethers resin, polyphenylenesulfides resin, and benzocyclobutene (BCB).

[0040] Referring to FIG. 4, first and second via holes

245a and 245b are formed in the first insulating layer to expose the drain electrode 230b and the first conductive layer 230c.

[0041] A taper angle θ1 of the first or second via hole may be 50° or less.

[0042] A conductive layer is deposited and patterned over the substrate 200 having the first and second via holes 245a and 245b to form a pixel electrode 250a and a second conductive layer 250b on the first and second via holes 245a and 245b, respectively.

[0043] The electrical characteristics of the circuit measuring pad region B on which the second conductive layer 250b is formed is checked to see if circuit operation is normally performed.

[0044] A reflecting layer may be interposed between the pixel electrode 250a and the planarization layer 240.

[0045] The pixel electrode 250a and the second conductive layer 250b may be formed of indium tin oxide (ITO) or indium zinc oxide (IZO). A taper angle θ2 of an edge of the second conductive layer 250b may be 50° or less.

[0046] An insulating layer is formed on the pixel electrode 250a and the second conductive layer 250b. The insulating layer is patterned to form pixel defining layers 260a and 260b. The pixel defining layer 260a exposes the pixel electrode 260a, and the pixel defining layer 260b covers and protects the second conductive layer 250b.

[0047] Due to the taper angles θ1 and θ2, the pixel defining layer 260b formed above the circuit measuring pad region B may be conformally formed without being broken.

[0048] Referring to FIG. 5, an organic layer 270 is formed on the exposed pixel electrode 250a. The organic layer 270 includes at least one selected from a group consisting of a hole injection layer, a hole transport layer, a hole blocking layer, and an electron injection layer in addition to an emission layer.

[0049] An opposite electrode 280 is formed on the organic layer 270 of the display region A and the pixel defining layer 260b of the circuit measuring pad region B, thereby completing the OLED.

[0050] Therefore, the pixel defining layer 260b is conformally formed without being broken and thus prevents a short circuit between the circuit measuring pad 260b and the opposite electrode 280.

[0051] As a result, the OLED having a thin pixel defining layer may be implemented, and a laser induced thermal imaging process of the OLED to which the thin pixel defining layer should be subjected may be easily performed.

[0052] Also, since a short circuit is prevented, reliability of the OLED may be improved.

[0053] FIG. 6 is a cross-sectional view of an OLED according to a second embodiment of the present invention.

[0054] Referring to FIG. 6, like the first embodiment of the present invention, a substrate 300 includes a display region A on which source and drain electrodes 330a and 330b are arranged and a circuit measuring pad region B on which a first conductive layer 330c is arranged.

[0055] A first insulating layer is arranged on the source and drain electrodes 330a and 330b and the first conductive layer 330c. The first insulating layer may be a passivation layer 335. In the second embodiment of the present invention, a planarization layer 340 is formed above only the display region A except the circuit measuring pad region B.

[0056] A taper angle θ1 of a second via hole may be 50° or less.

[0057] Thickness of a second conductive layer 350b may be in a range of 100 to 1,000 Å.

[0058] A taper angle θ2 of an edge of the second conductive layer 350b may be 50° or less.

[0059] A second insulating layer 360b arranged to cover the second conductive layer 350b may be formed of a thin layer having a thickness of 3,000 Å or less.

[0060] Therefore, like the first embodiment of the present invention, even though a pixel defining layer 360b is a thin layer, since a taper angle θ1 of the via hole and a taper angle θ2 of an edge of the second conductive layer 350b are 50° or less, the pixel defining layer 360b may be formed to a uniform thickness even at a tapered portion, thereby preventing a short circuit between the circuit measuring pad B and an opposite electrode 380.

[0061] As a result, the OLED having a thin pixel defining layer may be implemented, and a laser induced thermal imaging process of the OLED to which the thin pixel defining layer should be subjected may be easily performed. Also, since a short circuit is prevented, reliability of the OLED may be improved.

[0062] FIGS. 6 to 8 are cross-sectional views illustrating a method of fabricating an OLED according to a second embodiment of the present invention.

[0063] Referring to FIG. 7, like the first embodiment, a buffer layer 305 is formed on a substrate 300 having a display region A and a circuit measuring pad region B. A semiconductor layer 310, a gate electrode 320, and source and drain electrodes 330a and 330b are formed on a portion of the buffer layer 305 above the display region A, thereby forming a TFT.

[0064] Like the first embodiment, a first conductive layer 330c is formed at the same time as the source and drain electrodes 330a and 330b, above the circuit measuring pad region B. Then, a first insulating layer is formed over the substrate having the source and drain electrodes 330a and 330b and the first conductive layer 330c. The first insulating layer may be a passivation layer 335.

[0065] A planarization layer 340 may be formed on the passivation layer 335.

[0066] The planarization layer 340 is subjected to an exposure process using a halftone mask 400 which has portions 400a to 400c different in exposure level based on via holes of the display region and the circuit measuring pad region, and portions of the display regions and the circuit measuring pad region around the via holes.

[0067] Referring to FIG. 8, by the exposure process, a

first via hole which exposes the drain electrode 330b and a second via hole which exposes the first conductive layer 330c are formed while forming an opening which exposes the circuit measuring pad region in the planarization layer 340. That is, using the halftone mask 400, a portion of the planarization layer 340 corresponding to the display region A remains, and a portion of the planarization layer 340 corresponding to the circuit measuring pad region B is removed.

[0068] A taper angle θ1 of the first or second via hole may be 50° or less.

[0069] A conductive layer is deposited over the substrate having the first and second via hole and then patterned to form a pixel electrode 350a on the first via hole and a second conductive layer 350b on the second via hole.

[0070] The electrical characteristics of the circuit measuring pad portion B on which the second conductive layer 350b is formed are check to see if circuit operation is normally performed.

[0071] Like the first embodiment of the present invention, a reflecting layer may be interposed between the pixel electrode 350a and the planarization layer 340.

[0072] Also, the pixel electrode 350a and the second conductive layer 350b may be formed of ITO or IZO, and a taper angle of an edge of the second conductive layer 350b may be 50° or less.

[0073] Referring to FIG. 6, an insulating layer is formed on the pixel electrode 350a and the conductive layer 350b. The insulating layer is patterned to form pixel defining layers 360a and 360b. The pixel defining layer 360a exposes the pixel electrode 350a, and the pixel defining layer 360b covers and protects the second conductive layer 350b.

[0074] Due to the taper angles θ1 and θ2, the pixel defining layer 360b formed above the circuit measuring pad region B may be conformably formed without being broken.

[0075] An organic layer 370 is formed on the exposed pixel electrode 350a. The organic layer 370 includes at least one selected from a group consisting of a hole injection layer, a hole transport layer, a hole blocking layer, and an electron injection layer in addition to an emission layer.

[0076] An opposite electrode 380 is formed on the organic layer 370 of the display region A and the pixel defining layer 360b of the circuit measuring pad region B, thereby completing the OLED.

[0077] Therefore, the pixel defining layer 360b is conformally formed without being broken and thus prevents a short circuit between the circuit measuring pad 360b and the opposite electrode 380.

[0078] As a result, the OLED having a thin pixel defining layer may be implemented, and a laser induced thermal imaging process of the OLED to which the thin pixel defining layer should be subjected may be easily performed.

[0079] Also, since a short circuit is prevented, reliability of the OLED may be improved.

[0080] As described above, the OLED of the present invention may prevent a short circuit between the circuit measuring pad and the opposite electrode even at the tapered portion of the circuit measuring pad due to its uniform thickness. The OLED having a thin pixel defining layer may be implemented, and characteristics of the laser induced thermal imaging process of the OLED may be improved. Also, since a short circuit is prevented, reliability of the OLED may be improved.

[0081] Although the present invention has been described with reference to certain exemplary embodiments thereof, it will be understood by those skilled in the art that a variety of modifications and variations may be made to the present invention without departing from the spirit or scope of the present invention defined in the appended claims, and their equivalents.

Claims

1. An organic light emitting display comprising:

a substrate (200) having a display region (A) and a circuit measuring pad region (B) comprising;
a circuit measuring pad (15), wherein the circuit measuring pad (15) is arranged on a region (15a) between an emission region of the organic light emitting display and a data driver region (3a) or wherein the circuit measuring pad (15) is arranged on one side (15b) of an edge of the organic light emitting display; a first conductive layer (230c) arranged above the circuit measuring pad region (B) and source and drain electrodes (230a, 230b) arranged above the display region (A) on the same layer as the first conductive layer (230c);
a first insulating layer (235) arranged on the source and drain electrodes (230a, 230b) and the first conductive layer (230c);
first and second via holes (245a, 245b) formed in the first insulating layer (235), the first via hole (245a) exposing the source electrode (230a) or the drain electrode (230b), the second via hole (245b) exposing the first conductive layer (230c);
a pixel electrode (250a) contacting the source electrode (230a) or the drain electrode (230b) through the first via hole (245a), and a second conductive layer (250b) contacting the first conductive layer (230c) through the second via hole (245b); and
a pixel defining insulating layer (260a) which exposes the pixel electrode (250a) and formed on the second conductive layer (250b).

2. The display of claim 1, wherein the second conductive layer (250b) has a thickness in a range of 100

to 1,000 Å.

3. The display of claim 1, wherein the pixel defining layer (260a) has a thickness of 3,000 Å or less.

4. The display of claim 1, wherein the second via hole (245b) has a taper angle of 50° or less.

5. The display of claim 1, wherein an edge of the first conducive layer (230c) has a taper angle of 50° or less.

6. The display of claim 1, wherein the first insulating layer (235) is a passivation layer.

7. The display of claim 6, wherein the first insulating layer (235) further includes a planarization layer (240) arranged on the passivation layer (235).

8. The display of claim 7, wherein the second via hole (245b) has a taper angle of 50° or less.

9. The display of claim 7, wherein the planarization layer (240) includes an opening which exposes the circuit measuring pad region (B), and the second via hole (245b) is arranged in the passivation layer (235).

10. A method of fabricating an organic light emitting display, comprising:

preparing a substrate (200) having a display region (A) and a circuit measuring pad region (B), wherein a circuit measuring pad (15) is arranged on a region (15a) between an emission region of the organic light emitting display and a data driver region (3a) or wherein the circuit measuring pad (15) is arranged on one side (15b) of an edge of the organic light emitting display;
depositing and patterning a conductive layer on the substrate to form a first conductive layer (230c) above the circuit measuring pad region (B) while forming source and drain electrodes (230a, 230b) above the display region (A);
forming a first insulating layer (235) on the source and drain electrodes (230a, 230b) and the first conductive layer (230c);
simultaneously forming first and second via holes (245a, 245b) in the first insulating layer (235), the first via hole (245a) exposing the source electrode (230a) or the drain electrode (230b), the second via hole (245b) exposing the first conductive layer (230c);
depositing and patterning a conductive layer to form a pixel electrode (250a) contacting the source electrode (230a) or the drain electrode (230b) through the first via hole (245a), and a second conductive layer (250b) contacting the first conductive layer (230c) through the second via hole (245b); and
depositing and patterning a second insulating layer to form a pixel defining layer (260a) which exposes the pixel electrode (250a) above the display region (A) and covers the second conductive layer (250b) above the circuit measuring pad region (B).

11. The method of claim 10, wherein forming the first insulating layer (235) includes forming a passivation layer.

12. The method of claim 11, wherein forming the first insulating layer (235) further includes forming a planarization layer (240) on the passivation layer (235).

13. The method of claim 12, wherein the second via hole (245b) has a taper angle of 50° or less.

14. The method of claim 12, wherein while the first and second via holes (245a, 245b) are formed using a halftone mask, an opening which exposes the circuit measuring pad region (B) is formed in the planarization layer (240).

15. The method of claim 10, further comprising forming an organic layer having an emission layer on the exposed pixel electrode (250a), and forming an opposite electrode (280) above the display region (A) having the organic layer and above the circuit measuring pad region (B) having the second insulating layer.

16. The method of claim 10, wherein the second conductive layer (250b) has a thickness in a range of 100 to 1,000 Å.

17. The method of claim 10, wherein the pixel defining layer (260a) has a thickness of 3,000 Å or less.

18. The method of claim 10, wherein the first via hole (245a) has a taper angle of 50° or less.

19. The method of claim 10, wherein an edge of the first conductive layer (230c) has a taper angle of 50° or less.

Patentansprüche

1. Organische elektrolumineszierende Anzeigevorrichtung, aufweisend:

ein Substrat (200), das einen Anzeigebereich (A) und einen Schaltungsmesskontaktbereich (B) aufweist, der einen Schaltungsmesskontakt

(15) aufweist, wobei der Schaltungsmesskontakt (15) in einem Bereich (15a) zwischen einem Emissionsbereich der organischen elektrolumineszierenden Anzeigevorrichtung und einem Datentreiberbereich (3a) angeordnet ist oder wobei der Schaltungsmesskontakt (15) auf einer Seite (15b) eines Randes der organischen elektrolumineszierenden Anzeigevorrichtung angeordnet ist;
eine erste leitende Schicht (230c), die über dem Schaltungsmesskontaktbereich (B) angeordnet ist, und eine Source- und eine Drain-Elektrode (230a, 230b), die über dem Anzeigebereich (A) auf derselben Schicht wie die erste leitende Schicht (230c) angeordnet sind;
eine erste Isolierschicht (235), die auf der Source- und der Drain-Elektrode (230a, 230b) und der ersten leitenden Schicht (230c) angeordnet ist;
ein erstes und zweites Durchgangsloch (245a, 245b), die in der ersten Isolierschicht (235) ausgebildet sind, wobei das erste Durchgangsloch (245a) die Source-Elektrode (230a) oder die Drain-Elektrode (230b) freilegt, wobei das zweite Durchgangsloch (245b) die erste leitende Schicht (230c) freilegt;
eine Pixelelektrode (250a), die mit der Source-Elektrode (230a) oder der Drain-Elektrode (230b) durch das erste Durchgangsloch (245a) in Kontakt steht, und eine zweite leitende Schicht (250b), die mit der ersten leitenden Schicht (230c) durch das zweite Durchgangsloch (245) in Kontakt steht; und
eine Pixeldefinitions-Isolierschicht (260a), die die Pixelelektrode (250a) freilegt und auf der zweiten leitenden Schicht (250b) ausgebildet ist.

2. Anzeigevorrichtung nach Anspruch 1, wobei die zweite leitende Schicht (250b) eine Dicke in einem Bereich von 100 bis 1000 Å aufweist.

3. Anzeigevorrichtung nach Anspruch 1, wobei die Pixeldefinitionsschicht (260a) eine Dicke von 3000 Å oder weniger aufweist.

4. Anzeigevorrichtung nach Anspruch 1, wobei das zweite Durchgangsloch (245b) einen Kegelwinkel von 50° oder weniger aufweist.

5. Anzeigevorrichtung nach Anspruch 1, wobei ein Rand der ersten leitenden Schicht (230c) einen Kegelwinkel von 50° oder weniger aufweist.

6. Anzeigevorrichtung nach Anspruch 1, wobei die erste Isolierschicht (235) eine Passivierungsschicht ist.

7. Anzeigevorrichtung nach Anspruch 6, wobei die erste Isolierschicht (235) weiterhin eine Planarisierungsschicht (240) aufweist, die auf der Passivierungsschicht (235) angeordnet ist.

8. Anzeigevorrichtung nach Anspruch 7, wobei das zweite Durchgangsloch (245b) einen Kegelwinkel von 50° oder weniger aufweist.

9. Anzeigevorrichtung nach Anspruch 7, wobei die Planarisierungsschicht (240) eine Öffnung aufweist, die den Schaltungsmesskontaktbereich (B) freilegt, und das zweite Durchgangsloch (245b) in der Passivierungsschicht (235) angeordnet ist.

10. Verfahren zur Herstellung einer organischen elektrolumineszierenden Anzeigevorrichtung, aufweisend:

Herstellen eines Substrats (200), das einen Anzeigebereich (A) und einen Schaltungsmesskontaktbereich (B) aufweist, wobei ein Schaltungsmesskontakt (15) in einem Bereich (15a) zwischen einem Emissionsbereich der organischen elektrolumineszierenden Anzeigevorrichtung und einem Datentreiberbereich (3a) angeordnet ist oder wobei der Schaltungsmesskontakt (15) auf einer Seite (15b) eines Randes der organischen elektrolumineszierenden Anzeigevorrichtung angeordnet ist;
Abscheiden und Strukturieren einer leitenden Schicht auf dem Substrat, um eine erste leitende Schicht (230c) über dem Schaltungsmesskontaktbereich (B) auszubilden, während eine Source- und eine Drain-Elektrode (230a, 230b) über dem Anzeigebereich (A) ausgebildet wird;
Ausbilden einer ersten Isolierschicht (235) auf der Source- und der Drain-Elektrode (230a, 230b) und der ersten leitenden Schicht (230c);
gleichzeitiges Ausbilden eines ersten und zweiten Durchgangslochs (245a, 245b) in der ersten Isolierschicht (235), wobei das erste Durchgangsloch (245a) die Source-Elektrode (230a) oder die Drain-Elektrode (230b) freilegt, wobei das zweite Durchgangsloch (245b) die erste leitende Schicht (230c) freilegt;
Abscheiden und Strukturieren einer leitenden Schicht, um eine Pixelelektrode (250a), die mit der Source-Elektrode (230a) oder der Drain-Elektrode (230b) durch das erste Durchgangsloch (245a) in Kontakt steht, und eine zweite leitende Schicht (250b), die mit der ersten leitenden Schicht (230c) durch das zweite Durchgangsloch (245b) in Kontakt steht, auszubilden; und
Abscheiden und Strukturieren einer zweiten Isolierschicht, um eine Pixeldefinitionsschicht (260a) auszubilden, die die Pixelelektrode (250a) über dem Anzeigebereich (B) freilegt und

die zweite leitende Schicht (250b) über dem Schaltungsmesskontaktbereich (B) bedeckt.

11. Verfahren nach Anspruch 10, wobei das Ausbilden der ersten Isolierschicht (235) das Ausbilden einer Passivierungsschicht aufweist.

12. Verfahren nach Anspruch 11, wobei das Ausbilden der ersten Isolierschicht (235) weiterhin das Ausbilden einer Planarisierungsschicht (240) auf der Passivierungsschicht (235) aufweist.

13. Verfahren nach Anspruch 12, wobei das zweite Durchgangsloch (245b) einen Kegelwinkel von 50° oder weniger aufweist.

14. Verfahren nach Anspruch 12, wobei, während das erste und zweite Durchgangsloch (245a, 245b) unter Verwendung einer Halbtonmaske ausgebildet werden, eine Öffnung, die den Schaltungsmesskontaktbereich (B) freilegt, in der Planarisierungsschicht (240) ausgebildet wird.

15. Verfahren nach Anspruch 10, weiterhin aufweisend das Ausbilden einer organischen Schicht, die eine Emissionsschicht aufweist, auf der freiliegenden Pixelelektrode (250a), und das Ausbilden einer Gegenelektrode (280) über dem Anzeigebereich (A), der die organische Schicht aufweist, und über dem Schaltungsmesskontaktbereich (B), der die zweite Isolierschicht aufweist.

16. Verfahren nach Anspruch 10, wobei die zweite leitende Schicht (250b) eine Dicke in einem Bereich von 100 bis 1000 Å aufweist.

17. Verfahren nach Anspruch 10, wobei die Pixeldefinitionsschicht (260a) eine Dicke von 3000 Å oder weniger aufweist.

18. Verfahren nach Anspruch 10, wobei das erste Durchgangsloch (245a) einen Kegelwinkel von 50° oder weniger aufweist.

19. Verfahren nach Anspruch 10, wobei ein Rand der ersten leitenden Schicht (230c) einen Kegelwinkel von 50° oder weniger aufweist.

Revendications

1. Afficheur électroluminescent organique comprenant :

un substrat (200) comportant une région d'affichage (A) et une région de bornier de mesure de circuit (B) comprenant : un bornier de mesure de circuit (15), dans lequel le bornier de mesure de circuit (15) est agencé sur une région (15a) située entre une région d'émission de l'afficheur électroluminescent organique et une région de circuit d'attaque de données (3a) ou dans lequel le bornier de mesure de circuit (15) est agencé d'un côté (15b) d'un bord de l'afficheur électroluminescent organique ;
une première couche conductrice (230c) agencée audessus de la région de bornier de mesure de circuit (B) et des électrodes de source et de drain (230a, 230b) agencées au-dessus de la région d'affichage (A) sur la même couche que la première couche conductrice (230c) ;
une première couche isolante (235) agencée sur les électrodes de source et de drain (230a, 230b) et la première couche conductrice (230c) ;
des premier et second trous traversants (245a, 245b) formés dans la première couche isolante (235), le premier trou traversant (245a) exposant l'électrode de source (230a) ou l'électrode de drain (230b), le second trou traversant (245b) exposant la première couche conductrice (230c) ;
une électrode de pixel (250a) venant au contact de l'électrode de source (230a) ou de l'électrode de drain (230b) à travers le premier trou traversant (245a), et une seconde couche conductrice (250b) venant au contact de la première couche conductrice (230c) à travers le second trou traversant (245b) ; et
une couche isolante de définition de pixel (260a) qui expose l'électrode de pixel (250a) et est formée sur la seconde couche conductrice (250b).

2. Afficheur selon la revendication 1, dans lequel la seconde couche conductrice (250b) présente une épaisseur dans la gamme de 100 à 1000 Å.

3. Afficheur selon la revendication 1, dans lequel la couche de définition de pixel (260a) a une épaisseur de 3000 Å ou moins.

4. Afficheur selon la revendication 1, dans lequel le second trou traversant (245b) présente un angle de biseau de 50° ou moins.

5. Afficheur selon la revendication 1, dans lequel un bord de la première couche conductrice (230c) présente un angle de biseau de 50° ou moins.

6. Afficheur selon la revendication 1, dans lequel la première couche conductrice (235) est une couche de passivation.

7. Afficheur selon la revendication 6, dans lequel la première couche isolante (235) comporte en outre une couche de planarisation (240) agencée sur la couche

de passivation (235).

8. Afficheur selon la revendication 7, dans lequel le second trou traversant (245b) présente un angle de biseau de 50° ou moins.

9. Afficheur selon la revendication 7, dans lequel la couche de planarisation (240) comporte une ouverture qui expose la région de bornier de mesure de circuit (B) et le second trou traversant (245b) est agencé dans la couche de passivation (235).

10. Procédé de fabrication d'un afficheur électroluminescent organique, consistant à : préparer un substrat (200) présentant une région d'affichage (A) et une région de bornier de mesure de circuit (B), dans lequel un bornier de mesure de circuit (15) est agencé sur une région (15a) située entre une région d'émission de l'afficheur électroluminescent organique et une région de circuit d'attaque de données (3a) ou dans lequel le bornier de mesure de circuit (15) est agencé d'un côté (15b) d'un bord de l'afficheur électroluminescent organique ;
déposer et mettre sous forme de motif une couche conductrice sur le substrat afin de former une première couche conductrice (230c) au-dessus de la région de bornier de mesure de circuit (B) tout en formant des électrodes de source et de drain (230a, 230b) au-dessus de la région d'affichage (A) ;
former une première couche isolante (235) sur les électrodes de source et de drain (230a, 230b) et la première couche conductrice (230c) ;
former simultanément des premier et second trous traversants (245a, 245b) dans la première couche isolante (235), le premier trou traversant (245a) exposant l'électrode de source (230a) ou l'électrode de drain (230b), le second trou traversant (245b) exposant la première couche conductrice (230c) ;
déposer et mettre sous forme de motif une couche conductrice afin de former une électrode de pixel (250a) venant au contact de l'électrode de source (230a) ou de l'électrode de drain (230b) à travers le premier trou traversant (245a), et une seconde couche conductrice (250b) venant au contact de la première couche conductrice (230c) à travers le second trou traversant (245b) ; et
déposer et mettre sous forme de motif une seconde couche isolante afin de former une couche de définition de pixel (260a) qui expose l'électrode de pixel (250a) audessus de la région d'affichage (A) et recouvre la seconde couche conductrice (250b) audessus de la région de bornier de mesure de circuit (B).

11. Procédé selon la revendication 10, dans lequel la formation de la première couche isolante (235) inclut la formation d'une couche de passivation.

12. Procédé selon la revendication 11, dans lequel la formation de la première couche isolante (235) inclut en outre la formation d'une couche de planarisation (240) sur la couche de passivation (235).

13. Procédé selon la revendication 12, dans lequel le second trou traversant (245b) présente un angle de biseau de 50° ou moins.

14. Procédé selon la revendication 12, dans lequel, tandis que les premier second trous traversants (245a, 245b) sont formés en utilisant un masque de similigravure, une ouverture qui expose la région de bornier de mesure de circuit (B) est formée dans la couche de planarisation (240).

15. Procédé selon la revendication 10, consistant en outre à former une couche organique présentant une couche d'émission sur l'électrode de pixel exposée (250a), et à former une électrode opposée (280) audessus de la région d'affichage (A) présentant la couche organique et au-dessus de la région de bornier de mesure de circuit (B) présentant la seconde couche isolante.

16. Procédé selon la revendication 10, dans lequel la seconde couche conductrice (250b) présente une épaisseur dans la gamme de 100 à 1000 Å.

17. Procédé selon la revendication 10, dans lequel la couche de définition de pixel (260a) présente une épaisseur de 3000 Å ou moins.

18. Procédé selon la revendication 10, dans lequel le premier trou traversant (245a) présente un angle de biseau de 50° ou moins.

19. Procédé selon la revendication 10, dans lequel un bord de la première couche conductrice (230c) présente un angle de biseau de 50° ou moins.

FIG. 1

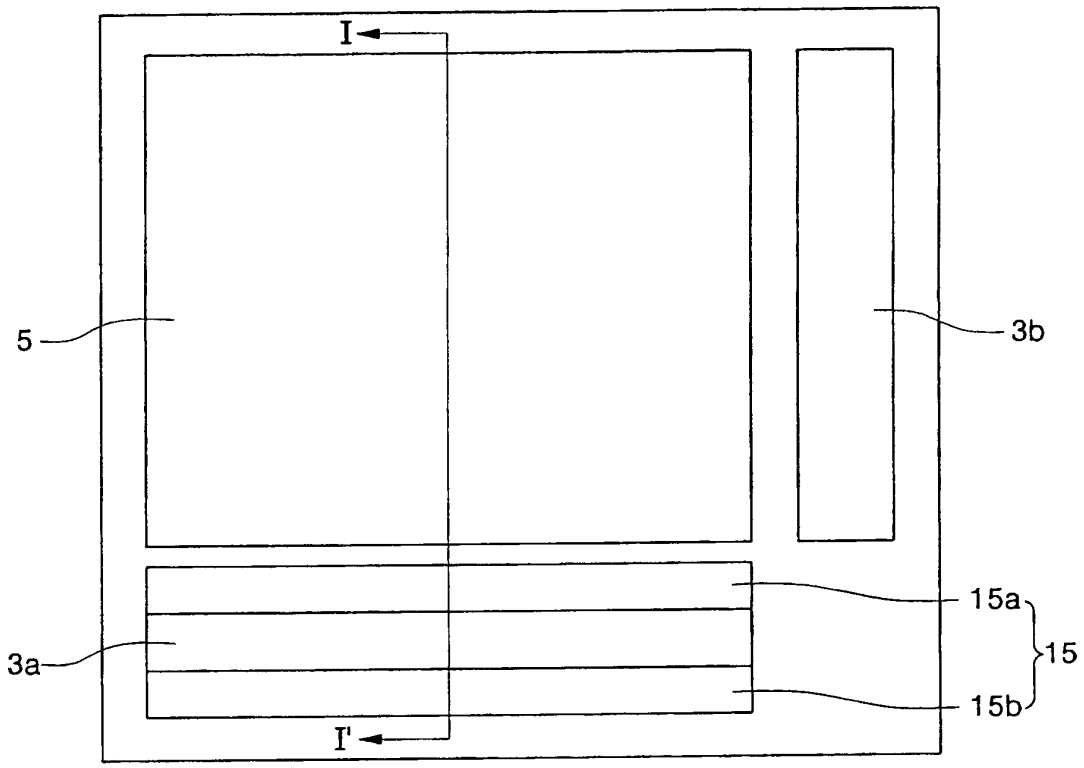


FIG. 2

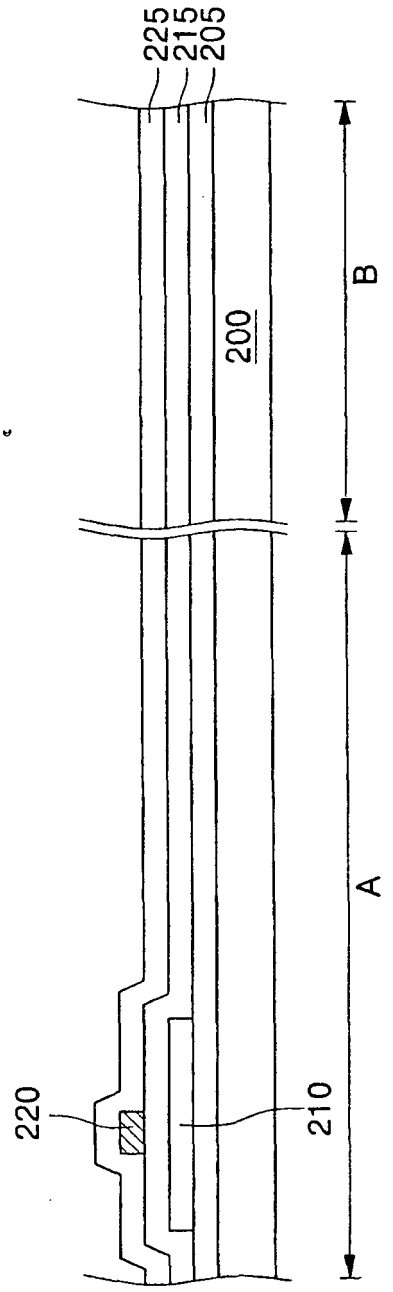


FIG. 3

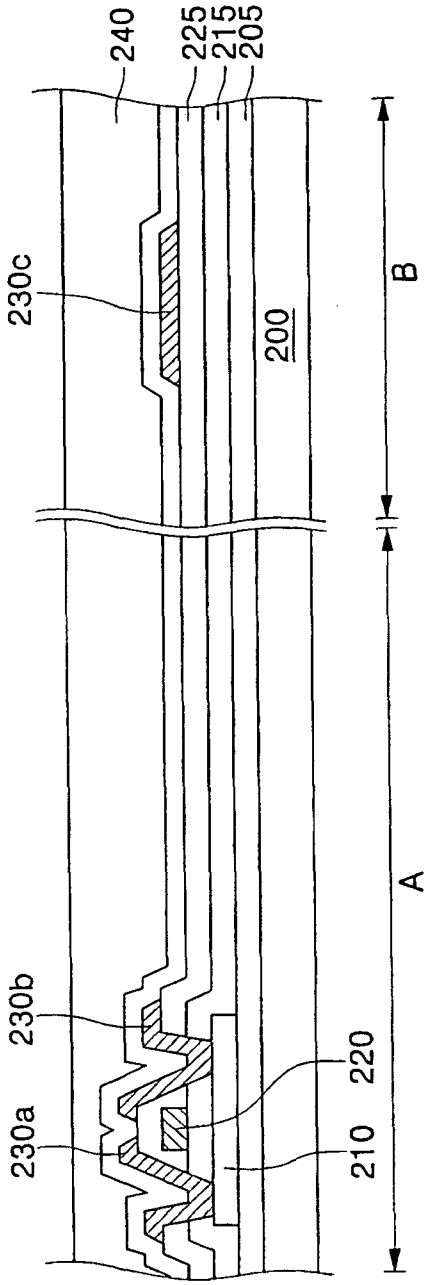


FIG. 4

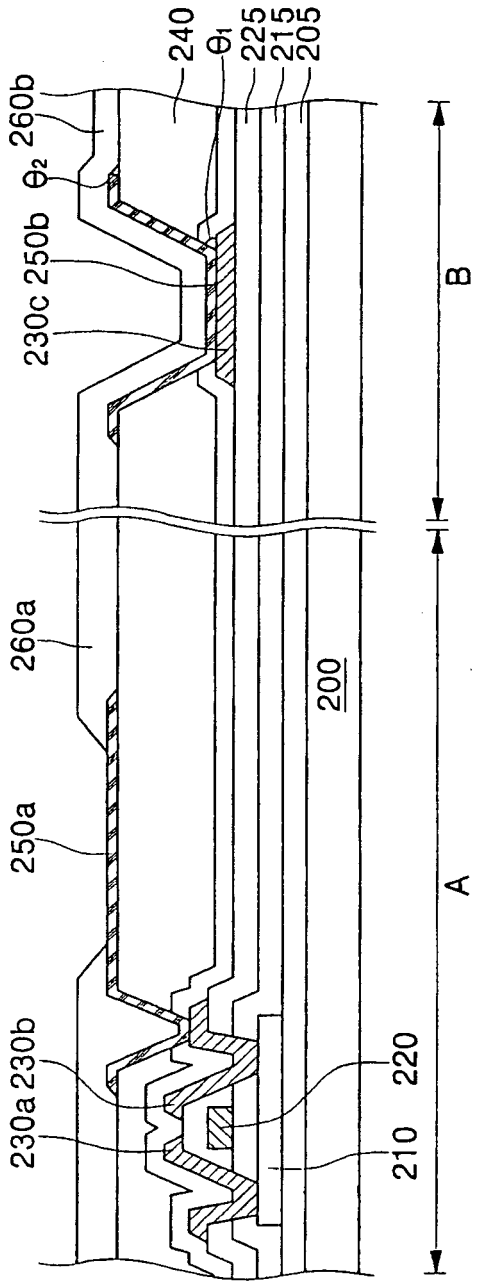

240
θ1
225
215
205
260b
θ2
250b
230c
B
260a
200
250a
230b
220
230a
210
A

FIG. 5

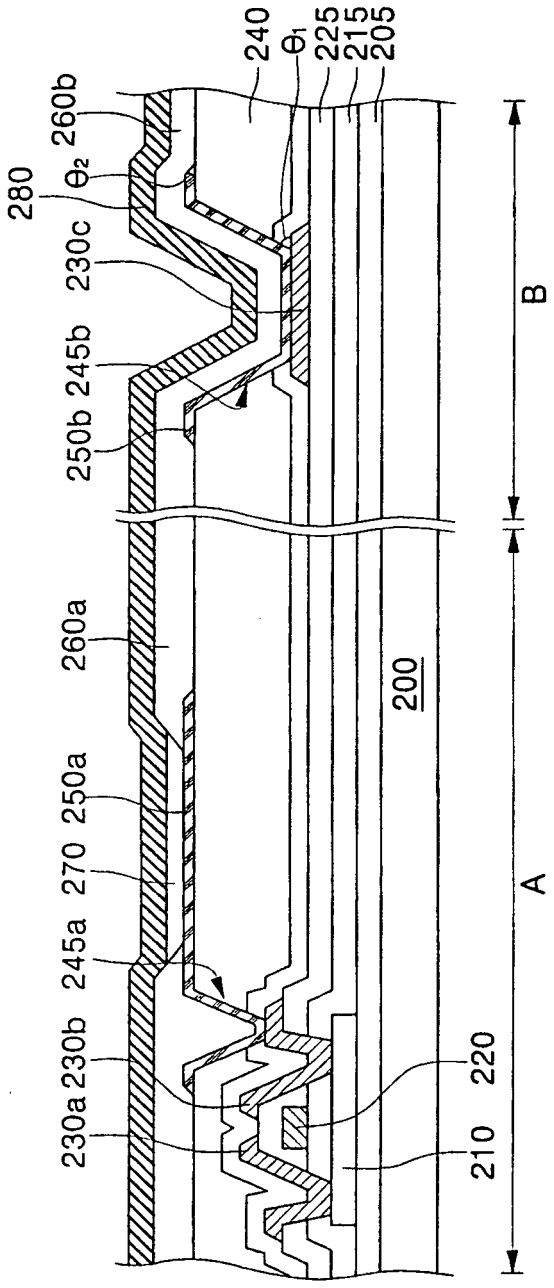

240
θ1
225
215
205
260b
θ2
280
230c
245b
250b
260a
250a
270
245a
230b
230a
200
220
210
B
A

FIG. 6

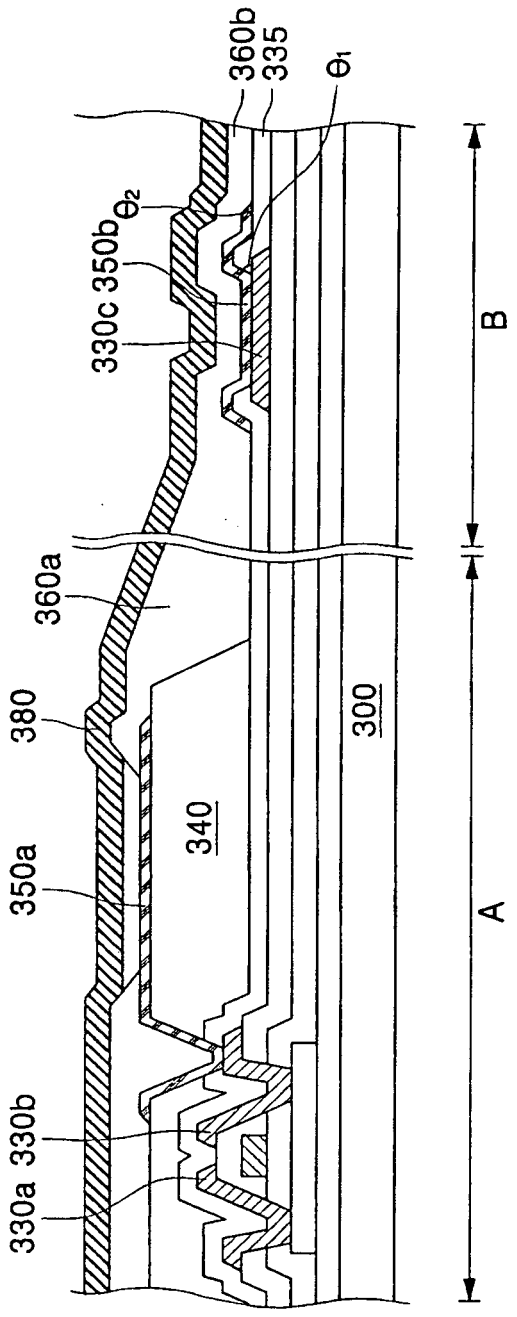


FIG. 7

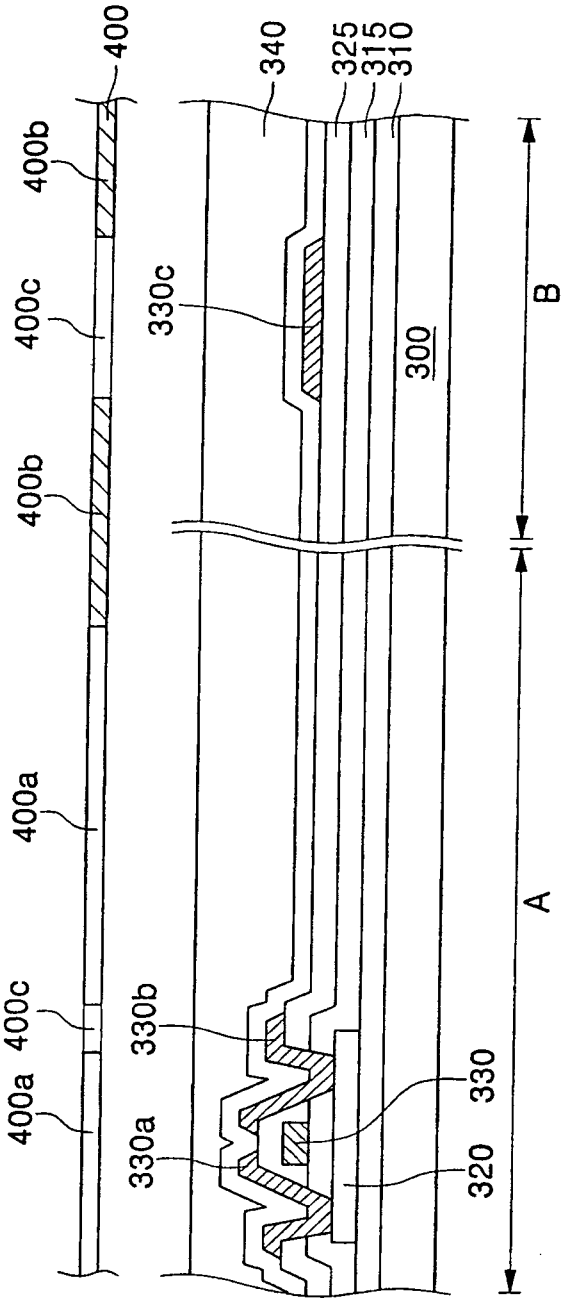
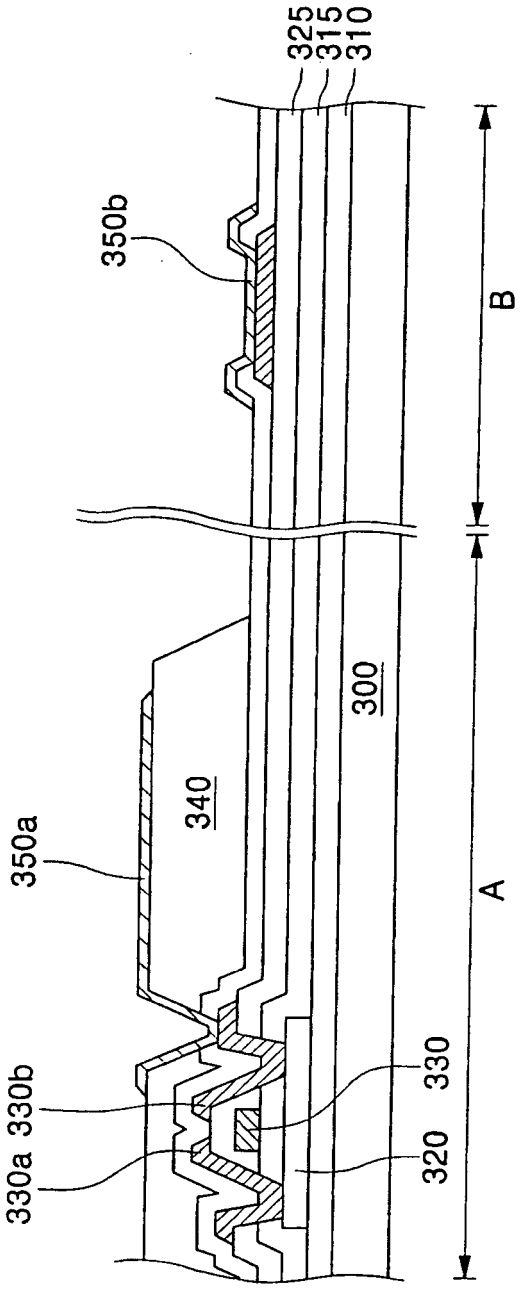

400
340
325
315
310
400b
400c
330c
300
B
400b
400a
400c
330b
330
400a
330a
320
A

FIG. 8



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 200470087 **[0001]**

专利名称(译)	具有电路测量垫的有机发光显示器及其制造方法		
公开(公告)号	EP1635407B1	公开(公告)日	2014-08-13
申请号	EP2004090505	申请日	2004-12-22
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	KIM MU HYUN KIM KEUM NAM		
发明人	KIM, MU-HYUN KIM, KEUM-NAM		
IPC分类号	H01L27/32 H01L51/56 H01L21/66		
CPC分类号	H01L27/3246 H01L27/3258 H01L27/3276 H01L51/56		
优先权	1020040070087 2004-09-02 KR		
其他公开文献	EP1635407A1		
外部链接	Espacenet		

摘要(译)

公开了一种有机发光显示器及其制造方法。发光显示器包括：具有显示区域和电路测量垫区域的基板;布置在显示区域上方的源电极和漏电极以及布置在电路测量焊盘区域上方的第一导电层与源电极和漏电极在同一层上;源电极和漏电极上的第一绝缘层和第一导电层;第一和第二通孔形成在第一绝缘层中，第一通孔暴露源或漏电极，第二通孔暴露第一导电层;像素电极通过第一通孔与源电极或漏电极接触，第二导电层通过第二通孔与第一导电层接触;像素限定层，其暴露像素电极并形成在第二导电层上。

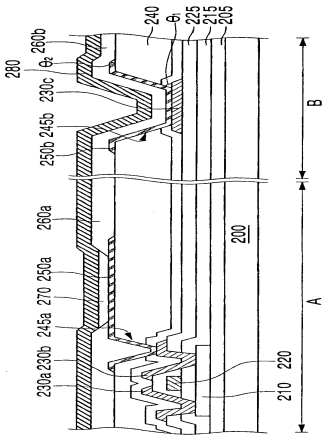

FIG. 5