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(54) PIXEL DRIVER CIRCUIT FOR AN ORGANIC LIGHT EMITTING DIODE

PIXELTREIBERSCHALTUNG FÜR EINE ORGANISCHE LEUCHTDIODE

CIRCUIT DE COMMANDE DE PIXEL POUR UNE DIODE ELECTROLUMINESCENTE ORGANIQUE

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Description

[0001] The present invention relates to a pixel driver circuit for an organic light emitting diode, and more particularly to a pixel current driver for an organic light emitting display (OLED), capable of minimizing parasitic coupling between the OLED and the transistor layers.

[0002] US-B-62522248 (= JP 11 354802) discloses a pixel current driver for an organic light emitting diode (OLED) having an OLED layer for emitting light, comprising a thin film transistor (TFT) having a source, a drain and a dual gate for driving the OLED layer. One top gate of the dual gate is formed between the source and the drain of the thin film transistor, to thereby minimize parasitic capacitance. However this reference only discloses the use of a single TFT to drive an OLED, which cannot supply a continuous excitation of the OLED during the entire frame period. Reference should also be made to JP-A-11 231805, which discloses the use of two TFTs in a pixel driver circuit for a display device. The circuit described here solves the problem of suppressing a leakage current to keep the electric potential of a gate electrode of a second thin film transistor constant and to allow a light emitting display picture element to emit light with luminance by forming a first thin film transistor into a double gate structure. For this, both first and second thin film transistors are top gate type thin film transistors with gate electrodes provided on active layers. Two gates are provided on the active layer through an insulating film, so that the first thin film transistor has a double gate structure. The active layer directly below the respective gates is provided with channel areas, areas filled with impurities, on both sides of each channel area, a source area higher in impurity concentration than the areas and a drain area. A leakage current of the first thin film transistor can therefore be suppressed and electric potential can be maintained constant without the electric potential of the gate electrode being changed following the change of a drain signal. It is apparent that this driver circuit minimizes parasitic capacitance in the driver circuit but not between the driver circuit and the OLED display. OLED displays have gained significant interest recently in display applications in view of their faster response times, larger viewing angles, higher contrast, lighter weight, lower power, amenability to flexible substrates, as compared to liquid crystal displays (LCDs). Despite the OLED's demonstrated superiority over the LCD, there still remain several challenging issues related to encapsulation and lifetime, yield, color efficiency, and drive electronics, all of which are receiving considerable attention. Although passive matrix addressed OLED displays are already in the marketplace, they do not support the resolution needed in the next generation displays, since high information content (HIC) formats are only possible with the active matrix addressing scheme. Active matrix addressing involves a layer of backplane electronics, based on thin-film transistors(TFTs) fabricated using amorphous silicon (a-Si: H), polycrystalline silicon (poly-Si), or polymer technologies, to provide the bias voltage and drive current needed in each OLED pixel. Here, the voltage on each pixel is lower and the current throughout the entire frame period is a low constant value, thus avoiding, the excessive peak driving and leakage, currents associated with passive matrix addressing. This in turn increases the lifetime of the OLED.

[0003] In active matrix OLED (AMOLED) displays, it is important to ensure that the aperture ratio or fill factor (defined as the ratio of light emitting display area to the total pixel area) should be high enough to ensure display quality. Conventional AMOLED displays are based on light emission through an aperture on the glass substrate where the backplane electronics is integrated. Increasing the on-pixel density of TFT integration for stable drive current reduces the size of the aperture. The same happens when pixel sizes are scaled down. The solution to having an aperture ratio that is invariant on scaling or on-pixel integration density is to vertically stack the OLED layer on the backplane electronics, along with a transparent top electrode (see Fig. 2). In Fig. 2, reference numerals S and D denote a source and a drain respectively. This implies a continuous back electrode over the OLED pixel. However, this continuous back electrode can give rise to parasitic capacitance, whose effects become significant when the electrode runs over the switching and other thin film transistors (TFTs). Here, the presence of the back electrode can induce a parasitic channel in TFTs giving rise to high leakage current. The leakage current is the current that flows between source and drain of the TFT when the gate of the TFT is in its OFF state.

[0004] Accordingly, it is an object of the present invention to provide to a pixel current driver for an organic light emitting display (OLED), capable of minimizing parasitic coupling between the OLED and the transistor layers of the driver-circuit. This object is solved by the present invention as claimed in the independent claims. Advantageous and preferred embodiments of the invention are defined by the dependent claims.

[0005] According to an example it is provided a pixel driver circuit for an organic light emitting diode (OLED) having an OLED layer for emitting light, an address line, a data line, and a plurality of thin film transistors, wherein the plurality of thin film transistors each has dual gates for driving the OLED layer, a top gate of the dual gates being formed between a source and a drain of each of the thin film transistors, to thereby minimize parasitic capacitance wherein the plurality of thin film transistors forms a current mirror comprising, either.

A) a first circuit including a first thin film transistor, having a first terminal of the first transistor connected to the data line and a gate of the first transistor connected to the address line; a second thin film transistor, having a first terminal of the second transistor connected to the data line and a gate of the second transistor connected to the address

line; a third thin film transistor, having a second terminal of the third transistor connected to a second terminal of the transistor, a gate of the third transistor connected to a second terminal of the first transistor, and a first terminal of the third transistor connected to a potential; and a fourth thin film transistor, having a gate of the fourth transistor connected to the gate of the third transistor, the pixel driver circuit driving a pixel through the fourth thin film transistor, or

B) a second circuit including: a first thin film transistor, having a second terminal of the first transistor connected to the data line and a gate of the first transistor connected to the address line; a second thin film transistor, having a gate of the second transistor connected to the address line, a first terminal of the second transistor connected to a potential; a third thin film transistor, having a first terminal and a gate of the third transistor connected to a first terminal of the first transistor, and a second terminal of the third transistor connected to a second terminal of the second transistor; and a fourth thin film transistor, having a gate of the fourth transistor connected to the gate of the third transistor, the pixel driver circuit driving a pixel through the fourth thin film transistor, or

C) a third circuit including: a first thin film transistor, having a first terminal of the first transistor connected to the data line and a gate of the first transistor connected to the address line; a second thin film transistor, having a first terminal of the second transistor connected to the data line and a gate of the second transistor connected to the address line; a third thin film transistor, having a second terminal of the third transistor connected to a second terminal of the second transistor, a gate of the third transistor connected to a second terminal of the first transistor and a first terminal of the third transistor connected to a ground potential; a fifth thin film transistor, having a second terminal and a gate of the fifth transistor connected to a potential, and a first terminal of the fifth transistor connected to the second terminal of the second transistor; and a fourth thin film transistor, having a gate of the fourth transistor connected to the gate of the third transistor, the pixel driver circuit driving a pixel through the fourth transistor, or

D) a fourth circuit including: a first thin film transistor, having a second terminal of the first transistor connected to the data line and a gate of the first transistor connected to the address line; a second thin film transistor, having a first terminal and a gate of the second transistor connected to the first terminal of the first transistor; a third thin film transistor having a first terminal connected to the gate terminal of the second transistor, a gate of the third transistor connected to a further address line, and a second terminal; and a fourth thin film transistor, having a gate of the fourth transistor connected to the second terminal of the third transistor, the pixel driver circuit driving a pixel through the fourth thin film transistor, wherein the light emitting diode is connected to the fourth transistor (T4; T5; T6, T7, T8) and a capacitor C_s, the capacitor C_s being connected between the gate of the fourth transistor (T4; T5; T6, T7, T8) and a ground potential.

[0006] Each of the thin film transistors may be an a-Si: H based thin film transistor or a polysilicon-based thin film transistor.

[0007] The pixel current driver is a current mirror based pixel current driver for automatically compensating for shifts in the Vth of each of the thin film transistor in a pixel and the pixel current driver is for monochrome displays or for-full color displays.

[0008] The dual gates are fabricated in a normal inverted staggered TFT structure. A width of each of the TFTs is formed larger than a length of the same to provide enough spacing between the source and drain for the top gate. Preferably, the length is 30 pm and the width is 1600 μm. The length and width of the transistors may change depending on the maximum drive current required by the circuit and the fabrication technology used. The top gate is grounded or electrically tied to a bottom gate. The plurality of thin film transistors may be two thin film transistors formed in voltage-programmed manner or five thin film transistors formed in a current-programmed ΔV_T- compensated manner, or four or The OLED layer is vertically stacked on the plurality of thin film transistors.

[0009] With the above structure of an a-Si: H current driver according to the present invention, the charge induced in the top channel of the TFT is minimized, and the leakage currents in the TFT is minimized so as to enhance circuit performance.

[0010] The above objects and features of the present invention will become more apparent from the accompanied description of preferred embodiments given with reference to the attached drawings in which:

Fig. 1 shows variation of required pixel areas with mobility for 2-T and 5-T pixel drivers;

Fig.2 shows a pixel architecture for surface emissive a Si: H AMOLED displays;

Fig. 3 shows a cross section of a dual-gate TFT structure;

Fig. 4 shows forward and reverse transfer characteristics of dual-gate TFT for various top gate biases;

Fig. 5A and Fig. 5B show an example of an equivalent circuit for a 2-T pixel driver and its associated input-output timing diagrams;

Fig. 6A and Fig.6B show an equivalent circuit for a 5-T pixel driver and its associated input-output timing diagrams;

Fig. 7 shows transient performance of the 5-T driver for three consecutive write cycles;

Fig. 8 shows input-output transfer characteristics for the 2-T pixel driver for different supply voltages;

Fig. 9 shows input-output transfer characteristics for the 5-T pixel driver for different supply voltages;

Fig. 10 shows variation in OLED current as a function of the normalized shift in threshold voltage;

Fig. 11 shows an example of a 2-T polysilicon based pixel current driver having p-channel drive TFTs ;

Fig. 12 shows a 4-T pixel current driver for OLED displays;

Fig. 13 shows a 4-T pixel current driver with a lower discharge time;

Fig. 14 shows a 4-T pixel current driver without non-linear gain;

Fig. 15 shows a 4-T pixel current driver that is the building block for the full color circuit; and

Fig. 16 shows a full color(RGB) pixel current driver for OLED displays.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0011] Although amorphous Si does not enjoy equivalent electronic properties compared to poly-Si, it adequately meets many of the drive requirements for small area displays such as those needed in pagers, cell phones, and other mobile devices. Poly-Si TFTs have one key advantage in that they are able to provide better pixel drive capability because of their higher mobility, which can be of the order of μ_{FE}-100cm^2/Vs. This makes poly-Si highly desirable for large area (e.g. laptop size) VGA and SVGA displays. The lower mobility associated with a-Si:H TFTs (μ_{FE}~lcm^2/Vs) is not a limiting factor since the drive transistor in the pixel can be scaled up in area to provide the needed drive current. The OLED drive current density is typically 10mA/cm^2 at 10V operation to provide a brightness of 100 cd/m^2 - the required luminance for most displays. For example, with an a-Si:H TFT mobility of 0.5cm^2/Vs and channel length of 25μm, this drive current requirement translates into required pixel area of 300 μm^2, which adequately meets the requirements of pixel resolution and speed for some 3 inch monochrome display applications. Figure 1 illustrates simulation results for the variation of the required pixel size with device mobility calculated for two types of drivers, which will be elaborated later, the 2-T and the 5-T drivers, wherein μ_0 denotes a reference mobility whose value is in the range 0.1 to 1 cm^2/Vs. For instance, the area of the pixel for the 2-T driver (see Figure 5A) comprises of the area of the switching transistors, area of the drive transistor, and the area occupied by interconnects, bias lines, etc. In Fig. 1, the drive current and frame rate are kept constant at 10μA and 50Hz, respectively, for a 230 x 230 array. It is clear that there is no significant savings in area between the 2-T and 5-T drivers but the savings are considerable with increasing mobility. This stems mainly from the reduction in the area of the drive transistor where there is a trade-off between μ_{FE} and TFT aspect ratio, W/L(Wide/Length).

[0012] In terms of threshold voltage (V_T) uniformity and stability, both poly-Si and a-Si:H share the same concerns, although in comparison, the latter provides for better spatial uniformity but not stability (ΔV_T). Thus the inter-pixel variation in the drive current can be a concern in both cases, although clever circuit design techniques can be employed to compensate for ΔV_T hence improving drive current uniformity. In terms of long term reliability, it is not quite clear with poly-Si technology, although there are already products based on a-Si:H technology for displays and imaging, although the reliability issues associated with OLEDs may yet be different. The fabrication processes associated with a-Si:H technology are standard and adapted from mainstream integrated circuit (IC) technology, but with capital equipment costs that are much lower. One of the main advantages of the a-Si:H technology is that it has become low cost and well-established technology, while poly-Si has yet to reach the stage of manufacturability. The technology also holds great promise for futuristic applications since good as-deposited a-Si:H, a-SiN$_x$:H, and TFT arrays can be achieved at low temperatures ($\leq$120°C) thus making it amenable to plastic substrates, which is a critical requirement for mechanically flexible displays.

[0013] To minimize the conduction induced in all TFTs in the pixel by the back electrode, an alternate TFT structure based on a dual-gate structure is employed. In a dual gate TFT (see Fig. 3), a top gate electrode is added to the TFT structure to prevent the OLED electrodes from biasing the a-Si:H channel area (refer to Fig. 2). The voltage on the top gate can be chosen such so as to minimize the charge induced in the (parasitic) top channel of the TFT. The objective underlying the choice of the voltage on the top gate is to minimize parasitic capacitance in the driver circuits and leakage currents in the TFTs so as to enhance circuit performance. In what follows, the operation of the dual-gate TFT is described, which will be central to surface emissive (100% aperture ratio) AMOLED displays based on a-Si:H backplane electronics.

[0014] Figure 3 illustrates the structure of a dual-gate TFT fabricated for this purpose, wherein reference numerals S and D denote a source and a drain respectively. The fabrication steps are the same as of that of a normal inverted staggered TFT structure except that it requires a sixth mask for patterning the top gate. The length of the TFT is around 30μm to provide enough spacing between the source and drain for the top gate, and the width is made very large (1600μm) with four of these TFTs are interconnected in parallel to create a sizeable leakage current for measurement. A delay time is inserted in the measurement of the current to ensure that the measurement has passed the transient period created by defects in the a-Si:H active layer, which give rise to a time-dependent capacitance.

[0015] Figure 4 shows results of static current measurements for four cases: first when the top gate is tied to -10V, second when the top gate is grounded, third when the top gate is floating, and lastly when the top gate is shorted to the bottom gate. With a floating top gate, the characteristics are almost similar to that of a normal single gate TFT. The leakage current is relatively high particularly when the top gate is biased with a negative voltage. The lowest values of leakage current are obtained when the top gate is pegged to either 0V or to the voltage of the bottom gate. In particular, with the latter the performance of the TFT in the (forward) sub-threshold regime of operation is significantly improved. This enhancement in sub-threshold performance can be explained by the forced shift of the effective conduction path away from the bottom interface to the bulk a-Si:H region due to the positive bias on the top gate. This in turn decreases the effect of the trap states at the bottom interface on the sub-threshold slope of the TFT.

[0016] It should be noted that although the addition of another metal contact as the top gate reduces the leakage current of the TFT, it can potentially degrade pixel circuit performance by possible parasitic capacitances introduced by vertically stacking the OLED pixel. Thus the choice of top gate connection becomes extremely critical. For example, if the top gates in the pixel circuit are connected to the bottom gates of the associated TFTs, this gives rise to parasitic capacitances located between the gates and the cathode, which can lead to undesirable display operation (due to the charging up of the parasitic capacitance) when the multiplexer O/P drives the TFT switch. On the other hand, if the top gates are grounded, this results in the parasitic capacitance being grounded to yield reliable and stable circuit operation.

[0017] The OLED drive circuits considered here are the well-known voltage-programmed 2-T driver and the more sophisticated current-programmed ΔV_T-compensated 5-T version (see Figs. 5A and 6A). The latter is a significant variation of the previous designs, leading to reduced pixel area (<300μm), reduced leakage, lower supply voltage (20V), higher linearity (~30dB), and larger dynamic range (-40dB). Before dwelling on the operation of the 5-T driver, the operation of the relatively simple voltage-driven 2-T driver is described. Fig. 5B shows input-output timing diagrams of the 2-T pixel driver. When the address line is activated, the voltage on the data line starts charging capacitor C_s and the gate capacitance of the driver transistor T_2. Depending on the voltage on the data line, the capacitor charges up to turn the driver transistor T_2 on, which then starts conducting to drive the OLED with the appropriate level of current. When the address line is turned off, T_1 is turned off but the voltage at the gate of T_2 remains since the leakage current of T_1 is trivial in comparison. Hence, the current through the OLED remains unchanged after the turn off process. The OLED current changes only the next time around when a different voltage is written into the pixel.

[0018] Unlike the previous driver, the data that is written into the 5-T pixel in this case is a current (see Fig. 6A). Fig. 6B shows input-output timing diagrams of a 5-T pixel driver. The address line voltage, $V_{address}$ and I_{data} are activated or deactivated simultaneously. When $V_{address}$ is activated, it forces T_1 and T_2 to turn on. T_1 immediately starts conducting but T_2 does not since T_3 and T_4 are off. Therefore, the voltages at the drain and source of T_2 become equal. The current flow through T_1 starts charging the gate capacitor of transistors T_3 and T_5, very much like the 2-T driver. The current of these transistors start increasing and consequently T_2 starts to conduct current. Therefore, T_1' share of I_{data} reduces and T_2's share of I_{data} increases. This process continues until the gate capacitors of T_3 and T_5 charge (via T_1) to a voltage that forces the current of T_3 to be I_{data}. At this time, the current of T_1 is zero and the entire I_{data} goes through T_2 and T_3. At the same time, T_5 drives a current through the OLED, which is ideally equal to $I_{data}*(W_5/W_3)$, which signifies a current gain. Now if I_{data} and $V_{address}$ are deactivated, T_2 will turn off, but due to the presence of capacitances in T_3 and T_5, the current of these two devices cannot be changed easily, since the capacitances keep the bias voltages constant. This forces T_4 to conduct the same current as that of T_3, to enable the driver T_5 to drive the same current into the OLED even when the write period is over. Writing a new value into the pixel then changes the current driven into the OLED.

[0019] The result of transient simulation for the 5-T driver circuit is shown in Fig. 7. As can be seen, the circuit has a write time of <70μs, which is acceptable for most applications. The 5-T driver circuit does not increase the required pixel size significantly (see Fig. 1) since the sizes of T2, T3, and T4 are scaled down. This also provides an internal gain *(W_5/*

W_3 = 8), which reduces the required input current to <2μA for 10μA OLED current. The transfer characteristics for the 2-T and 5-T driver circuits are illustrated in Figs. 8 and 9, respectively, generated using reliable physically-based TFT models for both forward and reverse regimes. A much improved linearity (-30dB) in the transfer characteristics (I_{data}/I_{OLED}) is observed for the 5-T driver circuit due to the geometrically-defined internal pixel gain as compared to similar designs. In addition, there are two components (OLED and T_5) in the high current path, which in turn decreases the required supply voltage and hence improves the dynamic range. According to Figure 9, a good dynamic range (-40dB) is observed for supply voltage of 20V and drive currents in the range $I_{OLED} \leq 10\mu A$, which is realistic for high brightness. Figure 10 illustrates variation in the OLED current with the shift in threshold voltage for the 2-T and 5-T driver circuits. The 5-T driver circuit compensates for the shift in threshold voltage particularly when the shift is smaller than 10% of the supply voltage. This is because the 5-T driver circuit is current-programmed. In contrast, the OLED current in the 2-T circuit changes significantly with a shift in threshold voltage. The 5-T driver circuit described here operates at much lower supply voltages, has a much larger drive current, and occupies less area.

[0020] The pixel architectures are compatible to surface (top) emissive AMOLED displays that enables high on-pixel TFT integration density for uniformity in OLED drive current and high aperture ratio. A 5-T driver circuit has been described that provides on-pixel gain, high linearity (-30dB), and high dynamic range (~40db) at low supply voltages (15-20V) compared to the similar designs (27V). The results described here illustrate the feasibility of using a-Si:H for 3-inch mobile monochrome display applications on both glass and plastic substrates. With the latter, although the mobility of the TFT is lower, the size of the drive transistor can be scaled up yet meeting the requirements on pixel area as depicted in Fig. 1.

[0021] Polysilicon has higher electron and hole mobilities than amorphous silicon. The hole mobilities are large enough to allow the fabrication of p-channel TFTs.

[0022] The advantage of having p-channel TFTs is that bottom emissive OLEDs can be used along with a p-channel drive TFT to make a very good current source. One such circuit is shown in Fig. 11. In Fig. 11, the source of the p-type drive TFT is connected to Vdd. Therefore, Vgs, gate-to-source voltage, and hence the drive current of the p-type TFT is independent of OLED characteristics. In other words, the driver shown in Fig. 11 performs as a good current source. Hence, bottom emissive OLEDs are suitable for use with p-channel drive TFTs, and top emissive OLEDs are suitable for use with n-channel TFTs.

[0023] The trade-off with using polysilicon is that the process of making polysilicon TFTs requires much higher temperatures than that of amorphous silicon. This high temperature processing requirement greatly increases the cost, and is not amenable to plastic substrates. Moreover, polysilicon technology is not as mature and widely available as amorphous silicon. In contrast, amorphous silicon is a well-established technology currently used in liquid crystal displays (LCDs). It is due to these reasons that amorphous silicon combined with top emissive OLED based circuit designs is most promising for AMOLED displays.

[0024] Compared to polysilicon TFTs, amorphous silicon TFTs are n-type and thus are more suitable for top emission circuits as shown in Fig. 2. However, amorphous silicon TFTs have inherent stability problems due to the material structure. In amorphous silicon circuit design, the biggest hurdle is the increase in threshold voltage V_{th} after prolonged gate bias. This shift is particularly evident in the drive TFT of an OLED display pixel. This drive TFT is always in the 'ON' state, in which there is a positive voltage at its gate. As a result, its V_{th} increases and the drive current decreases based on the current-voltage equation below:

$$Ids = (\mu C_{ox} W / 2L) (V_{gs} - V_{th})^2 \qquad \text{(in Saturation region)}$$

(in Saturation region)

[0025] In the display, this would mean that the brightness of the OLED would decrease over time, which is unacceptable. Hence, the 2-T circuits shown earlier are not practical for OLED displays as they do not compensate for any increase in V_{th}.

[0026] The first current mirror based pixel driver circuit is presented, which automatically compensated for shifts in the V_{th} of the drive TFT in a pixel. This circuit is the 5-T circuit shown in Fig. 6A.

[0027] Four more OLED pixel driver circuits are presented for monochrome displays, and one circuit for full colour displays. All these circuits have mechanisms that automatically compensate for V_{th} shift. The first circuit shown in Fig. 12 is a modification of the 5-T circuit of Fig. 6A. (Transistor T_4 has been removed from the 5-T circuit). This circuit occupies a smaller area than the 5-T circuit, and provides a higher dynamic range. The higher dynamic range allows for a larger signal swing at the input, which means that the OLED brightness can be adjusted over a larger range.

[0028] Fig. 12 shows a 4-T pixel driver circuit for OLED displays. The circuit shown in Fig. 13 is a 4-T pixel driver circuit based on a current mirror. The advantage of this circuit is that the discharge time of the capacitor Cs is substantially reduced. This is because the discharge path has two TFTs (as compared to three TFTs in the circuit of Fig. 12). The charging time remains the same. The other advantage is that there is an additional gain provided by this circuit because

T_3 and T_4 do not have the same source voltages. However, this gain is non-linear and may not be desirable in some cases.

[0029] In Fig. 14, another 4-T circuit is shown. This circuit does not have the non-linear gain present in the previous circuit (Fig. 13) since the source terminals of T_3 and T_4 are at the same voltage. It still maintains the lower capacitance discharge time, along with the other features of the circuit of Fig. 8.

[0030] Fig. 15 shows another version of the 4-T circuit. This circuit is does not have good current mirror properties. However, this circuit forms the building block for the 3 colour RGB circuit shown in Fig. 16. It also has a low capacitance discharge time and high dynamic range.

[0031] The full colour circuit shown in Fig. 16 minimizes the area required by an RGB pixel on a display, while maintaining the desirable features like threshold voltage shift compensation, in-pixel current gain, low capacitance discharge time, and high dynamic range.

[0032] It is important to note that the dual-gate TFTs are used in the above-mentioned circuits to enable vertical integration of the OLED layers with minimum parasitic effects. But nevertheless the circuit compensates for the Vth shift even if the simple single-gate TFTs. In addition, these circuits use n-type amorphous silicon TFTs. However, the circuits are applicable to polysilicon technology using p-type or n-type TFTs. These circuits when made in polysilicon can compensate for the non-uniformity of the threshold voltage, which is a problem in this technology. The p-type circuits are conjugates of the above-mentioned circuits and are suitable for the bottom emissive pixels.

Claims

1. A pixel current driver for an organic light emitting diode, "OLED", having an OLED layer for emitting light, an address line, a data line, and a plurality of thin film transistors, wherein the plurality of thin film transistors, "TFTs", each has dual gates for driving the OLED layer, a top gate of the dual gates being formed between a source and a drain of each of the thin film transistors, to thereby minimize parasitic capacitance wherein the plurality of TFTs forms a current mirror comprising, either:

   A) a first circuit including a first thin film transistor (T1) having a first terminal of the first transistor (T1) connected to the data line and a gate of the first transistor (T1) connected to the address line; a second thin film transistor (T2), having a first terminal of the second transistor (T2) connected to the data line and a gate of the second transistor (T2) connected to the address line; a third thin film transistor (T3), having a second terminal of the third transistor (T3) connected to a second terminal of the transistor (T2), a gate of the third transistor (T3) connected to a second terminal of the first transistor (T1), and a first terminal of the third transistor (T3) connected to a ground potential; and a fourth thin film transistor (T4), having a gate of the fourth transistor (T4) connected to the gate of the third transistor (T3), the pixel driver circuit driving a pixel through the fourth thin film transistor (T4), or

   B) a second circuit including: a first thin film transistor (T2) having a second terminal of the first transistor (T2) connected to the data line and a gate of the first transistor (T2) connected to the address line; a second thin film transistor (T1), having a gate of the second transistor (T1) connected to the address line, a first terminal of the second transistor (T1) connected to a ground potential; a third thin film transistor (T3), having a first terminal and a gate of the third transistor (T3) connected to a first terminal of the first transistor (T2), and a second terminal of the third transistor (T3) connected to a second terminal of the second transistor (T1); and a fourth thin film transistor (T4), having a gate of the fourth transistor (T4) connected to the gate of the third transistor (T3), the pixel driver circuit driving a pixel through the fourth thin film transistor (T4), or

   C) a third circuit including: a first thin film transistor (T1), having a first terminal of the first transistor (T1) connected to the data line and a gate of the first transistor (T1) connected to the address line; a second thin film transistor (T2), having a first terminal of the second transistor (T2) connected to the data line and a gate of the second transistor (T2) connected to the address line; a third thin film transistor (T3), having a second terminal of the third transistor (T3) connected to a second terminal of the second transistor (T2), a gate of the third transistor (T3) connected to a second terminal of first transistor (T1), and a first terminal of the third transistor (T3) connected to a ground potential; a fifth thin film transistor (T4), having a second terminal and a gate of the fifth transistor (T4) connected to a potential, and a first terminal of the fifth transistor (T4) connected to the second terminal of the second transistor (T2); and a fourth thin film transistor (T5), having a gate of the fourth transistor (T5) connected to the gate of the third transistor (T3), the pixel driver circuit driving a pixel through the fourth thin film transistor (T5), or

   D) a fourth circuit including: a first thin film transistor (T1), having a second terminal of the first transistor (T1) connected to the data line and a gate of the first transistor (T1) connected to the address line; a second thin film transistor (T2), having a first terminal and a gate of the second transistor (T2) connected to a first terminal of the first transistor (T1); a third thin film transistor (T3, T4, T5), having a first terminal connected to the gate

terminal of the second transistor (T2), a gate of the third transistor (T3, T4, T5) connected to a further address line, and a second terminal; and a fourth thin film transistor (T6, T7, T8) having a gate of the fourth transistor (T6, T7, T8) connected to the second terminal of the third transistor (T3, T4, T5), the pixel driver circuit driving a pixel through the fourth thin film transistor (T6, T7, T8); and
a capacitor (Cs), the capacitor (Cs) being connected between the gate of the fourth transistor (T4, T5, T6, T7, T8) and a ground potential in any of the first, second, third and fourth circuits,
wherein the organic light emitting diode is connected to the fourth transistor (T4; T5; T6, T7, T8).

2. The pixel current driver according to claim 1, wherein each of the thin film transistors is an a-Si:H based thin film transistor.

3. The pixel current driver according to claim 1, wherein each of the thin film transistors is a polysilicon-based thin film transistor.

4. The pixel current driver according to claim 3, wherein each of the thin film transistors is a p-channel thin film transistor.

5. The pixel driver circuit according to any one of claims 1 to 4, wherein the fourth circuit of the pixel driver circuit is provided for driving a colour pixel of a full colour display.

6. The pixel driver circuit according to any one of claims 1 to 4, wherein the pixel driver circuit is provided for a monochrome display.

7. The pixel driver circuit according to claim 2, wherein the thin film transistors are dual gate transistors in an inverted staggered TFT structure.

8. The pixel driver circuit according to claim 2, wherein a top gate of the dual gate is grounded.

9. The pixel driver circuit according to claim 2, wherein a top gate of the dual gate is electrically tied to a bottom gate of the dual gate.

Patentansprüche

1. Pixel-Stromansteuervorrichtung für eine organische Leuchtdiode (OLED), die eine OLED-Schicht zum Emittieren von Licht, eine Adressen-Leitung, eine Datenleitung, sowie eine Vielzahl von Dünnfilmtransistoren aufweist, wobei die Vielzahl von Dünnfilmtransistoren (TFT) jeweils Doppelgates zum Ansteuern der OLED-Schicht haben, ein oberes Gate der Doppelgates zwischen einer Source und einem Drain jedes der Dünnschichttransistoren ausgebildet ist, um so parasitäre Kapazität zu minimieren, und die Vielzahl von Dünnschichttransistoren einen Stromspiegel bilden, der entweder umfasst:

A) eine erste Schaltung, die enthält: einen ersten Dünnschichttransistor (T1), wobei ein erster Anschluss des ersten Transistors (T1) mit der Datenleitung verbunden ist und ein Gate des ersten Transistors (T1) mit der Adressenleitung verbunden ist; einen zweiten Dünnfilmtransistor (T2), wobei ein erster Anschluss des zweiten Transistors (T2) mit der Datenleitung verbunden ist und ein Gate des zweiten Transistors (T2) mit der Adressenleitung verbunden ist; einen dritten Dünnfilmtransistor (T3), wobei ein zweiter Anschluss des dritten Transistors (T3) mit einem zweiten Anschluss des zweiten Transistors (T2) verbunden ist, ein Gate des dritten Transistors (T3) mit einem zweiten Anschluss des ersten Transistors (T1) verbunden ist und ein erster Anschluss des dritten Transistors (T3) mit einem Erdpotential verbunden ist; und einen vierten Dünnfilmtransistor (T4), wobei ein Gate des vierten Transistors (T4) mit dem Gate des dritten Transistors (T3) verbunden ist und die Pixel-Ansteuerschaltung ein Pixel über den vierten Dünnfilmtransistor (T4) ansteuert, oder
B) eine zweite Schaltung, die enthält: einen ersten Dünnfilmtransistor (T2), wobei ein zweiter Anschluss des ersten Transistors (T2) mit der Datenleitung verbunden ist und ein Gate des ersten Transistors (T2) mit der Adressenleitung verbunden ist; einen zweiten Dünnfilmtransistor (T1), wobei ein Gate des zweiten Transistors (T1) mit der Adressenleitung verbunden ist, ein erster Anschluss des zweiten Transistors (T1) mit einem Erdpotential verbunden ist; einen dritten Dünnfilmtransistor (T3), wobei ein erster Anschluss sowie ein Gate des dritten Transistors (T3) mit einem ersten Anschluss des ersten Transistors (T2) verbunden sind und ein zweiter Anschluss des dritten Transistors (T3) mit einem zweiten Anschluss des zweiten Transistors (T1) verbunden ist; und einen vierten Dünnfilmtransistor (T4), wobei ein Gate des vierten Transistors (T4) mit dem Gate des

dritten Transistors (T3) verbunden ist und die Pixel-Ansteuerschaltung ein Pixel über den vierten Dünnfilmtransistor (T4) ansteuert, oder

C) eine dritte Schaltung, die enthält: einen ersten Dünnfilmtransistor (T1), wobei ein erster Anschluss des ersten Transistors (T1) mit der Datenleitung verbunden ist und ein Gate des ersten Transistors (T1) mit der Adressenleitung verbunden ist; einen zweiten Dünnfilmtransistor (T2), wobei ein erster Anschluss des zweiten Transistors (T2) mit der Datenleitung verbunden ist und ein Gate des zweiten Transistors (T2) mit der Adressenleitung verbunden ist; einen dritten Dünnfilmtransistor (T3), wobei ein zweiter Anschluss des dritten Transistors (T3) mit einem zweiten Anschluss des zweiten Transistors (T2) verbunden ist, ein Gate des dritten Transistors (T3) mit einem zweiten Anschluss des ersten Transistors (T2) verbunden ist und ein erster Anschluss des dritten Transistors (T3) mit einem Erdpotential verbunden ist; einen fünften Dünnfilmtransistor (T4), wobei ein zweiter Anschluss sowie ein Gate des fünften Transistors (T4) mit einem Potential verbunden sind und ein erster Anschluss des fünften Transistors (T4) mit dem zweiten Anschluss des zweiten Transistors (T2) verbunden ist; und einen vierten Dünnfilmtransistor (T5), wobei ein Gate des vierten Transistors (T5) mit dem Gate des dritten Transistors (T3) verbunden ist und die Pixel-Ansteuerschaltung ein Pixel über den vierten Dünnfilmtransistor (T5) ansteuert, oder

D) eine vierte Schaltung, die enthält: einen ersten Dünnfilmtransistor (T1), wobei ein zweiter Anschluss des ersten Transistors (T1) mit der Datenleitung verbunden ist und ein Gate des ersten Transistors (T1) mit der Adressenleitung verbunden ist; einen zweiten Dünnfilmtransistor (T2), wobei ein erster Anschluss sowie ein Gate des zweiten Transistors (T2) mit einem ersten Anschluss des ersten Transistors (T1) verbunden sind; einen dritten Dünnfilmtransistor (T3, T4, T5), der einen ersten Anschluss hat, der mit dem Gate-Anschluss des zweiten Transistors (T2) verbunden ist, wobei ein Gate des dritten Transistors (T3, T4, T5) mit einer weiteren Adressenleitung verbunden ist, und der einen zweiten Anschluss hat; und einen vierten Dünnfilmtransistor (T6, T7, T8), wobei ein Gate des vierten Transistors (T6, T7, T8) mit dem zweiten Anschluss des dritten Transistors (T3, T4, T5) verbunden ist und die Pixel-Ansteuerschaltung ein Pixel über den vierten Dünnfilmtransistor (T6, T7, T8) ansteuert; und

einen Kondensator (Cs), wobei der Kondensator (Cs) zwischen das Gate des vierten Transistors (T4, T5, T6, T7, T8) und ein Erdpotential in der ersten, zweiten, dritten und vierten Schaltung geschaltet ist, und die organische Leuchtdiode mit dem vierten Transistor (T4; T5; T6, T7, T8) verbunden ist.

2. Pixel-Stromansteuervorrichtung nach Anspruch 1, wobei jeder der Dünnfilmtransistoren ein Dünnfilmtransistor auf a-Si:H-Basis ist.

3. Pixel-Stromansteuervorrichtung nach Anspruch 1, wobei jeder der Dünnfilmtransistoren ein Dünnfilmtransistor auf Polysilizium-Basis ist.

4. Pixel-Stromansteuervorrichtung nach Anspruch 3, wobei jeder der Dünnfilm-Transistoren ein p-Kanal-Dünnfilmtransistor ist.

5. Pixel-Stromansteuervorrichtung nach einem der Ansprüche 1 bis 4, wobei die vierte Schaltung der Pixel-Ansteuerschaltung vorhanden ist, um ein Farb-Pixel einer Vollfarb-Anzeigeeinrichtung anzusteuern.

6. Pixel-Stromansteuervorrichtung nach einem der Ansprüche 1 bis 4, wobei die Pixel-Ansteuerschaltung für eine monochrome Anzeigeeinrichtung vorhanden ist.

7. Pixel-Stromansteuervorrichtung nach Anspruch 2, wobei die Dünnfilmtransistoren Doppelgate-Transistoren in einer invertiert versetzten TFT-Struktur sind.

8. Pixel-Stromansteuervorrichtung nach Anspruch 2, wobei ein oberes Gate des Doppelgate geerdet ist.

9. Pixel-Stromansteuervorrichtung nach Anspruch 2, wobei ein oberes Gate des Doppelgate elektrisch an ein unteres Gate des Doppelgate gebunden ist.

Revendications

1. Circuit de commande de pixel pour une diode électroluminescente organique, « OLED », comportant une couche OLED pour émettre de la lumière, une ligne d'adresse, une ligne de données et une pluralité de transistors à film mince, dans lequel chaque transistor de la pluralité de transistors à film mince, « TFT », possède une double grille

pour commander la couche OLED, une grille supérieure de la double grille étant formée entre la source et le drain de chacun des transistors à film mince, afin de réduire au maximum la capacité parasite, dans lequel la pluralité de TFT forment un miroir de courant comprenant, soit :

A) un premier circuit incluant : un premier transistor à film mince (T1), une première borne du premier transistor (T1) étant connectée à la ligne de données et une grille du premier transistor (T1) étant connectée à la ligne d'adresse ; un deuxième transistor à film mince (T2), une première borne du deuxième transistor (T2) étant connectée à la ligne de données et une grille du deuxième transistor (T2) étant connectée à la ligne d'adresse ; un troisième transistor à film mince (T3), une deuxième borne du troisième transistor (T3) étant connectée à une deuxième borne du deuxième transistor (T2), une grille du troisième transistor (T3) étant connectée à une deuxième borne du premier transistor (T1), et une première borne du troisième transistor (T3) étant connectée à un potentiel de la masse ; et un quatrième transistor à film mince (T4), une grille du quatrième transistor (T4) étant connectée à la grille du troisième transistor (T3), le circuit de commande de pixel commandant un pixel par l'intermédiaire du quatrième transistor à film mince (T4), soit

B) un deuxième circuit incluant : un premier transistor à film mince (T2), une deuxième borne du premier transistor (T2) étant connectée à la ligne de données et une grille du premier transistor (T2) étant connectée à la ligne d'adresse ; un deuxième transistor à film mince (T1), une grille du deuxième transistor (T1) étant connectée à la ligne d'adresse, une première borne du deuxième transistor (T1) étant connectée au potentiel de la masse ; un troisième transistor à film mince (T3), une première borne et une grille du troisième transistor (T3) étant connectée à une première borne du premier transistor (T2) et une deuxième borne du troisième transistor (T3) étant connectée à une deuxième borne du deuxième transistor (T1) ; et un quatrième transistor à film mince (T4), une grille du quatrième transistor (T4) étant connectée à une grille du troisième transistor (T3), le circuit de commande de pixel commandant un pixel par l'intermédiaire du quatrième transistor à film mince (T4), soit

C) un troisième circuit incluant : un premier transistor à film mince (T1), une première borne du premier transistor (T1) étant connectée à la ligne de données et une grille du premier transistor (T1) étant connectée à la ligne d'adresse ; un deuxième transistor à film mince (T2), une première borne du deuxième transistor (T2) étant connectée à la ligne de données et une grille du deuxième transistor (T2) étant connectée à la ligne d'adresse ; un troisième transistor à film mince (T3), une deuxième borne du troisième transistor (T3) étant connectée à une deuxième borne du deuxième transistor (T2), une grille du troisième transistor (T3) étant connectée à une deuxième borne du premier transistor (T1), et une première borne du troisième transistor (T3) étant connectée au potentiel de la masse ; un cinquième transistor à film mince (T4), une deuxième borne et une grille du cinquième transistor (T4) étant connectées à un potentiel et une première borne du cinquième transistor (T4) étant connectée à la deuxième borne du deuxième transistor (T2) ; et un quatrième transistor à film mince (T5), une grille du quatrième transistor (T5) étant connectée à une grille du troisième transistor (T3), le circuit de commande de pixel commandant un pixel par l'intermédiaire du quatrième transistor à film mince (T5), soit

D) un quatrième circuit incluant : un premier transistor à film mince (T1), une deuxième borne du premier transistor (T1) étant connectée à la ligne de données et une grille du premier transistor (T1) étant connectée à la ligne d'adresse ; un deuxième transistor à film mince (T2), une première borne et une grille du deuxième transistor (T2) étant connectées à une première borne du premier transistor (T1) ; un troisième transistor à film mince (T3, T4, T5) ayant une première borne connectée à la borne de grille du deuxième transistor (T2), une grille du troisième transistor (T3, T4, T5) étant connectée à une autre ligne d'adresse, et à une deuxième borne ; et un quatrième transistor à film mince (T6, T7, T8), une grille du quatrième transistor (T6, T7, T8) étant connectée à la deuxième borne du troisième transistor (T3, T4, T5), le circuit de commande de pixel commandant un pixel par l'intermédiaire du quatrième transistor à film mince (T6, T7, T8) ; et

un condensateur (Cs), le condensateur (Cs) étant connecté entre la grille du quatrième transistor (T4, T5, T6, T7, T8) et un potentiel de la masse dans l'un quelconque des premier, deuxième, troisième et quatrième circuits, dans lequel la diode électroluminescente organique est connectée au quatrième transistor (T4, T5, T6, T7, T8).

2. Circuit de commande de pixel selon la revendication 1, dans lequel chacun des transistors à film mince est un transistor à film mince au a-Si:H.

3. Circuit de commande de pixel selon la revendication 1, dans lequel chacun des transistors à film mince est un transistor à film mince à base de silicium polycristallin.

4. Circuit de commande de pixel selon la revendication 3, dans lequel chacun des transistors à film mince est un transistor à film mince à canal p.

5. Circuit de commande de pixel selon l'une quelconque des revendications 1 à 4, dans lequel le quatrième circuit du circuit de commande de pixel est prévu pour commander un pixel couleur d'un dispositif d'affichage couleur.

6. Circuit de commande de pixel selon l'une quelconque des revendications 1 à 4, dans lequel le circuit de commande de pixel est prévu pour un dispositif d'affichage monochrome.

7. Circuit de commande de pixel selon la revendication 2, dans lequel les transistors à film mince sont des transistors à double grille ayant une structure de TFT en quinconce inversée.

8. Circuit de commande de pixel selon la revendication 2, dans lequel la grille supérieure de la double grille est reliée à la masse.

9. Circuit de commande de pixel selon la revendication 2, dans lequel la grille supérieure de la double grille est reliée électriquement à une grille inférieure de la double grille.

Fig. 1

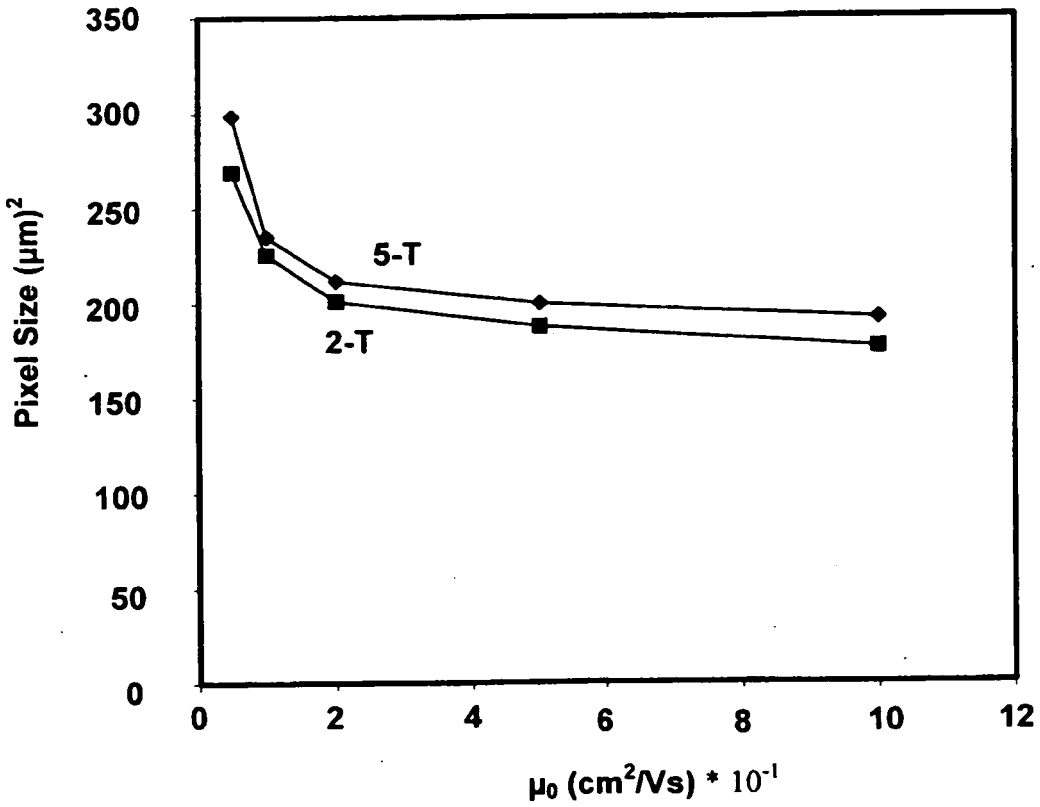

350
300
250
200
150
100
50
0
Pixel Size (µm)²
5-T
2-T
0
2
4
6
8
10
12
µ₀ (cm²/Vs) * 10⁻¹

Fig. 2

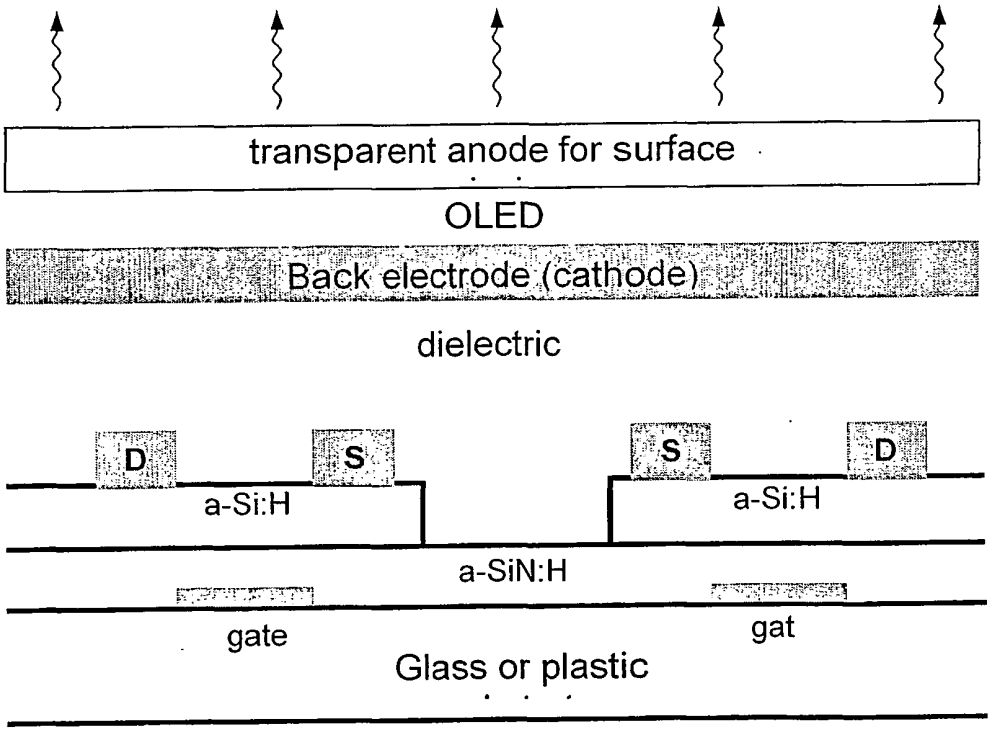
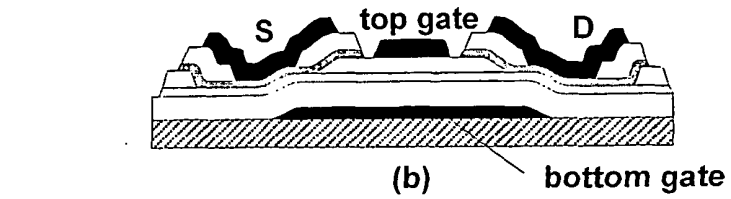

transparent anode for surface
OLED
Back electrode (cathode)
dielectric
D
S
S
D
a-Si:H
a-Si:H
a-SiN:H
gate
gat
Glass or plastic

Fig. 3



glass substrate a-SiN$_x$:H a-Si:H n$^+$µc-Si:H metal

Fig. 4

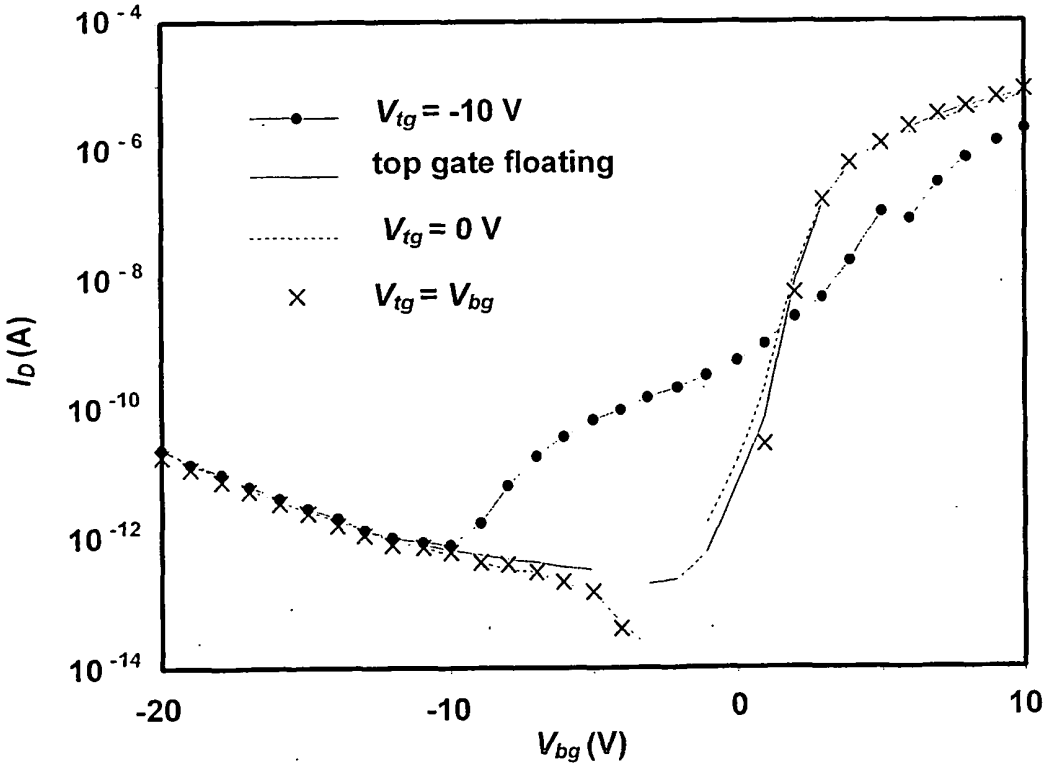


Fig. 5A

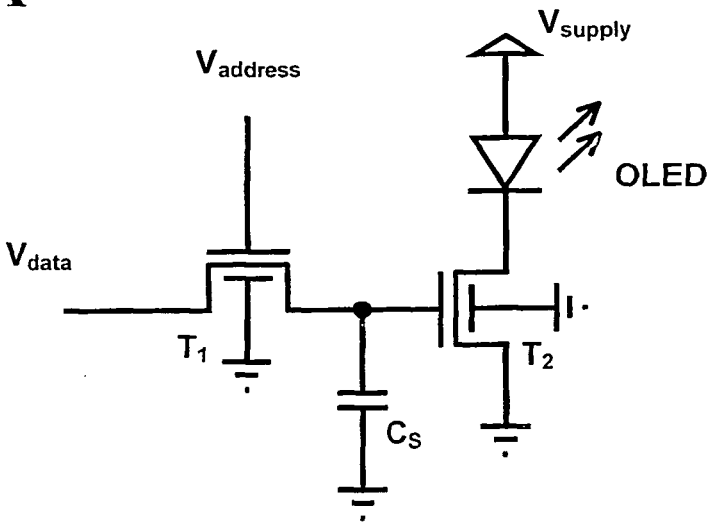


Fig. 5B

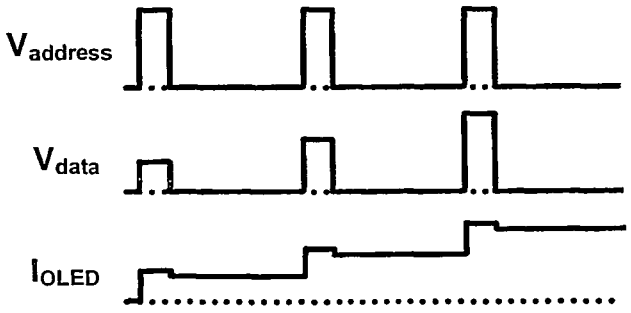


Fig. 6A

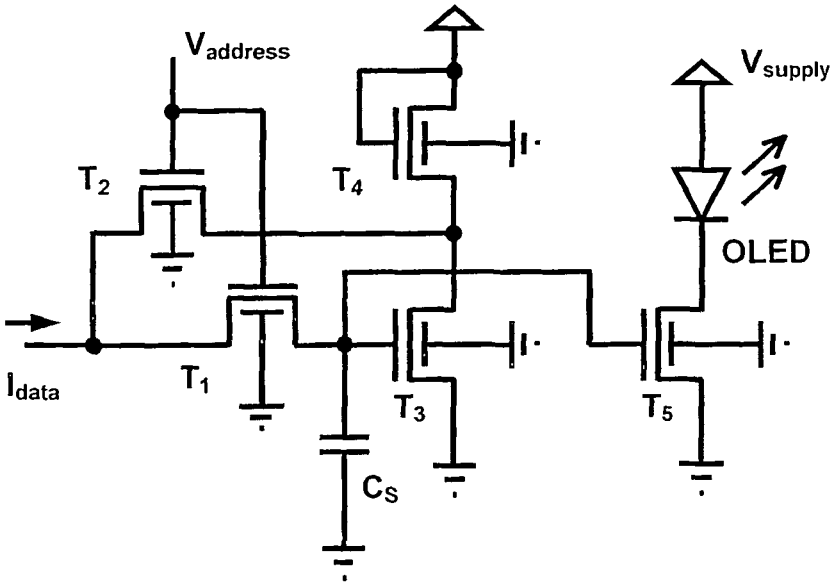

Vaddress
Vsupply
T2
T4
OLED
Idata
T1
T3
T5
CS

Fig. 6B

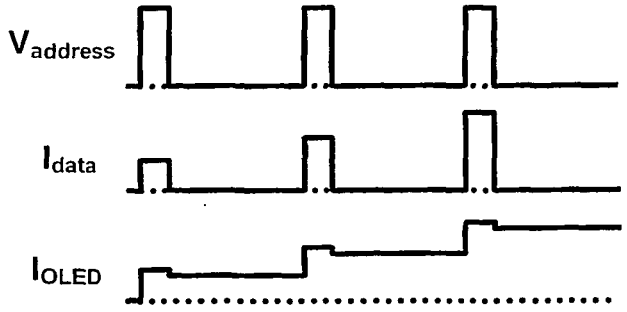

Vaddress
Idata
IOLED

Fig. 7

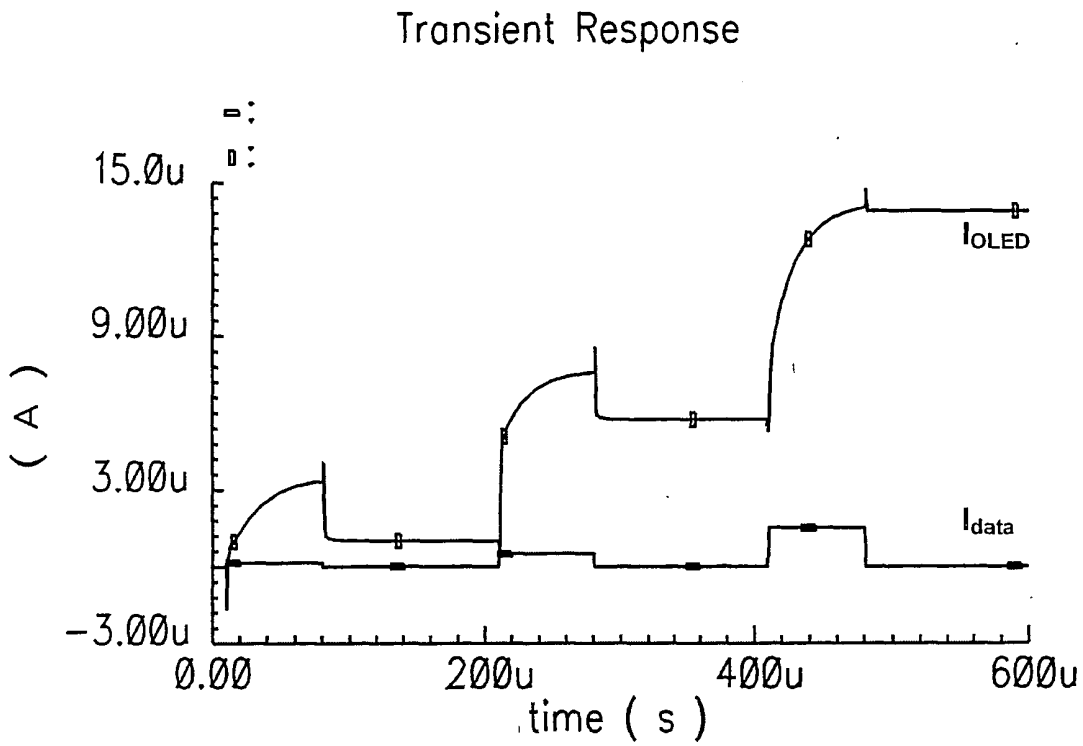

Transient Response
15.0u
9.00u
3.00u
-3.00u
(A)
0.00
200u
400u
600u
time (s)
IOLED
Idata

Fig. 8

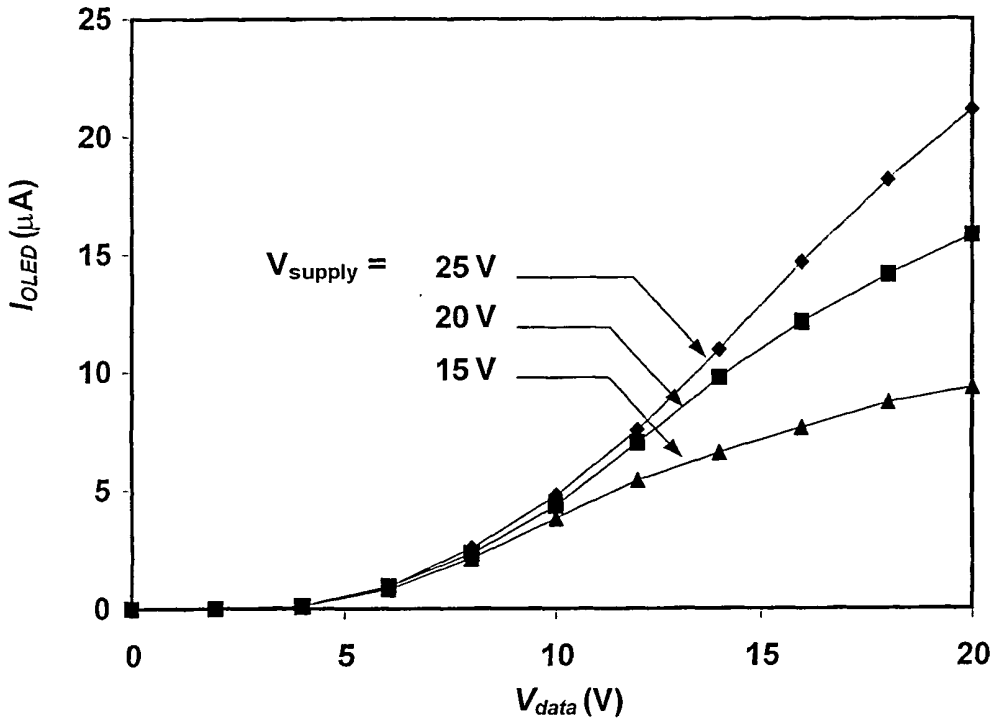


Fig. 9

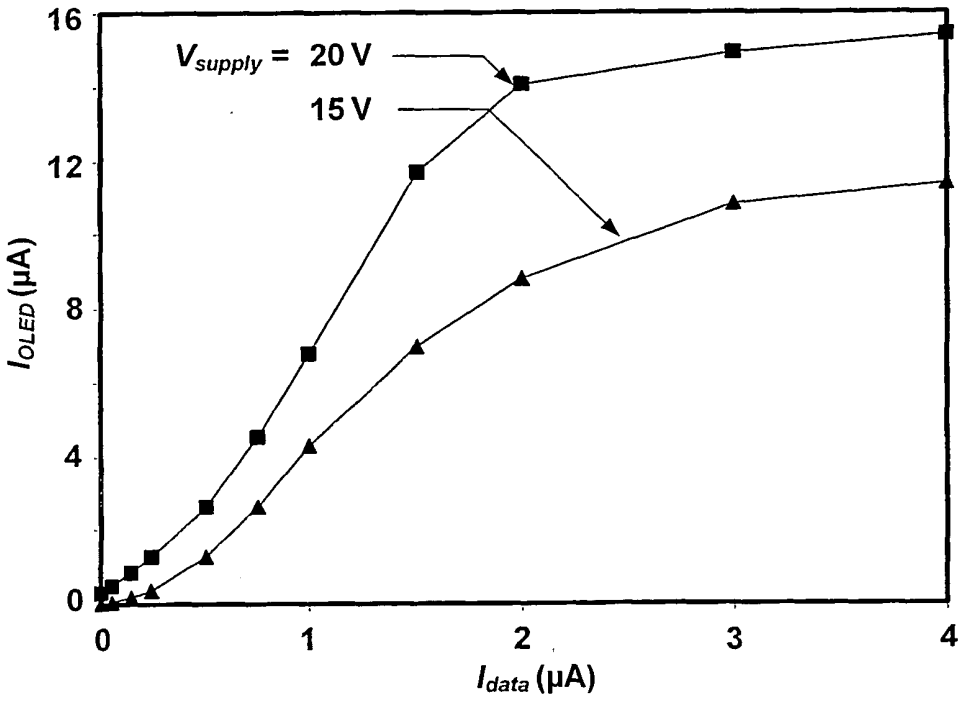


Fig. 10

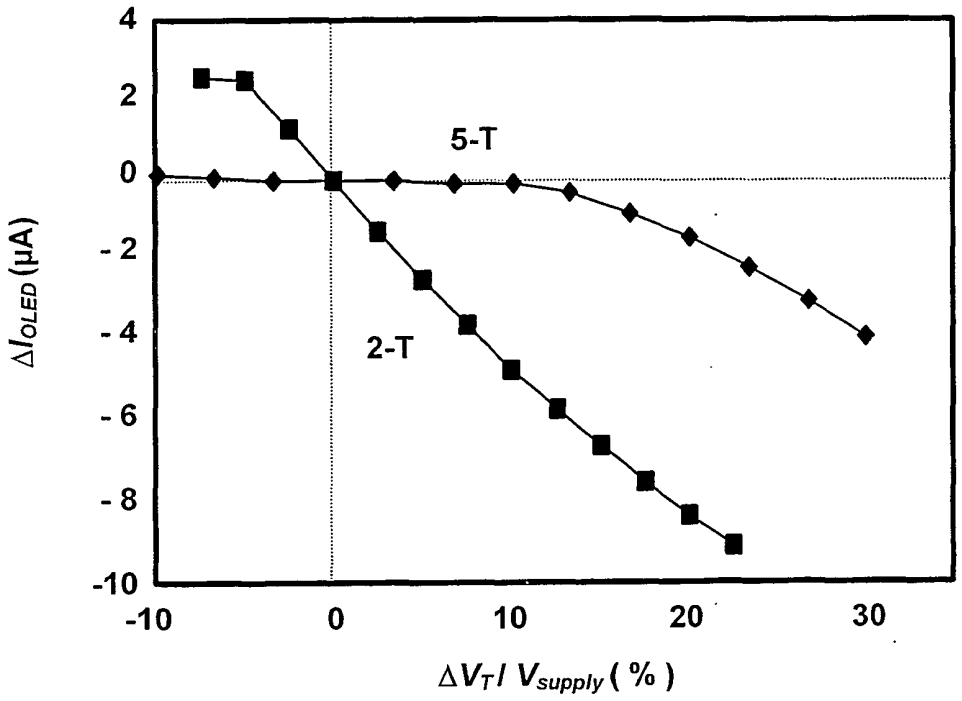


Fig. 11

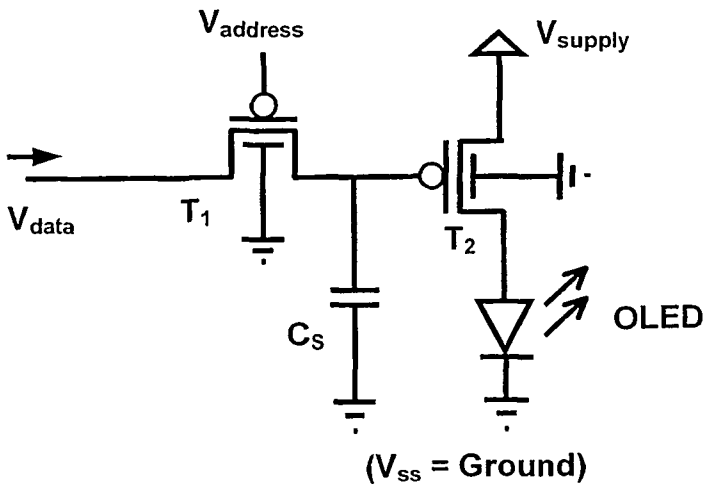
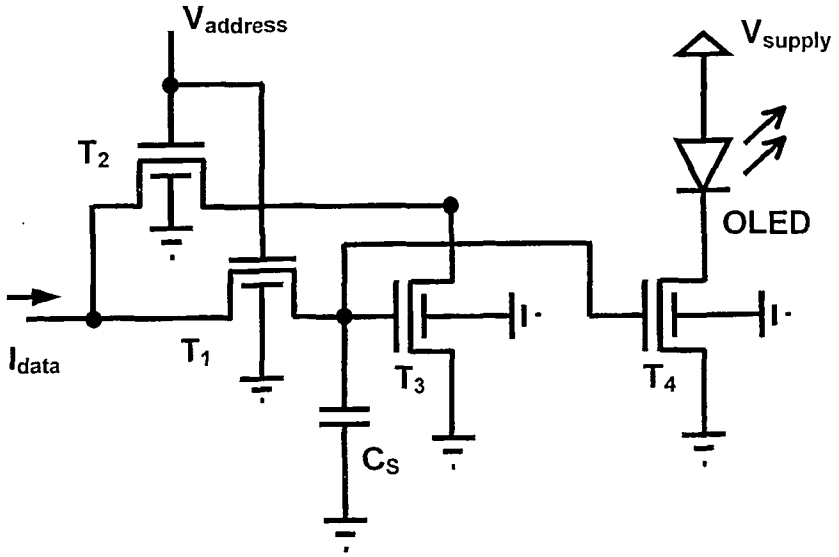

Vaddress
Vsupply
Vdata
T1
T2
CS
OLED
(Vss = Ground)

Fig. 12


Vaddress
Vsupply
T2
OLED
Idata
T1
T3
T4
CS

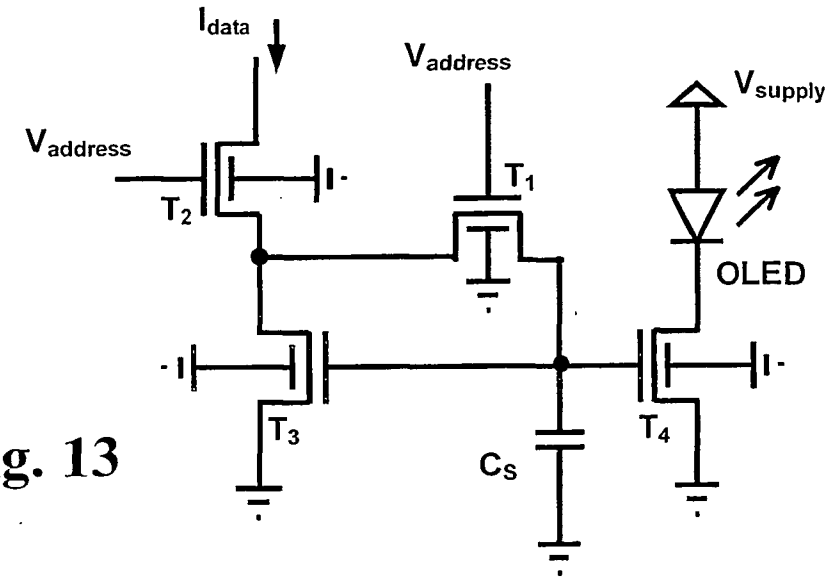

Idata
Vaddress
Vaddress
Vsupply
T2
T1
OLED
T3
T4
CS

Fig. 13

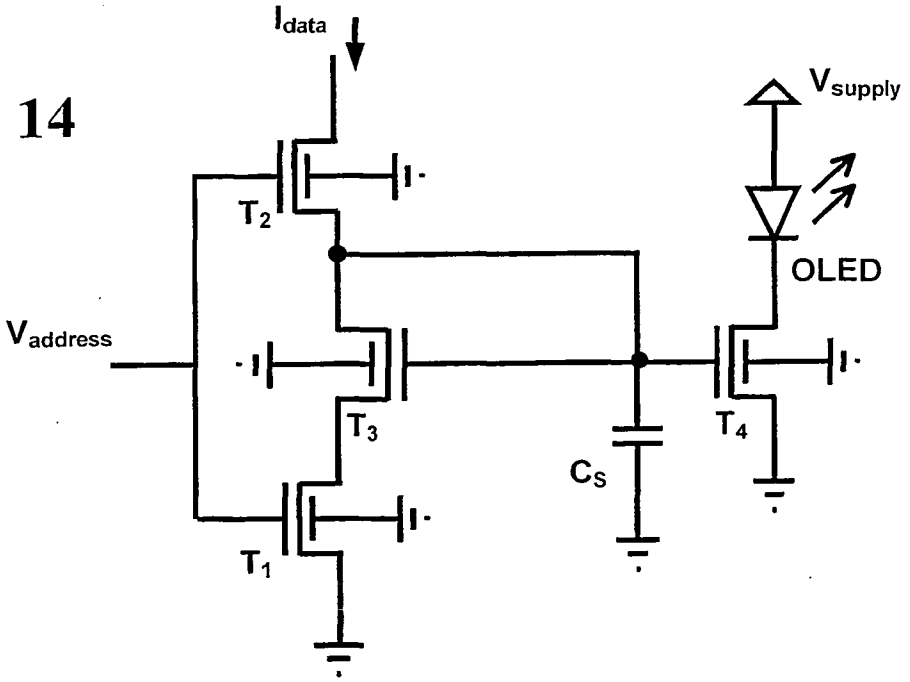

Idata
Vsupply
T2
OLED
Vaddress
T3
T4
CS
T1

Fig. 14

Fig. 15

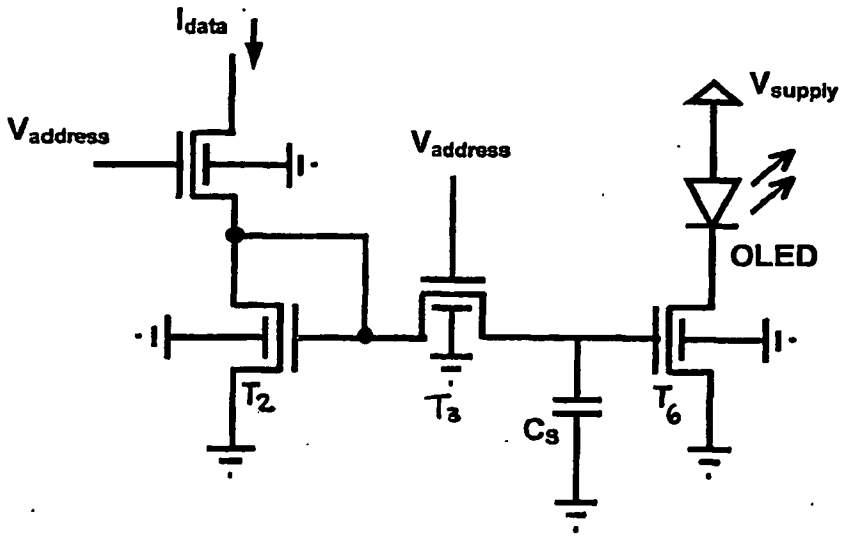
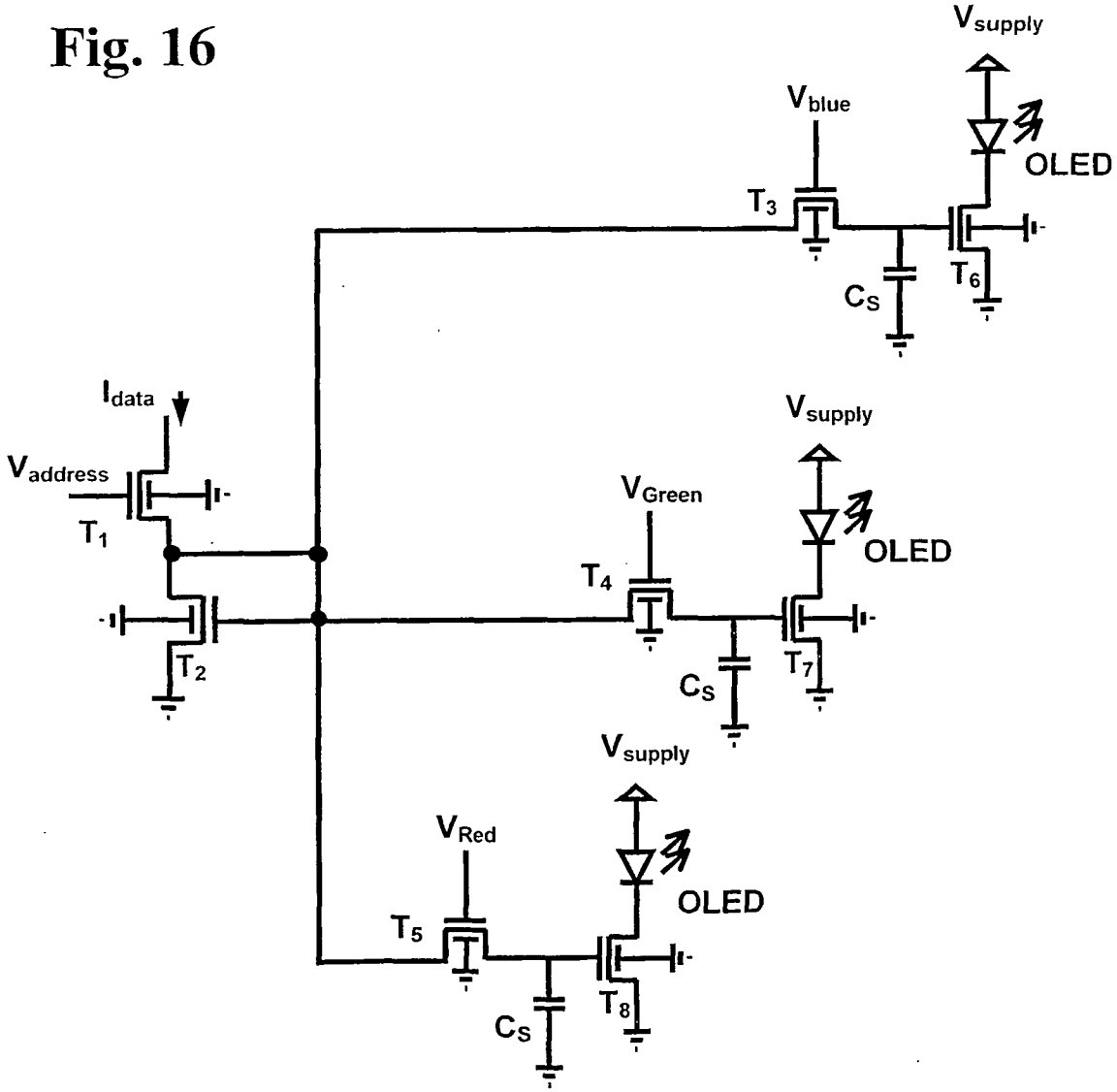


Fig. 16


Vsupply
Vblue
OLED
T3
T6
CS
Idata
Vaddress
T1
T2
Vsupply
VGreen
OLED
T4
T7
CS
Vsupply
VRed
OLED
T5
T8
CS

REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	用于有机发光二极管的像素驱动电路		
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其他公开文献	EP1488454A2		
外部链接	Espacenet		

摘要(译)

像素电流驱动器包括多个薄膜晶体管（TFT），每个薄膜晶体管具有双栅极并用于驱动OLED层。双栅极的顶栅形成在每个薄膜晶体管的源极和漏极之间，从而最小化寄生电容。顶栅接地或电连接到底栅。多个薄膜晶体管可以是以电压编程方式形成的两个薄膜晶体管，或者是以电流编程的ΔV> T T <。 OLED层连续且垂直地堆叠在多个薄膜晶体管上，以提供接近100％的孔径比。