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(72) Inventors:
• **Chung, Yun-mo**
Yongin-si, Gyeonggi-do (KR)
• **Lee, Tak-young**
Anyang-si, Gyeonggi-do (KR)
• **Yoon, Joosun**
Seoul (KR)

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(74) Representative: **Gulde & Partner**
Patent- und Rechtsanwaltskanzlei mbB
Wallstraße 58/59
10179 Berlin (DE)

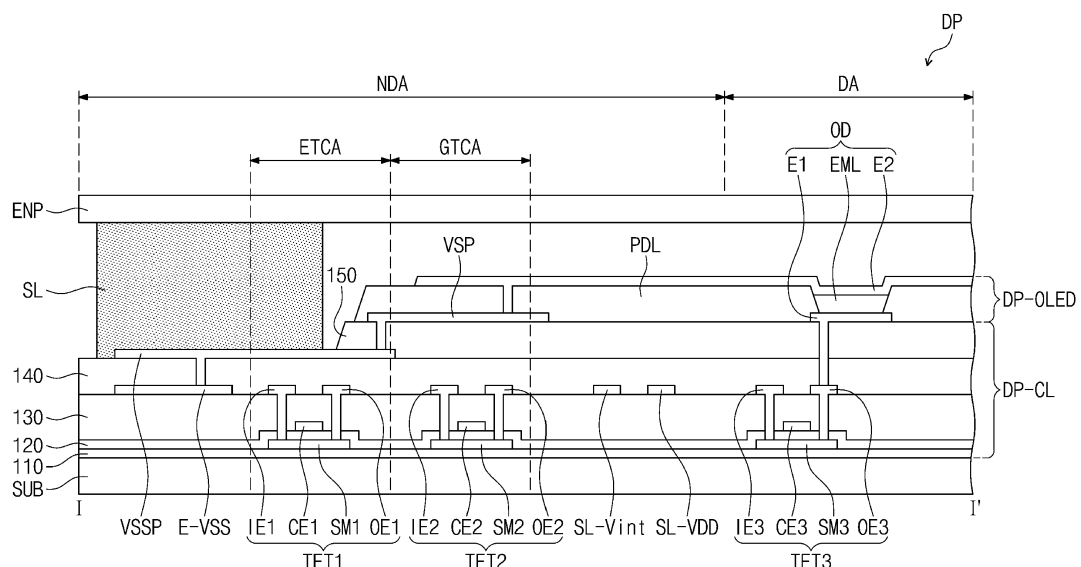
(71) Applicant: **Samsung Display Co., Ltd.**
Gyeonggi-Do (KR)

(54) **ORGANIC LIGHT EMITTING DISPLAY APPARATUS**

(57) An organic light emitting display apparatus includes a base layer (SUB), a circuit element layer (DP-CL), a display element layer (DP-OLED), an encapsulation layer (ENP), and a sealing member (SL). The circuit element layer (DP-CL) includes a power supply line (E-VSS) on the base layer and an auxiliary power supply pattern (VSSP) on and connected to the power supply line. The display element layer (DP-OLED) in-

cludes a first electrode (E1), a light emitting layer (EML), and a second electrode (E2), which are sequentially stacked on the circuit element layer. The second electrode (E2) is electrically connected to the auxiliary power supply pattern (VSSP). The sealing member (SL) is between the circuit element layer (DP-CL) and the encapsulation layer (ENP) to overlap with the auxiliary power supply pattern (VSSP) when viewed in a plan view.

FIG. 5



Description

BACKGROUND

1. Field

[0001] Aspects of embodiments of the present disclosure relate to an organic light emitting display apparatus.

2. Description of the Related Art

[0002] In recent years, an organic light emitting display apparatus has been employed in various display apparatuses since it has advantages, such as wide viewing angle, superior contrast, and fast response speed.

[0003] The organic light emitting display apparatus includes an organic light emitting diode to emit a light, and the organic light emitting diode is vulnerable to moisture and oxygen. For the organic light emitting diode, a sealing member is disposed on an exterior of the organic light emitting display apparatus to seal the organic light emitting diode.

[0004] The sealing member may be formed by placing a curable material between a lower substrate and an upper substrate and curing the curable material; however, a defect may occur in circuit elements around the sealing member during the curing process.

SUMMARY

[0005] According to an aspect of embodiments of the present disclosure, an organic light emitting display apparatus is capable of reducing a non-display area of a display panel.

[0006] According to another aspect of embodiments of the present disclosure, an organic light emitting display apparatus is capable of preventing or substantially preventing circuit elements overlapped with a sealing member from becoming defective during a curing process for the sealing member.

[0007] According to one or more embodiments of the inventive concept, an organic light emitting display apparatus includes a base layer, a circuit element layer, a display element layer, an encapsulation layer, and a sealing member.

[0008] In one or more embodiments, the base layer includes a display area and a non-display area adjacent to the display area.

[0009] In one or more embodiments, the circuit element layer includes a power supply line and an auxiliary power supply pattern. The power supply line is on the base layer to receive a common voltage. The auxiliary power supply pattern is on the power supply line, overlapped with the power supply line, and connected to the power supply line.

[0010] In one or more embodiments, the display element layer includes a first electrode, a light emitting layer, and a second electrode. The first electrode is on the circuit element layer. The light emitting layer is on the first electrode. The second electrode is on the light emitting layer and electrically connected to the auxiliary power supply pattern.

The light emitting layer is on the first electrode. The second electrode is on the light emitting layer and electrically connected to the auxiliary power supply pattern.

[0011] In one or more embodiments, the encapsulation layer is on the display element layer.

[0012] In one or more embodiments, the sealing member is between the circuit element layer and the encapsulation layer and disposed in the non-display area to overlap with the auxiliary power supply pattern when viewed in a plan view.

[0013] In one or more embodiments, the auxiliary power supply pattern may contact the sealing member.

[0014] In one or more embodiments, the display element layer may further include an auxiliary pattern in the non-display area, located on a same layer as the first electrode, and connected to the auxiliary power supply pattern.

[0015] In one or more embodiments, the circuit element layer may further include a first intermediate insulating layer and a second intermediate insulating layer. The first intermediate insulating layer may be between the power supply line and the auxiliary power supply pattern and include a contact hole through which the power supply line is connected to the auxiliary power supply pattern. The second intermediate insulating layer may be between the auxiliary power supply pattern and the auxiliary pattern and includes a contact hole through which the auxiliary power supply pattern is connected to the auxiliary pattern.

[0016] In one or more embodiments, the display element layer may further include a pixel definition layer between the auxiliary pattern and the second electrode, the pixel definition layer may include a contact hole through which the auxiliary pattern is connected to the second electrode, and an opening in which the light emitting layer is located.

[0017] In one or more embodiments, the circuit element layer may further include a switching transistor, a driving transistor, and a light emitting control transistor.

[0018] In one or more embodiments, the switching transistor may include a control electrode to receive a scan signal, an input electrode to receive a data signal, and an output electrode.

[0019] In one or more embodiments, the driving transistor may include an input electrode connected to the output electrode of the switching transistor.

[0020] In one or more embodiments, the light emitting control transistor may include a control electrode to receive a light emitting signal and may be connected between a voltage line and the driving transistor or between the driving transistor and the first electrode.

[0021] In one or more embodiments, the circuit element layer may further include a light emitting line driving circuit and a gate driving circuit. The light emitting line driving circuit may apply the light emitting signal to the light emitting control transistor. The gate driving circuit may apply the scan signal to the switching transistor. The

light emitting line driving circuit may be farther from the display area than the gate driving circuit when viewed in a plan view.

[0022] In one or more embodiments, the auxiliary power supply pattern may overlap with the light emitting line driving circuit.

[0023] In one or more embodiments, the auxiliary power supply pattern may include a material having a melting point higher than a melting point of the power supply line.

[0024] In one or more embodiments, the circuit element layer may further include a voltage line receiving a source voltage greater than the common voltage and an auxiliary voltage pattern above the voltage line and connected to the voltage line.

[0025] In one or more embodiments, the auxiliary voltage pattern may be on a same layer as the auxiliary power supply pattern and overlap with the sealing member.

[0026] In one or more embodiments, the auxiliary voltage pattern may contact the sealing member.

[0027] In one or more embodiments, the circuit element layer may further include a pad part in the non-display area. The auxiliary voltage pattern may be between the pad part and the display area when viewed in a plan view.

[0028] In one or more embodiments, the circuit element layer may further include a data line and a demultiplexer. The demultiplexer may be connected between the pad part and the data line. The auxiliary voltage pattern may cover the demultiplexer when viewed in a plan view.

[0029] In one or more embodiments, the circuit element layer may further include an anti-static pattern in the non-display area. The auxiliary voltage pattern may cover the anti-static pattern when viewed in a plan view.

[0030] In one or more embodiments, the circuit element layer may further include an insulating layer under the auxiliary power supply pattern. The auxiliary power supply pattern may comprise a hole defined there-through, and the sealing member may contact the insulating layer or the base layer through the hole.

[0031] According to one or more embodiments of the inventive concept, an organic light emitting display apparatus includes a base layer, a power supply line, a voltage supply line, an auxiliary power supply pattern, an auxiliary voltage pattern, an organic light emitting diode, an encapsulation layer, and a sealing member.

[0032] In one or more embodiments, the power supply line is on the base layer to receive a common voltage.

[0033] In one or more embodiments, the voltage supply line is on the base layer to receive source voltage greater than the common voltage.

[0034] In one or more embodiments, the auxiliary power supply pattern is on the power supply line, overlapped with the power supply line, and connected to the power supply line.

[0035] In one or more embodiments, the auxiliary voltage pattern is above the voltage supply line, overlapped with the voltage supply line, and connected to the voltage

supply line.

[0036] In one or more embodiments, the organic light emitting diode is above the auxiliary power supply pattern and the auxiliary voltage pattern.

5 **[0037]** In one or more embodiments, the encapsulation layer is on the organic light emitting diode.

[0038] In one or more embodiments, the sealing member is between the base layer and the encapsulation layer to seal the organic light emitting diode and overlapped with the auxiliary power supply pattern and the auxiliary voltage pattern.

10 **[0039]** In one or more embodiments, the auxiliary power supply pattern may be on a same layer as the auxiliary voltage pattern.

15 **[0040]** In one or more embodiments, each of the auxiliary power supply pattern and the auxiliary voltage pattern may include material having a melting point higher than a melting point of each of the power supply line and the voltage supply line.

20 **[0041]** In one or more embodiments, each of the auxiliary power supply pattern and the auxiliary voltage pattern may contact the sealing member.

[0042] According to one or more embodiments of the inventive concept, an organic light emitting display apparatus includes a base layer, a transistor, an organic light emitting diode, a power supply line, an auxiliary power supply pattern, an encapsulation layer, and a sealing member,

25 **[0043]** In one or more embodiments, the transistor is on the base layer and includes a control electrode, an input electrode, and an output electrode.

[0044] In one or more embodiments, the organic light emitting diode is above the transistor and connected to the transistor.

30 **[0045]** In one or more embodiments, the power supply line is on the base layer to receive a constant voltage, and is on a same layer as one of the control electrode, the input electrode, and the output electrode of the transistor.

35 **[0046]** In one or more embodiments, the auxiliary power supply pattern is above the power supply line and the transistor, under the organic light emitting diode, and connected to the power supply line.

40 **[0047]** In one or more embodiments, the encapsulation layer is on the organic light emitting diode.

[0048] In one or more embodiments, the sealing member is between the base layer and the encapsulation layer to seal the organic light emitting diode and overlapped with the auxiliary power supply pattern and the auxiliary voltage pattern.

45 **[0049]** According to an aspect of embodiments of the present disclosure, the non-display area of the display panel may be reduced.

50 **[0050]** In addition, circuit elements overlapped with the sealing member may be prevented or substantially prevented from becoming defective when the sealing member is cured.

BRIEF DESCRIPTION OF THE DRAWINGS

[0051] The above and other aspects of the present disclosure will become readily apparent by reference to the following detailed description when considered in conjunction with the accompanying drawings, wherein:

FIG. 1 is a perspective view showing a display apparatus according to an exemplary embodiment of the present disclosure;

FIG. 2 is a cross-sectional view showing a display module of FIG. 1;

FIG. 3 is a plan view showing a display panel according to an exemplary embodiment of the present disclosure;

FIG. 4 is an equivalent circuit diagram showing a pixel according to an exemplary embodiment of the present disclosure;

FIG. 5 is a cross-sectional view taken along the line I-I' of FIG. 3;

FIG. 6 is a view showing a region "AA" of FIG. 3;

FIG. 7 is a cross-sectional view taken along the line II-II' of FIG. 3;

FIG. 8 is a cross-sectional view showing a portion of a display panel of a display apparatus according to another exemplary embodiment of the present disclosure;

FIG. 9 is a circuit diagram showing a portion of a display panel of a display apparatus according to another exemplary embodiment of the present disclosure; and

FIG. 10 is a cross-sectional view showing the portion of the display panel according to the exemplary embodiment of FIG. 9.

DETAILED DESCRIPTION

[0052] Herein, some example embodiments of the present invention will be explained in further detail with reference to the accompanying drawings. In the following description, it is to be understood that when an element, such as a region, layer, or portion, is referred to as being "on," "connected to," or "coupled to" another element or layer, it may be directly on, connected, or coupled to the other element or layer or one or more intervening elements or layers may be present.

[0053] Like numerals refer to like elements throughout. In the drawings, the thicknesses and sizes of elements may be exaggerated for clarity. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0054] The use of the terms "first," "second," etc. does not denote any order or importance, but, rather, the terms "first," "second," etc. are used to distinguish one element from another. Thus, a first element, component, region, layer, or section discussed below could be termed a second element, component, region, layer, or section without departing from the teachings of the present disclosure.

It is to be understood that the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise.

[0055] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures.

[0056] It is to be further understood that the terms "includes" and/or "including," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0057] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which example embodiments of the inventive concept belong. It is to be further understood that terms, such as those defined in commonly-used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0058] FIG. 1 is a perspective view showing a display apparatus 1000 according to an exemplary embodiment of the present disclosure; and FIG. 2 is a cross-sectional view showing a display module DM of FIG. 1.

[0059] The display apparatus 1000 may be applied to a large-sized electronic device, such as a television set and a monitor, and a small and medium-sized electronic device, such as a mobile phone, a tablet computer, a car navigation unit, a game unit, and a smart watch, for example.

[0060] Referring to FIG. 1, the display apparatus 1000 according to an embodiment includes a display module DM, a window member WM, and a housing member HM.

[0061] A display surface IS, through which an image IM of the display module DM is displayed, is substantially parallel to a surface defined by a first direction axis DR1 and a second direction axis DR2. A third direction axis DR3 indicates a normal line direction of the display surface IS, i.e., a thickness direction of the display module DM. Front (or upper) and rear (or lower) surfaces of each member are distinguished from each other by the third direction axis DR3. However, directions indicated by the first, second, and third direction axes DR1, DR2, and DR3 are relative to each other, and, thus, the directions indicated by the first, second, and third direction axes DR1, DR2, and DR3 may be changed to other directions. Herein, first, second, and third directions, which are respectively indicated by the first, second, and third direction axes DR1, DR2, and DR3, will be assigned with the same reference numerals as those of the first, second, and third direction axes DR1, DR2, and DR3.

[0062] In an embodiment, the display module DM may be a flat and rigid display device; however, the display

module DM is not limited to the flat and rigid display device. That is, the display module DM may be a flexible display module.

[0063] As shown in FIG. 1, the display module DM includes a display area DM-DA through which the image IM is displayed, and a non-display area DM-NDA disposed adjacent to the display area DM-DA. The image IM is not displayed through the non-display area DM-NDA. FIG. 1 shows a vase as a representative example of the image IM. As an example, the display area DM-DA may have a quadrangular shape, and the non-display area DM-NDA surrounds the display area DM-DA, but the present disclosure is not limited thereto or thereby. That is, the shape of the display area DM-DA and the shape of the non-display area DM-NDA may be designed or varied relative to each other.

[0064] The window member WM is disposed on the display module DM. The window member WM protects the display module DM. The window member WM is coupled to the housing member HM to define an internal space therebetween. The window member WM and the housing member HM define an exterior of the display apparatus 1000.

[0065] The window member WM is divided into a transmission area TA and a bezel area BA when viewed in a plan view. The transmission area TA transmits most of light incident thereto. The transmission area TA has an optical transparency. In an embodiment, the transmission area TA has a light transmittance of about 90% or more. The transmission area TA corresponds to the display area DM-DA of the display module DM.

[0066] The bezel area BA blocks most of light incident thereto. In an embodiment, the bezel area BA ensures or provides that components arranged under the window member WM are not visible from an outside of the window member WM. In addition, the bezel area BA reduces a reflection of the light incident thereto from the outside of the window member WM. The bezel area BA corresponds to the non-display area DM-NDA of the display module DM.

[0067] The bezel area BA is adjacent to the transmission area TA. A shape of the transmission area TA in a plan view is defined by the bezel area BA.

[0068] The housing member HM provides an internal space (e.g., a predetermined internal space). The display module DM is accommodated in the internal space. In addition to the display module DM, various electronic parts, e.g., a power supply, a storage device, a sound input/output module, and a camera, may be arranged in the internal space of the housing member HM.

[0069] FIG. 2 is a cross-sectional view showing the display module DM according to an exemplary embodiment of the present disclosure. FIG. 2 shows a cross-section defined by the first direction axis DR1 and the third direction axis DR3.

[0070] As shown in FIG. 2, in an embodiment, the display module DM includes a display panel DP and a touch sensing unit TS (or "touch sensing layer"). Although not

shown separately, the display module DM according to an exemplary embodiment of the present disclosure may further include a protective member disposed on a lower surface of the display panel DP.

[0071] The display panel DP may be a light emitting type display panel, but is not particularly limited. For instance, the display panel DP may be an organic light emitting display panel or a quantum-dot light emitting display panel. A light emitting layer of the organic light emitting display panel includes an organic light emitting material. A light emitting layer of the quantum-dot light emitting display panel includes a quantum dot or a quantum rod. Herein, the organic light emitting display panel will be described as the display panel DP.

[0072] The display panel DP includes a base layer SUB, a circuit element layer DP-CL, a display element layer DP-OLED, and an encapsulation layer ENP. The circuit element layer DP-CL, the display element layer DP-OLED, and the encapsulation layer ENP are disposed on the base layer SUB. Although not shown separately, the display panel DP may further include functional layers, such as a refractive index control layer.

[0073] In an embodiment, the base layer SUB may include at least one plastic film. The base layer SUB may be a flexible substrate and may include a plastic substrate, a glass substrate, a metal substrate, or an organic-inorganic hybrid material substrate. The display area DM-DA and the non-display area DM-NDA described with reference to FIG. 1 may be defined in the base layer SUB.

[0074] The circuit element layer DP-CL includes at least one intermediate insulating layer and a circuit element. In an embodiment, the intermediate insulating layer includes at least one intermediate inorganic layer and at least one intermediate organic layer. The circuit element includes signal lines, a driving circuit for the pixel, and the like. These will be described in further detail later.

[0075] The display element layer DP-OLED includes at least organic light emitting diodes. The display element layer DP-OLED may further include an organic layer, such as a pixel definition layer.

[0076] The encapsulation layer ENP is disposed on the display element layer DP-OLED and encapsulates the display element layer DP-OLED.

[0077] The display panel DP includes a sealing member SL disposed between the circuit element layer DP-CL and the encapsulation layer ENP. The sealing member SL is disposed between the circuit element layer DP-CL and the encapsulation layer ENP to adhere the circuit element layer DP-CL and the encapsulation layer ENP. The sealing member SL blocks the display element layer DP-OLED from external moisture and oxygen together with the circuit element layer DP-CL and the encapsulation layer ENP.

[0078] The touch sensing unit TS obtains coordinate information of an external input. The touch sensing unit TS may be disposed on the encapsulation layer ENP. The touch sensing unit TS may be adhered to the encapsulation layer ENP by an adhesive layer and may be

formed on the encapsulation layer ENP through a thin film process.

[0079] The touch sensing unit TS may sense the external input, for example, using an electrostatic capacitive method. However, the operation method of the touch sensing unit TS is not particularly limited, and the touch sensing unit TS according to an exemplary embodiment of the present disclosure may sense the external input using an electromagnetic induction method or a pressure sensing method.

[0080] FIG. 3 is a plan view showing the display panel DP according to an exemplary embodiment of the present disclosure.

[0081] Referring to FIG. 3, the display panel DP includes a display area DA and a non-display area NDA when viewed in a plan view. In the present exemplary embodiment, the non-display area NDA may be defined along an edge of the display area DA. The display area DA and the non-display area NDA of the display panel DP respectively correspond to the display area DM-DA and the non-display area DM-NDA of the display module DM shown in FIG. 1. However, the display area DA and the non-display area NDA of the display panel DP need not necessarily be the same as the display area DM-DA and the non-display area DM-NDA of the display module DM and may be changed depending on structure and design of the display panel DP.

[0082] The display panel DP includes a plurality of pixels PX. The pixels PX are arranged in the display area DA. Each of the pixels PX includes an organic light emitting diode and a pixel driving circuit connected to the organic light emitting diode.

[0083] The display panel DP may include a plurality of signal lines and a pad part PD. The signal lines may include scan lines GL, data lines DL, light emitting lines EL, a control signal line SL-D, an initialization line SL-Vint, a voltage line SL-VDD, and a power supply line E-VSS. The signal lines and the pad part PD may be included in the circuit element layer DP-CL shown in FIG. 2.

[0084] Some lines of the scan lines GL, the data lines DL, the light emitting lines EL, the control signal line SL-D, the initialization line SL-Vint, the voltage line SL-VDD, and the power supply line E-VSS are arranged on a same layer, and the other lines are arranged on a different layer.

[0085] Each of the scan lines GL is connected to a corresponding pixel PX among the pixels PX, and each of the data lines DL is connected to a corresponding pixel PX among the pixels PX. In an embodiment, each of the light emitting lines EL is arranged parallel to a corresponding scan line among the scan lines GL. The control signal line SL-D applies control signals to a pixel driving circuit GDC. The initialization line SL-Vint applies an initialization voltage to the pixels PX. The voltage line SL-VDD is connected to the pixels PX and applies a source voltage (e.g., a first voltage) to the pixels PX. The voltage line SL-VDD includes a plurality of lines extending in the first direction DR1 and a plurality of lines extending in the second direction DR2. In an embodiment, the power supply

line E-VSS is disposed in the non-display area NDA to surround three side surfaces of the display area DA. The power supply line E-VSS applies a common voltage (e.g., a second voltage) to the pixels PX. The common voltage may have a voltage level lower than the source voltage.

[0086] The display panel DP may further include the pixel driving circuit GDC. The pixel driving circuit GDC is disposed at a side portion of the non-display area NDA and connected to the scan lines GL and the light emitting lines EL.

[0087] The pixel driving circuit GDC may include a gate driving circuit (not shown) and a light emitting line driving circuit (not shown). The gate driving circuit (not shown) may apply signals to the scan lines GL, and the light emitting line driving circuit (not shown) may apply signals to the light emitting lines EL.

[0088] The pixel driving circuit GDC may be included in the circuit element layer DP-CL shown in FIG. 2. In an embodiment, the pixel driving circuit GDC may include a plurality of thin film transistors formed through a same process as the driving circuit of the pixels PX, for example, a low temperature polycrystalline silicon (LTPS) process or a low temperature polycrystalline oxide (LTPO) process.

[0089] The pad part PD includes a plurality of pads. Some pads of the pad part PD are connected to ends of the data lines DL, the control signal line SL-D, the initialization line SL-Vint, and the voltage line SL-VDD, and the other pads of the pad part PD are connected to touch signal lines of the touch sensing unit TS.

[0090] Although not shown in figures, the display panel DP may further include a bank (not shown) disposed between the display area DA and the pad part PD. In addition, the display panel DP may further include a dam portion (not shown) surrounding the edge of the display area DA. When a specified layer is formed by a printing method during manufacture of the display panel DP, the bank and the dam portion may prevent or substantially prevent the specified layer from overflowing the bank or the dam portion.

[0091] When viewed in a plan view, the sealing member SL is disposed in the non-display area NDA of the display panel DP to surround the display area DA. In an embodiment, the sealing member SL is disposed to overlap with the power supply line E-VSS. In an embodiment, the sealing member SL may overlap with a portion of the pixel driving circuit GDC.

[0092] The display panel DP further includes an auxiliary power supply pattern VSSP and an auxiliary voltage pattern VDDP.

[0093] In an embodiment, when viewed in a plan view, the auxiliary power supply pattern VSSP is electrically connected to the power supply line E-VSS and overlaps with the sealing member SL.

[0094] In an embodiment, when viewed in a plan view, the auxiliary voltage pattern VDDP is electrically connected to the voltage line SL-VDD and overlaps with the seal-

ing member SL. The auxiliary voltage pattern VDDP may be disposed between the pad part PD and the display area DA when viewed in a plan view.

[0095] FIG. 4 is an equivalent circuit diagram showing a pixel PX of FIG. 3.

[0096] The pixel PX according to an exemplary embodiment of the present disclosure may include a plurality of thin film transistors T1 to T7, a storage capacitor Cst, and an organic light emitting diode OLED.

[0097] In an embodiment, the thin film transistors T1 to T7 include a driving transistor T1, a switching transistor T2, a compensating transistor T3, an initializing transistor T4, a first light emitting control transistor T5, a second light emitting control transistor T6, and a bypass transistor T7.

[0098] The pixel PX includes a first scan line 14 transmitting an n-th scan signal Sn to the switching transistor T2 and the compensating transistor T3, a second scan line 24 transmitting an (n-1)th scan signal Sn-1 to the initializing transistor T4, a third scan line 34 transmitting an (n+1)th scan signal Sn+1 to the bypass transistor T7, a light emitting line 15 transmitting a light emitting control signal En to the first light emitting control transistor T5 and the second light emitting control transistor T6, a data line 16 transmitting a data signal Dm, a voltage line 26 transmitting the source voltage ELVDD, and an initializing line 22 transmitting an initializing voltage Vint to initialize the driving transistor T1.

[0099] A gate electrode G1 of the driving transistor T1 is connected to a first electrode C1 of the storage capacitor Cst. A source electrode S1 of the driving transistor T1 is connected to the voltage line 26 via the first light emitting control transistor T5. A drain electrode D1 of the driving transistor T1 is electrically connected to an anode of the organic light emitting diode OLED via the second light emitting control transistor T6. The driving transistor T1 receives the data signal Dm in response to a switching operation of the switching transistor T2 to provide the organic light emitting diode OLED with a driving current Id.

[0100] A gate electrode G2 of the switching transistor T2 is connected to the first scan line 14. A source electrode S2 of the switching transistor T2 is connected to the data line 16. A drain electrode D2 of the switching transistor T2 is connected to the source electrode S1 of the driving transistor T1 and connected to the voltage line 26 via the first light emitting control transistor T5. The switching transistor T2 is turned on in response to the n-th scan signal Sn applied thereto through the first scan line 14 to perform the switching operation that transmits the data signal Dm applied to the data line 16 to the source electrode S1 of the driving transistor T1.

[0101] A gate electrode G3 of the compensating transistor T3 is connected to the first scan line 14. A source electrode S3 of the compensating transistor T3 is connected to the drain electrode D1 of the driving transistor T1 and connected to the anode of the organic light emitting diode OLED via the second light emitting control transistor T6.

A drain electrode D3 of the compensating transistor T3 is connected to the first electrode C1 of the storage capacitor Cst, a source electrode S4 of the initializing transistor T4, and the gate electrode G1 of the driving transistor T1. The compensating transistor T3 is turned on in response to the n-th scan signal Sn applied thereto through the first scan line 14 to connect the gate electrode G1 of the driving transistor T1 to the drain electrode D1 of the driving transistor T1, and, thus, the driving transistor T1 is connected in a diode configuration.

[0102] A gate electrode G4 of the initializing transistor T4 is connected to the second scan line 24. A drain electrode D4 of the initializing transistor T4 is connected to the initializing line 22. The source electrode S4 of the initializing transistor T4 is connected to the first electrode C1 of the storage capacitor Cst, the drain electrode D3 of the compensating transistor T3, and the gate electrode G1 of the driving transistor T1. The initializing transistor T4 is turned on in response to the (n-1)th scan signal Sn-1 applied thereto through the second scan line 24 and applies the initializing voltage Vint to the gate electrode G1 of the driving transistor T1 to initialize a voltage of the gate electrode G1 of the driving transistor T1.

[0103] A gate electrode G5 of the first light emitting control transistor T5 is connected to the light emitting line 15. The first light emitting control transistor T5 is connected between the voltage line 26 and the driving transistor T1. A source electrode S5 of the first light emitting control transistor T5 is connected to the voltage line 26. A drain electrode D5 of the first light emitting control transistor T5 is connected to the source electrode S1 of the driving transistor T1 and the drain electrode D2 of the switching transistor T2. When the light emitting control signal En is applied to the gate electrode G5 of the first light emitting control transistor T5, the first light emitting control transistor T5 is turned on, and, thus, the driving current Id flows through the organic light emitting diode OLED. The first light emitting control transistor T5 may determine a timing at which the driving current Id flows through the organic light emitting diode OLED.

[0104] A gate electrode G6 of the second light emitting control transistor T6 is connected to the light emitting line 15. The second light emitting control transistor T6 is connected between the driving transistor T1 and the organic light emitting diode OLED. A source electrode S6 of the second light emitting control transistor T6 is connected to the drain electrode D1 of the driving transistor T1 and the source electrode S3 of the compensating transistor T3. A drain electrode D6 of the second light emitting control transistor T6 is electrically connected to the anode of the organic light emitting diode OLED. The first light emitting control transistor T5 and the second light emitting control transistor T6 are turned on in response to the light emitting control signal En provided through the light emitting line 15. When the light emitting control signal En is applied to the gate electrode G6 of the second light emitting control transistor T6, the second light emitting control transistor T6 is turned on, and, thus, the driving

current I_d flows through the organic light emitting diode OLED. The second light emitting control transistor T6 may determine the timing at which the driving current I_d flows through the organic light emitting diode OLED.

[0105] A gate electrode G7 of the bypass transistor T7 is connected to the third scan line 34. A source electrode S7 of the bypass transistor T7 is connected to the anode of the organic light emitting diode OLED. A drain electrode D7 of the bypass transistor T7 is connected to the initializing line 22. The bypass transistor T7 is turned on in response to the (n+1)th scan signal S_{n+1} applied thereto through the third scan line 34 to initialize the anode of the organic light emitting diode OLED.

[0106] A second electrode C2 of the storage capacitor Cst is connected to the voltage line 26. The first electrode C1 of the storage capacitor Cst is connected to the gate electrode G1 of the driving transistor T1, the drain electrode D3 of the compensating transistor T3, and the source electrode S4 of the initializing transistor T4.

[0107] A cathode of the organic light emitting diode OLED receives a reference voltage ELVSS. The organic light emitting diode OLED receives the driving current I_d from the driving transistor T1 to emit a light.

[0108] In the pixel PX according to an exemplary embodiment of the present disclosure, the gate electrodes G2, G3, G4, and G7 of the switching transistor T2, the compensating transistor T3, the initializing transistor T4, and the bypass transistor T7 may receive signals from the gate driving circuit (not shown) of the pixel driving circuit GDC described with reference to FIG. 3.

[0109] In the pixel PX according to an exemplary embodiment of the present disclosure, the first light emitting control transistor T5 and the second light emitting control transistor T6 may receive signals from the light emitting line driving circuit (not shown) of the pixel driving circuit GDC described with reference to FIG. 3.

[0110] In another exemplary embodiment of the present disclosure, the number and connection of the transistors T1 to T7 in the pixels PX may be changed in various ways.

[0111] FIG. 5 is a cross-sectional view taken along the line I-I' of FIG. 3; and FIG. 6 is a view showing a region "AA" of FIG. 3.

[0112] Referring to FIGS. 2 and 5, the base layer SUB may be formed of various materials, such as glass, metal, or plastic. In an embodiment, the plastic may be polyimide (PI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polyarylate, polycarbonate (PC), polyetherimide (PEI), or polyether sulfone (PES).

[0113] In an embodiment, the display area DA and the non-display area NDA of the display panel DP may be substantially identically defined in the base layer SUB.

[0114] The circuit element layer DP-CL is disposed on the base layer SUB.

[0115] The circuit element layer DP-CL may include the pixel driving circuit GDC, the signal lines, and the pad part PD, which are described with reference to FIG. 3, and the transistors T1 to T7 of the pixel PX described

with reference to FIG. 4.

[0116] Referring to FIGS. 3 to 6, a light emitting line driving circuit ETC of the pixel driving circuit GDC may be disposed farther from the display area DA of the display panel DP than a gate driving circuit GTC when viewed in a plan view. Each of the gate driving circuit GTC and the light emitting line driving circuit ETC may include a plurality of transistors and electronic elements.

[0117] FIG. 5 shows a light emitting line driving circuit area ETCA in which the light emitting line driving circuit ETC is disposed and a gate driving circuit area GTCA in which the gate driving circuit GTC is disposed. FIG. 5 shows a first transistor TFT1 included in the light emitting line driving circuit ETC and a second transistor TFT2 included in the gate driving circuit GTC as representative examples. In addition, FIG. 5 shows a third transistor TFT3 included in the pixel PX.

[0118] The first transistor TFT1 includes a first semiconductor pattern SM1, a first control electrode CE1, a first input electrode IE1, and a first output electrode OE1.

[0119] The second transistor TFT2 includes a second semiconductor pattern SM2, a second control electrode CE2, a second input electrode IE2, and a second output electrode OE2.

[0120] The third transistor TFT3 includes a third semiconductor pattern SM3, a third control electrode CE3, a third input electrode IE3, and a third output electrode OE3.

[0121] The circuit element layer DP-CL may include a buffer layer 110 and first, second, third, and fourth insulating layers 120, 130, 140, and 150.

[0122] The buffer layer 110 is disposed on the base layer SUB. The buffer layer 110 is disposed to planarize an upper surface of the base layer SUB or to prevent or substantially prevent a foreign matter from entering the first, second, and third semiconductor patterns SM1, SM2, and SM3 of the first, second, and third transistors TFT1, TFT2, and TFT3. In an embodiment, the buffer layer 110 may be formed of silicon oxide or silicon nitride.

[0123] The first, second, and third semiconductor patterns SM1, SM2, and SM3 may be disposed on the buffer layer 110.

[0124] The first insulating layer 120 may be disposed on the first, second, and third semiconductor patterns SM1, SM2, and SM3. The first insulating layer 120 may include an organic or inorganic insulating layer.

[0125] The first, second, and third control electrodes CE1, CE2, and CE3 may be disposed on the first insulating layer 120.

[0126] The second insulating layer 130 may be disposed on the first, second, and third control electrodes CE1, CE2, and CE3. The second insulating layer 130 may include an organic or inorganic insulating layer.

[0127] The first, second, and third input electrodes IE1, IE2, and IE3 and the first, second, and third output electrodes OE1, OE2, and OE3 may be disposed on the second insulating layer 130.

[0128] The first input electrode IE1 and the first output

electrode OE1 are spaced apart from each other and connected to the first semiconductor pattern SM1 through contact holes (not shown) formed through the second insulating layer 130.

[0129] The second input electrode IE2 and the second output electrode OE2 are spaced apart from each other and connected to the second semiconductor pattern SM2 through contact holes (not shown) formed through the second insulating layer 130.

[0130] The third input electrode IE3 and the third output electrode OE3 are spaced apart from each other and connected to the third semiconductor pattern SM3 through contact holes (not shown) formed through the second insulating layer 130.

[0131] According to another exemplary embodiment of the present disclosure, positions of the first, second, and third semiconductor patterns SM1, SM2, and SM3, the first, second, and third control electrodes CE1, CE2, and CE3, the first, second, and third input electrodes IE1, IE2, and IE3, and the first, second, and third output electrodes OE1, OE2, and OE3 may be varied from the structure of each of the first, second, and third semiconductor patterns SM1, SM2, and SM3 shown in FIG. 5.

[0132] According to another exemplary embodiment of the present disclosure, some layers of the first, second, and third transistors TFT1, TFT2, and TFT3 may be formed on a same layer as and formed of a same material as those of the auxiliary power supply pattern VSSP. For example, in an embodiment, the third input electrode IE3 and the third output electrode OE3 of the third transistor TFT3 are disposed on a same layer as the power supply line E-VSS; however according to another embodiment, the third input electrode IE3 and the third output electrode OE3 of the third transistor TFT3 may be disposed on a same layer as the auxiliary power supply pattern VSSP and may be connected to the third semiconductor pattern SM3 through contact holes formed through the second and third insulating layers 130 and 140.

[0133] According to another exemplary embodiment of the present disclosure, a metal layer for the first, second, and third transistors TFT1, TFT2, and TFT3 is formed when the auxiliary power supply pattern VSSP is formed, and a design margin of the first, second, and third transistors TFT1, TFT2, and TFT3 may be improved, and, as a result, a display quality may be improved.

[0134] Referring to FIG. 5 again, the power supply line E-VSS may be disposed on the second insulating layer 130. In an exemplary embodiment of the present disclosure, the power supply line E-VSS may be disposed on a same layer as the first, second, and third input electrodes IE1, IE2, and IE3 and the first, second, and third output electrodes OE1, OE2, and OE3. In an exemplary embodiment of the present disclosure, the initializing line SL-Vint and the voltage line SL-VDD may be disposed on a same layer as the power supply line E-VSS.

[0135] The power supply line E-VSS may include a single layer or a plurality of layers. As an example, the power

supply line E-VSS may have a structure in which titanium/aluminum/titanium (Ti/Al/Ti) are sequentially stacked.

[0136] The third insulating layer 140 may be disposed on the power supply line E-VSS and the first, second, and third transistors TFT1, TFT2, and TFT3. The third insulating layer 140 may include an organic or inorganic insulating layer. The third insulating layer 140 may be defined as a first intermediate insulating layer.

[0137] The auxiliary power supply pattern VSSP may be disposed on the third insulating layer 140. The auxiliary power supply pattern VSSP may overlap with the power supply line E-VSS. The auxiliary power supply pattern VSSP may be electrically connected to the power supply line E-VSS through a contact hole (not shown) formed through the third insulating layer 140.

[0138] In an embodiment, the auxiliary power supply pattern VSSP may be formed of a material with a melting point higher than that of the first control electrode CE1, the first input electrode IE1, and the first output electrode OE1.

[0139] The auxiliary power supply pattern VSSP may include a metal material, e.g., molybdenum (Mo).

[0140] The fourth insulating layer 150 may be disposed on the auxiliary power supply pattern VSSP. The fourth insulating layer 150 may overlap with a portion of the auxiliary power supply pattern VSSP. The fourth insulating layer 150 may include an organic or inorganic insulating layer. The fourth insulating layer 150 may be defined as a second intermediate insulating layer.

[0141] The display element layer DP-OLED may include a pixel definition layer PDL and an organic light emitting element OD.

[0142] The pixel definition layer PDL is disposed on the fourth insulating layer 150. The pixel definition layer PDL is provided with a plurality of openings defined there-through. The organic light emitting element OD may be provided in each opening.

[0143] The organic light emitting element OD includes a first electrode E1, a second electrode E2, and a light emitting layer EML. The first electrode E1 may be disposed on the circuit element layer DP-CL. The first electrode E1 may be electrically connected to the third transistor TFT3 after passing through the third and fourth insulating layers 140 and 150. The first electrode E1 may be provided in a plural number. At least portions of each of the first electrodes E1 may be exposed through the openings.

[0144] The second electrode E2 is disposed on the first electrode E1. The second electrode E2 may overlap with the first electrodes E1 and the pixel definition layer PDL. When the organic light emitting element OD is provided in a plural number, the second electrode E2 of each of the organic light emitting elements OD may receive the same voltage. Accordingly, an additional patterning process required to form the second electrode E2 may be omitted. In an embodiment, the second electrode E2 may be provided in a plural number such that the second elec-

trodes E2 respectively correspond to the openings.

[0145] The light emitting layer EML is disposed between the first electrode E1 and the second electrode E2. The light emitting layer EML may be provided in a plural number to respectively correspond to the openings. The organic light emitting element OD may activate the light emitting layer EML according to a difference in electric potential between the first electrode E1 and the second electrode E2 to generate the light.

[0146] Although not shown in the figures, the organic light emitting element OD may further include an electron control layer disposed between the first electrode E1 and the light emitting layer EML and a hole control layer disposed between the light emitting layer EML and the second electrode E2.

[0147] The display element layer DP-OLED may further include an auxiliary pattern VSP disposed on the fourth insulating layer 150. The auxiliary pattern VSP may be disposed on a same layer as the first electrode E1.

[0148] The auxiliary pattern VSP may be disposed in the non-display area NDA of the display panel DP. The auxiliary pattern VSP may be connected to the auxiliary power supply pattern VSSP through a contact hole (not shown) formed through the fourth insulating layer 150.

[0149] The second electrode E2 may be connected to the auxiliary pattern VSP through a contact hole (not shown) formed through the pixel definition layer PDL in the non-display area NDA.

[0150] The power supply line E-VSS may apply a common voltage to the second electrode E2 through the auxiliary power supply pattern VSSP and the auxiliary pattern VSP.

[0151] The sealing member SL may overlap with the auxiliary power supply pattern VSSP. The sealing member SL may be disposed between the auxiliary power supply pattern VSSP and the encapsulation layer ENP and may make contact with the auxiliary power supply pattern VSSP.

[0152] The sealing member SL may include a light-curable resin or a heat-curable resin to be coupled to the auxiliary power supply pattern VSSP, the third insulating layer 140, and the encapsulation layer ENP.

[0153] The sealing member SL may overlap with a portion of the pixel driving circuit GDC of FIG. 3, i.e., the light emitting line driving circuit ETC. Accordingly, the non-display area NDA of the display panel DP may be reduced.

[0154] The auxiliary power supply pattern VSSP may cover metal layers of the circuit element layer DP-CL overlapped with the sealing member SL. In an embodiment, the auxiliary power supply pattern VSSP may cover components of the power supply line E-VSS and the light emitting line driving circuit ETC, i.e., the first transistor TFT1.

[0155] The sealing member SL may be formed by providing a curable material between the auxiliary power supply pattern VSSP and the encapsulation layer ENP and irradiating a laser beam downward from an upper

side of the encapsulation layer ENP. When the laser beam is irradiated to the curable material, if a temperature of metal layers disposed in an area overlapped with the curable material, for example, elements of the pixel driving circuit GDC and the power supply line E-VSS, rises above a melting point thereof, defects may occur.

[0156] However, according to the display apparatus of an exemplary embodiment of present disclosure, when the auxiliary power supply pattern VSSP is disposed above the pixel driving circuit GDC and the power supply line E-VSS to overlap with the sealing member SL, the pixel driving circuit GDC and the power supply line E-VSS may be prevented or substantially prevented from being made defective due to the laser beam. To this end, the auxiliary power supply pattern VSSP may include a material with a melting point higher than that of the metal layer of the power supply line E-VSS. In a case in which the metal layer of the power supply line E-VSS includes a plurality of layers, the auxiliary power supply pattern VSSP may include a material with a melting point higher than that of the metal layer with a lowest melting point among the layers of the power supply line E-VSS.

[0157] In addition, the auxiliary power supply pattern VSSP is connected to the power supply line E-VSS to reduce a resistance of a line supplying the common voltage, and, thus, the common voltage may be uniformly applied to the second electrode E2.

[0158] The light emitting line driving circuit ETC is turned on for most of a pixel operation period to reduce an influence caused by a parasitic capacitor formed between the auxiliary power supply pattern VSSP and the light emitting line driving circuit ETC. Accordingly, the light emitting line driving circuit ETC may be formed to overlap with the power supply pattern VSSP to reduce the non-display area NDA of the display panel DP.

[0159] The gate driving circuit GTC is turned off for most of the pixel operation period and is relatively affected by a parasitic capacitor formed between the gate driving circuit GTC and other elements. That is, since a pulse signal output from the gate driving circuit GTC has a pulse width corresponding to a very small period (less than about 1%) of the pixel operation period, a waveform damage due to a delay caused by the parasitic capacitor may cause defects in an operation of circuits. Accordingly, the gate driving circuit GTC may be disposed not to overlap with the power supply pattern VSSP in an exemplary embodiment of the present disclosure.

[0160] FIG. 7 is a cross-sectional view taken along the line II-II' of FIG. 3.

[0161] The pad part PD may include a first pad layer PD1 and a second pad layer PD2.

[0162] The first pad layer PD1 may be disposed on a same layer as the first, second, and third control electrodes CE1, CE2, and CE3. The second pad layer PD2 may be disposed on a same layer as the voltage line SL-VDD. The second pad layer PD2 may make contact with the first pad layer PD1 through a contact hole (not shown) formed through the second insulating layer 130.

[0163] In an embodiment, the display panel DP may further include a flexible printed circuit board FPC. The flexible printed circuit board FPC may be bent toward a rear surface of the display panel DP after being attached to the display panel DP.

[0164] The flexible printed circuit board FPC may be connected to the pad part DP through a conductive adhesive member ACF. The flexible printed circuit board FPC may include a flexible base film BF, a circuit board pad CPD, and an integrated circuit chip IC. The circuit board pad CPD may be disposed on the base film BF to make contact with the conductive adhesive member ACF. The integrated circuit chip IC may be mounted on the base film BF and may apply signals required to drive the display panel DP through the circuit board pad CPD.

[0165] The voltage line SL-VDD may be disposed on a same layer as the power supply line E-VSS.

[0166] The auxiliary voltage pattern VDDP may be disposed on the third insulating layer 140. The auxiliary voltage pattern VDDP may overlap with the voltage line SL-VDD. The auxiliary voltage pattern VDDP may be electrically connected to the voltage line SL-VDD through a contact hole (not shown) formed through the third insulating layer 140.

[0167] The auxiliary voltage pattern VDDP may be disposed on a same layer as that of the auxiliary power supply pattern VSSP and may include a same material as those of the auxiliary power supply pattern VSSP described with reference to FIG. 5.

[0168] The sealing member SL may overlap with the auxiliary voltage pattern VDDP. The sealing member SL may be disposed between the auxiliary voltage pattern VDDP and the encapsulation layer ENP and may make contact with the auxiliary voltage pattern VDDP.

[0169] The auxiliary voltage pattern VDDP may be connected to the voltage line SL-VDD to reduce the resistance of the line applying the source voltage, and the source voltage may be uniformly applied to the first light emitting control transistor T5 described with reference to FIG. 4.

[0170] FIG. 8 is a cross-sectional view showing a portion of a display panel DP1 of a display apparatus according to another exemplary embodiment of the present disclosure. FIG. 8 shows a cross-section corresponding to the line I-I' of FIG. 3 in the display panel DP1 according to another exemplary embodiment of the present disclosure.

[0171] An auxiliary power supply pattern VSSP1 of the display panel DP1 described with reference to FIG. 8 has substantially the same structure as the auxiliary power supply pattern VSSP described with reference to FIG. 5 except that the auxiliary power supply pattern VSSP1 includes one or more holes HL1 and HL2.

[0172] As shown in FIG. 8, one first hole HL1 and one second hole HL2 are defined through the auxiliary power supply pattern VSSP1; however, the number of each of the first and second holes HL1 and HL2 is not limited to one. That is, each of the first and second holes HL1 and

HL2 may be provided in a plural number through the auxiliary power supply pattern VSSP1, or only one of the first and second holes HL1 and HL2 may be provided through the auxiliary power supply pattern VSSP1.

[0173] The first hole HL1 and the second hole HL2 may be provided to overlap with the sealing member SL. The first hole HL1 and the second hole HL2 may penetrate through the auxiliary power supply pattern VSSP1.

[0174] In an embodiment, the first hole HL1 may further penetrate through at least one of the buffer layer 110 and the first, second, and third insulating layers 120, 130, and 140 in order of the third, second, and first insulating layers 140, 130, and 120 and the buffer layer 110. FIG. 8 shows, as a representative example, the first hole HL1 that penetrates through all of the buffer layer 110 and the first, second, and third insulating layers 120, 130, and 140.

[0175] In an embodiment, the second hole HL2 may penetrate through the auxiliary power supply pattern VSSP1 and may not penetrate through the first, second, third, and fourth insulating layers 120, 130, 140, and 150.

[0176] In an embodiment, a third hole HL3 may be defined through the third insulating layer 140. The third hole HL3 may overlap with the sealing member SL and may not overlap with the auxiliary power supply pattern VSSP1. The third hole HL3 may further penetrate through at least one of the buffer layer 110 and the first and second insulating layers 120 and 130 in order of the second and first insulating layers 130 and 120 and the buffer layer 110. FIG. 8 shows, as a representative example, the third hole HL3 that penetrates through all of the buffer layer 110 and the first and second insulating layers 120 and 130.

[0177] In an embodiment, the sealing member SL may be formed of a material obtained by mixing the curable material with a glass raw material. The sealing member SL may be more securely adhered to the insulating layer and the base layer SUB formed of a glass material than a metal material.

[0178] According to the display apparatus of an exemplary embodiment of the present disclosure, an area in which the sealing member SL makes contact with the insulating layers 110, 120, 130, and 140 and the base layer SUB increases due to at least one of the first, second, and third holes HL1, HL2, and HL3, and, thus, a mechanical strength of the display panel DP1 may be improved.

[0179] FIG. 9 is a circuit diagram showing a portion of a display panel of a display apparatus according to another exemplary embodiment of the present disclosure; and FIG. 10 is a cross-sectional view showing the portion of the display panel DP2 according to the exemplary embodiment of FIG. 9. FIG. 10 shows a cross-section corresponding to the line II-II' of FIG. 3 in the display panel DP2 according to another exemplary embodiment of the present disclosure.

[0180] Referring to FIG. 9, one pad part PD may be connected to at least two data lines DL1 and DL2 by a demultiplexer DX. FIG. 9 shows one pad part PD con-

nected to first and second data lines DL1 and DL2 as a representative example.

[0181] The demultiplexer DX may include a first switching device SW1 and a second switching device SW2.

[0182] The first switching device SW1 may be turned on in response to a first control signal CS1, and the second switching device SW2 may be turned on in response to a second control signal CS2. The first and second switching devices SW1 and SW2 may be turned on at different timings from each other.

[0183] The signal applied to the pad part PD may provide different data from each other to the first and second data lines DL1 and DL2 by the first and second switching devices SW1 and SW2 turned on at different timings from each other.

[0184] Referring to FIG. 10, the demultiplexer DX of the display panel DP2 according to another exemplary embodiment may be provided to the circuit element layer DP-CL. The first and second switching devices SW1 and SW2 included in the demultiplexer DX may have the same structure as the third transistor TFT3. FIG. 10 shows the first switching device SW1 as a representative example.

[0185] The first switching device SW1 may include a fourth semiconductor pattern SM4, a fourth control electrode CE4, a fourth input electrode IE4, and a fourth output electrode OE4.

[0186] In addition, the circuit element layer DP-CL may further include an anti-static pattern ESD. The anti-static pattern ESD may be provided in a plural number, and each anti-static pattern ESD may have an island shape. The anti-static patterns ESD may be provided in a floating state and spaced apart from each other. The anti-static patterns ESD may be formed on various layers and may include a metal material. In an exemplary embodiment of the present disclosure, the anti-static pattern ESD may be disposed on a same layer as the third control electrode CE3 of the third transistor TFT3. The anti-static pattern ESD may prevent or substantially prevent an external static electricity from entering the elements disposed in the display area DA.

[0187] The auxiliary voltage pattern VDDP may cover the demultiplexer DX, i.e., the first switching device SW1. The first switching device SW1 may overlap with the sealing member SL.

[0188] In an embodiment, the auxiliary voltage pattern VDDP may cover the anti-static pattern ESD. The anti-static pattern ESD may overlap with the sealing member SL.

[0189] When the laser beam is irradiated to the curable material while the sealing member SL is formed, if a temperature of the first switching device SW1 and the anti-static pattern ESD, which are disposed in an area overlapped with the curable material, rises above a melting point thereof, defects may occur.

[0190] However, according to the display apparatus of an exemplary embodiment of present disclosure, the auxiliary voltage pattern VDDP may include a material

with a melting point higher than that of the fourth control electrode CE4, the fourth input electrode IE4, and the fourth output electrode OE4.

[0191] When the auxiliary voltage pattern VDDP is disposed to overlap with the first switching device SW1 and the anti-static pattern ESD, the first switching device SW1 and the anti-static pattern ESD may be prevented or substantially prevented from being made defective due to the laser beam.

[0192] Although some exemplary embodiments of the present invention have been described, it is to be understood that the present invention should not be limited to these exemplary embodiments, but various changes and modifications can be made by one of ordinary skill in the art within the scope of the present invention as herein claimed.

[0193] Therefore, the disclosed subject matter should not be limited to any single embodiment described herein, and the scope of the present inventive concept shall be determined according to the attached claims.

Claims

1. An organic light emitting display apparatus comprising:

a base layer (SUB) comprising a display area (DA) and a non-display area (NDA) adjacent to the display area (DA);

a circuit element layer (DP-CL) comprising a power supply line (E-VSS) on the base layer (SUB) to receive a common voltage and an auxiliary power supply pattern (VSSP) on the power supply line, overlapped with the power supply line, and connected to the power supply line;

a display element layer (DP-OLED) comprising a first electrode (E1) on the circuit element layer, a light emitting layer (EML) on the first electrode (E1), and a second electrode (E2) on the light emitting layer and electrically connected to the auxiliary power supply pattern (VSSP);

an encapsulation layer (ENP) on the display element layer (EML); and

a sealing member (SL) between the circuit element layer (DP-CL) and the encapsulation layer (ENP) and located in the non-display area (DA) to overlap with the auxiliary power supply pattern (VSSP) when viewed in a plan view.

2. The organic light emitting display apparatus of claim 1, wherein the auxiliary power supply pattern (VSSP) contacts the sealing member (SL).

3. The organic light emitting display apparatus of claim 1 or 2, wherein the display element layer (DP-OLED) further comprises an auxiliary pattern (VSP) in the non-display area (NDA), located on a same layer as

the first electrode (E1), and connected to the auxiliary power supply pattern (VSSP).

4. The organic light emitting display apparatus of claim 3, wherein the circuit element layer (DP-CL) further comprises:

a first intermediate insulating layer (140) between the power supply line (E-VSS) and the auxiliary power supply pattern (VSSP) and comprising a contact hole through which the power supply line (E-VSS) is connected to the auxiliary power supply pattern (VSSP); and

a second intermediate insulating layer (150) between the auxiliary power supply pattern (VSSP) and the auxiliary pattern (VSP) and comprising a contact hole through which the auxiliary power supply pattern (VSSP) is connected to the auxiliary pattern (VSP),

the display element layer (DP-OLED) further comprising a pixel definition layer (PDL) between the auxiliary pattern (VSP) and the second electrode (E2), comprising a contact hole through which the auxiliary pattern (VSP) is connected to the second electrode (E2), and comprising an opening in which the light emitting layer is located.

5. The organic light emitting display apparatus of one of the preceding claims, wherein the circuit element layer (DP-CL) further comprises:

a switching transistor (T2) comprising a control electrode to receive a scan signal, an input electrode receiving a data signal, and an output electrode;

a driving transistor (T1) comprising an input electrode connected to the output electrode of the switching transistor; and

a light emitting control transistor (T5, T6) comprising a control electrode to receive a light emitting signal and being connected between a voltage line and the driving transistor or between the driving transistor and the first electrode.

6. The organic light emitting display apparatus of claim 5, wherein the circuit element layer (DP-CL) further comprises:

a light emitting line driving circuit to apply the light emitting signal to the light emitting control transistor; and

a gate driving circuit to apply the scan signal to the switching transistor, the light emitting line driving circuit being farther from the display area (DA) than the gate driving circuit when viewed in a plan view.

7. The organic light emitting display apparatus of claim 6, wherein the auxiliary power supply pattern (VSSP) overlaps with the light emitting line driving circuit.

8. The organic light emitting display apparatus of one of the preceding claims, wherein the auxiliary power supply pattern (VSSP) comprises material having a melting point higher than a melting point of the power supply line.

9. The organic light emitting display apparatus of one of the preceding claims, wherein the circuit element layer (DP-CL) further comprises:

a voltage line (SL-VDD) to receive a source voltage greater than the common voltage; and an auxiliary voltage pattern (VDDP) above the voltage line (SL-VDD) and connected to the voltage line (SL-VDD).

10. The organic light emitting display apparatus of claim 9, wherein the auxiliary voltage pattern (VDDP) is on a same layer as the auxiliary power supply pattern (VSSP) and overlaps with the sealing member (SL).

11. The organic light emitting display apparatus of claim 9, wherein the auxiliary voltage pattern (VDDP) contacts the sealing member (SL).

12. The organic light emitting display apparatus of one of claims 9 to 11, wherein the circuit element layer (DP-CL) further comprises a pad part (PD) in the non-display area (NDA), and the auxiliary voltage pattern (VDDP) is between the pad part (PD) and the display area (DA) when viewed in a plan view.

13. The organic light emitting display apparatus of claim 12, wherein the circuit element layer (DP-CL) further comprises:

a data line; and a demultiplexer (DX) connected between the pad part (PD) and the data line, and the auxiliary voltage pattern (VDDP) covers the demultiplexer (PD) when viewed in a plan view.

14. The organic light emitting display apparatus of claim 12, wherein the circuit element layer (DP-CL) further comprises an anti-static pattern (ESD) in the non-display area (NDA), and the auxiliary voltage pattern (VDDP) covers the anti-static pattern (ESD) when viewed in a plan view.

15. The organic light emitting display apparatus of claim 1, wherein the circuit element layer (DP-CL) further comprises an insulating layer (120, 130, 140) under the auxiliary power supply pattern (VSSP1),

the auxiliary power supply pattern (VSSP1) comprises a hole therethrough (HL1, HL2), and the sealing member (SL) contacts the insulating layer (120, 130, 140) or the base layer (SUB) through the hole.

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FIG. 1

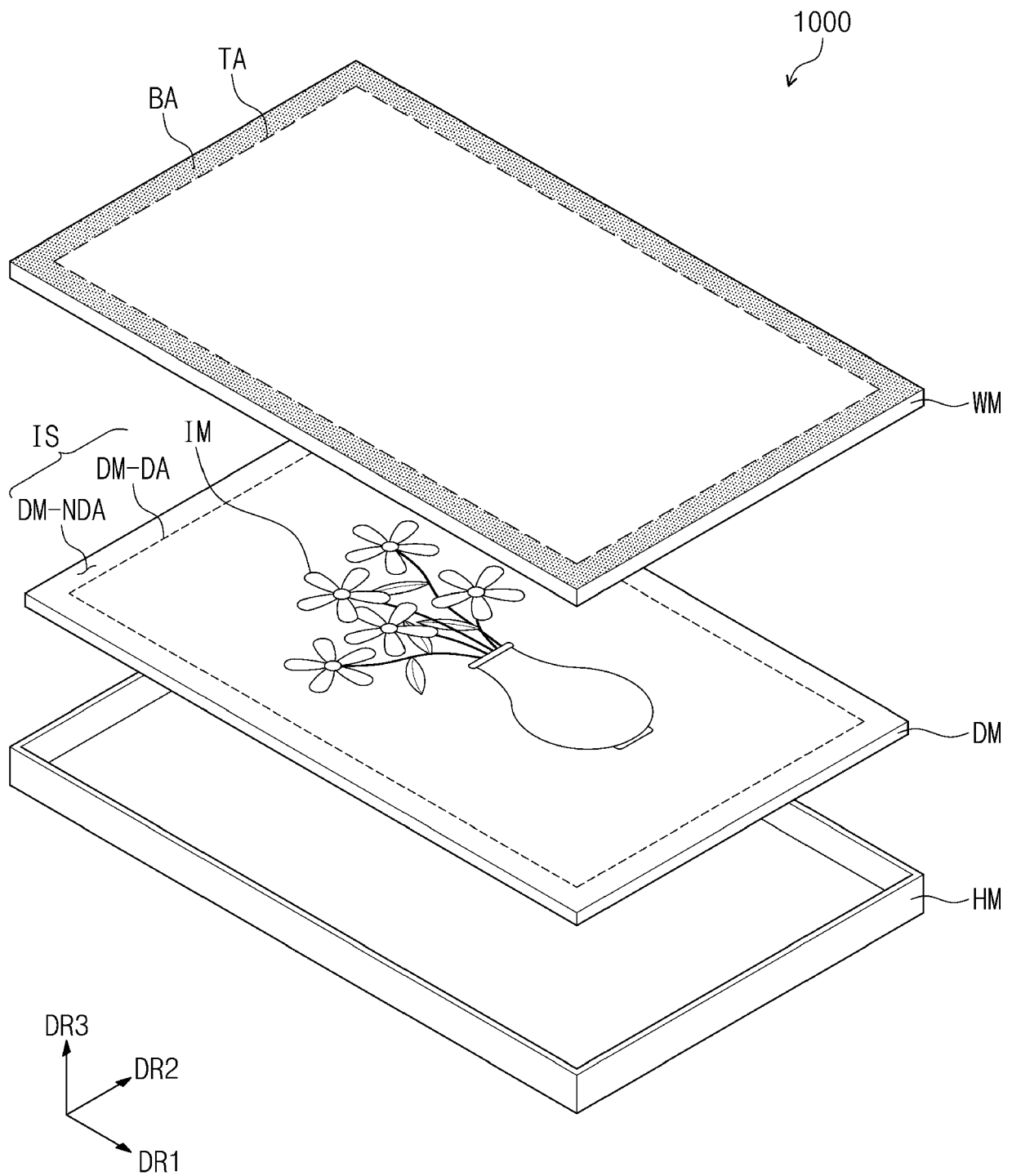


FIG. 2

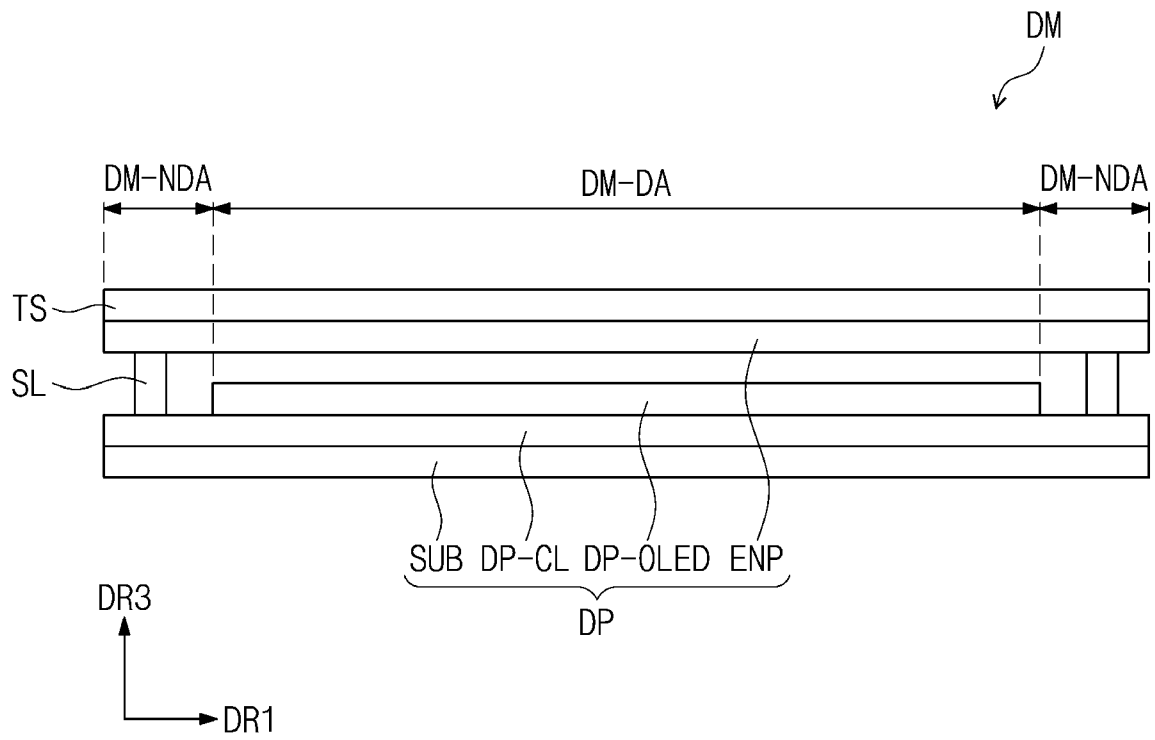


FIG. 3

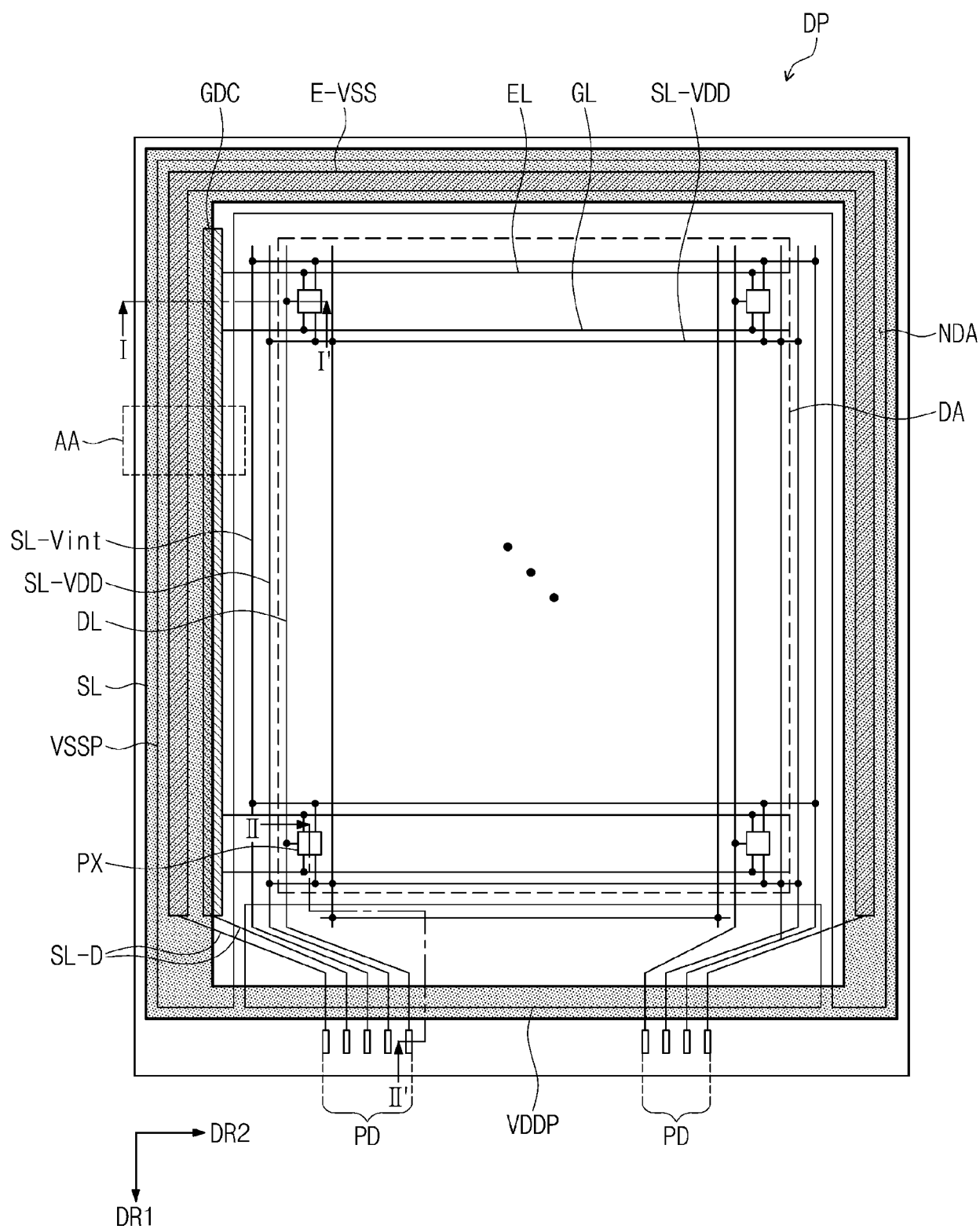


FIG. 4

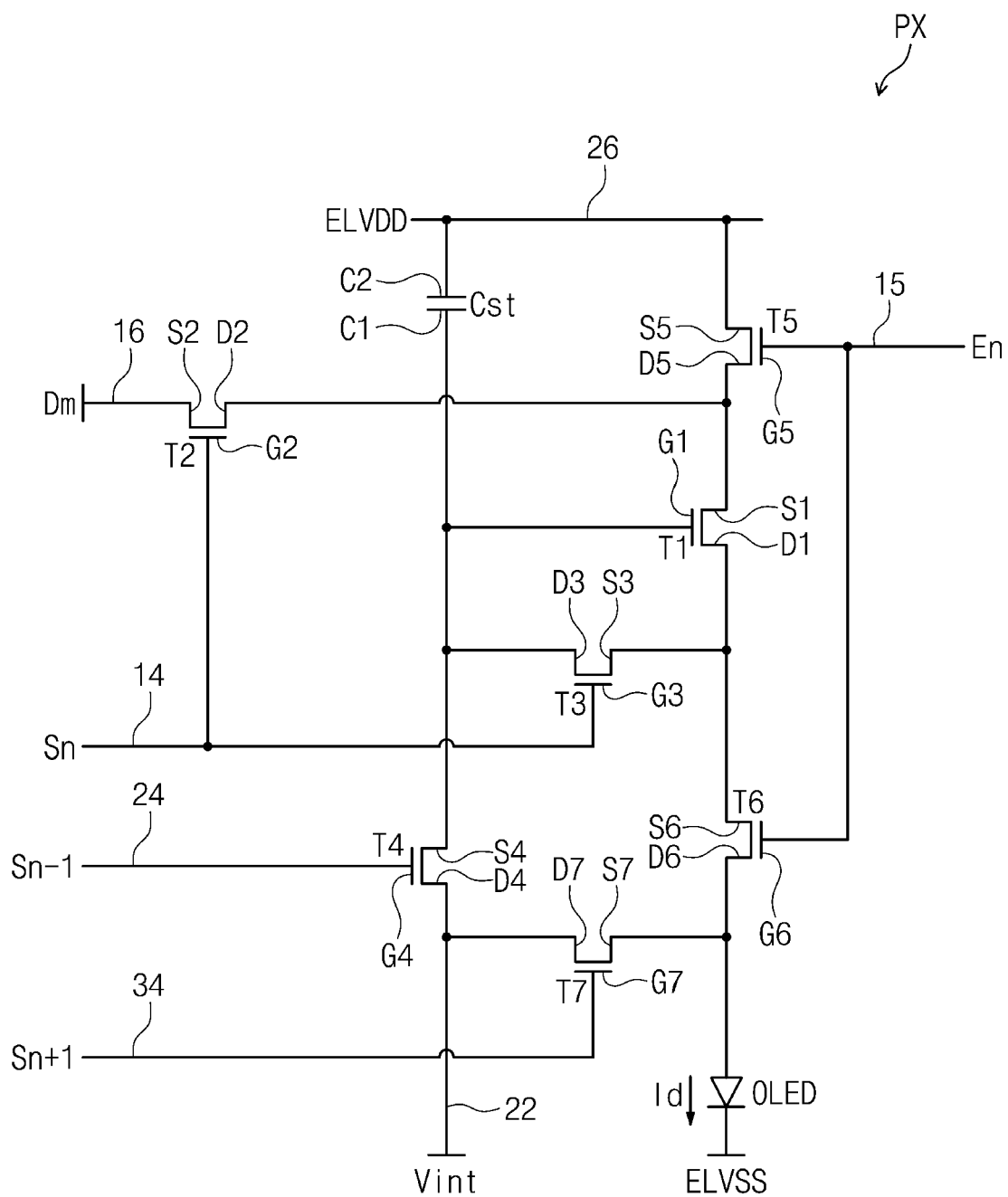


FIG. 5

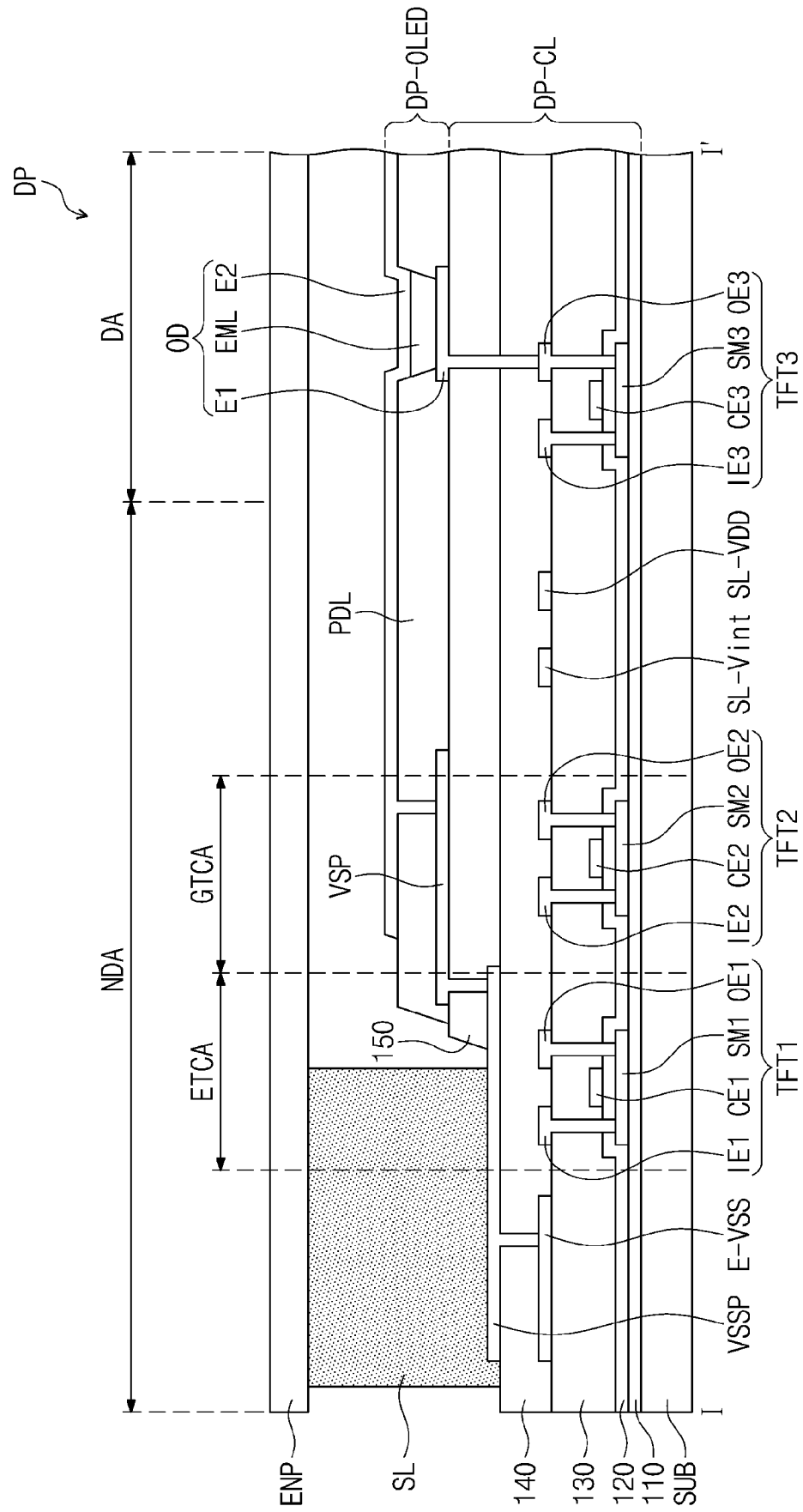


FIG. 6

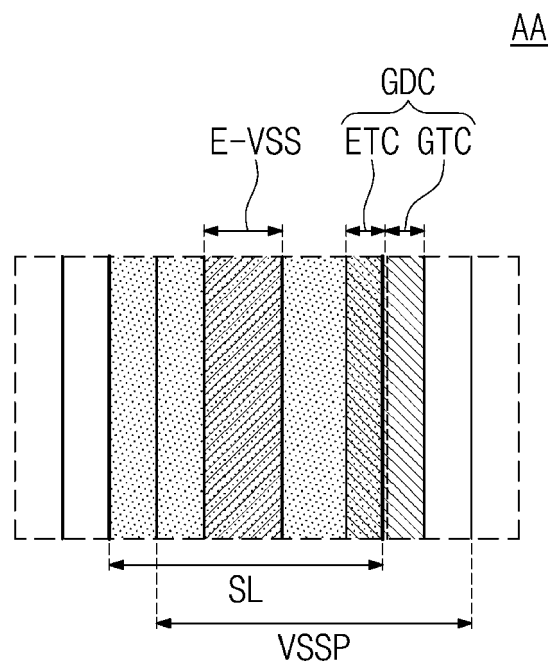


FIG. 7

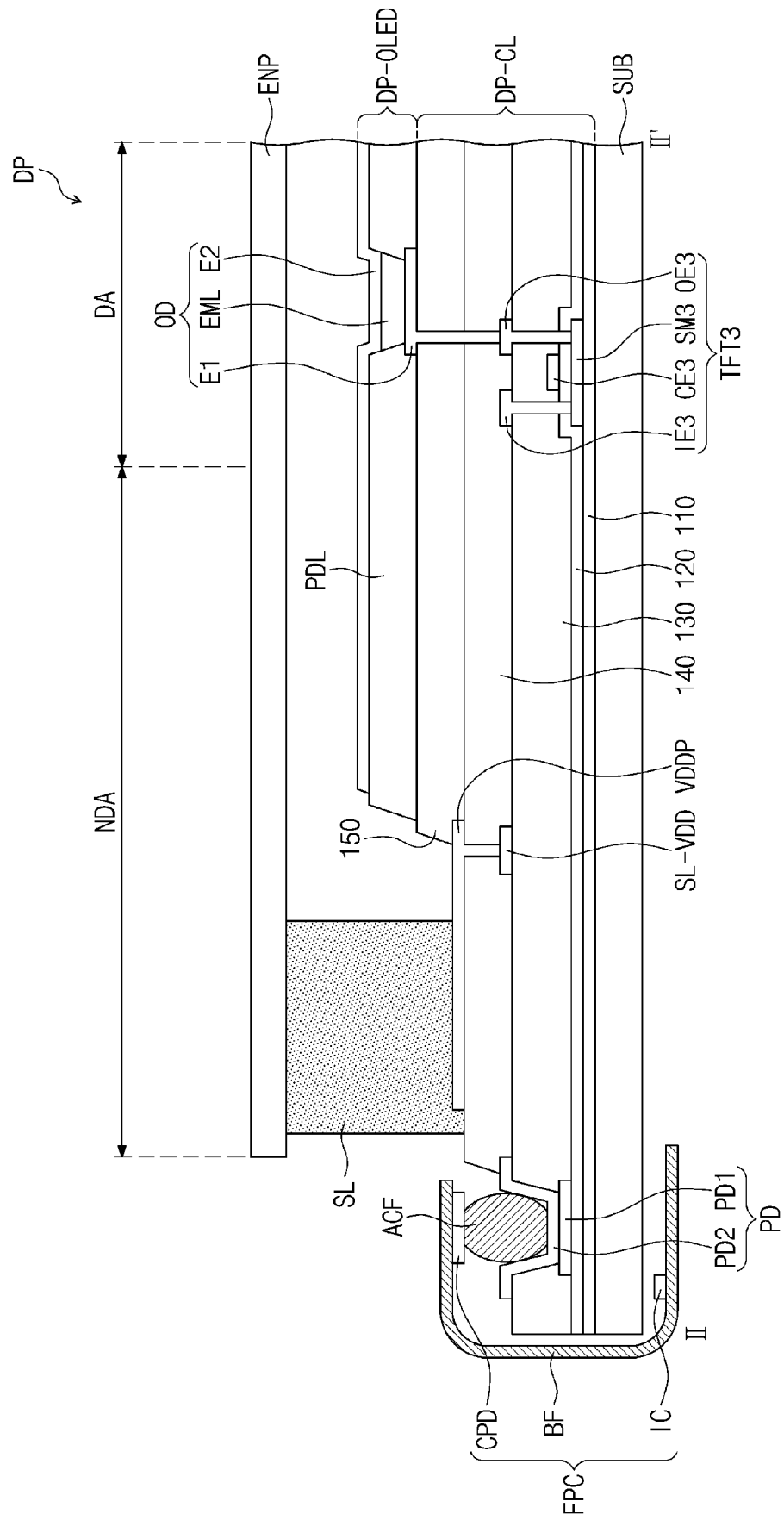


FIG. 8

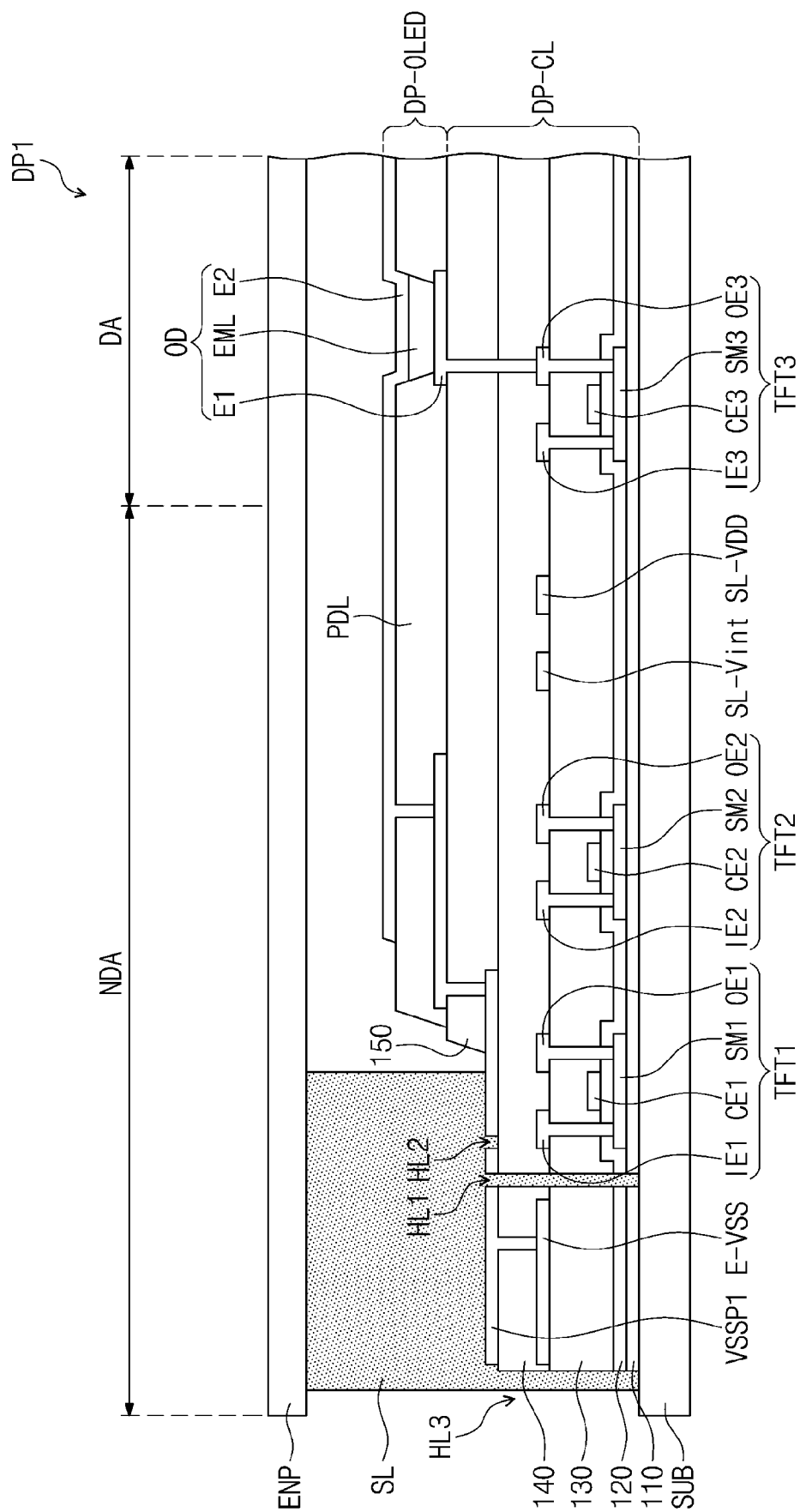


FIG. 9

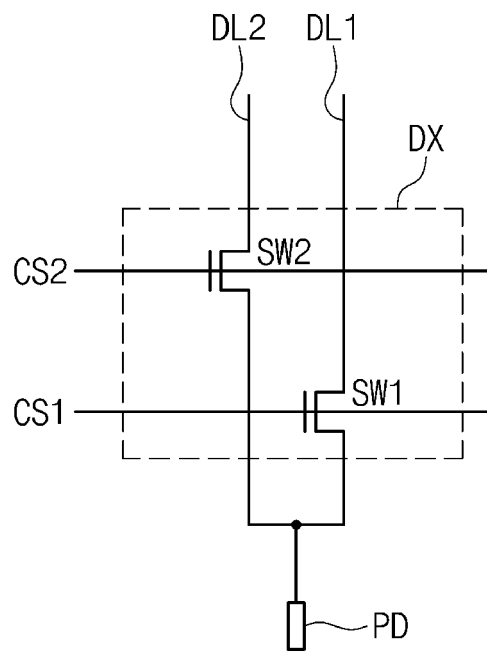
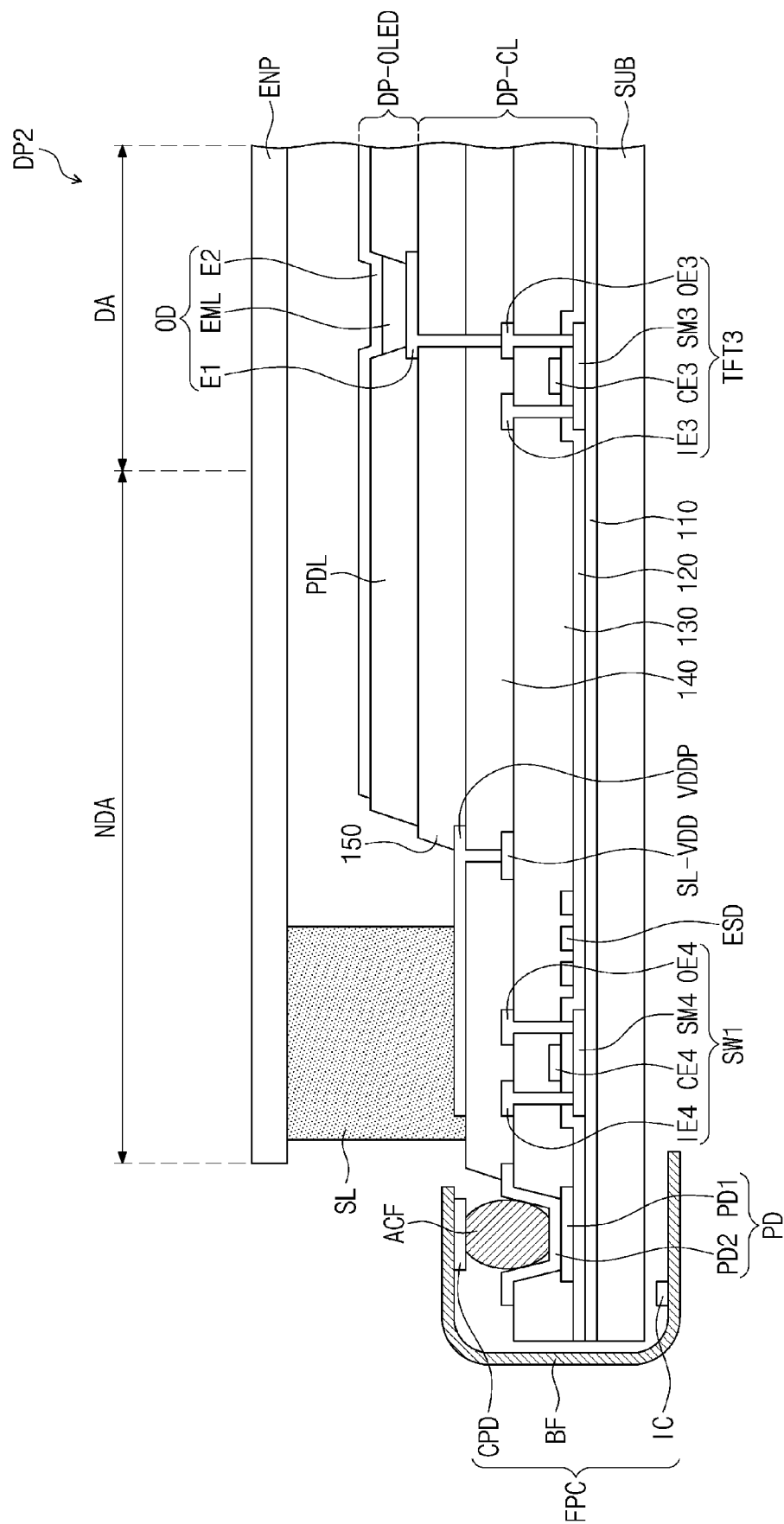


FIG. 10





EUROPEAN SEARCH REPORT

Application Number
EP 19 17 3706

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Y	* figures 3,5 *	8	
A	* paragraphs [0041] - [0048], [0054], [0057], [0062], [0066], [0072], [0075] - [0078], [0092] *	2,9-15	
X	US 2013/049003 A1 (CHOI HEE DONG [KR] ET AL) 28 February 2013 (2013-02-28)	1-3	
Y	* figures 4,7 *	8,15	
A	* paragraphs [0030] - [0042], [0090] - [0092] *	4-7,9-14	
X	EP 1 503 422 A2 (SAMSUNG SDI CO LTD [KR]) 2 February 2005 (2005-02-02)	1-3,9-14	
Y	* figures 4,8-10 *	15	
A	* paragraphs [0013] - [0023], [0071] - [0080] *	4-8	
X	US 2016/293883 A1 (HONG SANGMIN [KR] ET AL) 6 October 2016 (2016-10-06)	1,15	TECHNICAL FIELDS SEARCHED (IPC)
Y	* figures 3,8 *	15	H01L
A	* paragraph [0127] *	2-14	
Y	US 2013/049062 A1 (HATANO KAORU [JP] ET AL) 28 February 2013 (2013-02-28) * paragraph [0020] *	8	
The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 27 September 2019	Examiner De Laere, Ann
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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The members are as contained in the European Patent Office EDP file on
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27-09-2019

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专利名称(译)	有机发光显示装置		
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申请号	EP2019173706	申请日	2019-05-10
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	CHUNG YUN MO LEE TAK YOUNG YOON JOOSUN		
发明人	CHUNG, YUN-MO LEE, TAK-YOUNG YOON, JOOSUN		
IPC分类号	H01L51/52 H01L27/32		
CPC分类号	H01L27/3276 H01L51/5237 H01L51/5246 G09G3/3233 G09G3/3266 H01L27/0296 H01L27/323 H01L27/3246 H01L27/3258 H01L27/3262 H01L27/3279		
优先权	1020180053725 2018-05-10 KR		
外部链接	Espacenet		

摘要(译)

有机发光显示装置包括基础层 (SUB)，电路元件层 (DP-CL)，显示元件层 (DP-OLED)，封装层 (ENP) 和密封构件 (SL)。电路元件层 (DP-CL) 包括在基础层上的电源线 (E-VSS) 以及在电源线上并连接到电源线的辅助电源图案 (VSSP)。显示元件层 (DP-OLED) 包括依次堆叠在电路元件层上的第一电极 (E1)，发光层 (EML) 和第二电极 (E2)。第二电极 (E2) 电连接到辅助电源图案 (VSSP)。密封构件 (SL) 在电路元件层 (DP-CL) 和封装层 (ENP) 之间，以俯视时与辅助电源图案 (VSSP) 重叠的方式设置。

FIG. 5

