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(54) **ORGANIC LIGHT EMITTING DISPLAY DEVICE AND METHOD FOR DRIVING THE SAME**

(57) The present disclosure provides an organic light-emitting display device (10) comprising: an organic light-emitting element (OLED); a driving transistor (DT) connected with the organic light-emitting element (OLED); a first transistor (D1), wherein when the first transistor (T1) turns on based on an i-th scan signal (SCAN(i)), a data voltage is supplied to a first node (N1) via the turned-on first transistor, wherein i is a natural number equal to or greater than 2 and smaller than or equal to N, wherein N is a number of scan-lines; a capacitor (Cst) disposed between the first node (N1) and a gate electrode of the driving transistor (DT); and a second transistor (T2), wherein when the second transistor turns on based on a (i-1)-th scan signal (SCAN(i)), a first reference voltage is supplied to a second node (N2) via the turned-on second transistor, wherein the second node (N2) is disposed between the driving transistor (DT) and the capacitor (Cst).

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Description

Technical Field

[0001] The present disclosure relates to an active-matrix scheme-based organic light-emitting display device including a compensation circuit, and a method for driving the same.

Related Art

[0002] A display device applies to a variety of electronic devices such as TVs, mobile phones, notebooks and tablets. Therefore, studies are being continued to develop thinner, lighter and lower-power consuming display devices.

[0003] A typical example of the display device may include a liquid crystal display device (LCD), a plasma display panel device (PDP), a field emission display device (FED), an electro luminescence display device (ELD), an electro-wetting display device (EWD) and, an organic light-emitting display device (OLED), etc.

[0004] The organic light-emitting display device includes a plurality of organic light-emitting elements corresponding to a plurality of pixels respectively. The organic light-emitting element is a self-luminous element that emits light by itself. Thus, the organic light-emitting display device has a faster response speed than the liquid crystal display device. Further, the OLED has a high luminous efficiency, a high luminance and a wide viewing angle, and is excellent in contrast ratio and color reproducibility.

[0005] The organic light-emitting display device may be implemented in an active-matrix scheme in which multiple pixels are driven individually.

[0006] The active-matrix scheme-based organic light-emitting display device includes a driving element that supplies a driving current to the organic light-emitting element of each pixel. In this connection, the driving element is usually implemented as a thin film transistor. Further, in general, the driving element and the organic light-emitting element are connected in series between a first driving power source and a second driving power source having a lower potential than the first driving power source.

[0007] In order to prevent luminance differences between the pixels, a plurality of driving elements corresponding to a plurality of pixels respectively need to be designed so that electrical characteristics of the driving elements such as the threshold voltages and the mobilities are the same as each other. However, due to process conditions, driving environments, driving times, etc., uniformity between the electrical characteristics of the plurality of driving elements may be reduced.

[0008] Particularly, due to driving stress, the threshold voltage of the driving element may fluctuate. In this case, as the driving current is reduced due to the variation of the threshold voltage of the driving element, an image quality is deteriorated and the lifetime of the element is reduced.

[0009] In order to compensate for the difference between the threshold voltages of the driving elements, each pixel of the organic light-emitting display device may include a compensation circuit.

[0010] The compensation circuit within each pixel circuit is intended to automatically compensate for the threshold voltage differences between the driving elements. That is, due to the presence of the compensation circuit, the driving current supplied to the organic light-emitting element may not correspond to the threshold voltage of the driving element.

[0011] In general, when each pixel contains each compensation circuit, the organic light-emitting display device initializes a gate electrode of the driving element and an anode of the organic light-emitting element using an initialization voltage for an initialization period. To this end, the compensation circuit comprises at least one thin film transistor connected to an initialization power supply for supplying an initialization voltage.

[0012] However, for the initialization period, a gate-source voltage Vgs of the driving transistor may be above the threshold voltage. At this time, as the first driving power supply with a relatively high potential and the initialization power supply are shortcircuited with each other through the turned-on driving transistor. Thus, a ripple may occur in the initialization power supply. Due to the ripple in the initialization power supply, the gate electrode of the driving element and the anode of the organic light-emitting element may not be properly initialized. As a result, there is a problem that a luminance deviation is caused between the pixels, thereby causing a stain and an abnormal luminance.

SUMMARY

[0013] This Summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify all key features or essential features of the claimed subject matter, nor is it intended to be used alone as an aid in determining the scope of the claimed subject matter.

[0014] The present disclosure is intended to provide an organic light-emitting display device, and a method for driving the device, which may be capable of preventing the ripple in the initialization power supply.

[0015] The purposes of the present disclosure are not limited to the above-mentioned purposes. Other purposes and advantages of the present disclosure, as not mentioned above, may be understood from the following descriptions and more clearly understood from the examples of the present disclosure. Further, it will be readily appreciated that the objects and advantages of the present disclosure may be realized by features and combinations thereof as disclosed in the claims.

[0016] In one aspect of the present disclosure, there

is provided an organic light-emitting display device comprising: an organic light-emitting element; a driving transistor connected in series with the organic light-emitting element, wherein the driving transistor and the organic light-emitting element are disposed between and are connected to first and second driving power supply lines, wherein the first driving power supply line supplies first driving voltage and the second driving power supply line supplies second driving voltage which is lower than the first driving voltage; a first transistor, wherein when the first transistor turns on based on an i-th scan signal, a data voltage is supplied to a first node via the turned-on first transistor, wherein i is a natural number equal to or greater than 2 and smaller than or equal to N, wherein N is a number of scan-lines; a capacitor disposed between the first node and a gate electrode of the driving transistor, wherein the capacitor supplies a turn-on signal to the gate electrode of the driving transistor based on the data voltage; and a second transistor, wherein when the second transistor turns on based on a (i-1)-th scan signal, a first reference voltage is supplied to a second node via the turned-on second transistor, wherein the second node is disposed between the driving transistor and the capacitor, wherein the capacitor is disposed between the first and second nodes.

[0017] The device may further comprise: a third transistor, wherein when the third transistor turns on based on an emission signal, a second reference voltage is supplied to the first node via the turned-on third transistor; a fourth transistor disposed between and coupled to the second node and a third node, wherein the driving transistor is disposed between the first driving power supply line and the third node, wherein the fourth transistor turns on based on the i-th scan signal; a fifth transistor disposed between and coupled to the third node and an anode of the organic light-emitting element, wherein the fifth transistor turns on based on the emission signal; and a sixth transistor, wherein when the sixth transistor turns on based on the i-th scan signal, the first reference voltage is supplied to a fourth node via the turned-on sixth transistor, wherein the fourth node is disposed between the fifth transistor and the anode, wherein one of first and second electrodes of the driving transistor is connected to the first driving power supply line, while the other of the first and second electrodes of the driving transistor is connected to the third node, wherein a cathode of the organic light-emitting element is connected to the second driving power supply line.

[0018] The device may further comprise a seventh transistor, wherein when the seventh transistor turns on based on the (i-1)-th scan signal, the second reference voltage is supplied to the first node via the turned-on seventh transistor.

[0019] The first and second reference voltages may have different voltage levels, wherein the second transistor is coupled to a first reference power supply line for supplying the first reference voltage, wherein the third transistor is coupled to a second reference power supply line for supplying the second reference voltage.

[0020] The first and second reference voltages may have different voltage levels, wherein the first reference voltage have the same voltage level as a voltage level of the second driving voltage, wherein the second transistor is connected to the second driving power supply line, wherein the third transistor is coupled to a reference power supply line, wherein the reference power supply line supplies the second reference voltage different from the first reference voltage.

[0021] The first reference voltage may be provided by the second driving power supply line.

[0022] The first and second reference voltages may have the same voltage level, wherein the second and third transistors are connected to first and second reference power supply lines respectively, wherein the first and second reference power supply lines supply the first and second reference voltages respectively.

[0023] The first and second reference voltages may have the same voltage level, wherein the second and third transistors are connected to first and second reference power supply lines respectively, wherein the first and second reference power supply lines supply the first and second reference voltages respectively.

[0024] For a first period, the (i-1)-th scan signal may be supplied at a turn-on level, while each of the i-th scan signal and the emission signal is supplied at a turn-off level, wherein for a second period, the i-th scan signal is supplied at a turn-on level, while each of the (i-1)-th scan signal and the emission signal is supplied at a turn-off level, wherein for a third period, all of the (i-1)-th scan signal, the i-th scan signal, and the emission signal are supplied at a turn-off level, wherein for a fourth period, the emission signal is supplied at a turn-on level, while each of the (i-1)-th scan signal and the i-th scan signal is supplied at a turn-off level.

[0025] In another aspect of the present disclosure, there is provided a method for driving an organic light-emitting display device, wherein the device includes an organic light-emitting element; a driving transistor connected in series with the organic light-emitting element, wherein the driving transistor and the organic light-emitting element are disposed between and are connected to first and second driving power supply lines, wherein the first driving power supply line supplies first driving voltage and the second driving power supply line supplies second driving voltage which is lower than the first driving voltage; a first transistor, wherein when the first transistor turns on, a data voltage is supplied to a first node via the turned-on first transistor; a capacitor disposed between the first node and a gate electrode of the driving transistor; and a second transistor connected to a second node, wherein the second node is disposed between a gate electrode of the driving transistor and the capacitor, wherein the capacitor is disposed between the first and second nodes, wherein the method comprises: initializing the second node to a first reference voltage by turning on the second transistor for a first period; and turning off

the second transistor and supplying the data voltage to the first node by turning on the first transistor for a second period.

[0026] The organic light-emitting display device may further include; a third transistor coupled to the first node; a fourth transistor disposed between the second node and the third node, wherein the third node is disposed between the emitting element and driving transistor; a fifth transistor coupled to and disposed between the third node and an anode of the organic light-emitting element; and a sixth transistor coupled to a fourth node between the fifth transistor and the anode, wherein the method further comprises: turning on the fourth transistor for the second period, to sample the second node using a difference voltage between the first driving voltage supplied from the first driving power supply and a threshold voltage of the driving transistor; and supplying the first reference voltage by turning on the sixth transistor to the fourth node.

[0027] The method may further comprise: turning off the first to sixth transistors and boosting a potential of the second node for a third period; for a fourth period, turning on the driving transistor based on a turn-on signal corresponding to the potential of the second node; turning on the third transistor to supply a second reference voltage to the first node; and turning on the fifth transistor such that a driving current from the turned-on driving transistor is supplied to the organic light-emitting element.

[0028] The organic light-emitting display device may further comprise a seventh transistor coupled to the first node, wherein the method further comprises initializing the first node to the second reference voltage by turning on the seventh transistor for the first period.

[0029] The first and second reference voltages may have different voltage levels.

[0030] The first reference voltage may have the same voltage level as a voltage level of the second driving voltage.

[0031] The first and second reference voltages may have the same voltage level. Herein, the first period may be referred to as an initialization period, or an initial period. The second period may be referred to as a sampling period. The third period may be referred to as a boosting period. The fourth period may be referred to as an emission period.

[0032] An organic light-emitting display device according to one example of the present disclosure includes the transistor for initializing the node between the driving transistor and the capacitor to the reference voltage for an initialization period. In this connection, the transistor is turned on based on the signal (i-1)-th scan signal corresponding to the previous scan-line. This prevents a short circuit between the initialization power supply for supplying the reference voltage and the high potential driving power supply for the initialization period. This may suppress ripples in the initialization power supply. Thus, this may prevent the initialization driving failure due to the ripple in the power supply and may remove the luminance deviation between the pixels. This may suppress stains and abnormal luminance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033]

Figure 1 illustrates an organic light-emitting display device according to a first example of the present disclosure.

Figure 2 shows an equivalent circuit corresponding to any one pixel in an organic light-emitting display device according to the first example of the present disclosure.

Figure 3 shows a waveform of a driving signal in Figure 2 and an associated potential at each node.

Figure 4 shows an equivalent circuit corresponding to any one pixel in an organic light-emitting display device according to a second example of the present disclosure.

Figure 5 shows a waveform of a driving signal in Figure 4 and an associated potential at each node.

Figure 6 shows an equivalent circuit corresponding to any one pixel in an organic light-emitting display device according to a third example of the present disclosure.

Figure 7 shows an equivalent circuit corresponding to any one pixel in an organic light-emitting display device according to a fourth example of the present disclosure.

DETAILED DESCRIPTIONS

[0034] For simplicity and clarity of illustration, elements in the figures are not necessarily drawn to scale. The same reference numbers in different figures denote the same or similar elements, and as such perform similar functionality. Also, descriptions and details of well-known steps and elements are omitted for simplicity of the description. Furthermore, in the following detailed description of the present disclosure, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. However, it will be understood that the present disclosure may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present disclosure.

[0035] Examples of various examples are illustrated and described further below. It will be understood that the description herein is not intended to limit the claims to the specific examples described. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the scope of the present disclosure as defined by the appended claims.

[0036] It will be understood that, although the terms "first", "second", "third", and so on may be used herein to describe various elements, components, regions, lay-

ers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section described below could be termed a second element, component, region, layer or section, without departing from the scope of the present disclosure.

[0037] It will be understood that when an element or layer is referred to as being "connected to", or "coupled to" another element or layer, it can be directly on, connected to, or coupled to the other element or layer, or one or more intervening elements or layers may be present. In addition, it will also be understood that when an element or layer is referred to as being "between" two elements or layers, it can be the only element or layer between the two elements or layers, or one or more intervening elements or layers may also be present.

[0038] The terminology used herein is for the purpose of describing particular examples only and is not intended to be limiting of the present disclosure. As used herein, the singular forms "a" and "an" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises", "comprising", "includes", and "including" when used in this specification, specify the presence of the stated features, integers, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, operations, elements, components, and/or portions thereof. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. Expression such as "at least one of' when preceding a list of elements may modify the entire list of elements and may not modify the individual elements of the list.

[0039] Unless otherwise defined, all terms including technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this inventive concept belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0040] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. The present disclosure may be practiced without some or all of these specific details. In other instances, well-known process structures and/or processes have not been described in detail in order not to unnecessarily obscure the present disclosure.

[0041] Hereinafter, an organic light-emitting display device according to each example of the present disclosure and a method for driving the device will be described in detail with reference to the accompanying drawings.

[0042] First, an organic light-emitting display device according to a first example of the present disclosure and a method for driving the device will be described with reference to FIGS. 1 to 3.

[0043] Figure 1 illustrates an organic light-emitting display device according to a first example of the present disclosure. Figure 2 shows an equivalent circuit corresponding to any one pixel in an organic light-emitting display device according to the first example of the present disclosure. Figure 3 shows a waveform of a driving signal in Figure 2 and an associated potential at each node.

[0044] As illustrated in Figure 1, an organic light-emitting display device 10 according to a first example of the present disclosure includes a display panel 10 including a plurality of pixel PXLs, a data driving circuit 12 for driving data-lines 14 of the display panel 10, a gate driving circuit 13 for driving scan-lines 15 of the display panel 10, and a timing controller 11 for controlling the driving timing of the data driving circuit 12 and the gate driving circuit 13

[0045] The display panel 10 includes scan-lines 15 and data-lines 14 that intersect with each other. A plurality of pixel regions corresponding to the plurality of pixel PXLs respectively are defined as the intersection regions between the scan-lines 15 and the data-lines 14, respectively. As a result, the plurality of pixel regions are arranged in a matrix form in the display region.

[0046] Further, the display panel 10 further includes, per each horizontal line of the plurality of pixel PXLs, an emission-line for supplying an emission signal EM, a first driving power supply line for supplying a first driving voltage VDD, a second driving power supply line for supplying a second driving voltage VSS having a potential lower than the first driving voltage VDD, a reference power supply line for supplying a reference voltage VREF via an initialization power supply.

[0047] In this connection, the reference voltage VREF is set to a potential lower than a trigger voltage of the organic light-emitting element. In one example, the display panel 10 may include first and second reference power supply lines connected to first and second initialization power supplies, respectively, for supplying first and second reference voltages having different voltage levels.

[0048] The timing controller 11 rearranges digital video data RGB input from the outside based on a resolution of the display panel 10. The controller 11 supplies the rearranged digital video data RGB' to the data driving circuit 12.

[0049] Further, the timing controller 11 generates and output a data control signal DDC for controlling operation timing of the data driving circuit 12, and a gate control signal GDC for controlling operation timing of the gate driving circuit 13, based on timing signals such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a dot clock signal DCLK, and a data enable signal DE, etc.

[0050] The data driving circuit 12 converts the rearranged digital video data RGB' into an analog data volt-

age based on the data control signal DDC. Further, the data driving circuit 12 supplies a data signal (VDATA in FIG. 2) to the pixels in each horizontal line for each horizontal period based on the rearranged digital video data RGB'.

[0051] The gate driving circuit 13 may generate a scan signal SCAN and an emission signal EM based on the gate control signal GDC. The gate driving circuit 13 may include a scan drive unit and an emission drive unit. The scan drive unit may sequentially supply a scan signal SCAN to the scan lines in each horizontal line. The emission drive unit may supply the emission signal EM to the emission lines in each horizontal line for each horizontal period.

[0052] The gate driving circuit 13 may be disposed in a non-display region in the display panel 10 in a GIP (Gate-Driver In Panel) mode.

[0053] As illustrated in FIG. 2, in the organic light-emitting display device 10 according to the first example, each of the plurality of pixel PXLs includes an organic light-emitting element OLED, a driving transistor DT, first to sixth transistors T1, T2, T3, T4, T5, and T6, and a capacitor Cst.

[0054] In each pixel PXL, the driving transistor DT, the first transistor T1, and the capacitor Cst together define a pixel driving circuit for supplying driving current to the organic light-emitting element OLED for each frame, while the remaining second to sixth transistors T2 to T6 together define a compensation circuit for compensating the threshold voltage of the driving transistor DT.

[0055] The pixel illustrated in Figure 2 may be one of pixels arranged in the i-th horizontal line among a plurality of pixels. In this connection, i is greater than 2, is a natural number smaller than N, and N is the total number of horizontal lines.

[0056] The organic light-emitting element OLED may include an anode and a cathode, and an organic light-emitting layer disposed therebetween. By way of example, the organic light-emitting layer includes a hole injection layer, a hole transport layer, a light emitting layer, and an electron transport layer. Alternatively, the organic light-emitting layer may further include an electron injection layer.

[0057] The driving transistor DT is connected in series with the organic light-emitting element OLED and is disposed between the first driving power supply line for supplying the first driving voltage VDD and the second driving power supply line for supplying the second driving voltage VSS having a potential lower than the first driving power supply.

[0058] In the driving transistor DT, a gate electrode thereof is connected to the capacitor Cst. One of first and second electrodes (source electrode and drain electrode) thereof is connected to the first driving power supply VDD, while the other thereof is connected to a third node N3.

[0059] When this driving transistor DT turns on based on a turn-on signal supplied from the capacitor Cst, the organic light-emitting element OLED is supplied with the driving current.

[0060] When a first transistor T1 is turned on based on an i-th scan signal SCAN(i) (i is a natural number larger than 2 and smaller than N), the data voltage VDATA is supplied to the first node N1.

[0061] In this first transistor T1, a gate electrode thereof is connected to an i-th scan-line for supplying the i-th scan signal SCAN(i). One of first and second electrodes (source electrode and drain electrode) thereof, for example, the source electrode, is connected to a data-line for supplying the data voltage VDATA, while the other thereof, for example, the drain electrode, is connected to the first node N1. The first node N1 is a joint point between the first transistor T1 and the capacitor Cst.

[0062] The capacitor Cst is connected between the first node N1 and a second node N2. The second node N2 is a joint point between the capacitor Cst and the driving transistor DT.

[0063] That is, a first electrode of the capacitor Cst is connected to the first node N1 receiving the data voltage VDATA via the first transistor T1, while a second electrode of the capacitor Cst is connected to the second node N2 corresponding to the gate electrode of the driving transistor DT.

[0064] This capacitor Cst supplies the turn-on signal to the gate electrode of the driving transistor DT at least based on the data voltage VDATA.

[0065] When the second transistor T2 turns on based on an (i-1)-th scan signal SCAN(i-1), a reference voltage VREF is supplied to the second node N2. In this connection, the (i-1)-th scan signal SCAN(i-1) is a signal supplied via a (i-1)-th scan-line corresponding to a previous horizontal line.

[0066] A gate electrode of the second transistor T2 is connected to the (i-1)-th scan-line for supplying the (i-1)-th scan signal SCAN(i-1). One of first and second electrodes (source and drain electrodes) of the second transistor T2, for example, the source electrode, is connected to a reference power supply line for supplying the reference voltage VREF, while the other thereof, for example, the drain electrode, is connected to the second node N2.

[0067] When a third transistor T3 turns on based on an emission signal EM(i) corresponding to the i-th horizontal line, the reference voltage VREF is supplied to the first node N1.

[0068] A gate electrode of the third transistor T3 is connected to the i-th emission-line for supplying the emission signal EM(i). One of first and second electrodes (source and drain electrodes) of the transistor T3, for example, the source electrode, is connected to the reference power supply line for supplying the reference voltage VREF, while the other thereof, for example, the drain electrode, is connected to the first node N1.

[0069] A fourth transistor T4 is connected between the second node N2 and the third node N3, and turns on based on the i-th scan signal SCAN(i).

[0070] The second node N2 corresponds to the gate

electrode of the driving transistor DT. The third node N3 corresponds to the second electrode of the driving transistor DT, for example, the drain electrode, which is not connected to the first driving power supply VDD. That is, the fourth transistor T4 is disposed between the gate electrode and the drain electrode of the driving transistor DT.

[0071] Specifically, a gate electrode of the fourth transistor T4 is connected to the i-th scan-line for supplying the i-th scan signal SCAN(i). One of first and second electrodes (source and drain electrodes) of the transistor T4, for example, the source electrode, is connected to the third 3 node N3, while the other thereof, for example, the drain electrode is coupled to the 2 node N2.

[0072] When the fourth transistor T4 turns on, the gate electrode and the drain electrode of the driving transistor DT are connected to each other. As a result, a potential of the gate electrode of the driving transistor DT becomes close to a threshold voltage. In this connection, a difference voltage VDD-Vth between the first driving voltage VDD of the first driving power supply line and the threshold voltage of the driving transistor DT is supplied to the third node N3 via the driving transistor DT. Further, the difference voltage VDD-Vth of the third node N3 is supplied to the second node N2 via the turned-on fourth transistor T4.

[0073] The fifth transistor T5 is connected between the third node N3 and the anode of the organic light-emitting element OLED. The fifth transistor T5 turns on based on the emission signal EM(i).

[0074] A gate electrode of the fifth transistor T5 is connected to the i-th emission-line for supplying the emission signal EM(i). One of first and second electrodes (source electrode and drain electrode) of the fifth transistor T5, for example, the source electrode, is connected to the third node N3, while the other thereof, for example, the drain electrode, is connected to the anode of the organic light-emitting element OLED.

[0075] The cathode of the organic light-emitting element OLED is connected to the second driving power supply line which supplies the second driving voltage VSS.

[0076] When a sixth transistor T6 is turned on based on the i-th scan signal SCAN(i), the reference voltage VREF is supplied to a fourth node N4. The fourth node N4 is a joint point between the fifth transistor T5 and the organic light-emitting element OLED.

[0077] A gate electrode of the sixth transistor T6 is connected to the i-th scan-line for supplying the i-th scan signal SCAN(i). One of first and second electrodes (source electrode and drain electrode) of the sixth transistor T6, for example, the source electrode is connected to the reference power supply line, while the other thereof, for example, the drain electrode, is connected to the fourth node N4.

[0078] As illustrated in Figure 3, for an initialization period (Initial), the (i-1)-th scan signal SCAN (i-1), the i-th scan signal SCAN(i), and the emission signal EM(i) is supplied to the corresponding pixel PXL from the gate driving circuit (13 of FIG. 1). In this connection, the (i-1)-th scan signal SCAN(i-1) is supplied at a turn-on level (low level in FIG. 3), while each of the i-th scan signal SCAN(i) and the emission signal EM(i) is supplied at a turn-off level (high level in Figure 3).

[0079] Thus, the second transistor T2 is turned on based on the (i-1)-th scan signal SCAN(i-1) at the turn-on level. Thus, via the turn-on second transistor T2, a potential of the second node N2 is initialized to the reference voltage VREF.

[0080] For a sampling period (Sampling), the i-th scan signal SCAN(i) is supplied at a turn-on level (low level in FIG. 3), while each of the (i-1)-th scan signal SCAN(i-1) and emission signal EM(i) is supplied at a turn-off level (high level in FIG. 3).

[0081] Thus, the second transistor T2 is turned off based on the (i-1)-th scan signal SCAN(i-1) at the turn-off level.

[0082] Further, the first transistor T1, the fourth transistor T4 and the sixth transistor T6 are turned on based on the i-th scan signal SCAN(i) at the turn-on level.

[0083] The data voltage VDATA is supplied to the first node N1 via the turned-on first transistor T1. That is, the data voltage VDATA is supplied to one end of the capacitor Cst.

[0084] A potential of the gate electrode of the driving transistor DT is gradually changed to be close to the threshold voltage of the driving transistor DT via the turned-on fourth transistor T4. Thus, the difference voltage VDD-Vth between the first driving voltage VDD and the threshold voltage Vth of the driving transistor DT is supplied to the second node N2 via the driving transistor DT and the fourth transistor T4.

[0085] The reference voltage VREF is supplied to the fourth node N4 via the sixth transistor T6 which has been turned-on. This prevents the driving of the organic light-emitting element OLED for the sampling period (Sampling).

[0086] For a boosting period (Boosting), all of the (i-1)-th scan signal SCAN(i-1), the i-th scan signal SCAN(i) and the i-th emission signal EM(i) are supplied at a turn-off level. Thus, all of the first to sixth transistors T1, T2, T3, T4, T5, and T6, including the first, fourth, and sixth transistors T1, T4, and T6 are turned off.

[0087] In this connection, the potential of the second node N2 is boosted by parasitic capacitances of the capacitor Cst and of the fourth transistor T4.

[0088] Further, for an emission period (Emission), the emission signal EM(i) is supplied at turn-on level, while each of the (i-1)-th scan signal SCAN(i-1) and the i-th scan signal SCAN(i) is supplied at a turn-off level.

[0089] Thus, the third transistor T3 and the fifth transistor T5 are turned on based on the emission signal EM (i) at the turn-on level.

[0090] In this connection, the reference voltage VREF is supplied to the first node N1 via the third transistor T3 which has been turned on. As a result, a potential of the

first node N1 changes from the data voltage VDATA to the reference voltage VREF (ΔV = VDATA-VREF). Thus, a voltage of the second node N2 is decreased from the voltage VDD-Vth in the sampling period by the voltage change ΔV = VDATA-VREF of the first node.

[0091] The driving current of the driving transistor DT corresponding to the voltage of the second node is supplied to the organic light-emitting element OLED via the fifth transistor T5 which has been turned-on.

[0092] In this way, according to a first example of the present disclosure, for the initialization period (Initial in Figure 3), the present configuration may turn the second transistor T2, and, thus, initialize the second node N2, that is, the second electrode of the capacitor Cst, and the gate electrode of the driving transistor DT to the reference voltage VREF.

[0093] In this connection, the second transistor T2 is turned on based on the (i-1)-th scan signal SCAN(i-1), unlike the first, fourth and sixth transistors T1, T4 and T6. That is, when the second transistor T2 is turned on, the first, fourth, and sixth transistors T1, T4, and T6 are not turned on.

[0094] Thus, for the initialization period, a current path including the driving transistor DT, the fourth and sixth transistors T4 and T6 may be suppressed. Thus, the first driving power supply for supplying the first driving voltage VDD and the initialization power supply for supplying the reference voltage VREF are prevented from being connected to each other. As a result, the ripple in the initialization power supply may be suppressed.

[0095] Further, for the initialization period (Initial in FIG. 3), in order to initialize the second electrode of the capacitor Cst and the gate electrode of the driving transistor DT to the reference voltage VREF, the second transistor T2 may be turned on in a response to the (i-1)-th scan signal SCAN(i-1), i.e., a signal supplied through a scan line corresponding to a previous horizontal line.

[0096] Therefore, separate signal line and signal supply unit for supplying the signal for turning on the second transistor T2 and are unnecessary. That is, since the gate driving circuit (13 in Fig. 1) may be implemented as a scan drive unit and an emission drive unit corresponding to each horizontal line, the gate driving circuit 13 may be designed simply and easily. As a result, a width of a bezel region in the organic light-emitting display device may be reduced due to the GIP-based gate driving circuit 13.

[0097] For the initialization period (Initial), the potential of the second node N2 is initialized to the reference voltage VREF, while the potential of the first node N1 is in a floating state (floating).

[0098] Thus, for the initialization period (Initial), a charging voltage of the capacitor Cst in a previous frame ((k-1)-th frame) is not properly initialized.

[0099] Therefore, there is a problem that the potential of the second node N2 fluctuates depending on a luminance in the previous frame ((k-1)-th frame) at an initial timing of the sampling period.

[0100] Specifically, as shown by a relatively thin solid line with respect to the potential of the second node N2 in FIG. 3, there is a problem that the potential of the second node N2 may have an overshoot waveform at an initial point of the sampling period, especially when a black luminance is expressed in the previous frame ((k-1)-th frame).

[0101] Therefore, according to the first example, a luminance difference occurs between horizontal lines depending on the luminance in the previous frame ((k-1)-th frame).

[0102] To solve this problem, in accordance with the present disclosure, a second example is provided in which both potentials of the first and second nodes N1 and N2 are initialized for the initialization period (Initial).

[0103] Figure 4 shows an equivalent circuit corresponding to any one pixel in an organic light-emitting display device according to the second example of the present disclosure. Figure 5 shows a waveform of a driving signal in Figure 4 and an associated potential at each node.

[0104] As illustrated in Figure 4, the organic light-emitting display device according to the second example of the present disclosure further includes a seventh transistor T7. When the seventh transistor T7 is turned on based on the (i-1)-th scan signal SCAN(i-1), the reference voltage VREF is supplied to the first node N1 via the turned-on seventh transistor T7. Except for the presence of the seventh transistor T7, a configuration of the second example is the same as that of the first example illustrated in Figures 1 to 3. Therefore, the descriptions of the overlapping portions between the first and second examples may be omitted.

[0105] As illustrated in Figure 4, the seventh transistor T7 is connected between the first node N1 and the reference power supply line for supplying the reference voltage VREF.

[0106] A gate electrode of the seventh transistor T7 is connected to the (i-1)-th scan line for supplying the (i-1)-th scan signal SCAN(i-1). One of first and second electrodes (source electrode and drain electrode) of the seventh transistor T7, for example, the source electrode is connected to the reference power supply line for supplying the reference voltage VREF, while the other thereof, for example, the drain electrode, is connected to the first node N1.

[0107] Further, as illustrated in FIG. 5, for the initialization period (Initial), each of the second transistor T2 and the seventh transistor T7 is turned on based on the (i-1)-th scan signal SCAN (i-1) at the turn-on level.

[0108] Thus, the potential of the second node N2 is initialized to the reference voltage VREF via the turned-on second transistor T2, while the potential of the first node N1 is initialized to the reference voltage VREF via the turned-on seventh transistor T7.

[0109] That is, for the initialization period (Initial), potentials of both ends of the capacitor Cst are initialized to the reference voltage VREF.

[0110] Thus, at the initial time of the sampling period,

the potential of the second node N2 may be prevented from fluctuating depending on the luminance of the previous frame ((k-1)-th frame). Therefore, the luminance difference between horizontal lines depending on the luminance in the previous frame ((k-1)-th frame) may be suppressed.

[0111] Unlike the above first and second examples, in a third example of the present disclosure, a reference voltage for initializing the first node N1 and a reference voltage for initializing the second node N2 may have different voltage levels.

[0112] Figure 6 shows an equivalent circuit corresponding to any one pixel in an organic light-emitting display device according to a third example of the present disclosure.

[0113] As illustrated in Figure 6, in the organic light-emitting display device according to the third example of the present disclosure, when the second transistor T2 turns on, a first reference voltage VREF1 is supplied to the second node N2 via the turned-on transistor t2. At the same time, when the seventh transistor T7 turns on, the first node N1 is supplied with a second reference voltage VREF2 which is different from the first reference voltage VREF1. A configuration of the third example is the same as those of the first and second examples illustrated in Figures 1 to 5, except that, in the third example, the first reference voltage for initializing the first node N1 and the second reference voltage for initializing the second node N2 have different voltage levels. Therefore, the descriptions of the overlapping portions between the first, second, and third examples may be omitted.

[0114] As illustrated in Figure 6, when the second transistor T2 turns on based on the (i-1)-th scan signal SCAN(i-1), the first reference voltage VREF1 is supplied to the second node N2 via the turned-on second transistor.

[0115] To this end, one of first and second electrodes (source and drain electrodes) of the second transistor T2, for example, the source electrode, is connected to a first reference power supply line for supplying the first reference voltage VREF1, while the other thereof, for example, the drain electrode, is connected to the second node N2.

[0116] Further, when the seventh transistor T7 turns on based on the (i-1)-th scan signal SCAN(i-1), the second reference voltage VREF2 is supplied to the first node N1 via the turned-on seventh transistor.

[0117] To this end, one of first and second electrodes (source and drain electrodes) of the seventh transistor T7, for example, the source electrode, is connected to a second reference power supply line for supplying the second reference voltage VREF2, while the other thereof, for example, the drain electrode, is connected to the first node N1.

[0118] In this way, for the initialization period (Initial), the capacitor Cst may be initialized to a difference voltage between the first reference voltage VREF1 and the second reference voltage VREF2.

[0119] As a result, a response speed in the sampling period may be easily adjusted via the first reference voltage VREF1 and the second reference voltage VREF2. Further, the third example may allow easy compensation for degradation in overall pixels over the driving time of the organic light-emitting display device.

[0120] However, the first reference voltage (VREF1 in Figure 6) according to the third example may be set to a range as similar to a range of an operation-trigger voltage of the organic light-emitting element OLED. Alternatively, due to deterioration of the organic light-emitting element OLED, the first reference voltage (VREF1 in FIG. 6) according to the third example may be greater than or equal to the operation-trigger voltage of the organic light-emitting element OLED.

[0121] In this connection, when the first reference voltage (VREF1 in FIG. 6) according to the third example is supplied to the fourth node N4 through an off-current of the sixth transistor T6, there is a problem that the organic light-emitting element OLED may malfunction. In order to solve such a problem, a fourth example is provided according to the present disclosure.

[0122] Figure 7 shows an equivalent circuit corresponding to any one pixel in an organic light-emitting display device according to a fourth example of the present disclosure.

[0123] In an organic light-emitting display device according to the fourth example of the present disclosure, as illustrated in Figure 7, when the second transistor T2 turns on, the second driving voltage VSS instead of the first reference voltage VREF1 is supplied to the second node N2. Further, when the sixth transistor T6 turns on, the second driving voltage VSS instead of the first reference voltage VREF1 is supplied to the fourth node N4. Except for this configuration, a remaining configuration of the fourth example is the same as that of the third example as illustrated in Figure 6. Therefore, the descriptions of the overlapping portions between the third and fourth examples may be omitted.

[0124] As illustrated in Figure 7, when the second transistor T2 turns on based on the (i-1)-th scan signal SCAN(i-1), the second driving voltage VSS is supplied to the second node N2 via the turned-on second transistor.

[0125] To this end, one of first and second electrodes (source and drain electrodes) of the second transistor T2, for example, the source electrode, is connected to the second driving power supply line for supplying the second driving voltage VSS, while, the other thereof, for example, the drain electrode, is connected to the second node N2.

[0126] When the seventh transistor T7 turns on based on the (i-1)-th scan signal SCAN(i-1), the reference voltage VREF is supplied to the first node N1 via the turned-on seventh transistor.

[0127] When the sixth transistor T6 is turned on based on the i-th scan signal SCAN(i), the second driving voltage VSS is supplied to the fourth node N4 via the turned-

on sixth transistor.

[0128] To this end, one of first and second electrodes (source and drain electrodes) of the sixth transistor T6, for example, the source electrode, is connected to the second driving power supply line for supplying the second driving voltage VSS, while the other thereof, for example, the drain electrode, is connected to the fourth node N4.

[0129] In this way, even when the off-current of the sixth transistor T6 occurs, the second driving voltage VSS is supplied to the fourth node N4, that is, the anode of the organic light-emitting element OLED. Therefore, the organic light-emitting element OLED may be prevented from malfunctioning due to the off-current of the sixth transistor T6. Thus, an image quality of the device may be improved.

[0130] In the above description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. The present disclosure may be practiced without some or all of these specific details. Examples of various examples have been illustrated and described above. It will be understood that the description herein is not intended to limit the claims to the specific examples described. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the scope of the present disclosure as defined by the appended claims.

[0131] Also disclosed herein are the following numbered clauses, in which:

Clause 1. An organic light-emitting display device comprising:

an organic light-emitting element;
a driving transistor connected in series with the organic light-emitting element, wherein the driving transistor and the organic light-emitting element are disposed between first and second driving power supply lines, wherein the first driving power supply line supplies first driving voltage and the second driving power supply line supplies second driving voltage which is lower than the first driving voltage;
a first transistor, wherein when the first transistor turns on based on an i-th scan signal, a data voltage is supplied to a first node via the turned-on first transistor, wherein i is a natural number equal to or greater than 2 and smaller than or equal to N, wherein N is a number of scan-lines;
a capacitor disposed between the first node and a gate electrode of the driving transistor, wherein the capacitor supplies a turn-on signal of the driving transistor to the gate electrode of the driving transistor based on the data voltage; and
a second transistor, wherein when the second transistor turns on based on a (i-1)-th scan signal, a first reference voltage is supplied to a second node via the turned-on second transistor, wherein the second node is disposed between the driving transistor and the capacitor, wherein the capacitor is disposed between the first and second nodes.

Clause 2. The device of clause 1, further comprising:

a third transistor, wherein when the third transistor turns on based on an emission signal, a second reference voltage is supplied to the first node via the turned-on third transistor;
a fourth transistor disposed between the second node and a third node, wherein the driving transistor is disposed between the first driving power supply line and the third node, wherein the fourth transistor turns on based on the i-th scan signal;
a fifth transistor disposed between the third node and an anode of the organic light-emitting element, wherein the fifth transistor turns on based on the emission signal; and
a sixth transistor, wherein when the sixth transistor turns on based on the i-th scan signal, the first reference voltage is supplied to a fourth node via the turned-on sixth transistor, wherein the fourth node is disposed between the fifth transistor and the anode,
wherein one of first and second electrodes of the driving transistor is connected to the first driving power supply line, while the other of the first and second electrodes of the driving transistor is connected to the third node,
wherein a cathode of the organic light-emitting element is connected to the second driving power supply line.

Clause 3. The device of clause 2, further comprising a seventh transistor, wherein when the seventh transistor turns on based on the (i-1)-th scan signal, the second reference voltage is supplied to the first node via the turned-on seventh transistor.

Clause 4. The device of clause 2 or clause 3,
wherein the first and second reference voltages have different voltage levels,
wherein the second transistor is coupled to a first reference power supply line for supplying the first reference voltage,
wherein the third transistor is coupled to a second reference power supply line for supplying the second reference voltage.

Clause 5. The device of clause 2 or clause 3,
wherein the first and second reference voltages have different voltage levels,
wherein the first reference voltage have the same voltage level as a voltage level of the second driving voltage,
wherein the second transistor is connected to the second driving power supply line,
wherein the third transistor is coupled to a reference

power supply line.

Clause 6. The device of clause 2 or clause 3,
wherein the first and second reference voltages have the same voltage level,
wherein the second and third transistors are connected to first and second reference power supply lines respectively, wherein the first and second reference power supply lines supply the first and second reference voltages respectively.

Clause 7. The device of claim 2 or clause 3,
wherein the first and second reference voltages have the same voltage level,
wherein the second and third transistors are connected to first and second reference power supply lines respectively, wherein the first and second reference power supply lines supply the first and second reference voltages respectively.

Clause 8. The device of any of clauses 2 to 6,
wherein for a first period, the (i-1)-th scan signal is supplied at aturn-on level, while each of the i-th scan signal and the emission signal is supplied at a turn-off level,
wherein for a second period, the i-th scan signal is supplied at a turn-on level, while each of the (i-1)-th scan signal and the emission signal is supplied at a turn-off level,
wherein for a third period, all of the (i-1)-th scan signal, the i-th scan signal, and the emission signal are supplied at a turn-off level,
wherein for a fourth period, the emission signal is supplied at a turn-on level, while each of the (i-1)-th scan signal and the i-th scan signal is supplied at a turn-off level.

Clause 9. The device of any of clauses 2 to 7,
wherein for a first period, the (i-1)-th scan signal is supplied at a turn-on level, while each of the i-th scan signal and the emission signal is supplied at a turn-off level,
wherein for a second period, the i-th scan signal is supplied at a turn-on level, while each of the (i-1)-th scan signal and the emission signal is supplied at a turn-off level,
wherein for a third period, all of the (i-1)-th scan signal, the i-th scan signal, and the emission signal are supplied at a turn-off level,
wherein for a fourth period, the emission signal is supplied at a turn-on level, while each of the (i-1)-th scan signal and the i-th scan signal is supplied at a turn-off level.

Clause 10. A method for driving an organic light-emitting display device,
wherein the device includes an organic light-emitting element; a driving transistor connected in series with the organic light-emitting element, wherein the driving transistor and the organic light-emitting element are disposed between first and second driving power supply lines, wherein the first driving power supply line supplies first driving voltage and the second driving power supply line supplies second driving voltage which is lower than the first driving voltage; a first transistor, wherein when the first transistor turns on, a data voltage is supplied to a first node via the turned-on first transistor; a capacitor disposed between the first node and a gate electrode of the driving transistor; and a second transistor connected to a second node, wherein the second node is disposed between a gate electrode of the driving transistor and the capacitor, wherein the capacitor is disposed between the first and second nodes,
wherein the method comprises:

initializing the second node to a first reference voltage by turning on the second transistor for a first period; and
supplying the data voltage to the first node by turning off the second transistor and turning on the first transistor for a second period.

Clause 11. The method of clause 10,
wherein the organic light-emitting display device further includes; a third transistor coupled to the first node; a fourth transistor disposed between the second node and the third node, wherein the driving transistor is disposed between the first driving power supply line and the third node; a fifth transistor disposed between the third node and an anode of the organic light-emitting element; and a sixth transistor coupled to a fourth node, wherein the fourth node is disposed between the fifth transistor and the anode,
wherein the method further comprises:
for the second period, sampling the second node using a difference voltage between the first driving voltage supplied from the first driving power supply line and a threshold voltage of the driving transistor by turning on the fourth transistor, while supplying the first reference voltage to the fourth node by turning on the sixth transistor.

Clause 12. The method of clause 11, wherein the method further comprises:

turning off the first to sixth transistors and boosting a potential of the second node for a third period;
for a fourth period, turning on the driving transistor based on a turn-on signal corresponding to the potential of the second node, turning on the third transistor to supply a second reference voltage to the first node, and turning on the fifth transistor such that a driving current from the turned-on driving transistor is supplied to the organic light-emitting element.

Clause 13. The method of clause 12,
wherein the organic light-emitting display device further comprises a seventh transistor coupled to the first node,

wherein the method further comprises initializing the first node to the second reference voltage by turning on the seventh transistor for the first period.

Clause 13. The method of clause 12, wherein the first and second reference voltages have different voltage levels.

Clause 15. The method of clause 14, wherein the first reference voltage has the same voltage level as a voltage level of the second driving voltage.

Clause 16. The method of clause 12 or clause 13, wherein the first and second reference voltages have the same voltage level.

Clause 17. The method of clause 13, wherein the first and second reference voltages have the same voltage level.

Claims

1. An organic light-emitting display device (10) comprising:

an organic light-emitting element (OLED);
a driving transistor (DT) connected in series with the organic light-emitting element, wherein the driving transistor and the organic light-emitting element are disposed between first and second driving power supply lines, wherein the first driving power supply line supplies first driving voltage (VDD) and the second driving power supply line supplies second driving voltage (VSS) which is lower than the first driving voltage;
a first transistor (T1), wherein when the first transistor turns on based on an i-th scan signal (SCAN(i)), a data voltage (VDATA) is supplied to a first node (N1) via the turned-on first transistor, wherein i is a natural number equal to or greater than 2 and smaller than or equal to N, wherein N is a number of scan-lines;
a capacitor (Cst) disposed between the first node (N1) and a gate electrode of the driving transistor (DT), wherein the capacitor (Cst) supplies a turn-on signal to the gate electrode of the driving transistor based on the data voltage (VDATA); and
a second transistor (T2), wherein when the second transistor turns on based on a (i-1)-th scan signal (SCAN(i-1)), a first reference voltage (VSS, VREF or VREF1) is supplied to a second node (N2) via the turned-on second transistor (T2), wherein the second node (N2) is disposed between the driving transistor (DT) and the capacitor (Cst), wherein the capacitor (Cst) is disposed between the first and second nodes (N1, N2).

2. The device of claim 1, further comprising:

a third transistor (T3), wherein when the third transistor turns on based on an emission signal (EM(i)), a second reference voltage (VREF2) is supplied to the first node (N1) via the turned-on third transistor;
a fourth transistor (T4) disposed between the second node (N2) and a third node (N3), wherein the driving transistor (DT) is disposed between the first driving power supply line and the third node, wherein the fourth transistor turns on based on the i-th scan signal (SCAN(i));
a fifth transistor (T5) disposed between the third node (N3) and an anode of the organic light-emitting element (OLED), wherein the fifth transistor turns on based on the emission signal (EM(i)); and
a sixth transistor (T6), wherein when the sixth transistor turns on based on the i-th scan signal (SCAN(i)), the first reference voltage is supplied to a fourth node (N4) via the turned-on sixth transistor, wherein the fourth node (N4) is disposed between the fifth transistor (T5) and the anode of the organic light-emitting diode (OLED),
wherein one of first and second electrodes of the driving transistor (DT) is connected to the first driving power supply line, while the other of the first and second electrodes of the driving transistor is connected to the third node (N3),
wherein a cathode of the organic light-emitting element (OLED) is connected to the second driving power supply line.

3. The device of claim 2, further comprising a seventh transistor (T7), wherein when the seventh transistor (T7) turns on based on the (i-1)-th scan signal (SCAN(i-1)), the second reference voltage (VREF2) is supplied to the first node (N1) via the turned-on seventh transistor.

4. The device of claim 2 or claim 3,
wherein the first and second reference voltages (VREF1, VREF2) have different voltage levels,
wherein the second transistor (T2) is coupled to a first reference power supply line for supplying the first reference voltage,
wherein the third transistor (T3) is coupled to a second reference power supply line for supplying the second reference voltage.

5. The device of claim 2 or claim 3,
wherein the first and second reference voltages (VREF1, VREF2) have different voltage levels,
wherein the first reference voltage (VREF1) has the same voltage level as a voltage level of the second driving voltage (VSS),
wherein the second transistor (T2) is connected to the second driving power supply line,
wherein the third transistor (T3) is coupled to a ref-

erence power supply line.

6. The device of claim 2 or claim 3,
wherein the first and second reference voltages (VREF1, VREF2) have the same voltage level,
wherein the second and third transistors (T2, T3) are connected to first and second reference power supply lines respectively, wherein the first and second reference power supply lines supply the first and second reference voltages (VREF1, VREF2) respectively.

7. The device of any of claims 2 to 6,
wherein for a first period, the (i-1)-th scan signal (SCAN(i-1)) is supplied at a turn-on level, while each of the i-th scan signal (SCAN(i)) and the emission signal (EM(i)) is supplied at a turn-off level,
wherein for a second period, the i-th scan signal (SCAN(i)) is supplied at a turn-on level, while each of the (i-1)-th scan signal (SCAN(i-1)) and the emission signal (EM(i)) is supplied at a turn-off level,
wherein for a third period, all of the (i-1)-th scan signal (SCAN(i-1)), the i-th scan signal (SCAN(i)), and the emission signal (EM(i)) are supplied at a turn-off level,
wherein for a fourth period, the emission signal (EM(i)) is supplied at a turn-on level, while each of the (i-1)-th scan signal (SCAN(i-1)) and the i-th scan signal (SCAN(i)) is supplied at a turn-off level.

8. The device of any of claims 2 to 7,
wherein for a first period, the (i-1)-th scan signal (SCAN(i-1)) is supplied at a turn-on level, while each of the i-th scan signal (SCAN(i)) and the emission signal (EM(i)) is supplied at a turn-off level,
wherein for a second period, the i-th scan signal (SCAN(i)) is supplied at a turn-on level, while each of the (i-1)-th scan signal (SCAN(i-1)) and the emission signal (EM(i)) is supplied at a turn-off level,
wherein for a third period, all of the (i-1)-th scan signal (SCAN(i-1)), the i-th scan signal (SCAN(i)), and the emission signal (EM(i)) are supplied at a turn-off level,
wherein for a fourth period, the emission signal (EM(i)) is supplied at a turn-on level, while each of the (i-1)-th scan signal (SCAN(i-1)) and the i-th scan signal (SCAN(i)) is supplied at a turn-off level.

9. A method for driving an organic light-emitting display device,
wherein the device (10) includes an organic light-emitting element (OLED); a driving transistor (DT) connected in series with the organic light-emitting element, wherein the driving transistor and the organic light-emitting element are disposed between first and second driving power supply lines, wherein the first driving power supply line supplies first driving voltage (VDD) and the second driving power supply line supplies second driving voltage (VSS) which is lower than the first driving voltage; a first transistor (T1), wherein when the first transistor (T1) turns on, a data voltage (VDATA) is supplied to a first node (N1) via the turned-on first transistor; a capacitor (Cst) disposed between the first node (N1) and a gate electrode of the driving transistor (DT); and a second transistor (T2) connected to a second node (N2), wherein the second node (N2) is disposed between a gate electrode of the driving transistor (DT) and the capacitor (Cst), wherein the capacitor (Cst) is disposed between the first and second nodes (N1, N2),
wherein the method comprises:

initializing the second node (N2) to a first reference voltage (VREF, VREF1) by turning on the second transistor (T1) for a first period; and
supplying the data voltage (VDATA) to the first node (N1) by turning off the second transistor (T2) and turning on the first transistor (T1) for a second period.

10. The method of claim 9,
wherein the organic light-emitting display device further includes; a third transistor (T3) coupled to the first node (N1); a fourth transistor (T4) disposed between the second node (N2) and the third node (N3), wherein the driving transistor is disposed between the first driving power supply line and the third node; a fifth transistor (T5) disposed between the third node (N3) and an anode of the organic light-emitting element (OLED); and a sixth transistor (T6) coupled to a fourth node (N4), wherein the fourth node (N4) is disposed between the fifth transistor (T5) and the anode (OLED),
wherein the method further comprises:
for the second period, sampling the second node (N2) using a difference voltage between the first driving voltage (VDD) supplied from the first driving power supply line and a threshold voltage of the driving transistor (DT) by turning on the fourth transistor (T4), while supplying the first reference voltage (VSS, VREF or VREF1) to the fourth node (N4) by turning on the sixth transistor (T6).

11. The method of claim 10, wherein the method further comprises:

turning off the first to sixth transistors (T1, T6) and boosting a potential of the second node (N2) for a third period;
for a fourth period, turning on the driving transistor (DT) based on a turn-on signal corresponding to the potential of the second node (N2), turning on the third transistor (T3) to supply a second reference voltage (VREF2) to the first node (N1), and turning on the fifth transistor (T5)

such that a driving current from the turned-on driving transistor (DT) is supplied to the organic light-emitting element (OLED).

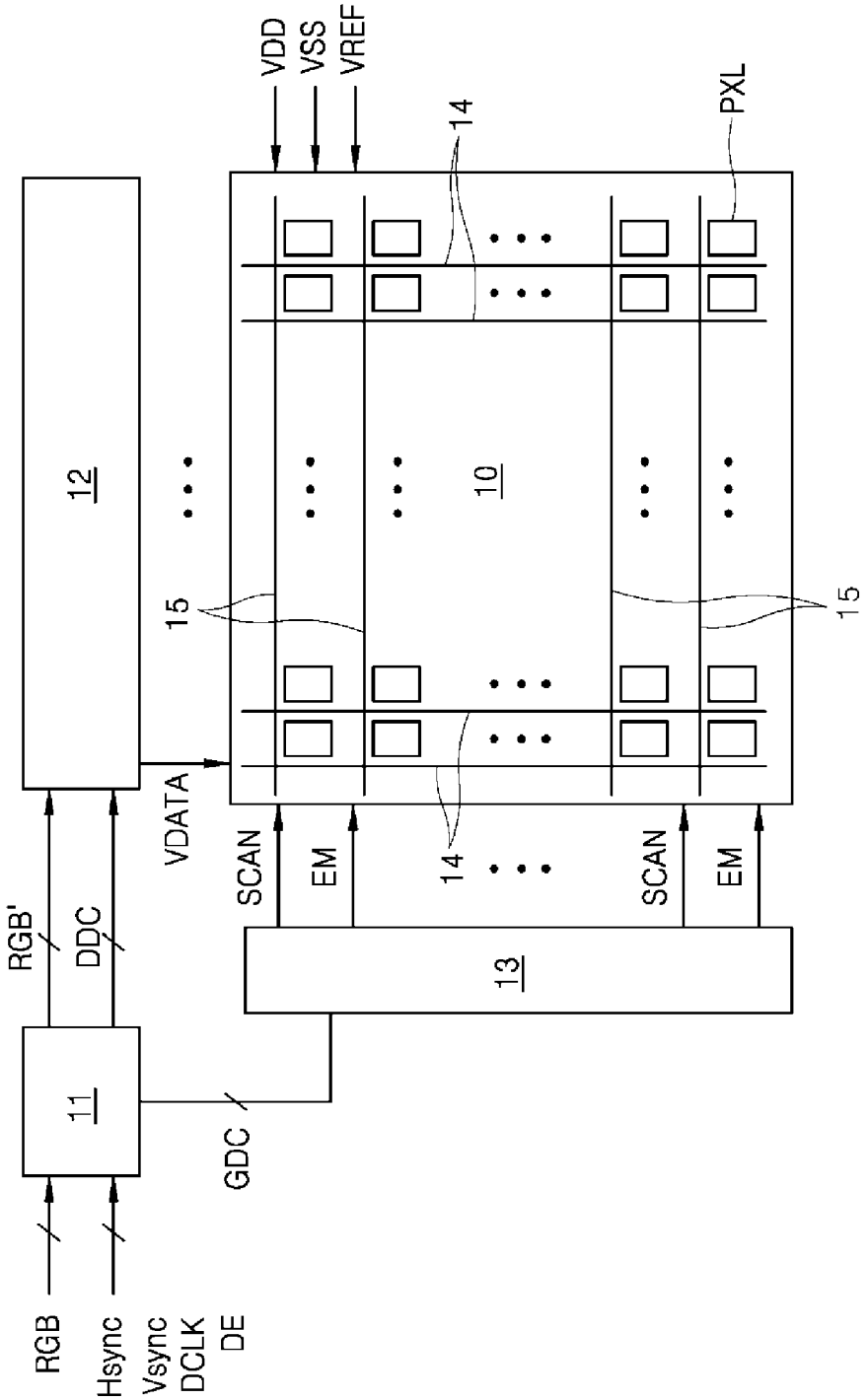
12. The method of claim 11,
wherein the organic light-emitting display device (10) further comprises a seventh transistor (T7) coupled to the first node (N1),
wherein the method further comprises initializing the first node (N1) to the second reference voltage (VREF2) by turning on the seventh transistor (T7) for the first period.

13. The method of claim 12, wherein the first and second reference voltages (VREF1, VREF2) have different voltage levels.

14. The method of claim 13, wherein the first reference voltage (VREF1) has the same voltage level as a voltage level of the second driving voltage (VREF2).

15. The method of claim 11 or claim 12, wherein the first and second reference voltages (VREF1, VREF2) have the same voltage level.

FIG. 1


VDD
VSS
VREF
14
PXL
12
10
15
15
VDATA
SCAN
EM
14
SCAN
EM
13
RGB'
DDC
11
GDC
RGB
Hsync
Vsync
DCLK
DE

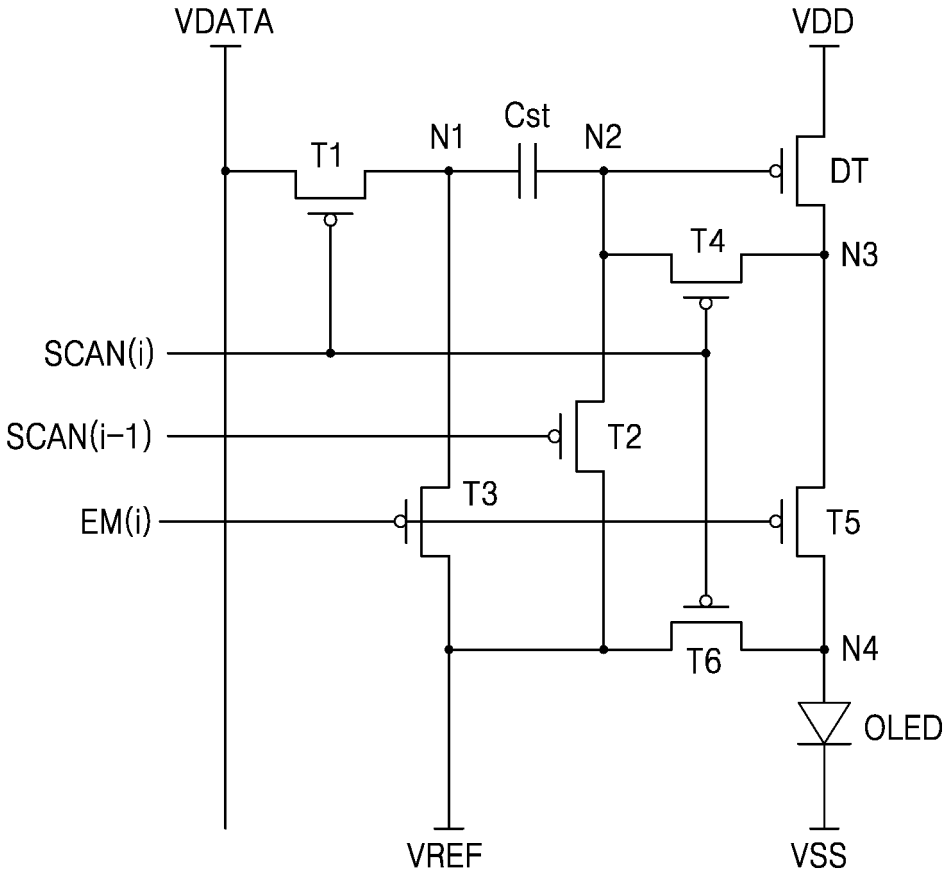
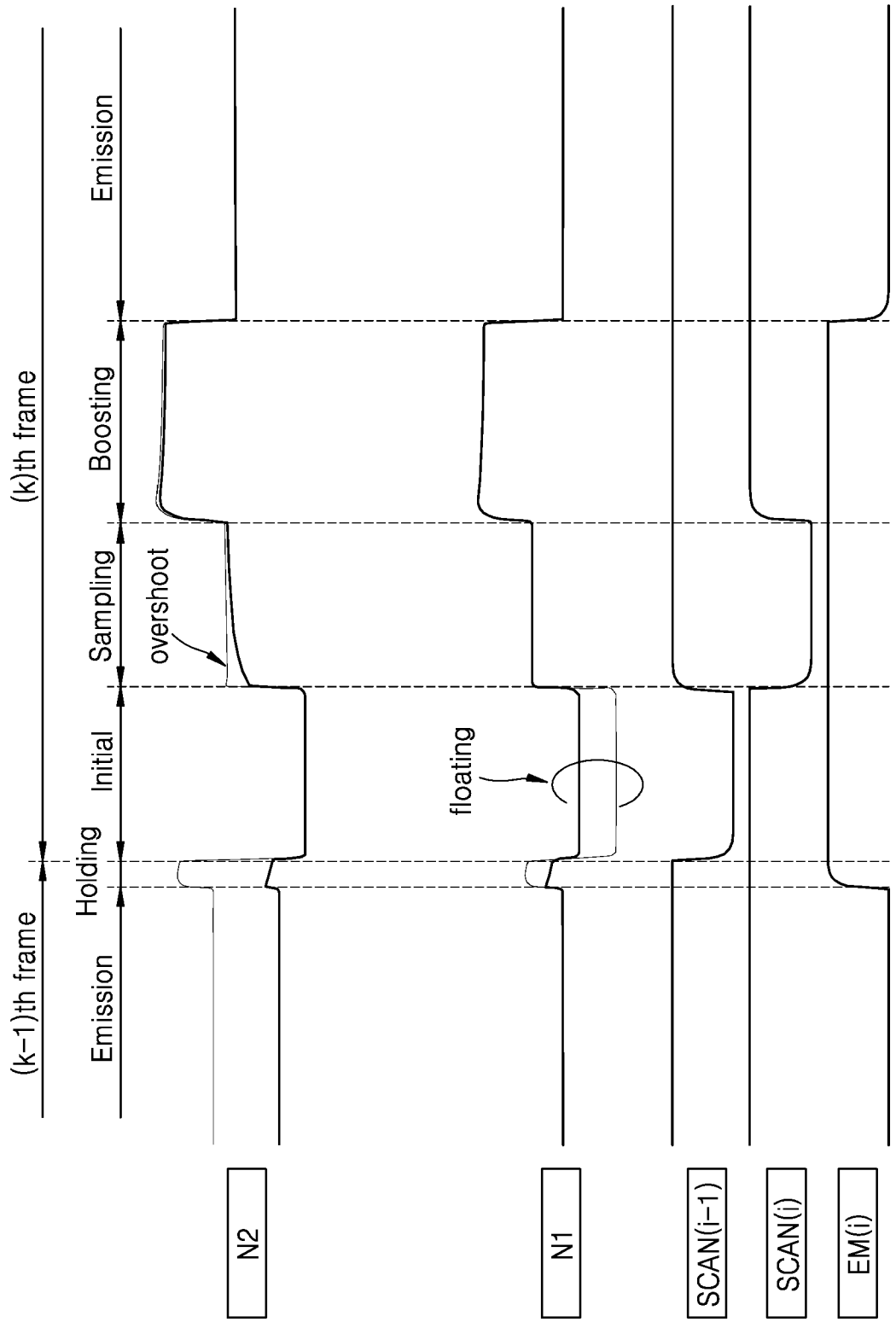

VDATA
VDD
Cst
N1
N2
T1
DT
T4
N3
SCAN(i)
SCAN(i-1)
T2
T3
EM(i)
T5
T6
N4
OLED
VREF
VSS

FIG. 3


(k−1)th frame
(k)th frame
Emission
Holding
Initial
Sampling
Boosting
Emission
overshoot
floating
N2
N1
SCAN(i−1)
SCAN(i)
EM(i)

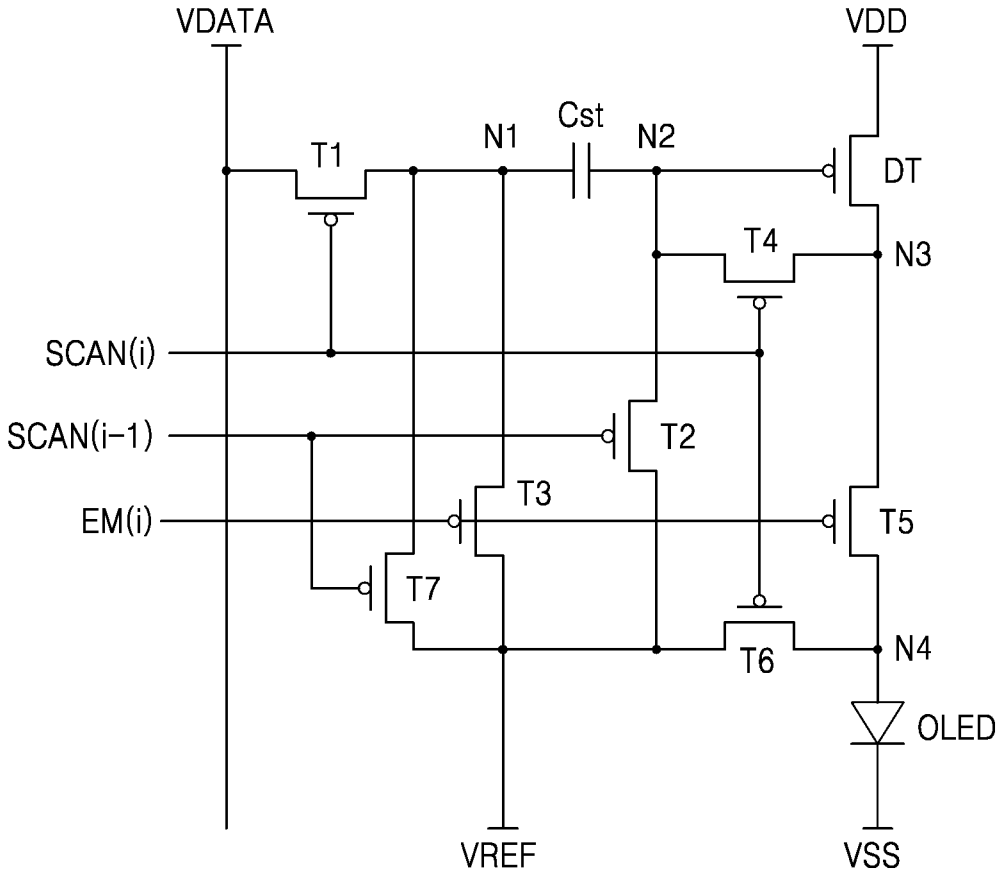
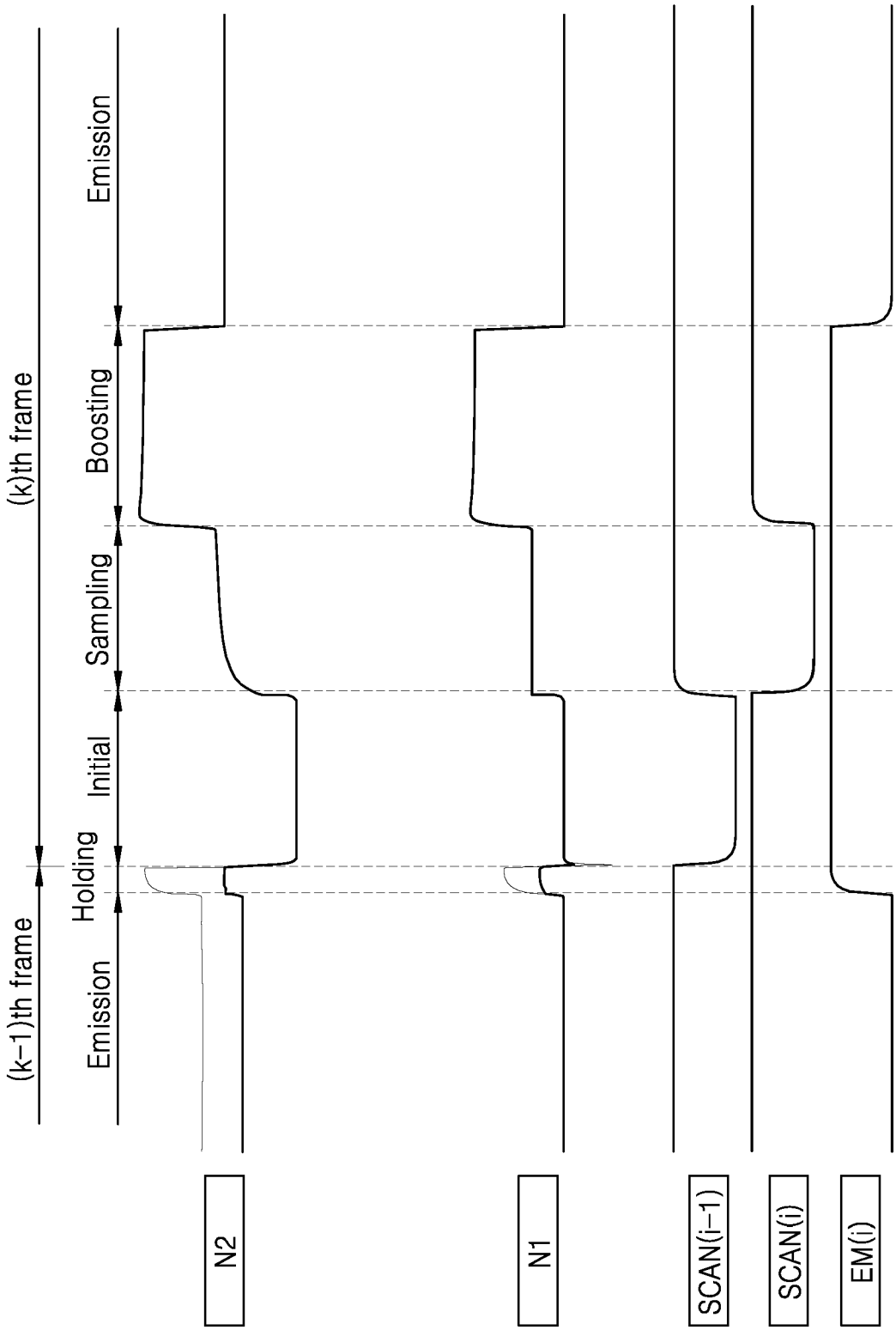
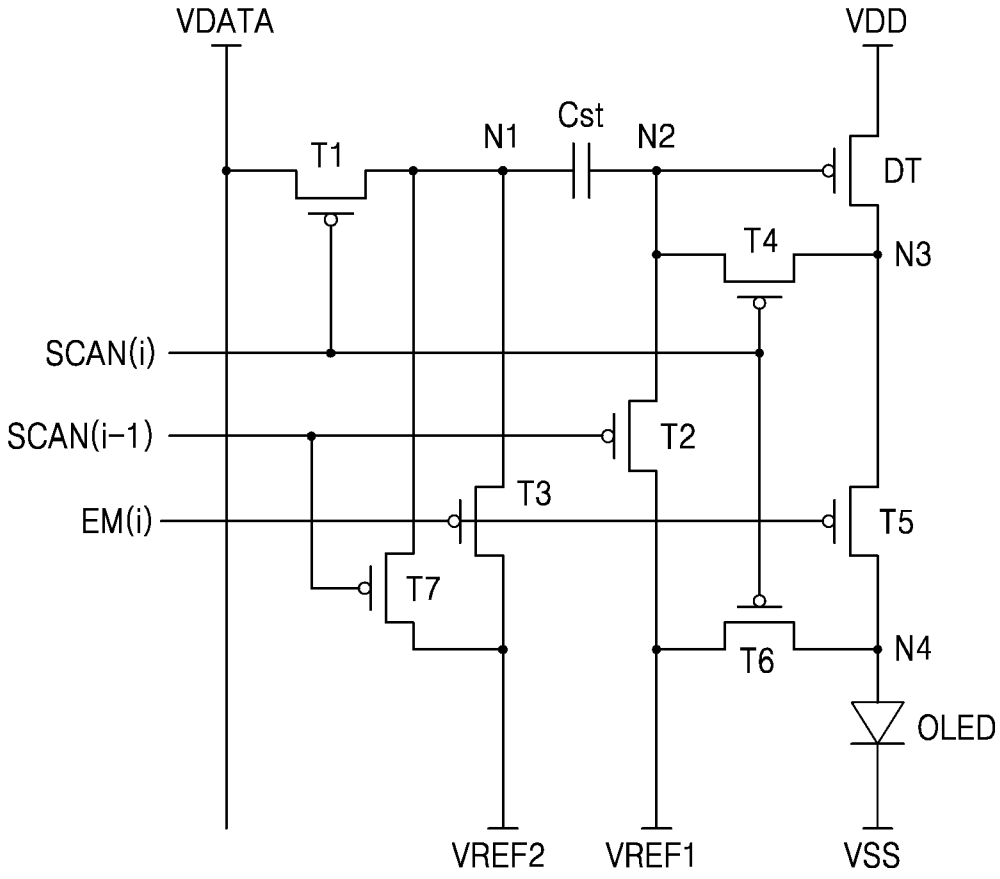
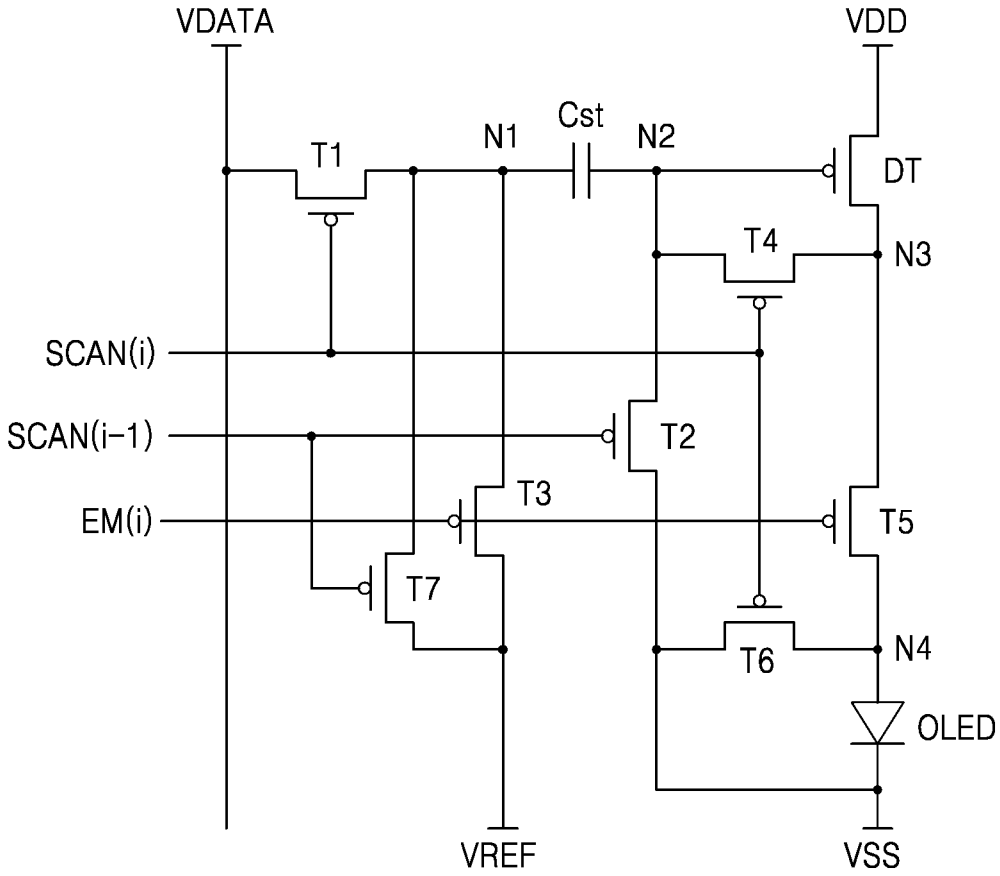

VDATA
VDD
T1
N1
Cst
N2
DT
T4
N3
SCAN(i)
SCAN(i-1)
T2
T3
EM(i)
T5
T7
T6
N4
OLED
VREF
VSS

FIG. 5


(k−1)th frame
(k)th frame
Emission
Holding
Initial
Sampling
Boosting
Emission
N2
N1
SCAN(i−1)
SCAN(i)
EM(i)


VDATA
VDD
T1
N1
Cst
N2
DT
T4
N3
SCAN(i)
SCAN(i-1)
T2
T3
EM(i)
T5
T7
T6
N4
OLED
VREF2
VREF1
VSS


VDATA
VDD
T1
N1
Cst
N2
DT
T4
N3
SCAN(i)
SCAN(i-1)
T2
T3
EM(i)
T5
T7
T6
N4
OLED
VREF
VSS

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 18 19 6056

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2017/025062 A1 (WANG HUANNAN [CN]) 26 January 2017 (2017-01-26) * paragraph [0006] - paragraph [0040]; figures 1-5 *	1-15	INV. G09G3/3233

TECHNICAL FIELDS SEARCHED (IPC)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	5 November 2018	Gartlan, Michael

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 18 19 6056

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05-11-2018

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2017025062 A1	26-01-2017	CN 104992674 A	21-10-2015
		US 2017025062 A1	26-01-2017

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	有机发光显示装置及其驱动方法		
公开(公告)号	EP3462437A1	公开(公告)日	2019-04-03
申请号	EP2018196056	申请日	2018-09-21
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	LEE TAEKYEONG		
发明人	LEE, TAEKYEONG		
IPC分类号	G09G3/3233		
CPC分类号	G09G3/3208 G09G3/3233 G09G3/3258 G09G3/3266 G09G2300/0819 G09G2300/0861 G09G2310/0262 G09G2310/061 G09G2320/043 G09G3/3291 G09G2300/0426 G09G2300/043 G09G2310/08 H01L27/3244		
审查员(译)	GARTLAN，MICHAEL		
优先权	1020170126235 2017-09-28 KR		
外部链接	Espacenet		

摘要(译)

本发明提供一种有机发光显示装置（10），包括：有机发光元件（OLED）;驱动晶体管（DT）与有机发光元件（OLED）连接;第一晶体管（D1），其中当第一晶体管（T1）基于第i扫描信号（SCAN（i））导通时，数据电压经由导通的第一节点（N1）提供给第一节点（N1）晶体管，其中i是等于或大于2且小于或等于N的自然数，其中N是扫描线的数量;电容器（Cst），设置在第一节点（N1）和驱动晶体管（DT）的栅极之间;第二晶体管（T2），其中当第二晶体管基于第（i-1）扫描信号（SCAN（i））导通时，第一参考电压经由转向被提供给第二节点（N2）- 第二晶体管，其中第二节点（N2）设置在驱动晶体管（DT）和电容器（Cst）之间。

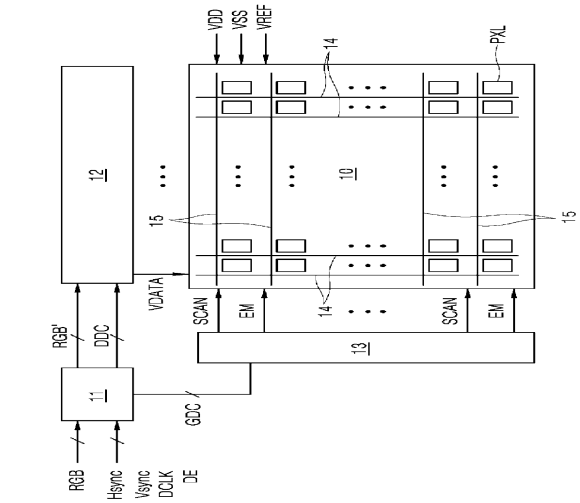

FIG. 1