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(54) PIXEL CIRCUIT, ORGANIC ELECTROLUMINESCENCE DISPLAY PANEL, AND DISPLAY DEVICE AND DRIVING METHOD THEREFOR

(57) The present invention discloses a pixel circuit, an organic electroluminescent display panel, a display apparatus and a driving method thereof. The pixel circuit performs initialization on a first node and a third node in an initialization phase, performs compensation on a threshold voltage of a drive module for the first node in a compensation phase, and performs data writing on the first node in a data writing phase. In a light emitting phase, the drive module drives a light emitting device in a light emitting module to emit light, thereby realizing a normal light emitting function of the light emitting device. In this way, compared with a pixel circuit in the prior art, the pixel circuit provided by an embodiment of the present invention can perform initialization on a control end of the drive module in the initialization phase, perform compensation on the threshold voltage of the drive module in the compensation phase, and perform data writing on the drive module in the data writing phase, thereby preventing a change in the threshold voltage of the drive module from affecting a luminous brightness of the light emitting device, improving the uniformity of the luminous brightness of the light emitting device, and further ensuring the quality of a display frame.

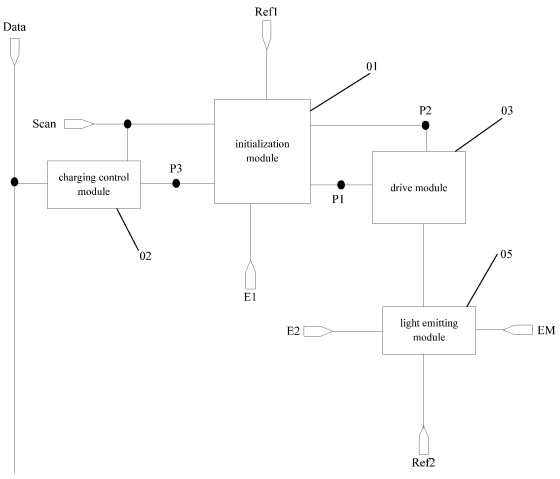

FIG. 2

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Description

REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority to Chinese Patent Application No. 201410640340.0, filed on November 13, 2014, which is herein incorporated by reference in its entirety as a part of this application.

TECHNICAL FIELD

[0002] The present invention relates to the technical field of display, and particularly relates to a pixel circuit, an organic electroluminescent display panel, a display apparatus and a driving method thereof.

BACKGROUND ART

[0003] As the display technique has progressed, more and more active matrix organic light emitting diode (AMOLED) display panels are going to enter the market. Compared with a conventional thin film transistor liquid crystal display (TFT LCD) panel, the active matrix organic light emitting diode display panel has the advantages of low energy consumption, low production cost, self light emission, wide viewing angle, high response speed and the like. At present, the active matrix organic light emitting diode display panel has already started replacing a conventional LCD display screen gradually in the fields of cellphone, PDA, digital camera and the like. Unlike a TFT LCD which controls brightness with a stable voltage, AMOLED is current-driven and needs a stable current to control light emission.

[0004] As shown in FIG. 1, an existing pixel circuit driving an OLED to emit light comprises a drive transistor M1, a switch transistor M2, a storage capacitor C and a light emitting device OLED, wherein a gate electrode of the drive transistor M1 is connected with a drain electrode of the switch transistor M2 and one end of the storage capacitor C, a source electrode thereof is connected with a high-voltage signal end VDD, and a drain electrode thereof is connected with the other end of the storage capacitor and one end of the light emitting device OLED; a gate electrode of the switch transistor M2 is connected with a scan signal end Gate, and a source electrode thereof is connected with a data signal end Data; the other end of the light emitting device OLED is connected with a low-voltage signal end VSS; when the drive transistor M1 drives the light emitting device OLED to emit light, a driving current is controlled jointly by the high-voltage signal end VDD, the data signal end Data and the drive transistor M1. Because a luminous brightness of the OLED is quite sensitive to a change in the driving current thereof, and the drive transistor M1 may not be made completely consistent in a fabrication process, in addition, due to reasons such as a process flow and device aging, as well as a temperature change in a working process, a threshold voltage Vth of the drive transistor M1 in each pixel circuit is non-uniform, which causes a change to the current flowing through each pixel point OLED, such that a display brightness is non-uniform, thereby affecting a display effect of the whole image.

[0005] Accordingly, how to eliminate the influence of the change in the threshold voltage of the drive transistor in the pixel circuit on the luminous brightness of the light emitting device, to ensure the uniformity of the current for driving the light emitting device OLED so as to ensure the quality of a display frame, is a problem to be solved by a person skilled in the art.

SUMMARY OF THE INVENTION

[0006] Embodiments of the present invention provide a pixel circuit, an organic electroluminescent display panel, a display apparatus and a driving method thereof, which are used for solving a problem that a luminous brightness of a light emitting device is affected by a change in a threshold voltage of a drive transistor in a pixel circuit in the prior art.

[0007] An embodiment of the present invention provides a pixel circuit, comprising an initialization module, a charging control module, a drive module, and a light emitting module with a light emitting device, wherein

a control end of the drive module is connected with a first node, an input end thereof is connected with a second node, and an output end thereof is connected with an input end of the light emitting module; a control end of the charging control module is connected with a scan signal end, an input end thereof is connected with a data signal end, and an output end thereof is connected with a third node; the initialization module is connected with the first node, the second node, the third node, a first reference signal end, a first signal control end and the scan signal end; a first control end of the light emitting module is connected with a second signal control end, a second control end thereof is connected with a light emission signal control end, and an output end thereof is connected with a second reference signal end;

in an initialization phase, the initialization module is configured to initialize the first node under a control of the scan signal end, and the charging control module is configured to initialize the third node under the control of the scan signal end;

in a compensation phase, the light emitting module is configured to realize a conduction between an output end of the drive module and the second reference signal end under a control of the second signal control end, and the initialization module is configured to compensate a threshold voltage of the drive module for the first node under a control of the first signal control end and the scan signal end; and

in a data writing phase, the charging control module is configured to perform data writing on the first node through the initialization module under the control of the scan signal end.

[0008] In one possible implementation, in the above

pixel circuit provided by the embodiment of the present invention, in a light emitting phase, the initialization module is configured to realize a conduction between the first reference signal end and an input end of the drive module under a control of the first signal control end, such that the drive module drives the light emitting device in the light emitting module to emit light.

[0009] In one possible implementation, in the above pixel circuit provided by the embodiment of the present invention, the drive module particularly comprises a drive transistor; wherein

a gate electrode of the drive transistor is connected with the first node, a source electrode thereof is connected with the second node, and a drain electrode thereof is connected with an input end of the light emitting module.

[0010] In one possible implementation, in the above pixel circuit provided by the embodiment of the present invention, the initialization module particularly comprises a first switch transistor, a second switch transistor and a storage capacitor; wherein

a gate electrode of the first switch transistor is connected with the scan signal end, a source electrode thereof is connected with the first reference signal end, and a drain electrode thereof is connected with the first node;

a gate electrode of the second switch transistor is connected with the first signal control end, a source electrode thereof is connected with the first reference signal end, and a drain electrode thereof is connected with the second node; and

the storage capacitor is connected between the first node and the third node.

[0011] In one possible implementation, in the above pixel circuit provided by the embodiment of the present invention, the charging control module particularly comprises a third switch transistor; wherein

a gate electrode of the third switch transistor is connected with the scan signal end, a source electrode thereof is connected with the data signal end, and a drain electrode thereof is connected with the third node.

[0012] In one possible implementation, in the above pixel circuit provided by the embodiment of the present invention, the first switch transistor and the third switch transistor are both P-type transistors, or are both N-type transistors.

[0013] In one possible implementation, in the above pixel circuit provided by the embodiment of the present invention, the light emitting module particularly comprises a light emitting device, a fourth switch transistor and a fifth switch transistor, wherein

a gate electrode of the fourth switch transistor is connected with the second signal control end, a source electrode thereof is connected with an output end of the drive module and a source electrode of the fifth switch transistor, and a drain electrode thereof is connected with an output end of the light emitting device and the second reference signal end; and

a gate electrode of the fifth switch transistor is connected with the light emission signal control end, and a drain electrode thereof is connected with an input end of the light emitting device.

[0014] An embodiment of the present invention provides an organic electroluminescent display panel, comprising the above pixel circuit provided by the embodiment of the present invention.

[0015] An embodiment of the present invention provides a display apparatus, comprising the organic electroluminescent display panel provided by the embodiment of the present invention.

[0016] An embodiment of the present invention provides a driving method of a pixel circuit, wherein the pixel circuit comprises an initialization module, a charging control module, a drive module, and a light emitting module with a light emitting device, wherein a control end of the drive module is connected with a first node, an input end thereof is connected with a second node, and an output end thereof is connected with an input end of the light emitting module; a control end of the charging control module is connected with a scan signal end, an input end thereof is connected with a data signal end, and an output end thereof is connected with a third node; the initialization module is connected with the first node, the second node, the third node, a first reference signal end, a first signal control end and the scan signal end; a first control end of the light emitting module is connected with a second signal control end, a second control end thereof is connected with a light emission signal control end, and an output end thereof is connected with a second reference signal end;

the method comprises the following steps:

in an initialization phase, initializing the first node by the initialization module under a control of the scan signal end, and initializing the third node by the charging control module under the control of the scan signal end;

in a compensation phase, realizing a conduction between an output end of the drive module and the second reference signal end by the light emitting module under a control of the second signal control end, and compensating a threshold voltage of the drive module for the first node by the initialization module under the control of the first signal control end and the scan signal end; and

in a data writing phase, performing data writing on the first node by the charging control module through the initialization module under the control of the scan signal end.

[0017] Advantageous effects of the embodiments of the present invention are as follows.

[0018] The embodiments of the present invention provide a pixel circuit, an organic electroluminescent display panel, a display apparatus and a driving method thereof. The pixel circuit comprises an initialization module, a charging control module, a drive module, and a light emitting module with a light emitting device. In the initialization

phase, the initialization module initializes the first node, and the charging control module initializes the third node; in the compensation phase, the light emitting module realizes a conduction between the output end of the drive module and the second reference signal end, and the initialization module compensates the threshold voltage of the drive module for the first node; in the data writing phase, the charging control module performs data writing on the first node through the initialization module. In the light emitting phase, the initialization module realizes a conduction between the first reference signal end and the input end of the drive module, such that the drive module drives the light emitting device in the light emitting module to emit light, thereby realizing a normal light emitting function of the light emitting device. In this way, compared with a pixel circuit in the prior art, the pixel circuit provided by the embodiment of the present invention can perform initialization on the control end of the drive module in the initialization phase, perform compensation on the threshold voltage of the drive module in the compensation phase, and perform data writing on the drive module in the data writing phase, thereby preventing the change in the threshold voltage of the drive module from affecting the luminous brightness of the light emitting device, improving the uniformity of the luminous brightness of the light emitting device, and further ensuring the quality of a display frame.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019]

FIG. 1 is a schematic structural view of a pixel circuit in the prior art;

FIG. 2 is a schematic structural view of a pixel circuit provided by an embodiment of the present invention;

FIG. 3a and FIG. 3b are respectively schematic specific structural views of a pixel circuit provided by an embodiment of the present invention; and

FIG. 4a and FIG. 4b are respectively schematic timing sequence views of an embodiment I and an embodiment II provided by an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0020] The detailed description of a pixel circuit, an organic electroluminescent display panel, a display apparatus and a driving method thereof provided by embodiments of the present invention will be illustrated in detail with reference to the accompanying drawings.

[0021] An embodiment of the present invention provides a pixel circuit, as shown in FIG. 2, comprising an initialization module 01, a charging control module 02, a drive module 03, and a light emitting module 05 with a light emitting device 04, wherein

a control end of the drive module 03 is connected with a first node P1, an input end thereof is connected with a second node P2, and an output end thereof is connected with an input end of the light emitting module 05; a control end of the charging control module 02 is connected with a scan signal end Scan, an input end thereof is connected with a data signal end Data, and an output end thereof is connected with a third node P3; the initialization module 01 is connected with the first node P1, the second node P2, the third node P3, a first reference signal end Ref1, a first signal control end E1 and the scan signal end Scan; a first control end of the light emitting module 05 is connected with a second signal control end E2, a second control end thereof is connected with a light emission signal control end EM, and an output end thereof is connected with a second reference signal end Ref2;

in an initialization phase, the initialization module 01 is configured to initialize the first node P1 under a control of the scan signal end Scan, and the charging control module 02 is configured to initialize the third node P3 under the control of the scan signal end Scan;

in a compensation phase, the light emitting module 05 is configured to realize a conduction between an output end of the drive module 03 and the second reference signal end Ref2 under a control of the second signal control end E2, and the initialization module 01 is configured to compensate a threshold voltage of the drive module 03 for the first node P1 under a control of the first signal control end E1 and the scan signal end Scan; and

in a data writing phase, the charging control module 02 is configured to perform data writing on the first node P1 through the initialization module 01 under the control of the scan signal end Scan.

[0022] In a light emitting phase, the initialization module 01 is configured to realize a conduction between the first reference signal end Ref1 and the input end of the drive module 03 under the control of the first signal control end E1, such that the drive module 03 drives the light emitting device 04 in the light emitting module 05 to emit light.

[0023] In the above pixel circuit provided by the embodiment of the present invention, in the initialization phase, the initialization module 01 initializes the first node P1, and the charging control module 02 initializes the third node P3; in the compensation phase, the light emitting module 05 realizes a conduction between the output end of the drive module 03 and the second reference signal end Ref2, and the initialization module 01 compensates the threshold voltage of the drive module 03 for the first node P1; and in the data writing phase, the charging control module 02 performs data writing on the first node P1 through the initialization module 01. In the light emitting phase, the initialization module 01 realizes a conduction between the first reference signal end Ref1 and the input end of the drive module 03, such that the drive module 03 drives the light emitting device 04 in the light emitting module 05 to emit light, thereby realizing a normal light emitting function of the light emitting device 04. In this way, compared with a pixel circuit in the prior art, the pixel circuit provided by the embodiment of the

present invention can perform initialization on the control end of the drive module 03 in the initialization phase, perform compensation on the threshold voltage of the drive module 03 in the compensation phase, and perform data writing on the drive module 03 in the data writing phase, thereby preventing a change in the threshold voltage of the drive module 03 from affecting a luminous brightness of the light emitting device 04, improving the uniformity of the luminous brightness of the light emitting device 04, and further ensuring the quality of a display frame.

[0024] In a specific implementation, in the above pixel circuit provided by the embodiment of the present invention, as shown in FIG. 3a and FIG. 3b, the drive module 03 may particularly comprise a drive transistor D1; wherein a gate electrode of the drive transistor D1 is connected with the first node P1, a source electrode thereof is connected with the second node P2, and a drain electrode thereof is connected with an input end of the light emitting module 05.

[0025] Particularly, in the above pixel circuit provided by the embodiment of the present invention, as shown in FIG. 3a, the drive transistor D1 may be an N-type transistor; as shown in FIG. 3b, the drive transistor D1 may also be a P-type transistor, which will not be defined here. In an initialization time period, the initialization module 01 realizes a conduction between the first reference signal end Ref1 and the first node P1 under the control of the scan signal end Scan to initialize the first node P1, that is, the gate electrode of the drive transistor D1, such that the drive transistor D1 is in a saturated on state; in the compensation phase, the initialization module 01 and the drive transistor D1 form a discharge loop to discharge a voltage for the first node P1 to a threshold voltage Vth of the drive transistor D1, that is, the compensation for the threshold voltage of the drive transistor D1 is realized; in the data writing phase, the charging control module 02 writes a data signal input by the data signal end Data into the first node P1 through the initialization module 01, that is, performs data writing on the gate electrode of the drive transistor D1; and in the light emitting phase, the initialization module 01 realizes a conduction between the first reference signal end Ref1 and the source electrode of the drive transistor D1, such that the drive transistor D1 drives the light emitting device 04 in the light emitting module 05 to emit light by using a voltage signal input by the first reference signal end Ref1 as a driving voltage.

[0026] In a specific implementation, in the above pixel circuit provided by the embodiment of the present invention, as shown in FIG. 3a and FIG. 3b, the initialization module 01 may particularly comprise a first switch transistor T1, a second switch transistor T2 and a storage capacitor C1; wherein a gate electrode of the first switch transistor T1 is connected with the scan signal end Scan, a source electrode thereof is connected with the first reference signal end Ref1, and a drain electrode thereof is connected with the first node P1; a gate electrode of the second switch transistor T2 is connected with the first signal control end E1, a source electrode thereof is connected with the first reference signal end Ref1, and a drain electrode thereof is connected with the second node P2; and the storage capacitor C1 is connected between the first node P1 and the third node P3.

[0027] Particularly, in the above pixel circuit provided by the embodiment of the present invention, as shown in FIG. 3a, the first switch transistor T1 and the second switch transistor T2 may be N-type transistors; as shown in FIG. 3b, the first switch transistor T1 and the second switch transistor T2 may be P-type transistors, which will not be defined here. In the initialization phase, the first switch transistor T1 is conducted under the control of the scan signal end Scan, the conducted first switch transistor T1 realizes a conduction between the first reference signal end Ref1 and the first node P1 to initialize the first node P1; in the compensation phase, the first switch transistor T1 and the second switch transistor T2 are conducted respectively under the control of the scan signal end Scan and the first signal control end E1, the first switch transistor T1 and the second switch transistor T2 which are conducted form a discharge loop with the drive transistor D1 to discharge a voltage for the first node P1 to a threshold voltage Vth of the drive transistor; and in the light emitting phase, the second switch transistor T2 is conducted under the control of the first signal control end E1, the conducted second switch transistor T2 realizes a conduction between the first reference signal end Ref1 and the source electrode of the drive transistor D1, such that the drive transistor D1 drives the light emitting device 04 in the light emitting module 05 to emit light by using a voltage signal input by the first reference signal end Ref1 as a driving voltage.

[0028] In a specific implementation, in the above pixel circuit provided by the embodiment of the present invention, as shown in FIG. 3a and FIG. 3b, the charging control module 02 may particularly comprise a third switch transistor T3; wherein a gate electrode of the third switch transistor T3 is connected with the scan signal end Scan, a source electrode thereof is connected with the data signal end Data, and a drain electrode thereof is connected with the third node P3.

[0029] Particularly, in the above pixel circuit provided by the embodiment of the present invention, as shown in FIG. 3a, the third switch transistor T3 may be an N-type transistor; as shown in FIG. 3b, the third switch transistor T3 may be a P-type transistor, which will not be defined here. In the initialization phase, the third switch transistor T3 is conducted under the control of the scan signal end Scan, the conducted third switch transistor T3 realizes a conduction between the data signal end Data and the third node P3 to initialize the third node P3 by a voltage signal input by the data signal end Data; in the compensation phase, the similarly conducted third switch transistor T3 keeps a voltage for the third node P3 constant; and in the data writing phase, the similarly conducted third switch transistor T3 writes a data signal input by the data signal end Data into the third node P3.

[0030] In a specific implementation, in the above pixel circuit provided by the embodiment of the present invention, because the first switch transistor T1 and the third switch transistor T3 employ the same scan signal end Scan as a control end, in order to enable the two transistors to complete respective functions in different phases under the control of the same scan signal end Scan, the first switch transistor T1 and the third switch transistor T3 are set to be transistors of the same type. As shown in FIG. 3a, the first switch transistor T1 and the third switch transistor T3 may be both N-type transistors; as shown in FIG. 3b, the first switch transistor T1 and the third switch transistor T3 may also be both P-type transistors.

[0031] In a specific implementation, in the above pixel circuit provided by the embodiment of the present invention, as shown in FIG. 3a and FIG. 3b, the light emitting module 05 particularly comprises a light emitting device 04, a fourth switch transistor T4 and a fifth switch transistor T5, wherein a gate electrode of the fourth switch transistor T4 is connected with the second signal control end E2, a source electrode thereof is connected with an output end of the drive module 03 and a source electrode of the fifth switch transistor T5, and a drain electrode thereof is connected with an output end of the light emitting device 04 and the second reference signal end Ref2; and a gate electrode of the fifth switch transistor T5 is connected with the light emission signal control end EM, and a drain electrode thereof is connected with an input end of the light emitting device 04.

[0032] Particularly, in the above pixel circuit provided by the embodiment of the present invention, as shown in FIG. 3a, the fourth switch transistor T4 and the fifth switch transistor T5 may be N-type transistors; as shown in FIG. 3b, the fourth switch transistor T4 and the fifth switch transistor T5 may be P-type transistors, which will not be defined here. In the compensation phase, the fourth switch transistor T4 is conducted under the control of the second signal control end E2, the conducted fourth switch transistor T4 realizes a conduction between the output end of the drive module 03 and the second reference signal end Ref2; in the data writing phase, the similarly conducted fourth switch transistor T4 keeps a voltage for the output end of the drive module 03 constant; and in the light emitting phase, the fifth switch transistor T5 is conducted under a control of the light emission signal control end EM, and the conducted fifth switch transistor T5 realizes a conduction between the output end of the drive module 03 and the input end of the light emitting device 04, such that the driving module 03 drives the light emitting device 04 to emit light.

[0033] It should be noted that, the switch transistors and the drive transistors mentioned in the embodiment of the present invention may be thin film transistors (TFT), and may also be metal oxide semiconductor (MOS) field effect transistors, which will not be defined here. In a specific implementation, source electrodes and drain electrodes of these transistors may be interchanged without being particularly distinguished. The thin film transistor is used as an example when particular embodiments are described.

[0034] Moreover, the switch transistors and the drive transistors mentioned in the embodiment of the present invention may all employ P-type transistors or all employ N-type transistors. In this way, a fabricating process for the pixel circuit may be simplified.

[0035] A working process of the pixel circuit provided by the embodiment of the present invention is described in detail below in conjunction with a structure and a timing sequence of a pixel circuit provided by the embodiment of the present invention, wherein the switch transistors and the drive transistors of the pixel circuit in the embodiment I are all designed to employ N-type transistors; and the switch transistors and the drive transistors of the pixel circuit in the embodiment II are all designed to employ P-type transistors.

[0036] Embodiment I: the working process of the pixel circuit provided by the embodiment of the present invention is described in detail below in conjunction with the pixel circuit as shown in FIG. 3a and an input-output timing sequence view for FIG. 3a as shown in FIG. 4a. Particularly, four phases t1-t4 in the input-output timing sequence view as shown in FIG. 4a are selected. In the following description, 1 represents a high-level signal, and 0 represents a low-level signal.

[0037] In the t1 phase, Scan=1, E1=0, E2=0, EM=0, Data=VL, Ref1=Vdd, and Ref2=0. Because Scan=1, the first switch transistor T1 and the third switch transistor T3 are conducted; and because E1=0, E2=0 and EM=0, the second switch transistor T2, the fourth switch transistor T4 and the fifth switch transistor T5 are cut off. The conducted first switch transistor T1 realizes a conduction between the first reference signal end Ref1 and the first node P1 to initialize the first node P, that is, to initialize the gate electrode of the drive transistor D1, at this moment, a voltage for the first node P1, that is, a voltage for the right end of the storage capacitor C1, is Vdd; the conducted third switch transistor T3 transmits a voltage signal VL input by the data signal end Data to the third node P3, at this moment, a voltage for the third node, that is, a voltage for the left end of the storage capacitor C1, is VL, in this phase, a voltage for the gate electrode of the drive transistor D1 is initialized to Vdd, so that the drive transistor D1 is in a saturated on state. The t1 phase is an initialization phase.

[0038] In the t2 phase, Scan=1, E1=1, E2=1, EM=0, Data=VL, Ref1=Vdd and Ref2=0. Because Scan=1, E1=1 and E2=1, the first switch transistor T1, the second switch transistor T2, the third switch transistor T3 and the fourth switch transistor T4 are conducted; and because EM=0, the fifth switch transistor T5 is cut off. The first switch transistor T1 and the second switch transistor T2 which are conducted form a discharge loop with the drive transistor D1 to discharge a voltage for the first node P1 to a threshold voltage Vth of the drive transistor D1, that is, at this moment, a voltage for the right end of the

storage capacitor C1 is Vth, and at this moment, the drive transistor D1 is in a critical on state, the conducted third switch transistor T3 keeps a voltage for the third node P3 at VL, that is, the voltage for the left end of the storage capacitor C1 is still VL, at this moment, a voltage difference across two ends of the storage capacitor C1 is VL-Vth; and the conducted fourth switch transistor T4 realizes a conduction between the drain electrode of the drive transistor D1 and the second reference signal end Ref2. The t2 phase is a compensation phase.

[0039] In the t3 phase, Scan=1, E1=0, E2=1, EM=0, Data=Vdata, Ref1=Vdd and Ref2=0. Because Scan=1 and E2=1, the first switch transistor T1, the third switch transistor T3 and the fourth switch transistor T4 are conducted; and because E1=0 and EM=0, the second switch transistor T2 and the fifth switch transistor T5 are cut off. The conducted first switch transistor T1 realizes a conduction between the first reference signal end Ref1 and the gate electrode of the drive transistor D1, the conducted fourth switch transistor T4 realizes a conduction between the drain electrode of the transistor D1 and the second reference signal end Ref2; the conducted third switch transistor T3 transmits a data signal Vdata input by the data signal end Data to the third node P3, thus the voltage for the left end of the storage capacitor C1 is regulated to Vdata; because the voltage difference across two ends of the storage capacitor C1 is kept at VL-Vth as the last phase, the voltage for the right end of the storage capacitor C1, that is, a voltage for the first node P1, is Vdata-VL+Vth. The t3 phase is a data writing phase.

[0040] In the t4 phase, Scan=0, E1=1, E2=0, EM=1, Data=VL, Ref1=Vdd and Ref2=0. Because E1=1 and EM=1, the second switch transistor T2 and the fifth switch transistor T5 are conducted; and because Scan=0 and E2=0, the first switch transistor T1, the third switch transistor T3 and the fourth switch transistor T4 are cut off. The conducted second switch transistor T2 realizes a conduction between the first reference signal end Ref1 and the source electrode of the drive transistor D1, the conducted fifth switch transistor T5 realizes a conduction between the drain electrode of the drive transistor D1 and the input end of the light emitting device 04, such that the drive transistor D1 drives the light emitting device 04 to emit light by using a voltage signal input by the first reference signal end Ref1 as a driving voltage. As can be known from the last phase, the voltage for the gate electrode of the drive transistor D1 is Vdata-VL+Vth, thus a driving current for driving the light emitting device 04 to emit light is $I=K(Vgs-Vth)^2=K(Vdata-VL+Vth-Vth)^2=K(Vdata-VL)^2$, wherein Vgs is a voltage difference between the gate electrode and the source electrode of the drive transistor D1, K is a constant related to a process parameter and a geometric size of the drive transistor D1. As can be known, the driving current for driving the light emitting device 04 to emit light is independent of the threshold voltage of the drive transistor D1, so that the influence of the change in the threshold voltage of the drive transistor D1 on the luminous brightness of the light emitting device 04 is eliminated, and the uniformity of the luminous brightness of the light emitting device 04 is improved. The t4 phase is a light emitting phase.

[0041] In a subsequent time period, the drive transistor D1 will be continuously in an on state to drive the light emitting device 04 to continuously emit light, until the next high-level signal of the scan signal end Scan arrives.

[0042] Embodiment II: the working process of the pixel circuit provided by the embodiment of the present invention is described in detail below in conjunction with the pixel circuit as shown in FIG. 3b and an input-output timing sequence view for FIG. 3b as shown in FIG. 4b. Particularly, four phases t1-t4 in the input-output timing sequence view as shown in FIG. 4b are selected. In the following description, 1 represents a high-level signal, and 0 represents a low-level signal.

[0043] In the t1 phase, Scan=0, E1=1, E2=1, EM=1, Data=VL, Ref1=Vdd, and Ref2=1. Because Scan=0, the first switch transistor T1 and the third switch transistor T3 are conducted; and because E1=1, E2=1 and EM=1, the second switch transistor T2, the fourth switch transistor T4 and the fifth switch transistor T5 are cut off. The conducted first switch transistor T1 realizes a conduction between the first reference signal end Ref1 and the first node P1 to initialize the first node P, that is, to initialize the gate electrode of the drive transistor D1, at this moment, a voltage for the first node P1, that is, a voltage for the right end of the storage capacitor C1, is Vdd; the conducted third switch transistor T3 transmits a voltage signal VL input by the data signal end Data to the third node P3, at this moment, a voltage for the third node, this is, a voltage for the left end of the storage capacitor C1, is VL, in this phase, a voltage for the gate electrode of the drive transistor D1 is initialized to Vdd, so that the drive transistor D1 is in a saturated on state. The t1 phase is an initialization phase.

[0044] In the t2 phase, Scan=0, E1=0, E2=0, EM=1, Data=VL, Ref1=Vdd and Ref2=1. Because Scan=0, E1=0 and E2=0, the first switch transistor T1, the second switch transistor T2, the third switch transistor T3 and the fourth switch transistor T4 are conducted; and because EM=1, the fifth switch transistor T5 is cut off. The first switch transistor T1 and the second switch transistor T2 which are conducted form a discharge loop with the drive transistor D1 to discharge a voltage for the first node P1 to a threshold voltage Vth of the drive transistor D1, that is, at this moment, a voltage for the right end of the storage capacitor C1 is Vth, and at this moment, the drive transistor D1 is in a critical on state; the conducted third switch transistor T3 keeps a voltage for the third node P3 at VL, that is, the voltage for the left end of the storage capacitor C1 is still VL, at this moment, a voltage difference across two ends of the storage capacitor C1 is VL-Vth; the conducted fourth switch transistor T4 realizes a conduction between the drain electrode of the drive transistor D1 and the second reference signal end Ref2. The t2 phase is a compensation phase.

[0045] In the t3 phase, Scan=0, E1=1, E2=0, EM=1, Data=Vdata, Ref1=Vdd and Ref2=1. Because Scan=0 and E2=0, the first switch transistor T1, the third switch transistor T3 and the fourth switch transistor T4 are conducted; and because E1=1 and EM=1, the second switch transistor T2 and the fifth switch transistor T5 are cut off. The conducted first switch transistor T1 realizes a conduction between the first reference signal end Ref1 and the gate electrode of the drive transistor D1, the conducted fourth switch transistor T4 realizes a conduction between the drain electrode of the transistor D1 and the second reference signal end Ref2; the conducted third switch transistor T3 transmits a data signal Vdata input by the data signal end Data to the third node P3, thus the voltage for the left end of the storage capacitor C1 is regulated to Vdata; because the voltage difference across two ends of the storage capacitor C1 is kept at VL-Vth as the last phase, the voltage for the right end of the storage capacitor C1, that is, a voltage for the first node P1, is Vdata-VL+Vth. The t3 phase is a data writing phase.

[0046] In the t4 phase, Scan=1, E1=0, E2=1, EM=0, Data=VL, Ref1=Vdd and Ref2=1. Because E1=0 and EM=0, the second switch transistor T2 and the fifth switch transistor T5 are conducted; and because Scan=1 and E2=1, the first switch transistor T1, the third switch transistor T3 and the fourth switch transistor T4 are cut off. The conducted second switch transistor T2 realizes a conduction between the first reference signal end Ref1 and the source electrode of the drive transistor D1, the conducted fifth switch transistor T5 realizes a conduction between the drain electrode of the drive transistor D1 and the input end of the light emitting device 04, such that the drive transistor D1 drives the light emitting device 04 to emit light by using a voltage signal input by the first reference signal end Ref1 as a driving voltage. As can be known from the last phase, the voltage for the gate electrode of the drive transistor D1 is Vdata-VL+Vth, thus a driving current for driving the light emitting device 04 to emit light is $I=K(Vgs-Vth)^2=K(Vdata-VL+Vth-Vth)^2=K(Vdata-VL)^2$, wherein Vgs is a voltage difference between the gate electrode and the source electrode of the drive transistor D1, K is a constant related to a process parameter and a geometric size of the drive transistor D1. As can be known, the driving current for driving the light emitting device 04 to emit light is independent of the threshold voltage of the drive transistor D1, so that the influence of the change in the threshold voltage of the drive transistor D1 on the luminous brightness of the light emitting device 04 is eliminated, and the uniformity of the luminous brightness of the light emitting device 04 is improved. The t4 phase is a light emitting phase.

[0047] In a subsequent time period, the drive transistor D1 will be continuously in an on state to drive the light emitting device 04 to continuously emit light, until the next low-level signal of the scan signal end Scan arrives.

[0048] Based on the same inventive concept, an embodiment of the present invention provides an organic electroluminescent display panel, comprising the above pixel circuit provided by the embodiment of the present invention. Because a principle for solving a problem by the organic electroluminescent display panel is similar to that by the pixel circuit, implementations for the organic electroluminescent display panel may refer to that for the pixel circuit, and repeated parts will not be described in detail.

[0049] Based on the same inventive concept, an embodiment of the present invention provides a display apparatus, comprising the above organic electroluminescent display panel provided by the embodiment of the present invention. The display apparatus may be any products or components such as a cellphone, a tablet computer, a television, a display, a notebook computer, a digital photo frame and a navigator, with a display function. Because a principle for solving a problem by the display apparatus is similar to that by the organic electroluminescent display panel, implementations for the display apparatus may refer to that for the organic electroluminescent display panel, and repeated parts will not be described in detail.

[0050] Based on the same inventive concept, an embodiment of the present invention provides a driving method of a pixel circuit. Because a principle of the driving method is similar to that of the pixel circuit, implementations for the driving method may refer to that for the pixel circuit, and repeated parts will not be described in detail.

[0051] The embodiments of the present invention provide a pixel circuit, an organic electroluminescent display panel, a display apparatus and a driving method thereof. The pixel circuit comprises an initialization module, a charging control module, a drive module, and a light emitting module with a light emitting device. In the initialization phase, the initialization module initializes the first node, and the charging control module initializes the third node; in the compensation phase, the light emitting module realizes a conduction between the output end of the drive module and the second reference signal end, the initialization module compensates the threshold voltage of the drive module for the first node; and in the data writing phase, the charging control module performs data writing on the first node through the initialization module. In the light emitting phase, the initialization module realizes a conduction between the first reference signal end and the input end of the drive module, such that the drive module drives the light emitting device in the light emitting module to emit light, thereby realizing a normal light emitting function of the light emitting device. In this way, compared with a pixel circuit in the prior art, the pixel circuit provided by the embodiment of the present invention can perform initialization on the control end of the drive module in the initialization phase, perform compensation on the threshold voltage of the drive module in the compensation phase, and perform data writing on the drive module in the data writing phase, thereby preventing the change in the threshold voltage of the drive module from affecting the luminous brightness of the light emitting de-

vice, improving the uniformity of the luminous brightness of the light emitting device, and further ensuring the quality of the display frame.

[0052] It will be apparent to those skilled in the art that various modifications and variations may be made to the present invention without departing from the scope or spirit of the present invention. In this way, it is intended that the present invention covers these modifications and variations provided they come within the scope of the appended claims and their equivalents of the present invention.

Claims

1. A pixel circuit, comprising an initialization module, a charging control module, a drive module, and a light emitting module with a light emitting device, wherein
a control end of said drive module is connected with a first node, an input end thereof is connected with a second node, and an output end thereof is connected with an input end of said light emitting module;
a control end of said charging control module is connected with a scan signal end, an input end thereof is connected with a data signal end, and an output end thereof is connected with a third node; said initialization module is connected with said first node, said second node, said third node, a first reference signal end, a first signal control end and said scan signal end; a first control end of said light emitting module is connected with a second signal control end, a second control end thereof is connected with a light emission signal control end, and an output end thereof is connected with a second reference signal end;
in an initialization phase, said initialization module is configured to initialize said first node under a control of said scan signal end, and said charging control module is configured to initialize said third node under the control of said scan signal end;
in a compensation phase, said light emitting module is configured to realize a conduction between an output end of said drive module and said second reference signal end under a control of said second signal control end, and said initialization module is configured to compensate a threshold voltage of said drive module for said first node under a control of said first signal control end and said scan signal end; and
in a data writing phase, said charging control module is configured to perform data writing on said first node through said initialization module under the control of said scan signal end.

2. The pixel circuit according to claim 1, wherein
in a light emitting phase, said initialization module is configured to realize a conduction between said first reference signal end and an input end of said drive module under a control of said first signal control end, such that said drive module drives said light emitting device in said light emitting module to emit light.

3. The pixel circuit according to claim 1, wherein said drive module comprises a drive transistor;
a gate electrode of said drive transistor is connected with said first node, a source electrode thereof is connected with said second node, and a drain electrode thereof is connected with an input end of said light emitting module.

4. The pixel circuit according to claim 3, wherein said initialization module comprises a first switch transistor, a second switch transistor and a storage capacitor; wherein
a gate electrode of said first switch transistor is connected with said scan signal end, a source electrode thereof is connected with said first reference signal end, and a drain electrode thereof is connected with said first node;
a gate electrode of the second switch transistor is connected with said first signal control end, a source electrode thereof is connected with said first reference signal end, and a drain electrode thereof is connected with said second node; and
said storage capacitor is connected between said first node and said third node.

5. The pixel circuit according to claim 4, wherein said charging control module comprises a third switch transistor;
a gate electrode of said third switch transistor is connected with said scan signal end, a source electrode thereof is connected with said data signal end, and a drain electrode thereof is connected with said third node.

6. The pixel circuit according to claim 5, wherein said first switch transistor and said third switch transistor are both P-type transistors, or are both N-type transistors.

7. The pixel circuit according to any one of claims 1-6, wherein said light emitting module comprises a light emitting device, a fourth switch transistor and a fifth switch transistor, wherein
a gate electrode of said fourth switch transistor is connected with said second signal control end, a source electrode thereof is connected with an output end of said drive module and a source electrode of said fifth switch transistor, and a drain electrode thereof is connected with an output end of said light emitting device and said second reference signal end; and
a gate electrode of said fifth switch transistor is connected with said light emission signal control end, and a drain electrode thereof is connected with an

input end of said light emitting device.

8. An organic electroluminescent display panel, comprising the pixel circuit according to any one of claims 1-7.

9. A display apparatus, comprising the organic electroluminescent display panel according to claim 8.

10. A driving method of a pixel circuit, wherein
said pixel circuit comprises an initialization module, a charging control module, a drive module, and a light emitting module with a light emitting device, wherein a control end of said drive module is connected with a first node, an input end thereof is connected with a second node, and an output end thereof is connected with an input end of said light emitting module; a control end of said charging control module is connected with a scan signal end, an input end thereof is connected with a data signal end, and an output end thereof is connected with a third node; said initialization module is connected with said first node, said second node, said third node, a first reference signal end, a first signal control end and said scan signal end; a first control end of said light emitting module is connected with a second signal control end, a second control end thereof is connected with a light emission signal control end, and an output end thereof is connected with a second reference signal end;
said method comprises the following steps:

in an initialization phase, initializing said first node by said initialization module under a control of said scan signal end, and initializing said third node by said charging control module under the control of said scan signal end;
in a compensation phase, realizing a conduction between an output end of said drive module and said second reference signal end by said light emitting module under a control of said second signal control end, and compensating a threshold voltage of said drive module for said first node by said initialization module under a control of said first signal control end and said scan signal end; and
in a data writing phase, performing data writing on said first node by said charging control module through said initialization module under the control of said scan signal end.

11. The method according to claim 10, further comprising the following step:

in a light emitting phase, realizing a conduction between said first reference signal end and an input end of said drive module by said initialization module under a control of said first signal control end, such that said drive module drives said light emitting device in said light emitting module to emit light.

12. The method according to claim 10, wherein said drive module comprises a drive transistor;
a gate electrode of said drive transistor is connected with said first node, a source electrode thereof is connected with said second node, and a drain electrode thereof is connected with an input end of said light emitting module.

13. The method according to claim 12, wherein said initialization module comprises a first switch transistor, a second switch transistor and a storage capacitor; wherein
a gate electrode of said first switch transistor is connected with said scan signal end, a source electrode thereof is connected with said first reference signal end, and a drain electrode thereof is connected with said first node;
a gate electrode of the second switch transistor is connected with said first signal control end, a source electrode thereof is connected with said first reference signal end, and a drain electrode thereof is connected with said second node; and
said storage capacitor is connected between said first node and said third node.

14. The method according to claim 13, wherein said charging control module comprises a third switch transistor;
a gate electrode of said third switch transistor is connected with said scan signal end, a source electrode thereof is connected with said data signal end, and a drain electrode thereof is connected with said third node.

15. The method according to claim 14, wherein said first switch transistor and said third switch transistor are both P-type transistors, or are both N-type transistors.

16. The method according to any one of claims 10-15, wherein said light emitting module comprises a light emitting device, a fourth switch transistor and a fifth switch transistor, wherein
a gate electrode of said fourth switch transistor is connected with said second signal control end, a source electrode thereof is connected with an output end of said drive module and a source electrode of said fifth switch transistor, and a drain electrode thereof is connected with an output end of said light emitting device and said second reference signal end; and
a gate electrode of said fifth switch transistor is connected with said light emission signal control end, and a drain electrode thereof is connected with an

input end of said light emitting device.

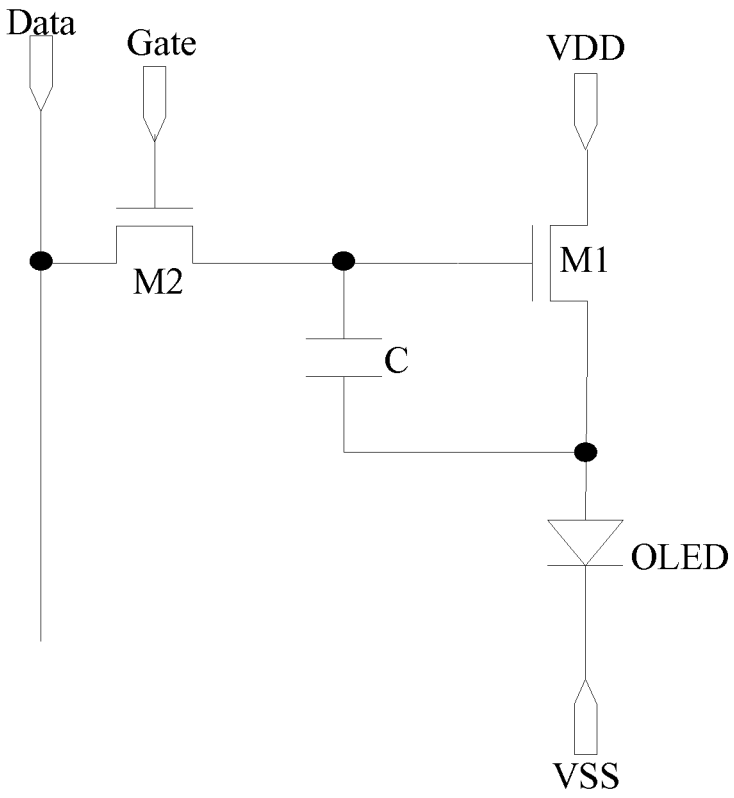

FIG. 1

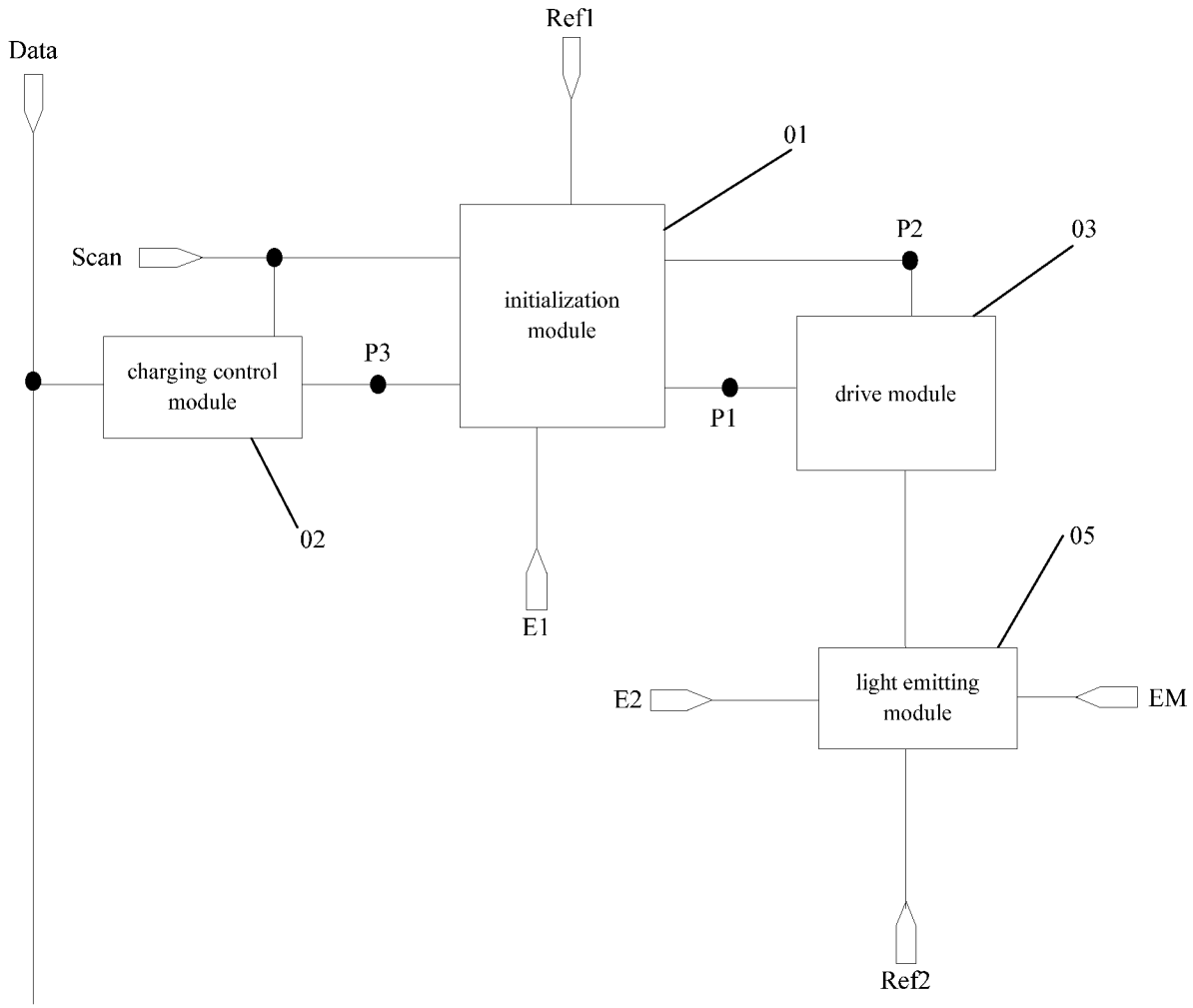
Ref1
Data
01
Scan
P2
03
initialization module
charging control module
P3
drive module
P1
02
E1
05
light emitting module
E2
EM
Ref2

FIG. 2

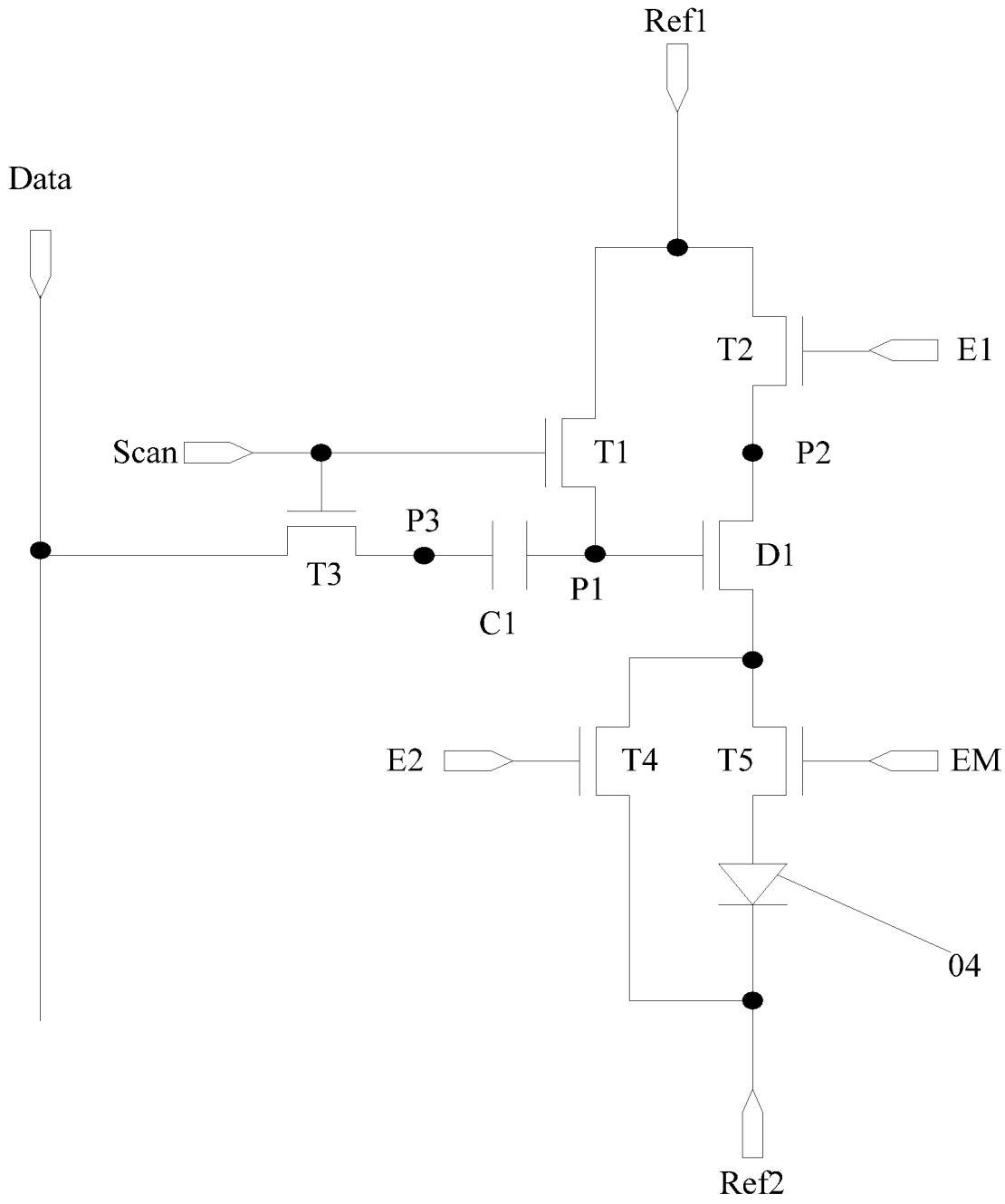

FIG. 3a

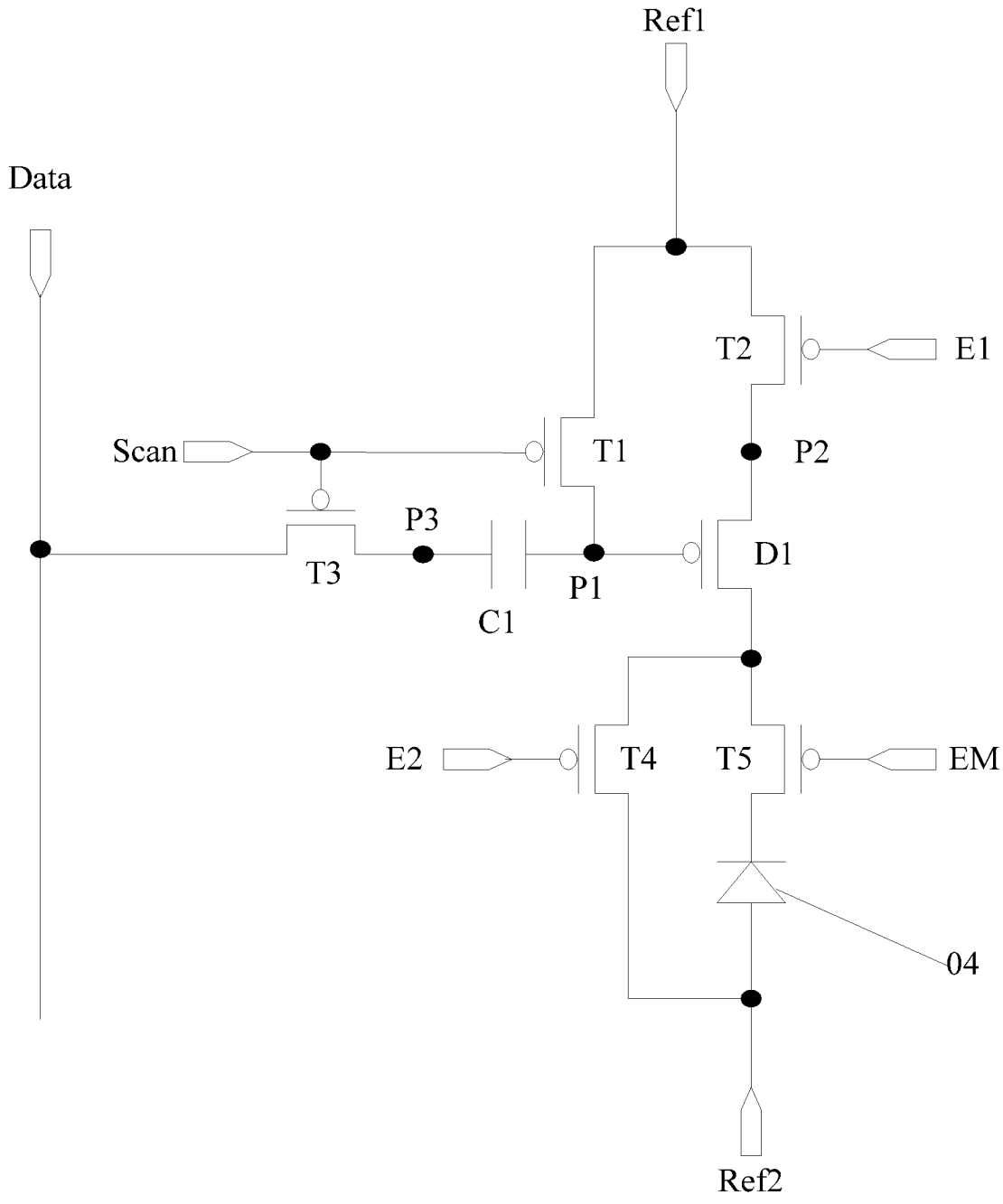

FIG. 3b

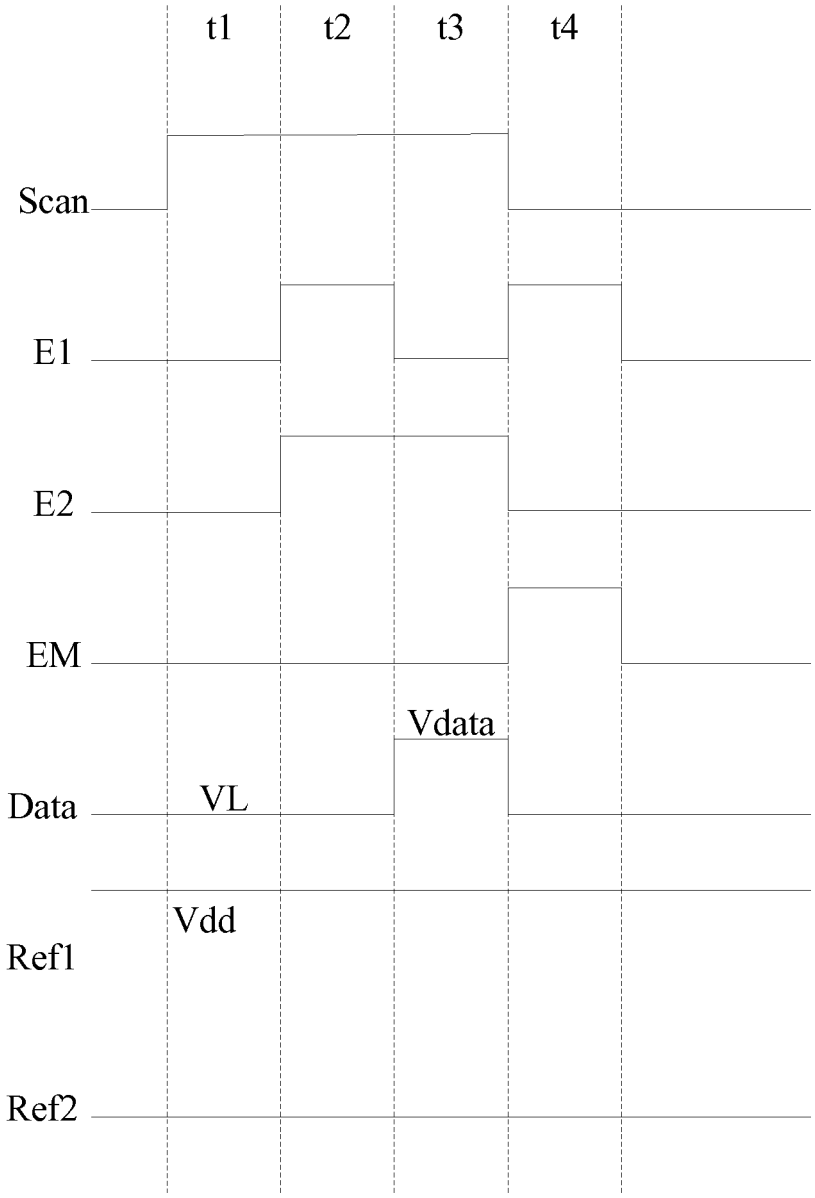

FIG. 4a

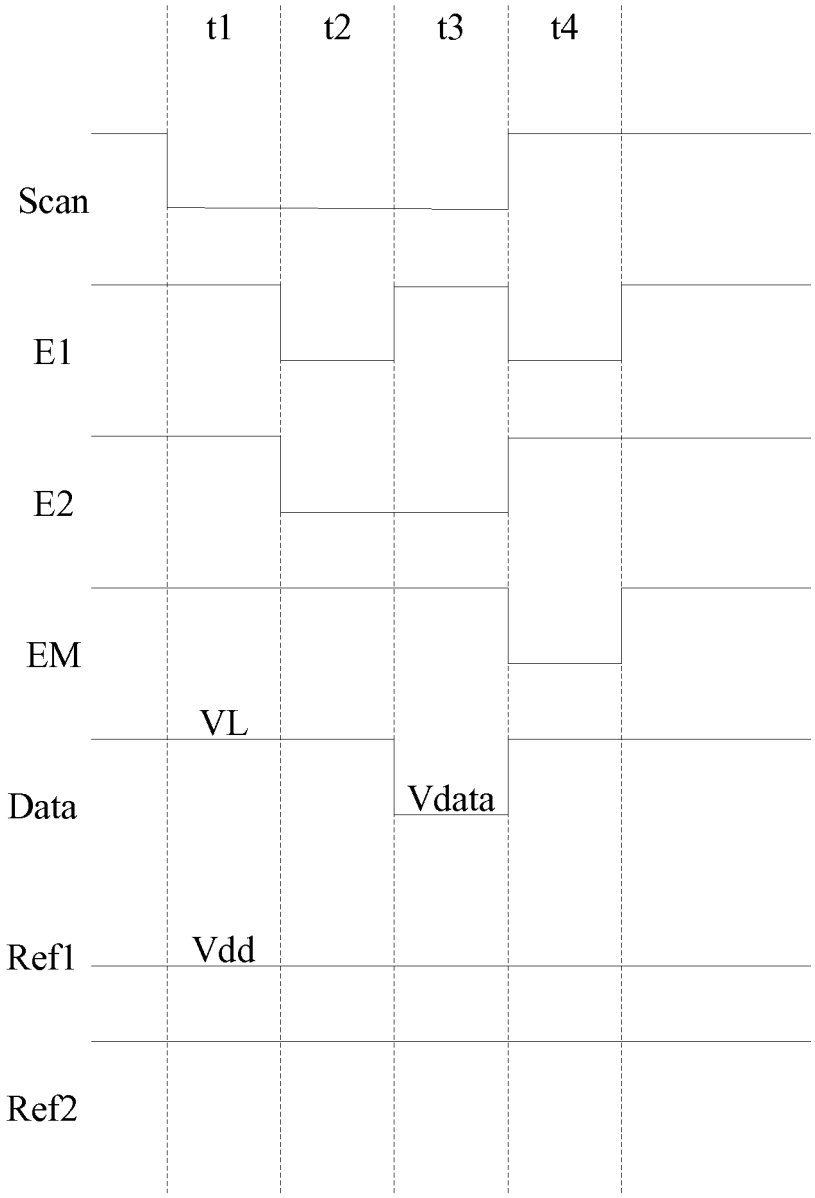

FIG. 4b

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/072623

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/32 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G 3/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, EPODOC, WPI: BOE TECHNOLOGY GROUP CO., LTD.; HEFEI XINSHENG OPTOELECTRONIC TECHNOLOGY CO., LTD.; MU, Suzhen; HU, Zuquan; luminescence, threshold voltage, pixel w circuit, initial+, compensat+, charg+, driv+, light, threshold, voltage

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 104318897 A (HEFEI XINSHENG OPTOELECTRONIC TECHNOLOGY CO., LTD. et al.), 28 January 2015 (28.01.2015), claims 1-8	1-16
PX	CN 204130142 U (HEFEI XINSHENG OPTOELECTRONIC TECHNOLOGY CO., LTD. et al.), 28 January 2015 (28.01.2015), claims 1-8	1-16
A	CN 103325343 A (BOE TECHNOLOGY GROUP CO., LTD. et al.), 25 September 2013 (25.09.2013), description, paragraphs 88-124, and figures 1, 4 and 5	1-16
A	CN 203300194 U (BOE TECHNOLOGY GROUP CO., LTD. et al.), 20 November 2013 (20.11.2013), the whole document	1-16
A	CN 103531151 A (BOE TECHNOLOGY GROUP CO., LTD. et al.), 22 January 2014 (22.01.2014), the whole document	1-16

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 July 2015 (22.07.2015)	**29 July 2015 (29.07.2015)**
Name and mailing address of the ISA/CN: State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No.: (86-10) 62019451	Authorized officer **ZHU, Xiaolin** Telephone No.: (86-10) **82245856**

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/072623

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010201673 A1 (SAMSUNG MOBILE DISPLAY CO., LTD.), 12 August 2010 (12.08.2010), the whole document	1-16
A	CN 102930813 A (BOE TECHNOLOGY GROUP CO., LTD. et al.), 13 February 2013 (13.02.2013), the whole document	1-16

Form PCT/ISA/210 (continuation of second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2015/072623

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN 104318897 A	28 January 2015	None	
CN 204130142 U	28 January 2015	None	
CN 103325343 A	25 September 2013	WO 2015000275 A1	08 January 2015
CN 203300194 U	20 November 2013	None	
CN 103531151 A	22 January 2014	WO 2015062298 A1	07 May 2015
US 2010201673 A1	12 August 2010	KR 20100090527 A	16 August 2010
CN 102930813 A	13 February 2013	None	

Form PCT/ISA/210 (patent family annex) (July 2009)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 201410640340 **[0001]**

专利名称(译)	像素电路，有机电致发光显示面板，以及显示装置及其驱动方法		
公开(公告)号	EP3220380A1	公开(公告)日	2017-09-20
申请号	EP2015775356	申请日	2015-02-10
[标]申请(专利权)人(译)	京东方科技集团股份有限公司 合肥鑫晟光电科技有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司. 合肥新盛光电科技有限公司有限公司		
当前申请(专利权)人(译)	京东方科技集团股份有限公司. 合肥新盛光电科技有限公司有限公司		
[标]发明人	MU SUZHEN HU ZUQUAN		
发明人	MU, SUZHEN HU, ZUQUAN		
IPC分类号	G09G3/32 G09G3/3233 G09G3/3266		
CPC分类号	G09G3/3225 G09G3/3258 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2300/0866 G09G2310/0251 G09G2310/08 G09G2320/043 G09G2320/045 G09G2320/0626 G09G3/3233 G09G2320/0233 G09G2300/0439		
代理机构(译)	Fritzsche也，THOMAS		
优先权	201410640340.0 2014-11-13 CN		
其他公开文献	EP3220380A4		
外部链接	Espacenet		

摘要(译)

本发明公开了一种像素电路，有机电致发光显示面板，显示装置及其驱动方法。像素电路在初始化阶段对第一节点和第三节点进行初始化，在补偿阶段对第一节点的驱动模块的阈值电压进行补偿，并在数据写入阶段对第一节点进行数据写入。。在发光阶段，驱动模块驱动发光模块中的发光器件发光，从而实现发光器件的正常发光功能。这样，与现有技术中的像素电路相比，本发明实施例提供的像素电路可以在初始化阶段对驱动模块的控制端进行初始化，对驱动器的阈值电压进行补偿。模块处于补偿阶段，并在数据写入阶段对驱动模块进行数据写入，从而防止驱动模块的阈值电压的变化影响发光器件的发光亮度，提高发光亮度的均匀性发光装置的结构，进一步确保了显示框架的质量。

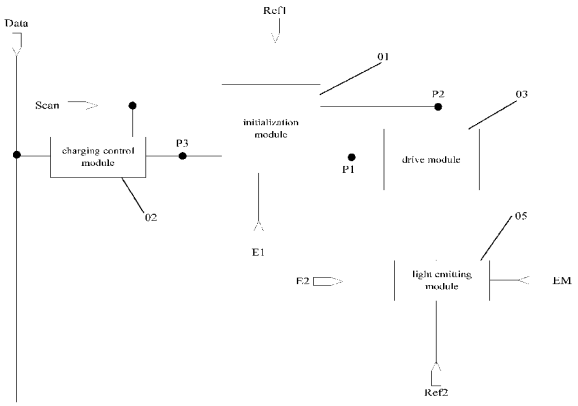

FIG. 2