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(54) PIXEL CIRCUIT, DISPLAY DEVICE, AND DRIVE METHOD THEREFOR

PIXELSCHALTUNG, ANZEIGEVORRICHTUNG UND ANSTEUERUNGSVERFAHREN DAFÜR

CIRCUIT DE PIXEL, DISPOSITIF D'AFFICHAGE, ET SON PROCÉDÉ DE PILOTAGE

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Description

TECHNICAL FIELD

[0001] The present invention relates to a pixel circuit, a display device and a method for driving the pixel circuit, and more particularly relates to a pixel circuit of an organic light-emitting diode capable of compensating a threshold voltage of a driving transistor, a display device and a method for driving the pixel circuit.

BACKGROUND

[0002] In recent years, various types of flat panel display devices, which have light weight and small size compared with cathode ray tube (CRT) displays, have been developed. Among the various types of flat panel display devices, by using a self-light-emitting organic light-emitting diode (OELD) to display images, an active matrix organic light-emitting display device with a thin-film transistor (TFT) backplane usually has the characteristics of short response time, low power consumption for driving, and better brightness and color purity. Therefore, the organic light-emitting display device has become a focus of the next-generation display devices.

[0003] FIG. 1 schematically shows a circuit diagram of a traditional active matrix organic light-emitting display device 100, wherein the active matrix organic light-emitting display device 100 comprises a data driver and a scanning driver (not shown in FIG. 1). The data driver is configured to control a plurality of data lines DA1...DAm in transversal arrangement, and the scanning driver is configured to control a plurality of scanning lines SC1...SCn in longitudinal arrangement. A plurality of pixel circuits 110 are formed in intersection areas between the plurality of data lines DA1...DAm and the plurality of scanning lines SC1...SCn.

[0004] With reference to FIG.1, the pixel circuit 110 comprises an organic light-emitting diode (OLED)1, a storage capacitor C11, a switching transistor T11, a driving transistor T12, a first power source ELVDD1, and a second power source ELVSS1, wherein both the transistors T11 and T12 are P-channel metal-oxide semiconductor transistors (PMOS). A grid of the switching transistor of the switching transistor T11 is coupled to one scanning line SC1, a source of the switching transistor T11 is coupled to one data line DA1, and a drain of the switching transistor T11 is coupled to a grid of the second transistor T12. A source of the driving transistor T12 is coupled to the high-voltage power source ELVDD1, and a drain of the driving transistor T12 is coupled to an anode of the OLED1. A cathode of the OLED1 is coupled to the low-voltage power source ELVSS1. A first terminal of the storage capacitor C11 is coupled to the first power source ELVDD1, and a second terminal of the storage capacitor C11 is coupled to the grid of the second transistor.

[0005] The scanning driver applies scanning signals to the scanning lines SC1 to SCn in sequence, and the data driver applies corresponding data signals via the data lines DA1 to DAm according to image data to be displayed. Thus, the pixel circuits 110 located in the intersection areas supply a driving current flowing through the organic light-emitting diode according to the signals of the scanning lines and data lines coupled to the pixel circuits.

[0006] Using the pixel circuit 110 shown in FIG. 1 as an example, when the scanning drive applies the scanning signals to the scanning line SC1, the switching transistor T11 is conducted, and at this point, a voltage of the data signals on the data line DA1 is stored in the storage capacitor C11 through the switching transistor T11. The driving transistor T12 supplies a driving current I_{OLED1} according to the voltage stored in the storage capacitor C11 to drive the organic light-emitting diode OLED1 to emit the light of the corresponding brightness. A formula for the driving current is shown as below:

$$I_{OLED1} = 1/12\mu_{12} \times C_{ox12} \times W_{12}/L_{12} \ (V_{GS12}-V_{TH12})^2 \ \text{(Formula 1)},$$

wherein μ_{12} is a carrier mobility of the driving transistor T12, C_{ox12} is a capacitance of a control end oxidation layer per unit area of the driving transistor T12, W_{12} is a channel width of the driving transistor T12, L_{12} is a channel length of the driving transistor T12, V_{GS12} is a voltage difference between the grid and the source of the driving transistor T12, and V_{TH12} is a threshold voltage of the driving transistor T12. That is, the driving current flowing through the organic light-emitting diode OLED1 can be controlled according to the magnitude of a data voltage from the data line DA1 to display a predefined grayscale.

[0007] A large active matrix organic light-emitting display device comprises a number of pixel circuits, and each of which need to comprise a driving transistor. The electric difference among different driving transistors results in different threshold voltages on the driving transistors. Therefore, according to the formula 1, it can be known that when the data voltages supplied to the pixel circuits 110 are the same, the driving currents supplied to the organic light-emitting diodes may vary with different threshold voltages of the driving transistors. This will result in the problems of poor quality uniformity and poor consistency of an image displayed by a plurality of pixel circuits.

[0008] US 2003/0132931 discloses a pixel circuit configured to apply a desired electric potential to a gate electrode

of a driving TFT of an EL device through a second TFT having its gate and drain connected to each other and configured such that a voltage equal to the threshold voltage of driving TFT is produced between the source and the drain of the second TFT. The TFTs are disposed in close proximity to each other within the pixel.

[0009] EP 2 146 337 discloses a pixel circuit capable of improving response characteristics and displaying an image having a uniform image quality.

[0010] US 2006/0082524 discloses a pixel circuit comprising an organic EL element, a first switch for switching data voltage supplied to a data line in response to a select signal, a first TFT for supplying the current to the organic EL element in response to the data voltage, a second TFT having a gate coupled to the gate of the first TFT for compensating deviations of the threshold voltage of the first TFT, and a capacitor for maintaining the data voltage supplied to the gate of the first TFT.

[0011] CN101847365 discloses a pixel circuit comprising a light-emitting component and a drive unit electrically connected with the light-emitting component. The drive unit comprising a first transistor configured to compensate the threshold voltage of a driving transistor and configured to control the light-emitting component to stop emitting light in response to a time-varying signal.

SUMMARY

[0012] In view of this, a main objective of the present invention is to provide a novel pixel circuit structure capable of compensating a difference in a threshold voltage of the driving transistor. The present invention provides a pixel circuit capable of producing a desired brightness and an active matrix organic light-emitting display device employing the pixel circuit, wherein the pixel circuit is capable of improving the response characteristic of the active matrix organic light-emitting diode to display the image with uniform image quality.

[0013] To achieve the above objective, the present teaching provides a pixel circuit as detailed in claim 1. Also provided is a method according to claim 9 and a display device according to claim 13.

[0014] Advantageous features are provided in dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

FIG. 1 is a diagram of a pixel circuit of a traditional active matrix organic light-emitting display device;
FIG. 2 is a schematic diagram of a pixel circuit according to a first embodiment of the present invention;
FIG. 3 is a signal timing diagram of a method for driving the pixel circuit as shown in FIG. 2.
FIG. 4 is a schematic diagram of a pixel circuit according to a second embodiment of the present invention;
FIG. 5 is a signal timing diagram of a method for driving the pixel circuit as shown in FIG. 4.
FIG. 6 is a schematic diagram of a pixel circuit according to a third embodiment of the present invention;
FIG. 7 is a signal timing diagram of a method for driving the pixel circuit as shown in FIG. 6.
FIG. 8 is a schematic diagram of a pixel circuit according to a fourth embodiment of the present invention;
FIG. 9 is a schematic diagram of a pixel circuit according to a fifth embodiment of the present invention; and
FIG. 10 is a schematic diagram of an active matrix organic light-emitting display device of the present invention.

DETAILED DESCRIPTION

[0016] In the following, the pixel circuit and the method for driving the pixel circuit according to the present invention will be further described in detail with reference to the appended drawings and the embodiments of the present invention.

[0017] It is necessary to note that the term "coupled/couple/coupling" as referred to in the present invention includes either direct connection between elements or connection between elements via other components.

[0018] For ease of description, a pixel circuit and a method for driving the pixel circuit according to an embodiment of the present invention will be described with reference to FIG. 2 and FIG. 3.

[0019] FIG. 2 shows a schematic diagram of a pixel circuit 200 according to a first embodiment of the present invention.

[0020] With reference to FIG. 2, the pixel circuit 200 comprises: a first transistor T1, a second transistor T2, a third transistor T3, a capacitor C1, and an organic light-emitting diode (OLED). Each of the transistors T1 to T3 comprises a control end, a first electrode 1, and a second electrode 2. The first electrode of the first transistor T1 is coupled to a data line Dm, the control end of the first transistor T1 is coupled to a node N1, and the second electrode of the first transistor T1 is coupled to the first electrode of the second transistor T2. The control end of the second transistor T2 is coupled to a first scanning line Sn1 configured to receive a first scanning signal from the first scanning line Sn1, the first electrode of the second transistor T2 is coupled to the second electrode of the second transistor, and the second electrode of the second transistor T2 is coupled to the node N1. A first terminal of the capacitor C1 is coupled to the node N1, and a

second terminal of the capacitor C1 is coupled to a second power source ELVSS. The control end of the third transistor T3 is coupled to the node N1, the first electrode of the third transistor T3 is coupled to the first power source ELVDD, and the second electrode of the third transistor T3 is coupled to an anode of the OLED. A cathode of the OLED is coupled to the second power source ELVSSO. Preferably, the control end may be a grid of each of the transistors T1 to T3, the first electrode may be a source of each of the transistors T1 to T3, and the second electrode may be a drain of each of the transistors T1 to T3. Similarly, the control end of each of the transistors T4, T5 and T6 may be a grid of each of the transistors T4 to T6, the first electrode may be a drain of each of the transistors T1 to T3, and the second electrode may be a drain of each of the transistors T1 to T3.

[0021] FIG. 3 shows a signal timing diagram for a method for driving the pixel circuit 200 as shown in FIG. 2. The signal timing as shown in FIG. 3 includes a first phase and a second phase, wherein the first phase t1 is a data writing phase, and the second phase t2 is a normal light-emitting phase. As all the transistors T1 to T3 in the pixel circuit 200 as shown in FIG. 2 are described using PMOS transistors as an example, the transistors are conducted when low-level signals are applied to the control ends of the transistors.

[0022] As shown in FIG. 3, in the first phase, i.e., a time period t1 in which the scanning signals are applied to the scanning line Sn1, the first transistor T1 and the second transistor T2 respond to the low-level scanning signals Sn1 to be conducted. Therefore, the data signals Vdata from the data line Dm are provided to the node N1 via the first transistor T1 and the second transistor T2. It can be understood that, at this point, the voltage value at the node N1 is a voltage value corresponding to a differential value between the data signals Vdata and the threshold voltage of the first transistor T1, i.e., Vdata-$|V_{TH1}|$, which is equivalent to Vdata+V_{TH1}. Further, the voltage at the node N1 is also stored in the capacitor C1. That is, the data signals Vdata on the data line Dmare are read into the pixel circuit 200.

[0023] In the second phase t2, that is, after the voltage of the first scanning line Sn1 jumps to a high level, the OLED enters the normal light-emitting phase. At this point, a current of the first power source ELVDD flows through the third transistor T3 into the anode of the OLED.

[0024] The driving current flowing into the OLED is shown as a formula below:

$$I_{OLED}=1/2\mu_3\times C_{ox3}\times W_3/L_3\times(V_{GS3}-V_{TH3})^2 \text{ (Formula 2),}$$

wherein μ_3 is a carrier mobility of the third transistor T3; C_{ox3} is a capacitance of a control end oxidation layer per unit area of the third transistor T3, W_3 is a channel width of the third transistor, and L_3 is a channel length of the third transistor T3. V_{GS3} is a voltage difference between the grid and the source of the third transistor T3, and V_{TH3} is the threshold voltage of the third transistor T3.

[0025] At this point, as the third transistor is conducted, the voltage V_{GS3} for the grid and the source is the voltage (Vdata+V_{TH1}) at the node N1, and the voltage difference between the voltage V_{GS3} and the voltage Vdd of the first power source is Vdata+V_{TH1}-Vdd. Therefore, through calculation in the above formula, the following formula may be obtained:

$$I_{OLED}=1/2\mu_3\times C_{ox3}\times W_3/L_3\times(V_{data}+V_{TH1}-V_{dd}-V_{TH3})^2 \text{ (Formula 3).}$$

[0026] It follows that the impact of the threshold voltage of the third transistor T3 to the driving current of OLED may be reduced by arranging the first transistor T1 with appropriate electric characteristics.

[0027] Preferably, if the transistors T1 and T3 with similar electrical characteristics as much as possible are arranged, the threshold voltage of the third transistor T3 can be offset to almost zero, thereby allowing the driving current flowing into the OLED to be free from the impact of the threshold voltage of the third transistor T3. That is, the current value of the OLED is as follows:

$$I_{OLED}=1/2\mu_3\times C_{ox3}\times W_3/L_3\times(V_{data}-V_{dd})^2 \text{ (Formula 4).}$$

[0028] Wherein for the arrangement of the first transistor T1 and the third transistor T3 with similar electrical characteristics as much as possible, two transistors approximate in channel width and channel length as much as possible may be arranged, and are arranged in the pixel circuit 200 in a close range.

[0029] Preferably, the pixel circuit 200 may also be arranged on a TFT backplane, with the first and third transistors T1 and T3 symmetrically arranged, so that the threshold voltages of the first and third transistors T1 and T3 are as close as possible.

[0030] FIG. 4 shows a schematic diagram of a pixel circuit 300 according to a second embodiment of the present invention. Compared with the pixel circuit as shown in FIG. 2, the pixel circuit 300 further comprises a fourth transistor

T4; wherein a control end of the fourth transistor T4 is coupled to a second scanning line Sn2 configured to receive a second scanning signal from the second scanning line Sn2, a first electrode of the fourth transistor T4 is coupled to the second electrode of the third transistor T3, and a second electrode of the fourth transistor T4 is coupled to the anode of the OLED

[0031] FIG. 5 shows a signal timing diagram of a drive method according to the pixel circuit 300 as shown in FIG. 4. Compared with the signal timing diagram as shown in FIG. 3, the signal timing diagram as shown in FIG.4 is different in that the scanning signal is provided to the second scanning line Sn2 in the second phase t2. At this point, the third transistor T3 and the fourth transistor T4 are conducted simultaneously, thereby providing the data signals to the OLED through the third transistor T3 and the fourth transistor T4. Furthermore, the OLED enters the normal light-emitting phase.

[0032] It can be understood that as the fourth transistor T4 is arranged in the pixel circuit 300, the conduction time and the shutdown time of the fourth transistor T4 may be controlled through the second scanning line Sn2, thereby controlling the light-emitting time of the OLED through the fourth transistor T4. That is, when the transistor T4 is shut down, the OLED does not emit light; and when the transistor T4 is conducted, the OLED emits light. The OLED in the pixel circuit 200 as shown in FIG. 2 is always in a light-emitting state since the third transistor T3 is conducted continuously. Therefore, the light-emitting effect of the pixel circuit 3 becomes more stable.

[0033] FIG. 6 shows a schematic diagram of a pixel circuit 400 according to a third embodiment of the present invention. Compared with the pixel circuit 300 as shown in FIG. 4, the pixel circuit 400 further comprises a fifth transistor T5; wherein a control end of the fifth transistor T5 is coupled to a third scanning line Sn3 configured to receive a third scanning signal from the third scanning line Sn3, a first electrode of the fifth transistor T5 is coupled to the node N1, and a second electrode of the fifth transistor T5 is coupled to the third power source. The voltage Vinit of the third power source is not higher than $V_{ELVSS.}$

[0034] For those skilled in the art, it can be understood that when the value of Vinit is equal to that of V_{ElVSS}, the source electrode of the fifth transistor can be coupled to the second power source ELVSS.

[0035] FIG. 7 shows a signal timing diagram of a pixel circuit 400 as shown in FIG. 6. The signal timing further comprises an initialization phase before the first phase.

[0036] In the initialization phase, i.e., the time period t0 in which the scanning signals are provided to the scanning line Sn3, the fifth transistor T5 is conducted, thereby supplying the voltage of the third power source Vinit to the node N1 and the anode of the OLED.

[0037] That is, the fifth transistor T5 supplies a constant voltage to the node N1 and the anode of the OLED in the initialization time period. Thus, the voltage at the node N1 and the voltage of the capacitor C1 are initialized to be Vinit.

[0038] Preferably, the initialized voltage Vinit may be set to be the same as the voltage of the second power source ELVSS.

[0039] FIG. 8 shows a schematic diagram of a pixel circuit 500 according to the fourth embodiment of the present invention. Compared with the circuit as shown in FIG. 6, the pixel circuit 500 further comprises a sixth transistor T6.

[0040] The sixth transistor T6 is coupled between the anode of the OLED and the second power source ELVSS. A control end of the sixth transistor T6 and the control end of the fifth transistor T5 are jointly coupled to the scanning line Sn3 configured to receive a third scanning signal; and a first electrode and a second electrode of the sixth transistor T6 are respectively coupled to the anode and the cathode of the OLED. In the time period in which the low-level scanning signal is provided to the scanning line Sn3, the sixth transistor T6 is conducted. Since the first and second electrodes of the sixth transistor T6 are respectively coupled to the anode and the cathode of the OLED, the driving current may be prevented from being supplied to the OLED.

[0041] FIG. 9 shows a schematic diagram of a pixel circuit 600 according to a fifth embodiment of the present invention. Compared with the circuit as shown in FIG. 7, the pixel circuit 600 further comprises a second capacitor C2. The second capacitor C2 is coupled between the control end of the second transistor T2 and the node N1.

[0042] It can be understood that in the time period in which the scanning signal of the scanning line Sn1 jumps from low level to high level, since Vdata is stored in the node N1, the voltage increases the potential of the node N1 through the coupling effect of the second capacitor C2 when the voltage of the scanning line Sn1 turns into high level, thereby correspondingly improving the voltage $Vdata+V_{TH1}$ of the control end of the third transistor T3 and storing the corresponding voltage into the second capacitor C2.Due to Vdata < Vdd, from the formula 4, it can be known that the increase in the voltage value of the control end of the third transistor T3 results in the decrease of the differential value between the voltage of the control end of the third transistor T3 and Vdd. Therefore, when the voltage of the data signals, read into the pixel circuit 600, is very small, i.e. when the grayscale for light emitting is very low, the driving current flowing through the OLED is made to decrease further, thereby improving the contrast among different grayscales of the pixel circuit.

[0043] It is necessary to note that the first transistor T1, the second transistor T2, the third transistor T3, the fourth transistor T4, the fifth transistor T5, and the sixth transistor T6 in the pixel circuits of the embodiments above are described by using the P-channel metal-oxide semiconductor transistor as an example. Those skilled in the art may understand that the transistors T1 to T6 in the pixel circuit of the present invention may also be implemented by using N-channel

metal-oxide semiconductor transistors.

[0044] FIG. 10 shows an active matrix organic light-emitting display device 600 comprising the pixel circuit according to the embodiments of the present invention.

[0045] With reference to FIG. 10, a display device 700 comprises: a first power source ELVDD, a second power source ELVSS, a scanning driver 702, a data driver 703, and a plurality of pixel circuits 701 arranged in intersection areas between the scanning lines Sn1, Sn2 and Sn3 and the data lines D1 to Dm in a matrix manner. The first power source ELVDD and the second power source ELVSS supply corresponding power voltages to the plurality of pixel circuits 701 through corresponding row lines (with the number of n) and column lines (with the number of m).

[0046] Each pixel circuit 701 is coupled to the corresponding scanning line (for example, Sn2, Sn2 and Sn3) and data line respectively. For example, the pixel circuit 701 located in the row i and the column j is coupled to the scanning lines Si1, Si2 and Si3 of the row i and the data line Dj of the column j.

[0047] The scanning driver 702 generates the scanning signals corresponding to the scanning signals provided externally (for example, by a certain control unit). The scanning signals generated by the scanning driver 702 are respectively provided to the pixel circuits 701 in sequence through the scanning lines Si1 to Sin.

[0048] The data driver 703 generates the data signals corresponding to the data and data control signals provided externally (for example, by a certain control unit). The data signals generated by the data driver 703 are provided to the pixel circuit 701 through the data lines D1 to Dm in synchronization with the scanning signals, wherein the pixel circuit 701 may be any one pixel circuit as shown in the embodiments above. It can be understood that the number of the scanning lines in each row may be differently arranged accordingly according to different embodiments of the pixel circuit.

[0049] Although the present invention is described with reference to specific exemplary embodiments, it should be understood that the present invention is not limited to such embodiments.

Claims

1. A pixel circuit, comprising: a first power source (ELVDD), a second power source (ELVSS), an organic light-emitting diode (OLED), a first capacitor (C1), a first transistor (T1), a second transistor (T2), and a third transistor (T3); wherein a cathode of the organic light-emitting diode is coupled to the second power source;
each of the first transistor, the second transistor, and the third transistor is provided with a control end, a first electrode (1), and a second electrode (2); wherein
the control end of the first transistor is coupled to a node (N1), and the first electrode of the first transistor is configured to receive a data signal (Vdata);
the control end of the second transistor (T2) is configured to receive a first scanning signal, the first electrode of the second transistor is coupled to the second electrode of the first transistor, and the second electrode of the second transistor is coupled to the node and a terminal of the first capacitor (C1);
the control end of the third transistor is coupled to the node, the first electrode of the third transistor is coupled to the first power source, and the second electrode of the third transistor is coupled to an anode of the light-emitting diode and wherein there is a direct connection of the control end of the first transistor and the control end of the third transistor at the node;
characterized in that the first capacitor is coupled between the node (N1) and the second power source, and **in that** the first transistor and the third transistor are configured to be approximate in channel width and channel length, and are arranged in the pixel circuit in a close range to compensate a threshold voltage of the third transistor (T3).

2. The pixel circuit according to claim 1, wherein:

the pixel circuit is arranged on a TFT backplane; and
the first transistor and the third transistor are symmetrically arranged on the TFT backplane.

3. The pixel circuit according to claim 1, further comprising a fourth transistor; wherein,
a control end of the fourth transistor is configured to receive a second scanning signal, a first electrode of the fourth transistor is coupled to the second electrode of the third transistor, and a second electrode of the fourth transistor is coupled to an anode of the light-emitting diode.

4. The pixel circuit according to claim 1, further comprising a fifth transistor and a third power source;
wherein the fifth transistor comprises: a control end configured to receive a third scanning signal, a first electrode coupled to the node, and a second electrode coupled to the third power source.

5. The pixel circuit according to claim 4, wherein a voltage of the third power source is lower than or equal to a voltage

of the second power source.

6. The pixel circuit according to claim 4, further comprising a sixth transistor;
wherein the sixth transistor comprises: a control end configured to receive the third scanning signal, a first electrode coupled to the anode of the light-emitting diode, and a second electrode coupled to the second power source.

7. The pixel circuit according to claim 1, further comprising a second capacitor coupled between the control end of the second transistor and the node.

8. The pixel circuit according to any one of claims 1 to 7, wherein:

the transistors are P-channel metal-oxide semiconductor transistors.

9. A method for driving the pixel circuit according to claim 1, the drive method comprises applying a first scanning signal to a first scanning line for conducting the second transistor such that data signals from a data line are provided to the node (N1) via the first transistor and the second transistor, and storing a voltage at the node in the first capacitor; providing the data signals to the light-emitting diode via the third transistor; and emitting, by the light-emitting diode, light with a brightness matching the data signals.

10. The drive method according to claim 9, wherein:

the pixel circuit further comprises a fourth transistor according to claim 3, and
the method further comprises:

applying a second scanning signal to a second scanning line for conducting the fourth transistor such that the data signals are provided to the light-emitting diode via the third transistor.

11. The drive method according to claim 10, wherein:

the pixel circuit further comprises a fifth transistor according to claim 4, and the method comprises applying a third scanning signal for conducting the fifth transistor, before applying the first scanning signal, to initialize the node.

12. The drive method according to claim 9, wherein:

the pixel circuits are arranged on a TFT backplane; and
the first transistor and the third transistor are symmetrically arranged on the TFT backplane.

13. A display device (700), comprising:

a scanning driver (702), configured to apply a scanning signal to a scanning line (Sn1, Sn2, Sn3);
a data driver (703), configured to apply a data signal to a data line (D1-Dm); and
a pixel circuit (701) coupled between the data lines and scanning lines, in accordance with any one of claims 1 to 8.

Patentansprüche

1. Pixelschaltung, die Folgendes umfasst: eine erste Stromquelle (ELVDD), eine zweite Stromquelle (ELVSS), eine organische Leuchtdiode (OLED), einen ersten Kondensator (C1), einen ersten Transistor (T1), einen zweiten Transistor (T2) und einen dritten Transistor (T3), wobei
eine Kathode der organischen Leuchtdiode an die zweite Stromquelle gekoppelt ist;
jeder des ersten Transistors, des zweiten Transistors und des dritten Transistors über ein Steuerende, eine erste Elektrode (1) und eine zweite Elektrode (2) verfügt; wobei
das Steuerende des ersten Transistors an einen Knoten (N1) gekoppelt ist, und die erste Elektrode des ersten Transistors konfiguriert ist, ein Datensignal (Vdata) zu empfangen;
das Steuerende des zweiten Transistors (T2) konfiguriert ist, ein erstes Abtastsignal zu empfangen, die erste Elektrode des zweiten Transistors an die zweite Elektrode des ersten Transistors gekoppelt ist und die zweite Elektrode des zweiten Transistors an den Knoten und einen Anschluss des ersten Kondensators (C1) gekoppelt ist;

das Steuerende des dritten Transistors an den Knoten gekoppelt ist, die erste Elektrode des dritten Transistors an die erste Stromquelle gekoppelt ist und die zweite Elektrode des dritten Transistors an eine Anode der Leuchtdiode gekoppelt ist, und wobei es eine direkte Verbindung des Steuerendes des ersten Transistors und des Steuerendes des dritten Transistors am Knoten gibt;
dadurch gekennzeichnet, dass der erste Kondensator zwischen den Knoten (N1) und die zweite Stromquelle gekoppelt ist, und dass der erste Transistor und der dritte Transistor konfiguriert sind, annähernd in Kanalbreite und Kanallänge zu sein, und in der Pixelschaltung in unmittelbarer Nähe angeordnet sind,
um eine Schwellenspannung des dritten Transistors (T3) zu kompensieren.

2. Pixelschaltung nach Anspruch 1, wobei:

die Pixelschaltung auf einer TFT-Rückwandplatine angeordnet ist; und
der erste Transistor und der dritte Transistor symmetrisch auf der TFT-Rückwandplatine angeordnet sind.

3. Pixelschaltung nach Anspruch 1, die ferner einen vierten Transistor umfasst; wobei ein Steuerende des vierten Transistors konfiguriert ist, ein zweites Abtastsignal zu empfangen, eine erste Elektrode des vierten Transistors an die zweite Elektrode des dritten Transistors gekoppelt ist und eine zweite Elektrode des vierten Transistors an eine Anode der Leuchtdiode gekoppelt ist.

4. Pixelschaltung nach Anspruch 1, die ferner einen fünften Transistor und eine dritte Stromquelle umfasst;
wobei der fünfte Transistor Folgendes umfasst: ein Steuerende, das konfiguriert ist, ein drittes Abtastsignal zu empfangen, eine erste Elektrode, die an den Knoten gekoppelt ist, und eine zweite Elektrode, die an die dritte Stromquelle gekoppelt ist.

5. Pixelschaltung nach Anspruch 4, wobei eine Spannung der dritten Stromquelle niedriger als oder gleichgroß wie eine Spannung der zweiten Stromquelle ist.

6. Pixelschaltung nach Anspruch 4, die ferner einen sechsten Transistor umfasst;
wobei der sechste Transistor Folgendes umfasst: ein Steuerende, das konfiguriert ist, das dritte Abtastsignal zu empfangen, eine erste Elektrode, die an die Anode der Leuchtdiode gekoppelt ist, und eine zweite Elektrode, die an die zweite Stromquelle gekoppelt ist.

7. Pixelschaltung nach Anspruch 1, die ferner einen zweiten Kondensator umfasst, der zwischen das Steuerende des zweiten Transistors und den Knoten gekoppelt ist.

8. Pixelschaltung nach einem der Ansprüche 1 bis 7, wobei:

die Transistoren P-Kanal-Metalloxid-Halbleitertransistoren sind.

9. Verfahren zum Ansteuern der Pixelschaltung nach Anspruch 1, wobei das Ansteuerungsverfahren Folgendes umfasst:

Anlegen eines ersten Abtastsignals an eine erste Abtastlinie zum Leiten des zweiten Transistors, sodass Datensignale von einer Datenlinie dem Knoten (N1) über den ersten Transistor und den zweiten Transistor bereitgestellt werden,
Speichern einer Spannung am Knoten im ersten Kondensator;
Bereitstellen der Datensignale an die Leuchtdiode über den dritten Transistor; und
Ausstrahlen von Licht durch die Leuchtdiode, dessen Helligkeit den Datensignalen entspricht.

10. Ansteuerungsverfahren nach Anspruch 9, wobei:

die Pixelschaltung ferner einen vierten Transistor nach Anspruch 3 umfasst und das Verfahren ferner Folgendes umfasst:

Anlegen eines zweiten Abtastsignals an eine zweite Abtastlinie zum Leiten des vierten Transistors, sodass die Datensignale der Leuchtdiode über den dritten Transistor bereitgestellt werden.

11. Ansteuerungsverfahren nach Anspruch 10, wobei:

die Pixelschaltung ferner einen fünften Transistor nach Anspruch 4 umfasst und das Verfahren Folgendes umfasst:

Anlegen eines dritten Abtastsignals zum Leiten des fünften Transistors vor dem Anlegen des ersten Abtastsignals, um den Knoten zu initialisieren.

12. Ansteuerungsverfahren nach Anspruch 9, wobei:

die Pixelschaltungen auf einer TFT-Rückwandplatine angeordnet sind; und
der erste Transistor und der dritte Transistor symmetrisch auf der TFT-Rückwandplatine angeordnet sind.

13. Anzeigevorrichtung (700), die Folgendes umfasst:

einen Abtasttreiber (702), der konfiguriert ist, ein Abtastsignal an eine Abtastlinie (Sn1, Sn2, Sn3) anzulegen;
einen Datentreiber (703), der konfiguriert ist, ein Datensignal an eine Datenlinie (D1 - Dm) anzulegen; und
eine Pixelschaltung (701) nach einem der Ansprüche 1 bis 8, die zwischen die Datenlinien und die Abtastlinien gekoppelt ist.

Revendications

1. Circuit de pixel, comprenant : une première source d'alimentation (ELVDD), une deuxième source d'alimentation (ELVSS), une diode électroluminescente organique (OLED), un premier condensateur (C1), un premier transistor (T1), un deuxième transistor (T2) et un troisième transistor (T3);
dans lequel
une cathode de la diode électroluminescente organique est couplée à la deuxième source d'alimentation ;
chacun du premier transistor, du deuxième transistor et du troisième transistor est doté d'une extrémité de commande, d'une première électrode (1) et d'une seconde électrode (2); dans lequel
l'extrémité de commande du premier transistor est couplée à un noeud (N1),
et la première électrode du premier transistor est configurée pour recevoir un signal de données (Vdata) ;
l'extrémité de commande du deuxième transistor (T2) est configurée pour recevoir un premier signal de balayage, la première électrode du deuxième transistor est couplée à la seconde électrode du premier transistor, et la seconde électrode du deuxième transistor est couplée au noeud et à une borne du premier condensateur (C1) ;
l'extrémité de commande du troisième transistor est couplée au noeud, la première électrode du troisième transistor est couplée à la première source d'alimentation, et la seconde électrode du troisième transistor est couplée à une anode de la diode électroluminescente et dans lequel il existe une connexion directe de l'extrémité de commande du premier transistor et de l'extrémité de commande du troisième transistor au niveau du noeud ;
caractérisé en ce que le premier condensateur est couplé entre le noeud (N1) et la deuxième source d'alimentation, et **en ce que** le premier transistor et le troisième transistor sont configurés pour se trouver approximativement dans la largeur de canal et la longueur de canal, et sont agencés dans le circuit de pixel à distance rapprochée pour compenser une tension de seuil du troisième transistor (T3).

2. Circuit de pixel selon la revendication 1, dans lequel :

le circuit de pixel est agencé sur une face arrière de TFT ; et
le premier transistor et le troisième transistor sont agencés symétriquement sur la face arrière de TFT.

3. Circuit de pixel selon la revendication 1, comprenant en outre un quatrième transistor ; dans lequel,
une extrémité de commande du quatrième transistor est configurée pour recevoir un deuxième signal de balayage,
une première électrode du quatrième transistor est couplée à la seconde électrode du troisième transistor, et une seconde électrode du quatrième transistor est couplée à une anode de la diode électroluminescente.

4. Circuit de pixel selon la revendication 1, comprenant en outre un cinquième transistor et une troisième source d'alimentation ;
dans lequel le cinquième transistor comprend : une extrémité de commande configurée pour recevoir un troisième signal de balayage, une première électrode couplée au noeud, et une seconde électrode couplée à la troisième source d'alimentation.

5. Circuit de pixel selon la revendication 4,
dans lequel une tension de la troisième source d'alimentation est inférieure ou égale à une tension de la deuxième source d'alimentation.

6. Circuit de pixel selon la revendication 4, comprenant en outre un sixième transistor ;
dans lequel le sixième transistor comprend : une extrémité de commande configurée pour recevoir le troisième signal de balayage, une première électrode couplée à l'anode de la diode électroluminescente, et une seconde électrode couplée à la deuxième source d'alimentation.

7. Circuit de pixel selon la revendication 1, comprenant en outre un second condensateur couplé entre l'extrémité de commande du deuxième transistor et le noeud.

8. Circuit de pixel selon l'une quelconque des revendications 1 à 7, dans lequel :

les transistors sont des transistors métal-oxyde-semi-conducteurs à canal P.

9. Procédé de pilotage du circuit de pixel selon la revendication 1, le procédé de pilotage comprend
l'application d'un premier signal de balayage à une première ligne de balayage pour conduire le deuxième transistor de telle sorte que les signaux de données provenant d'une ligne de données soient fournis au noeud (N1) via le premier transistor et le deuxième transistor, et le stockage d'une tension au niveau du noeud dans le premier condensateur ;
la fourniture des signaux de données à la diode électroluminescente via le troisième transistor ; et l'émission, par la diode électroluminescente, de lumière avec une luminosité s'adaptant aux signaux de données.

10. Procédé de pilotage selon la revendication 9, dans lequel :

le circuit de pixel comprend en outre un quatrième transistor selon la revendication 3, et le procédé comprend en outre :

l'application d'un deuxième signal de balayage à une seconde ligne de balayage pour conduire le quatrième transistor de telle sorte que les signaux de données soient fournis à la diode électroluminescente via le troisième transistor.

11. Procédé de pilotage selon la revendication 10, dans lequel :

le circuit de pixel comprend en outre un cinquième transistor selon la revendication 4, et le procédé comprend l'application d'un troisième signal de balayage pour conduire le cinquième transistor, avant d'appliquer le premier signal de balayage, afin d'initialiser le noeud.

12. Procédé de pilotage selon la revendication 9, dans lequel :

les circuits de pixel sont agencés sur une face arrière de TFT ; et
le premier transistor et le troisième transistor sont agencés de manière symétrique sur la face arrière du TFT.

13. Dispositif d'affichage (700), comprenant :

un pilote de balayage (702), configuré pour appliquer un signal de balayage à une ligne de balayage (Sn1, Sn2, Sn3) ;
un pilote de données (703), configuré pour appliquer un signal de données à une ligne de données (D1-Dm) ; et un circuit de pixel (701) couplé entre les lignes de données et les lignes de balayage, selon l'une quelconque des revendications 1 à 8.

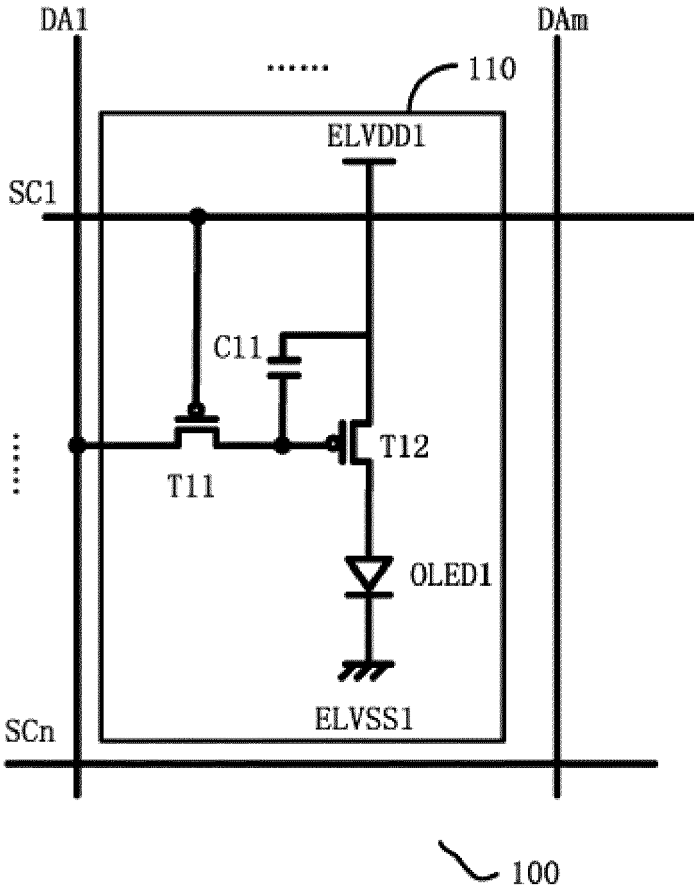

FIG. 1

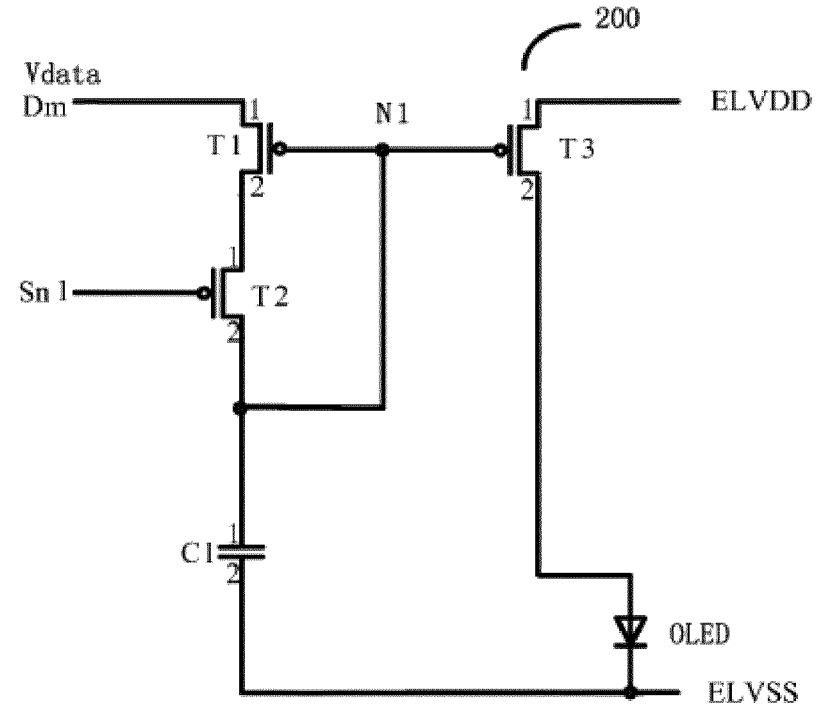

FIG. 2

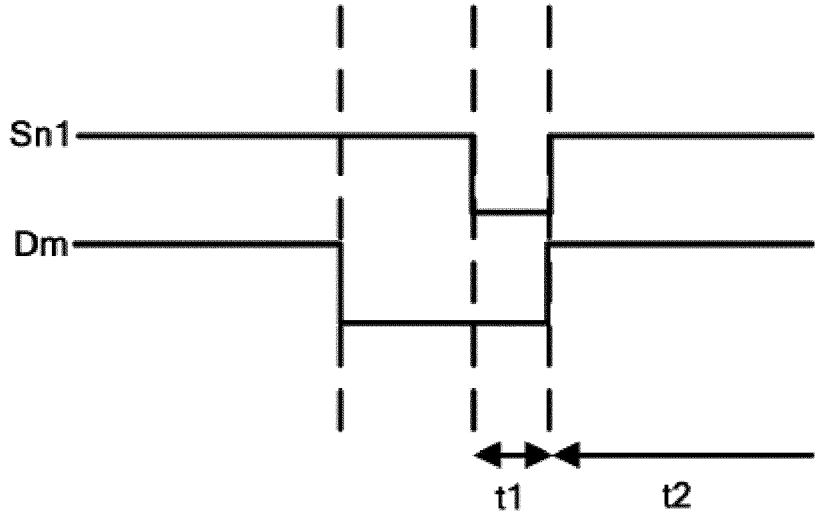

FIG. 3

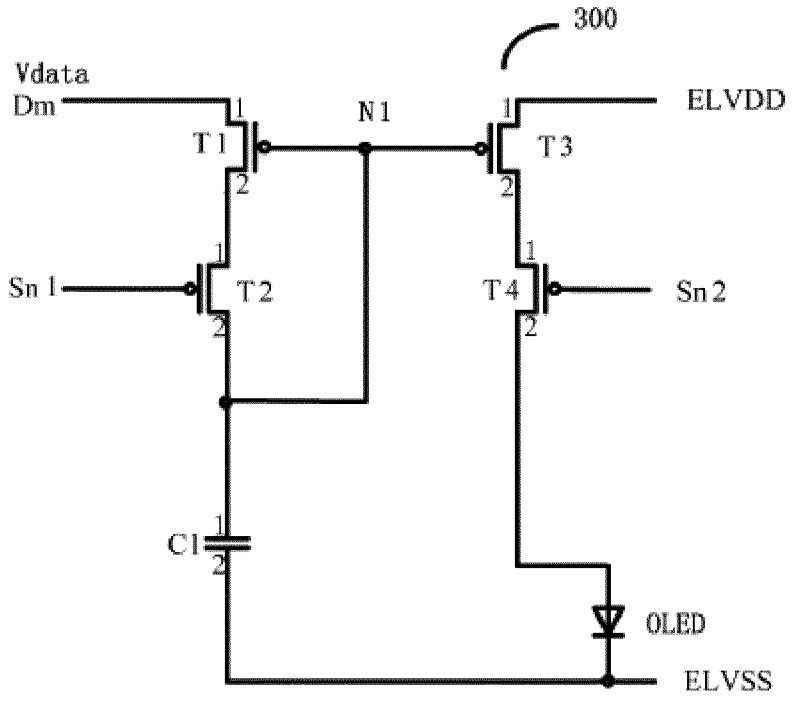
300
Vdata
Dm
N1
ELVDD
T1
T3
Sn1
T2
T4
Sn2
C1
OLED
ELVSS

FIG. 4

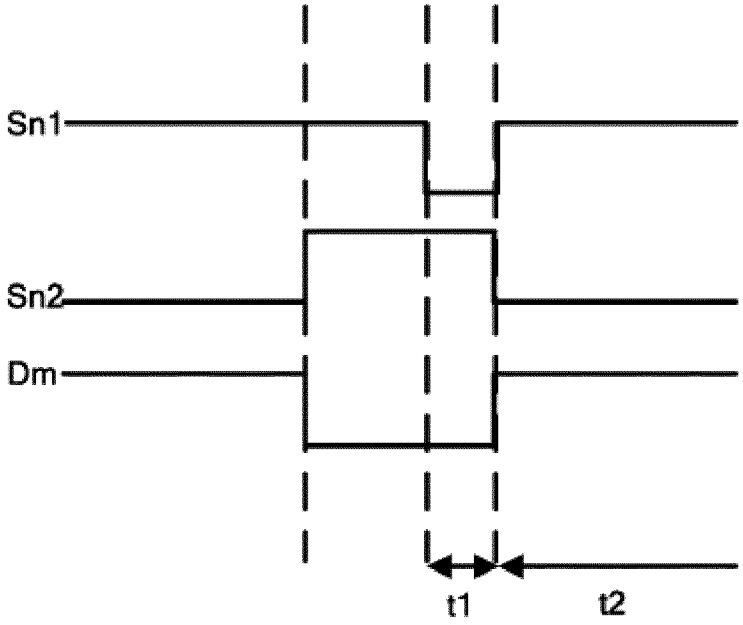
Sn1
Sn2
Dm
t1
t2

FIG. 5

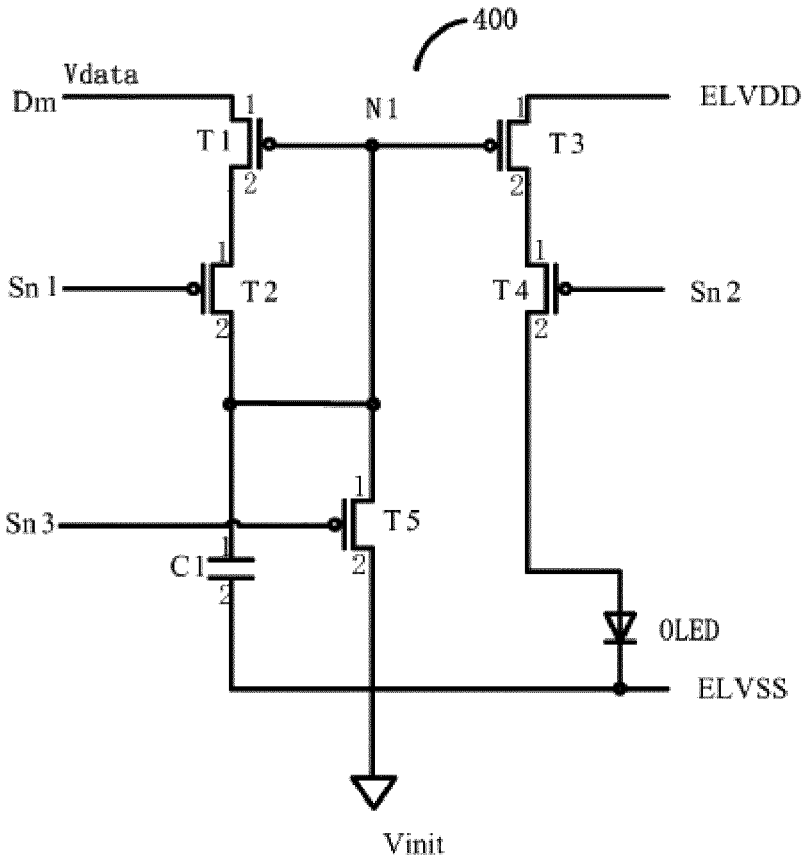
400
Vdata
Dm
N1
ELVDD
T1
T3
Sn1
T2
T4
Sn2
Sn3
T5
C1
OLED
ELVSS
Vinit

FIG. 6

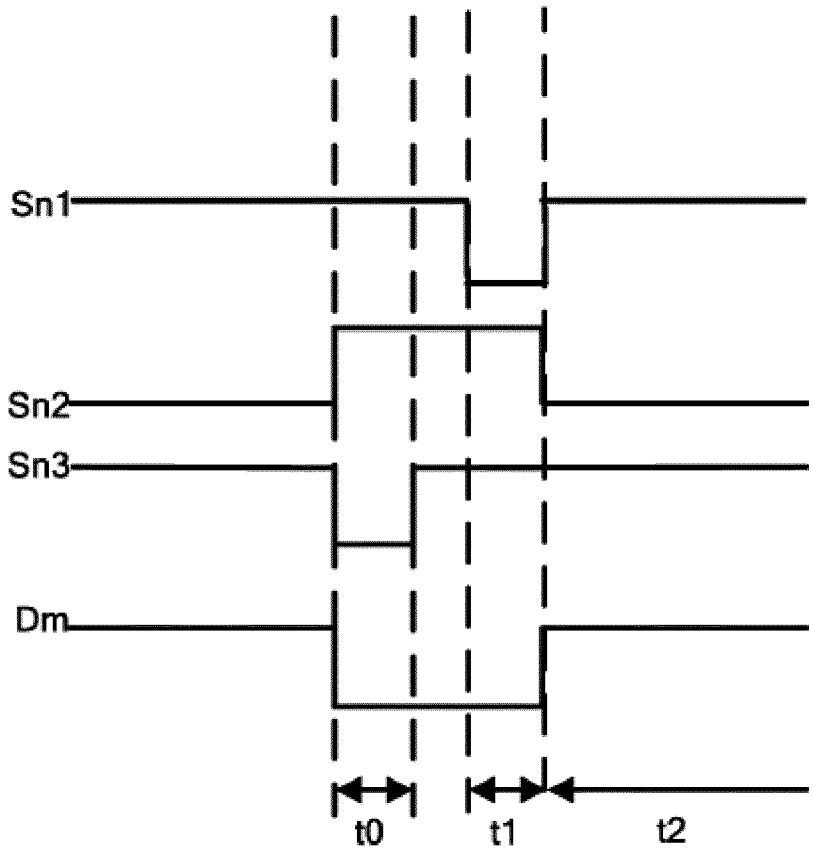

FIG. 7

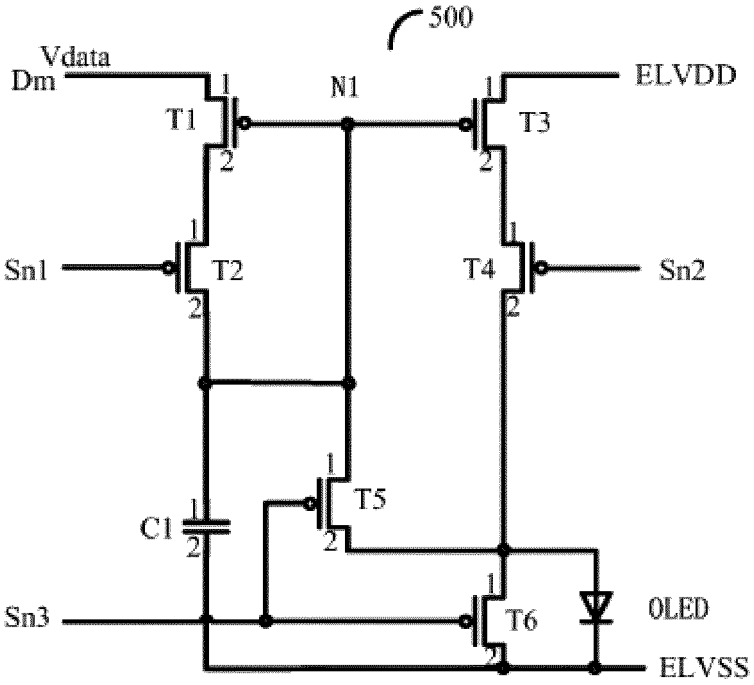

FIG. 8

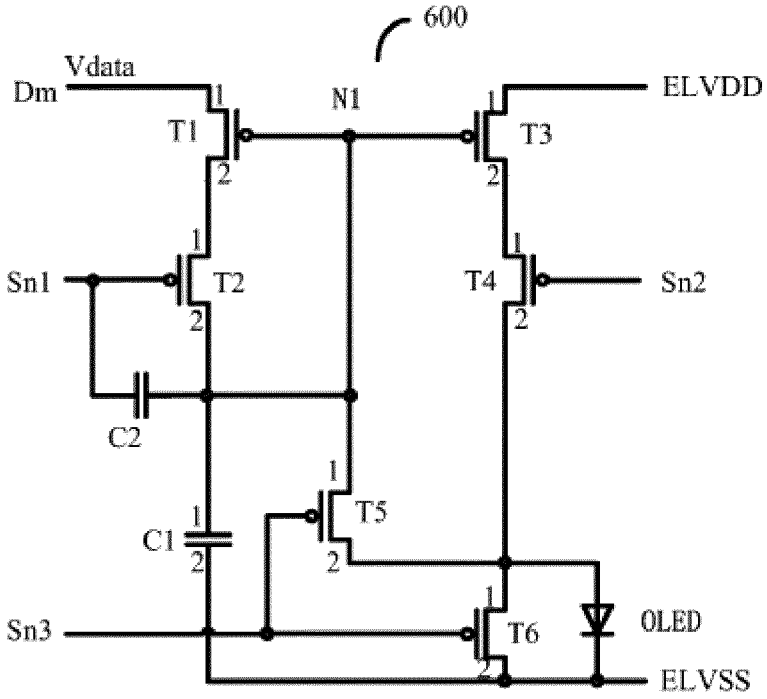
600
Vdata
Dm
N1
ELVDD
T1
T3
Sn1
T2
T4
Sn2
C2
T5
C1
Sn3
T6
OLED
ELVSS

FIG. 9

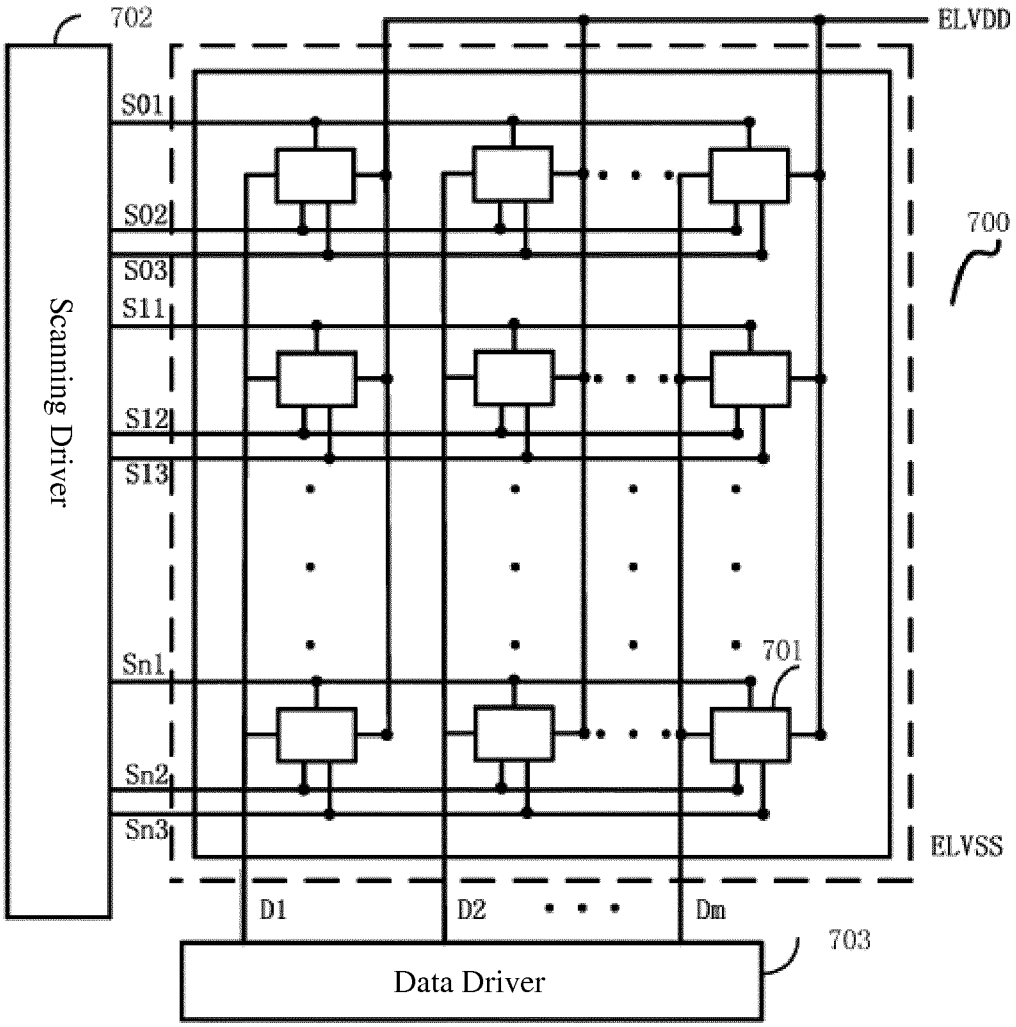
702
ELVDD
S01
S02
S03
S11
S12
S13
Scanning Driver
700
701
Sn1
Sn2
Sn3
ELVSS
D1
D2
Dm
703
Data Driver

FIG. 10

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20030132931 A **[0008]**
- EP 2146337 A **[0009]**
- US 20060082524 A **[0010]**
- CN 101847365 **[0011]**

专利名称(译)	像素电路，显示装置及其驱动方法		
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[标]申请(专利权)人(译)	昆山工研院新型平板显示技术中心有限公司 昆山国显光电有限公司		
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当前申请(专利权)人(译)	昆山新型平板显示技术中心CO.LTD 昆山GO-维信诺光电科技有限公司.		
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发明人	ZHU, HUI QIU, YONG HUANG, XIUQI GAO, XIAOYU HU, SIMING HAN, ZHENZHEN		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3258 G09G3/3233 G09G3/3291 G09G2300/0814 G09G2300/0819 G09G2300/0842 G09G2300/0852 G09G2300/0861 G09G2310/0251 G09G2310/0262 G09G2320/043 G09G2330/028		
优先权	201210587996.1 2012-12-31 CN		
其他公开文献	EP2940682A1 EP2940682A4		
外部链接	Espacenet		

摘要(译)

像素电路，显示装置及其驱动方法。像素电路包括：第一电源（ELVDD），第二电源（ELVSS），有机发光二极管（OLED），第一电容（C1），第一晶体管（T1），第二晶体管（T2））和第三晶体管（T3），其中第一晶体管（T1）被配置为补偿第三晶体管（T3）的阈值电压。根据该驱动方法，通过顺序地将扫描信号施加到扫描线（Sn1，Sn2，Sn3）上的像素电路来驱动像素电路发光。像素电路和用于驱动像素电路的方法可以改善有源矩阵有机发光二极管的响应特性，从而使显示装置能够显示具有均匀图像质量的图像。