(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 806 458 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
04.07.2018 Bulletin 2018/27

(21) Application number: **14169289.7**

(22) Date of filing: **21.05.2014**

(51) Int Cl.:
H01L 27/32 *(2006.01)* ***H01L 27/12*** *(2006.01)*
G09G 3/32 *(2016.01)*

(54) **Organic light-emitting display apparatus and method of repairing the same**

Organische lichtemittierende Anzeigevorrichtung und Verfahren zur Reparatur davon

Appareil d'affichage électroluminescent organique et son procédé de réparation

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **22.05.2013 KR 20130057959**
14.06.2013 KR 20130068638

(43) Date of publication of application:
26.11.2014 Bulletin 2014/48

(73) Proprietor: **Samsung Display Co., Ltd.**
Gyeonggi-do (KR)

(72) Inventors:
- **Cho, Young-Jin**
  Yongin-City, Gyeonggi-Do (KR)
- **Hwang, Young-In**
  Yongin-City, Gyeonggi-Do (KR)
- **Kim, Dong-Gyu**
  Yongin-City, Gyeonggi-Do (KR)

(74) Representative: **Niepelt, Carsten**
Gulde & Partner
Patent- und Rechtsanwaltskanzlei mbB
Wallstraße 58/59
10179 Berlin (DE)

(56) References cited:
EP-A1- 2 535 888
WO-A1-2012/001740
US-A1- 2001 028 429
US-A1- 2005 173 707
US-A1- 2006 017 674
US-A1- 2007 046 186
US-A1- 2007 152 567
US-A1- 2008 062 096
US-A1- 2010 001 941
US-A1- 2011 175 885
US-A1- 2012 113 077
US-A1- 2012 146 999

EP 2 806 458 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND

1. Field

[0001] The present invention relates to an organic light-emitting display apparatus.

2. Description of the Related Art

[0002] Light-emitting display apparatuses are disclosed in US 2007/152567 A1, US 2008/062096 A1, US 2007/046186 A1, EP 2 535 888 A1, WO 2012/001740 A1, US 2005/173707 A1, US 2012/146999 A1, US 2012/113077 A1, US 2006/017674 A1, US 2010/001941 A1 and US 2001/028429 A1. In an organic light-emitting display apparatus, when a pixel is defective, the pixel may emit light all the time or may display black (e.g., may not emit light), regardless of a scan signal and a data signal applied to the pixel. Pixels that emit light all the time, regardless of the scan or data signals, are regarded as bright spots (or hot spots). By contrast, pixels that do not emit light (e.g., displayed in black), regardless of the scan or data signals, is regarded as a dark spot (or a black spot). For example, US 2007/152567 A1 discloses that the light-emitting display apparatus comprises pixels, each of which having a redundant transistor. As a circuit in the pixel becomes more complex, bright spots or dark spots due to circuit defects may not be easily solved or prevented.

SUMMARY

[0003] The present invention provides an organic light-emitting display apparatus according to claim 1.

[0004] The organic light-emitting display apparatus is provided for forming a redundancy pattern in each column of pixels on a panel and normally driving a defective pixel by using the redundancy pattern.

[0005] A method of repairing a defective pixel in an organic light emitting display apparatus mentioned in the following is useful for the understanding of, but not part of the invention as claimed.

[0006] According to an embodiment of the present invention, there is provided An organic light-emitting display apparatus including: an emission device including a plurality of sub-emission devices; an emission pixel circuit configured to supply a driving current to the emission device; a dummy pixel circuit configured to supply the driving current to the emission device; and a repair line coupling the emission device to
the dummy pixel circuit, wherein the emission device is configured to receive the driving current from the emission pixel circuit or the dummy pixel circuit.

[0007] Each of the plurality of sub-emission devices may include: a lower electrode among a plurality of separated lower electrodes; an upper electrode commonly facing the plurality of separated lower electrodes; and an emission layer between the lower electrode and the upper electrode, wherein the plurality of separated lower electrodes are electrically coupled to each other through an electrode connection wiring.

[0008] The electrode connection wiring may include at least one of metal, amorphous silicon, crystalline silicon, and an oxide semiconductor.

[0009] The electrode connection wiring may be at a same layer and of a same material as an active layer of the emission pixel circuit.

[0010] The electrode connection wiring may be integrally formed with the plurality of separated lower electrodes.

[0011] The electrode connection wiring may include: a plurality of first connection units coupled to the plurality of separated lower electrodes; a second connection unit coupled to the emission pixel circuit; and a plurality of cut nodes between the first connection units and the second connection unit, wherein the cut nodes are cut to electrically isolate the plurality of separated lower electrodes from each other.

[0012] The electrode connection wiring may be coupled to the plurality of separated lower electrodes in each of the first connection units through a first contact hole and may be coupled to the emission pixel circuit through a second contact hole in the second connection unit.

[0013] The organic light-emitting display apparatus may further include at least one circuit wiring having one end coupled to the emission pixel circuit and another end coupled to the second connection unit, wherein the at least one circuit wiring may be configured to be cut to electrically isolate the emission pixel circuit from the emission device.

[0014] The organic light-emitting display apparatus may further include a first repair connection wiring having one end coupled to the repair line and another end overlapping with a first short wiring coupled to one of the first connection units; and an insulating layer between the first repair connection wiring and the first short wiring, wherein the first repair connection wiring is configured to be coupled to the first short wiring utilizing a laser beam.

[0015] Each of the first repair connection wiring and the first short wiring may be at a same layer and of a same material as respective conductive layers formed on different layers of the emission pixel circuit.

[0016] The dummy pixel circuit may be on at least one row among first and last rows of each column, or at least one column among first and last columns of each row.

[0017] The emission pixel circuit may be in a display area and the dummy pixel circuit is in a non-display area.

[0018] The emission pixel circuit and the dummy pixel circuit may have a same component structure and/or function.

[0019] The dummy pixel circuit may be coupled to the emission device through a second repair connection wiring having one end coupled to the repair line and another end overlapping with a second short wiring coupled to

the dummy pixel circuit, wherein an insulating layer may be between the second repair connection wiring and the second short wiring.

[0020] The repair line may be coupled to a power voltage line through a power connection wiring and may be configured to be electrically isolated from the power voltage line by cutting the power connection wiring.

[0021] The repair line may be in each column or row.

[0022] The emission pixel circuit may include: a first transistor configured to transfer a data signal in response to a scan signal; a capacitor configured to be charged with a voltage corresponding to the data signal; and a second transistor configured to transfer a driving current corresponding to the voltage charged in the capacitor to the emission device.

[0023] The emission pixel circuit may include: a first transistor configured to receive a data signal from a data line in response to a scan signal; a second transistor configured to transfer a driving current corresponding to the data signal to the emission device; a third transistor configured to diode-connect the second transistor; a first capacitor configured to be charged with a voltage corresponding to the data signal; and a second capacitor connected to one electrode of the first capacitor and a gate electrode of the second transistor.

[0024] The emission pixel circuit may further include: a fourth transistor connected to between the first transistor and the one electrode of the first capacitor; a fifth transistor connected to between the data line and the one electrode of the first capacitor; and a third capacitor having one electrode connected to a node between the first transistor and the fourth transistor and another electrode connected to a gate electrode of the fifth transistor.

[0025] The emission pixel circuit may include: a first transistor configured to receive a data signal from a data line in response to a scan signal; a second transistor configured to transfer a driving current corresponding to the data signal to the emission device; a third transistor configured to diode-connect the second transistor; a fourth transistor connected to between the first transistor and the second transistor; a fifth transistor connected to between the second transistor and the emission device; a sixth transistor connected to between a gate electrode of the second transistor and an initial power; a first capacitor connected to between the gate electrode of the second transistor and a first power source; and a second capacitor having one electrode connected to a node between the first transistor and the fourth transistor and another electrode connected to a second power source.

[0026] The dummy pixel circuit may be configured to supply the driving current to the emission device at a predetermined time.

[0027] The dummy pixel circuit may be configured to supply a same data signal as that supplied by the emission pixel circuit to the emission device.

[0028] The plurality of sub-emission devices may include: a first sub-emission device including a first lower electrode, an upper electrode facing the first lower electrode, and a first emission layer between the first lower electrode and the upper electrode; and a second sub-emission device including a second lower electrode, the upper electrode facing the second lower electrode, and a second emission layer between the second lower electrode and the upper electrode, wherein the first lower electrode and the second lower electrode are coupled to each other through an electrode connection wiring.

[0029] The electrode connection wiring may include: a first connection unit coupled to the first lower electrode; a second connection unit coupled to the second lower electrode; a third connection unit coupled to the emission pixel circuit; a first node between the first connection unit and the third connection unit and configured to be cut to electrically isolate the first sub-emission device from the emission pixel circuit; and a second node between the second connection unit and the third connection unit and configured to be cut to electrically isolate the second sub-emission device from the emission pixel circuit.

[0030] The organic light-emitting display apparatus may further include a first repair connection wiring having one end coupled to the repair line and another end overlapping with a first short wiring coupled to the first connection unit; a first insulating layer between the first repair connection wiring and the first short wiring, wherein the first repair connection wiring is configured to be coupled to the first short wiring utilizing a laser beam; a second repair connection wiring having one end coupled to the repair line and another end overlapping with a second short wiring coupled to the dummy pixel circuit; and a second insulating layer between the second repair connection wiring and the second short wiring, wherein the second repair connection wiring is configured to be coupled to the second short wiring utilizing the laser beam.

[0031] According to another embodiment of the present invention there is provided a method of repairing a defective pixel in an organic light emitting display apparatus, the organic light emitting display apparatus including a plurality of emission pixels including an emission device including a plurality of sub-emission devices, the sub-emission devices being configured to receive a corresponding driving current from one of an emission pixel circuit and a dummy pixel circuit, the method including: connecting the defective pixel to the dummy pixel circuit through a repair line; and after connecting the defective pixel to the dummy pixel circuit, if the defective pixel does not normally emit light, separating the plurality of sub-emission devices.

[0032] The separating of the plurality of sub-emission devices may include: cutting between a connection unit of the emission pixel circuit and a connection unit of each of lower electrodes of the plurality of sub-emission devices in an electrode connection wiring that couples the lower electrodes to each other.

[0033] The method may further include after coupling the defective pixel to the dummy pixel circuit, if the defective pixel normally emits light, separating the emission pixel circuit and the emission device from each other.

[0034] The separating of the emission pixel circuit and the emission device may include: cutting at least one wiring coupled between the emission pixel circuit and the lower electrodes of the emission device.

[0035] The coupling of the defective pixel to the dummy pixel circuit may include: shorting a first short wiring coupled to the emission device and a second short wiring coupled to the dummy pixel circuit by: irradiating a laser beam onto a first repair connection wiring having one end coupled to the repair line and another end overlapping with the first short wiring, wherein a first insulating layer is between the first repair connection wiring and the first short wiring, and irradiating the laser beam onto a second repair connection wiring having one end coupled to the repair line and another end overlapping with the second short wiring with a second insulating layer between the second repair connection wiring and the second short wiring.

The method may further include separating a defective sub-emission device among a plurality of sub-emission devices of the defective pixel from the other sub-emission devices.

The separating of the defective sub-emission device among the plurality of sub-emission devices of the defective pixel from the other sub-emission devices may include: cutting between a connection unit of a lower electrode of the defective sub-emission device and a connection unit of the emission pixel circuit in an electrode connection wiring that couples lower electrodes of the plurality of sub-emission devices to each other.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] The above and other features and aspects of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a block diagram of a display apparatus according to an embodiment of the present invention;
FIGS. 2 through 4 are schematic diagrams of examples of a display panel illustrated in FIG. 1;
FIG. 5 is a diagram for describing a method of repairing a defective pixel by using a plurality of repair lines of the display panel of FIG. 2;
FIGS. 6 and 7 show waveforms of scan signals and data signals provided to the display panel repaired by using the method illustrated in FIG. 5;
FIG. 8 is a diagram for describing a method of repairing a defective pixel by using a plurality of repair lines of the display panel of FIG. 3;
FIGS. 9 and 10 show waveforms of scan signals and data signals provided to the display panel repaired by using the method illustrated in FIG. 8;
FIG. 11 is a diagram for describing a method of repairing a defective pixel by using a plurality of repair lines of the display panel of FIG. 4;
FIGS. 12 and 13 show waveforms of scan signals and data signals provided to the display panel repaired by using the method illustrated in FIG. 11;
FIG. 14 is a schematic diagram of an emission pixel;
FIG. 15 is a plan view of an emission device of the emission pixel of FIG. 14;
FIG. 16 is a cross-sectional view taken along the line A-A' of FIG. 15;
FIG. 17 is a schematic diagram of a dummy pixel according to an embodiment of the present invention;
FIG. 18 is a plan view of a part of the dummy pixel of FIG. 17;
FIG. 19 is a cross-sectional view taken along the line B-B' of FIG. 18;
FIG. 20 is a flowchart for explaining a method of repairing a defective pixel;
FIGS. 21 through 26 are diagrams for explaining a method of repairing a defective pixel in a case of a visible defect of FIG. 20;
FIGS. 27 through 29B are diagrams for explaining a method of repairing a defective pixel in the case of the invisible defect of FIG. 20;
FIGS. 30A through 32 are diagrams for explaining a method of repairing a defective pixel in the case of the invisible defect of FIG. 20;
FIGS. 33 through 36 are circuit diagrams of an emission pixel according to embodiments of the present invention;
FIG. 37 is a schematic diagram of a display panel, according to another embodiment of the present invention;
FIG. 38 is a circuit diagram of an emission pixel according to another embodiment of the present invention;
FIG. 39 is a plan view of an emission pixel including a pixel circuit of FIG. 38;
FIG. 40 is a plan view of a dummy pixel including a pixel circuit of FIG. 38;
FIG. 41 is a plan view of an emission device of an emission pixel according to another embodiment of the present invention;
FIG. 42 is a cross-sectional view taken along a line C-C' of FIG. 41; and
FIG. 43 is a cross-sectional diagram of an organic light emitting display apparatus including an emission pixel, according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0037] Hereinafter, embodiments of the present invention will be described in some detail by explaining embodiments of the invention with reference to the attached drawings. Like reference numerals in the drawings denote like elements. In the following description of the present invention, a detailed description of known functions and configurations incorporated herein will be omitted when it may make the subject matter of the present

invention unclear.

[0038] In the drawings, the thickness of layers and regions are exaggerated for clarity. It will be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present.

[0039] It will be further understood that the terms "comprises" and/or "comprising" when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. Also, the term "on" refers to an upper or lower side of a target and does not always mean an upper side in a direction of gravity.

[0040] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present invention.

[0041] As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. Expressions such as "at least one of," when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list.

[0042] FIG. 1 is a block diagram of a display apparatus 100 according to an embodiment of the present invention.

[0043] Referring to FIG. 1, the display apparatus 100 includes a display panel 10 including a plurality of pixels, a scan driving unit 20, a data driving unit 30, and a control unit 40. The scan driving unit 20, the data driving unit 30, and the control unit 40 may be separately formed on different semiconductor chips, or may be integrated on a single semiconductor chip. Also, the scan driving unit 20 may be formed on the same substrate as the display panel 10.

[0044] A plurality of scan lines SL extending in a horizontal direction and a plurality of the data lines DL extending in a vertical direction and perpendicularly crossing the scan lines SL are formed on the display panel 10. Also, a plurality of repair lines RL extending almost parallel or substantially parallel with and spaced apart from the data lines DL and perpendicularly crossing the scan lines SL are formed on the display panel 10. A plurality of pixels P aligned in a matrix-like shape are formed where the scan lines SL, the data lines DL, and the repair lines RL cross each other.

[0045] Although the data line DL is formed at a right side of the pixel P and the repair line RL is formed at a left side of the pixel P in FIG. 1, the present invention is not limited thereto. For example, the positions of the data line DL and the repair line RL may be switched according to the design and function of the display panel 10. One or more repair lines RL may be formed in each pixel column. The one or more repair lines RL may be formed or arranged in parallel to the scan lines SL according to a pixel design so that the one or more repair lines RL may be formed or arranged in each pixel row. Although not shown in FIG. 1, additional signal or voltage lines such as a plurality of emission control lines for providing an emission control signal, an initialization voltage line for providing an initialization voltage, and a driving voltage line for providing a power voltage may be additionally formed or arranged on the display panel 10.

[0046] The scan driving unit 20 may generate and sequentially provide scan signals via the scan lines SL to the display panel 10.

[0047] The data driving unit 30 may sequentially provide data signals via the data lines DL to the display panel 10. The data driving unit 30 transforms input image data DATA, input from the control unit 40 and having a gray-scale (e.g., grey levels), into a voltage or current data signal.

[0048] The control unit 40 generates and transmits a scan control signal SCS and a data control signal DCS respectively to the scan driving unit 20 and the data driving unit 30. As such, the scan driving unit 20 sequentially provides or activates scan signals to the scan lines SL, and the data driving unit 30 provides data signals to the pixels P. Additional voltage or control signals such as a first power voltage ELVDD, a second power voltage ELVSS, an emission control signal EM, and an initialization voltage Vint may be provided to the pixels P under the control of the control unit 40. The control unit 40 may control a time when the scan driving unit 20 provides a scan signal to a dummy pixel and may control the data driving unit 30 to provide a data signal that is the same as the data signal provided or to be provided to a defective signal, to the dummy pixel when the scan signal is provided to the dummy pixel.

[0049] FIGS. 2 through 4 are schematic diagrams of examples of the display panel 10 illustrated in FIG. 1.

[0050] Referring to FIGS. 2 through 4, a plurality of pixels P aligned in a matrix-like shape are formed where a plurality of scan lines SL, a plurality of data lines DL, and a plurality of repair lines RL cross each other, on a display panel 10a, 10b, or 10c. The pixels P include emission pixels EP formed on a display area AA and dummy pixels DP formed on a non-display area NA. The non-display area NA may be formed on at least one of top and bottom regions or left and right regions of the display area AA. As such, one or more dummy pixels DP may be formed in each pixel column on at least one of top and bottom regions of the pixel column, or one or more dummy pixels DP may be formed in each pixel row on at least one of left and right regions of the pixel row. An example of forming the dummy pixels DP in the pixel column of the non-display area NA on the top and bottom regions of the display area AA is explained with respect to FIGS. 2 through 4. This may apply to a case where the dummy pixels DP are formed in the pixel row of the non-display area NA on the left and right regions of the display area

AA.

[0051] Referring to FIG. 2, the display panel 10a includes a display area AA and a non-display area NA formed below the display area AA. From among first through (n+1)th scan lines SL1 through SLn+1, the first through nth scan lines SL1 through SLn are formed on the display area AA, and the (n+1)th scan line SLn+1 is formed on the non-display area NA. First through mth data lines DL1 through DLm and first through mth repair lines RL1 through RLm are formed separately in pixel columns in the display area AA and extending into the non-display area NA. A plurality of emission pixels EP coupled to the first through nth scan lines SL1 through SLn and the first through mth data lines DL1 through DLm are formed in the display area AA, and a plurality of dummy pixels DP coupled to the (n+1)th scan line SLn+1 and the first through mth data lines DL1 through DLm are formed in the non-display area NA.

[0052] Referring to FIG. 3, the display panel 10b includes a display area AA and a non-display area NA above the display area AA. From among zeroth through nth scan lines SL0 through SLn, the first through nth scan lines SL1 through SLn are formed on the display area AA, and the zeroth scan line SL0 is formed on the non-display area NA. First through mth data lines DL1 through DLm and first through mth repair lines RL1 through RLm are formed separately in pixel columns in the display area AA and extending into the non-display area NA. A plurality of emission pixels EP coupled to the first through nth scan lines SL1 through SLn and the first through mth data lines DL1 through DLm are formed in the display area AA, and a plurality of dummy pixels DP coupled to the zeroth scan line SL0 and the first through mth data lines DL1 through DLm are formed in the non-display area NA.

[0053] Referring to FIG. 4, the display panel 10c includes a display area AA and a non-display area NA formed above and below the display area AA. From among zeroth through (n+1)th scan lines SL0 through SLn+1, the first through nth scan lines SL1 through SLn are formed on the display area AA, and the zeroth and (n+1)th scan lines SL0 and SLn+1 are formed on the non-display area NA. First through mth data lines DL1 through DLm and first through mth repair lines RL1 through RLm are formed separately in pixel columns on the display area AA and the non-display area NA. A plurality of emission pixels EP coupled to the first through nth scan lines SL1 through SLn and the first through mth data lines DL1 through DLm are formed on the display area AA, and a plurality of dummy pixels DP coupled to the zeroth and (n+1)th scan lines SL0 and SLn+1 and the first through mth data lines DL1 through DLm are formed on the non-display area NA.

FIG. 5 is a diagram for describing a method of repairing a defective pixel by using repair lines of the display panel 10a of FIG. 2.

Referring to FIG. 5, the emission pixels EP formed in the display area AA may include pixel circuits PC that are coupled to the first through nth scan lines SL1 through SLn and the first through mth data lines DL1 through DLm, and emission devices E that emit light by receiving a driving current from the pixel circuits PC. The dummy pixels DP formed in the non-display area NA may include only the pixel circuits PC that are coupled to the (n+1)th scan line SLn+1 and the first through mth data lines DL1 through DLm.

When an emission pixel EPi coupled to an ith scan line SLi of a first column is defective, the emission device E of the defective emission pixel EPi is disconnected from the corresponding pixel circuit PC, and the disconnected emission device E is coupled to the pixel circuit PC of the dummy pixel DP that is coupled to the (n+1)th scan line SLn+1 through the repair line RL. The disconnection of the emission device E and the corresponding pixel circuit PC, the coupling of the repair line RL and the emission device E, and the coupling of the repair line RL and the dummy pixel DP may be performed by cutting or shorting by irradiating a laser beam from a substrate side or from an opposite side of a substrate.

FIGS. 6 and 7 show waveforms of scan signals and data signals provided to the display panel repaired by using the method illustrated in FIG. 5.

Referring to FIG. 6, the scan driving unit 20 sequentially provides or activates the first through nth scan signals S1 through Sn to first through nth scan line SL1 through SLn and provides the (n+1)th scan signal Sn+1 to the (n+1)th scan line SLn+1 at the same time as the scan signal Si is provided to the repaired emission pixel EPi.

The data driving unit 30 sequentially provides or activates the first through nth data signals D1 through Dn to the data line DL1 in synchronization with the first through (n+1)th scan signals S1 through Sn+1. In this regard, a data signal Di that is the same as the data signal Di provided to the defective emission pixel EPi is concurrently provided to the dummy pixel DP. Accordingly, the emission device E of the defective emission pixel EPi may receive a current corresponding to the data signal Di via the pixel circuits PC of the dummy pixels DP and the repair lines RL1, thereby suppressing or reducing generation of a bright spot or a dark spot of the defective emission pixel EPi.

Referring to FIG. 7, the scan driving unit 20 sequentially provides or activates the first through (n+1)th scan signals S1 through Sn+1 to the first through (n+1)th scan lines SL1 through SLn+1.

The data driving unit 30 sequentially provides or activates the first through nth data signals D1 through Dn to the data line DL1 in synchronization with the first through (n+1)th scan signals S1 through Sn+1. In this regard, a data signal Di that is the same as the data signal Di provided to the defective emission pixel EPi is again provided to the dummy pixel DP. Accordingly, the emission device E of the defective emission pixel EPi may receive a current corresponding to the data signal Di via the pixel circuits PC of the dummy pixels DP and the repair lines RL1, thereby suppressing or reducing generation of a

bright spot or a dark spot of the defective emission pixel EPi.

Although a width of the first through (n+1)th scan signals S1 through Sn+1 may be provided as one horizontal period (1H) in FIGS. 6 and 7, a width of a scan signal may be provided as two horizontal periods (2H), and widths of adjacent scan signals, for example, widths of the (n-1)th scan signal Sn-1 and the nth scan signal Sn, may be provided to overlap by 1H or less. Accordingly, a lack of charges due to a resistive-capacitive (RC) delay of signal lines caused by a large-sized display area may be solved or reduced.

FIG. 8 is a diagram for describing a method of repairing a defective pixel by using the repair lines of the display panel 10b of FIG. 3.

Referring to FIG. 8, the emission pixels EP formed in the display area AA may include the pixel circuits PC and the emission devices E that emit light by receiving a driving current from the pixel circuits PC. The dummy pixels DP formed in the non-display area NA may include only the pixel circuits PC.

When the emission pixel EPi coupled to the ith scan line SLi of a first column is defective, the emission device E of the defective emission pixel EPi is disconnected from the pixel circuit PC, and the disconnected emission device E is coupled to the pixel circuit PC of the dummy pixel DP that is coupled to the zeroth scan line SL0 through the repair line RL1. The disconnection of the emission device E and the pixel circuit PC, the coupling of the repair line RL and the emission device E, and the coupling of the repair line RL and the dummy pixel DP may be performed by cutting or shorting by irradiating a laser beam from a substrate side or from an opposite side of a substrate. FIGS. 9 and 10 show waveforms of scan signals and data signals provided to the display panel 10b repaired by using the method illustrated in FIG. 8.

Referring to FIG. 9, the scan driving unit 20 sequentially provides or activates the first through nth scan signals S1 through Sn to the first through nth scan line SL1 through SLn and provides the zeroth scan signal S0 to the zeroth scan line S0 at the same time as the scan signal Si is provided to the repaired emission pixel EPi.

The data driving unit 30 sequentially provides or activates the first through nth data signals D1 through Dn to the data line DL1 in synchronization with the zeroth through nth scan signals S0 through Sn. In this regard, the data signal Di that is the same as the data signal Di provided to the defective emission pixel EPi is concurrently provided to the dummy pixel DP. Accordingly, the emission device E of the defective emission pixel EPi may receive a current corresponding to the data signal Di via the pixel circuits PC of the dummy pixels DP and the repair lines RL1, thereby suppressing or reducing generation of a bright spot or a dark spot of the defective emission pixel EPi.

Referring to FIG. 10, the scan driving unit 20 sequentially provides or activates the zeroth through nth scan signals S0 through Sn to the zeroth through nth scan lines SL0 through SLn.

The data driving unit 30 sequentially provides or activates the first through nth data signals D1 through Dn to the data line DL1 in synchronization with the zeroth through nth scan signals S0 through Sn. In this regard, the data signal Di that is the same as the data signal Di that is to be provided to the defective emission pixel EPi is first provided to the dummy pixel DP. Accordingly, the emission device E of the defective emission pixel EPi may receive a current corresponding to the data signal Di via the pixel circuits PC of the dummy pixels DP and the repair lines RL1, thereby suppressing or reducing generation of a bright spot or a dark spot of the defective emission pixel EPi.

Although a width of the zeroth through nth scan signals S0 through Sn may be provided as one horizontal period (1H) in FIGS. 9 and 10, a width of a scan signal may be provided as two horizontal periods (2H), and widths of adjacent scan signals, for example, widths of the (n-1)th scan signal Sn-1 and the nth scan signal Sn, may be provided to overlap by 1H or less. Accordingly, a lack of charges due to a RC delay of signal lines caused by a large-sized display area may be solved or reduced.

FIG. 11 is a diagram for describing a method of repairing a defective pixel by using repair lines of the display panel 10c of FIG. 4.

Referring to FIG. 11, the emission pixels EP formed in the display area AA may include the pixel circuits PC and the emission devices E that emit light by receiving a driving current from the pixel circuits PC. The dummy pixels DP formed in the non-display area NA may include only the pixel circuits PC.

When the emission pixel EPi coupled to the ith scan line SLi of a first column and an emission pixel EPp coupled to a pth scan line SLp of the first column are defective, the repair line RL1 between the defective emission pixels EPi and EPp is disconnected, the emission devices E of the defective emission pixels EPi and EPp are disconnected from the pixel circuits PC, and the disconnected emission devices E are coupled to the pixel circuits PC of a first dummy pixel DP1 and a second dummy pixle DP2 that are respectively coupled to the zeroth scan line SL0 and the (n+1)th scan line SLn+1 through the repair lines RL1. The disconnection of the emission devices E and the pixel circuits PC, the coupling of the repair lines RL and the emission devices E, and the coupling of the repair lines RL and the dummy pixels DP may be performed by cutting or shorting by irradiating a laser beam from a substrate side or from an opposite side of a substrate.

FIGS. 12 and 13 show waveforms of the scan signals and the data signals provided to the display panel 10c repaired by using the method illustrated in FIG. 11.

Referring to FIG. 12, the scan driving unit 20 sequentially provides or activates the first through nth scan signals S1 through Sn to the first through nth scan line SL1 through SLn and respectively provides the zeroth and

(n+1)th scan signals S0 and Sn+1 to the zeroth and (n+1)th scan line SL0 and SLn+1 at the same time as the scan signals Si and Sp are respectively provided to the repaired emission pixels EPi and EPp.

The data driving unit 30 sequentially provides or activates the first through nth data signals D1 through Dn to the data line DL1 in synchronization with the zeroth through (n+1)th scan signals S0 through Sn+1. In this regard, the data signals Di and Dp that are the same as the data signals Di and Dp provided to the defective emission pixels EPi and EPp are concurrently provided to the first and second dummy pixels DP1 and DP2. Accordingly, the emission devices E of the defective emission pixels EPi and EPp may receive current corresponding to the data signals Di and Dp via the pixel circuits PC of the first and second dummy pixels DP1 and DP2 and the repair lines RL1, thereby suppressing or reducing generation of a bright spot or a dark spot of the defective emission pixels EPi and EPp.

[0054] Referring to FIG. 13, the scan driving unit 20 sequentially provides or activates the zeroth through (n+1)th scan signals S0 through Sn+1 to the zeroth through (n+1)th scan line SL0 through SLn+1.

[0055] The data driving unit 30 sequentially provides or activates the first through nth data signals D1 through Dn to the data line DL1 in synchronization with the zeroth through (n+1)th scan signals S0 through Sn+1. In this regard, the data signal Di that is the same as the data signal Di that is to be provided to the defective emission pixel EPi is first provided to the first dummy pixel DP1. The data signal Dp that is the same as the data signal Dp provided to the defective emission pixel EPp is again provided to the second dummy pixel DP2. Accordingly, the emission devices E of the defective emission pixels EPi and EPp may receive current corresponding to the data signals Di and Dp via the pixel circuits PC of the first and second dummy pixels DP1 and DP2 and the repair lines RL1, thereby suppressing or reducing generation of a bright spot or a dark spot of the defective emission pixels EPi and EPp.

[0056] Although a width of the zeroth through (n+1)th scan signals S0 through Sn+1 may be provided as one horizontal period (1H) in FIGS. 12 and 13, a width of a scan signal may be provided as two horizontal periods (2H), and widths of adjacent scan signals (for example, widths of the (n-1)th scan signal Sn-1 and the nth scan signal Sn) may be provided to overlap by 1H or less. Accordingly, a lack of charges due to a RC delay of signal lines caused by a large-sized display area may be solved. FIG. 14 is a schematic diagram of the emission pixel EP. FIG. 15 is a plan view of an emission device of the emission pixel EP of FIG. 14. FIG. 16 is a cross-sectional view taken along a line A-A' of FIG. 15.

Referring to FIG. 14, the emission pixel EP that is coupled to the scan line SL and the data line DL may include the pixel circuit PC and the emission device E that emits light by receiving a driving current from the pixel circuit PC. The pixel circuit PC may include at least one thin film transistor (TFT) and at least one capacitor. The emission device E may be an organic light emitting diode (OLED) including an anode, a cathode, and an emission layer formed or located between the anode and the cathode. The anode of the emission device E may be split or separated (e.g., physically separated by a gap or space) into at least two anodes so that the emission device E may include at least two sub-emission devices SE1 and SE2. Referring to FIGS. 15 and 16, the first sub-emission device SE1 includes a first anode AD1, an organic layer OL including an emission layer, and a cathode (not shown). The second sub-emission device SE2 includes a second anode AD2, the organic layer OL including the emission layer, and a cathode. The organic layer OL may be separately or commonly formed in the first and second sub-emission devices SE1 and SE2. The cathode may be commonly formed in the first and second sub-emission devices SE1 and SE2, and may be formed on an entire surface of a substrate 101 so that the cathode may be commonly formed in the first anode AD1 and the second anode AD2 to face each other.

An electrode connection wiring 11 is formed on the substrate 101 and a buffer layer 102. The electrode connection wiring 11 may be formed of a conductive material. For example, the electrode connection wiring 11 may be formed of amorphous silicon, crystalline silicon, or an oxide semiconductor. In this case, the electrode connection wiring 11 may be formed on the same layer and of the same material as an active layer included in the TFT of the pixel circuit PC. The electrode connection wiring 11 may be formed of metal. In this case, the electrode connection wiring 11 may have a single layer structure including metal, semitransparent metal, or a transparent conductive oxide or a three layer structure including the semitransparent metal and the transparent conductive oxide formed on top and bottom portions of the semitransparent metal and protecting the semitransparent metal. The semitransparent metal may include silver (Ag) or a silver alloy. The transparent conductive oxide may include at least one selected from the group consisting of indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium oxide (In_2O_3), indium gallium oxide (IGO), and aluminum zinc oxide (AZO). A first insulating film 103 is formed on the electrode connection wiring 11. A repair connection wiring 13 is formed on the first insulating film 103.

[0057] The repair connection wiring 13 may be formed on the same layer and of the same material as a conductive electrode included in the TFT of the pixel circuit PC, for example, a gate electrode. A second insulating layer 104 is formed on the repair connection wiring 13. In a first connection unit CU1, a first contact metal CM1 and a second contact metal CM2 formed on the second insulating layer 104 are coupled to the electrode connection wiring 11 through contact holes. A circuit connection wiring 12, that is coupled to a circuit wiring 15 coupled to the pixel circuit PC, is coupled to the electrode connection wiring 11 through a contact hole, in a second

connection unit CU2. The circuit wiring 15, along with the active layer included in the TFT of the pixel circuit PC, may be formed of amorphous silicon, crystalline silicon, or an oxide semiconductor or may be formed on the same layer and of the same material as a source electrode and a drain electrode that are included in the TFT. The circuit connection wiring 12 is coupled to the electrode connection wiring 11 between the first connection units CU1 so that a first cut node CN1 and a second cut node CN2 are formed in the electrode connection wiring 11. A short wiring 14 extending from the first contact metal CM1 overlaps with a part of the repair connection wiring 13 in a first short node SN1 and is provisionally coupled to the repair connection wiring 13. The repair line RL is coupled to the repair connection wiring 13 through a contact hole. The repair line RL, the circuit connection wiring 12, the first and second contact metals CM1 and CM2, and the short wiring 14 may be formed on the same layer and of the same material as a conductive electrode included in the TFT of the pixel circuit PC, for example, the source electrode and the drain electrode. A third insulating layer 105 is formed on the repair line RL, the first and second contact metals CM1 and CM2, and the short wiring 14. The first anode AD1 and the second anode AD2 are formed on the third insulating layer 105.

[0058] A first protrusion unit AD1' extending from the first anode AD1 is coupled to the electrode connection wiring 11 through the first contact meal CM1 in the first connection unit CU1. A second protrusion unit AD2' extending from the second anode AD2 is coupled to the electrode connection wiring 11 through the second contact meal CM2 in the first connection unit CU1. Accordingly, the first anode AD1 and the second anode AD2 are electrically coupled to each other by the electrode connection wiring 11. A fourth insulating layer 106 that covers edges of the first anode AD1 and the second anode AD2 is formed on the first anode AD1 and the second anode AD2.

[0059] FIG. 17 is a schematic diagram of the dummy pixel DP according to an embodiment of the present invention. FIG. 18 is a plan view of a part of the dummy pixel DP of FIG. 17. FIG. 19 is a cross-sectional view taken along a line B-B' of FIG. 18.

[0060] Referring to FIG. 17, the dummy pixel DP that is coupled to the zeroth scan line SL0 and/or the (n+1)th scan line SLn+1 and the data line DL may include only the pixel circuit PC. The pixel circuit PC of the dummy pixel DP may be the same (e.g., the same design, structure, and/or function) as the pixel circuit PC of the emission pixel EP.

[0061] Referring to FIGS. 18 and 19, a power connection wiring 18 is formed on the substrate 101 and the buffer layer 102. The power connection wiring 18 may be formed of amorphous silicon, crystalline silicon, or an oxide semiconductor. The power connection wiring 18 may be formed on the same layer and of the same material as an active layer included in the TFT of the pixel circuit PC. The first insulating layer 103 is formed on the power connection wiring 18. A repair connection wiring 16 is formed on the first insulating layer 103.

The repair connection wiring 16 may be formed on the same layer and of the same material as a conductive electrode included in a TFT of the pixel circuit PC, for example, a gate electrode. The second insulating layer 104 is formed on the repair connection wiring 16. On the second insulating layer 104, a short wiring 17 coupled to the pixel circuit PC overlaps with a part of the repair connection wiring 16 in the first short node SN2 and is provisionally coupled to the repair connection wiring 16. The repair line RL is coupled to the repair connection wiring 16 through a contact hole. The repair line RL and a power voltage line ELVDDL in a boundary of the display panel 10 are coupled to the power connection wiring 18 so that the repair line RL and the power voltage line ELVDDL are electrically coupled to each other. When the repair line RL is used to repair the emission pixel EP, the power voltage line ELVDDL is disconnected from the repair line RL by cutting the power connection wiring 18.

The repair line RL, the short wiring 17, and the power voltage line ELVDDL may be formed on the same layer and of the same material as a conductive electrode included in the TFT of the pixel circuit PC, for example, a source electrode and a drain electrode. The third insulating layer 105 and the fourth insulating layer 106 are sequentially formed on the repair line RL, the short wiring 17, and the power voltage line ELVDDL. FIG. 20 is a flowchart for explaining a method of repairing a defective pixel.

Referring to FIG. 20, after the display panel 10 is manufactured, the defective pixel of the display area AA is detected through a panel test performed on the display panel 10 (operation S21). The panel test may include, for example, a lighting test, an aging test, etc. The defective pixel is an emission pixel recognized as a bright spot or a dark spot.

The bright spot or the dark spot may be generated due to a defective pixel circuit or a defective emission device. When an anode and a cathode of an emission device are shorted due to a defect present therebetween, and when a value of a resistance Rdef formed in parallel with the anode and the cathode is small, a driving current generated in the pixel circuit PC flows from the anode to the cathode through the resistance Rdef, and thus a voltage of the anode is not sufficiently higher than a turn-on voltage of the emission device, which causes the dark spot in which the emission device does not emit light.

A pixel that is visibly recognized as a bright spot or a dark spot of the display panel 10 may be detected through an optical microscope of a lighting inspection apparatus.

In a case of a visible defect in which a sub-emission device that is the bright spot or the dark spot is visibly recognized among a plurality of sub-emission devices, the sub-emission device having the defect of the bright spot or the dark spot is separated or electrically isolated from the pixel circuit PC (operation S22).

In a case of an invisible defect in which a defective sub-

emission device is not visibly recognized among a plurality of sub-emission devices, an emission device of the defective pixel is coupled to the repair line RL and the pixel circuit PC of the dummy pixel DP is coupled to the repair line RL so that the defective pixel is coupled to the dummy pixel DP (operation S23). It is determined whether the defective pixel normally emits light (operation S24). When the defective pixel normally emits light by the coupling of the defective pixel and the dummy pixel DP, the defective pixel is determined to have resulted from the defective pixel circuit. Thus, in order to completely insulate the defective pixel circuit from the emission device, the pixel circuit PC of the defective pixel may be selectively separated or electrically isolated from the emission device (operation S25). Operation S25 may be selectively performed.

When the defective pixel does not normally emit light by the coupling of the defective pixel and the dummy pixel DP, the defective pixel is determined to have resulted from the short defect of the emission device, and the sub-emission devices are disconnected from each other (operation S26).

FIGS. 21 through 26 are diagrams for explaining a method of repairing a defective pixel (operation S22) in a case of a visible defect of FIG. 20.

The repairing method of FIGS. 21 through 26 describes an example of the dummy pixel DP coupled to the (n+1)th scan line SLn+1 among the first through (n+1)th scan lines SL1 through SLn+1 like the display panel 10a of FIG. 2. This may apply to the display panels 10b and 10c of FIGS. 3 and 4.

Referring to FIGS. 21 through 23, when the first sub-emission device SE1 of the defective emission pixel EPi is visibly recognized to have a short defect, the first sub-emission device SE1 is disconnected from the second sub-emission device SE2. In this regard, the first cut node CN1 of the electrode connection wiring 11 is cut by irradiating a laser beam. Accordingly, the first sub-emission device SE1 becomes a dark spot and a driving current flows from an emission pixel circuit PCi to the second sub-emission device SE2 so that the second sub-emission device SE2 may emit light without any perceivable brightness reduction.

Referring to FIGS. 24 through 26, when the second sub-emission device SE2 of the defective emission pixel EPi is visibly recognized to have a short defect, the second sub-emission device SE2 is disconnected from the first sub-emission device SE1. In this regard, the second cut node CN2 of the electrode connection wiring 11 is cut by irradiating the laser beam. Accordingly, the second sub-emission device SE2 becomes the dark spot, and the driving current flows from the emission pixel circuit PCi to the first sub-emission device SE1 so that the first sub-emission device SE1 may emit light without any perceivable brightness reduction.

In the embodiments described with reference to FIGS. 21 through 26, the emission pixel EPi has a short defect, and the emission pixel circuit PCi is normal, and thus the emission pixel EPi is not necessarily coupled to the dummy pixel DP through the repair line RL.

FIGS. 27 through 29B are diagrams for explaining a method of repairing a defective pixel (operations S23 and S25) in the case of an invisible defect of FIG. 20.

The repairing method of FIGS. 27 through 29B describes an example of the dummy pixel DP coupled to the (n+1)th scan line SLn+1 among the first through (n+1)th scan lines SL1 through SLn+1 like the display panel 10a of FIG. 2. This may apply to the display panels 10b and 10c of FIGS. 3 and 4.

Referring to FIGS. 27 through 29B, although the emission pixel EPi coupled to the ith scan line SLi is determined to be defective, when it is not determined whether the defective emission pixel EPi has resulted from a defective pixel circuit or a defective emission device, the provisionally coupled repair connection wiring 13 and the short wiring 14 are shorted by irradiating a laser beam onto the first short node SN1, and then the provisionally coupled repair connection wiring 16 and the short wiring 17 are shorted by irradiating the laser beam onto the second short node SN2, and thus the emission pixel EPi and the dummy pixel DP are electrically coupled to each other (operation S23). The power voltage line ELVDDL and the repair line RL are disconnected from each other by irradiating the laser beam onto the power connection wiring 18.

After the coupling of the repair line RL and the dummy pixel DP and defective emission pixel EPi, when the first sub-emission device SE1 and the second sub-emission device SE2 normally emit light, because the defective emission pixel EPi is determined to have resulted from the defective emission pixel circuit PCi, to completely insulate the defective emission pixel circuit PCi from the defective emission pixel EPi, the circuit connection wiring 12 and the circuit wiring 15 are separated or electrically isolated from each other by cutting the circuit wiring 15 by irradiating the laser beam onto the circuit wiring 15, and thus the emission pixel circuit PCi is separated or electrically isolated from the emission pixel EPi (operation S25).

Accordingly, a driving current flows from a dummy pixel circuit PCn+1 to the first sub-emission device SE1 and the second sub-emission device SE so that the emission pixel EPi may emit light without any perceivable brightness reduction.

FIGS. 30A through 32 are diagrams for explaining a method of repairing a defective pixel (operations S23 and S26) in the case of the invisible defect of FIG. 20.

The repairing method of FIGS. 30A through 32 describes an example of the dummy pixel DP coupled to the (n+1)th scan line SLn+1 among the first through(n+1)th scan lines SL1 through SLn+1 like the display panel 10a of FIG. 2. This may apply to the display panels 10b and 10c of FIGS. 3 and 4.

Referring to FIGS. 28B and 30A through 32, although the emission pixel EPi coupled to the ith scan line SLi is determined to be defective, when it is not determined

whether the defective emission pixel EPi has resulted from a defective pixel circuit or a defective emission device, the provisionally coupled repair connection wiring 13 and the short wiring 14 are shorted by irradiating a laser beam onto the first short node SN1, and the provisionally coupled repair connection wiring 16 and the short wiring 17 are shorted by irradiating the laser beam onto the second short node SN2, and thus the emission pixel EPi and the dummy pixel DP are electrically coupled to each other (operation S23). The power voltage line ELVDDL and the repair line RL are disconnected from each other by irradiating the laser beam onto the power connection wiring 18.

[0062] After the coupling of the repair line RL, the dummy pixel DP, and the emission pixel EPi, when the first sub-emission device SE1 and the second sub-emission device SE2 do not normally emit light, because the defective emission pixel EPi is determined to have resulted from the defective emission device E, the first cut node CN1 of the electrode connection wiring 11 is cut by irradiating the laser beam onto the electrode connection wiring 11 (operation S26). Thus, the first sub-emission device SE1 and the second sub-emission device SE2 are separated or electrically isolated from each other, the first sub-emission device SE1 receives a driving current from the dummy pixel circuit PCn+1, and the second sub-emission device SE2 receives a driving current from the emission pixel circuit PCi.

[0063] If the defective emission pixel EPi is determined to have resulted from a short defect of the first sub-emission device SE1, as shown in FIG. 30A, the first sub-emission device SE1 becomes a dark spot, and the second sub-emission device SE2 may emit light by the driving current from the emission pixel circuit PCi without any perceivable brightness reduction.

[0064] If the defective emission pixel EPi is determined to have resulted from a short defect of the second sub-emission device SE2, as shown in FIG. 30B, the second sub-emission device SE2 becomes the dark spot, and the first sub-emission device SE1 may emit light by the driving current from the dummy pixel circuit PCn+1 without any perceivable brightness reduction.

[0065] FIG. 33 is a circuit diagram of an emission pixel EP1 according to an embodiment of the present invention.

[0066] Referring to FIG. 33, the emission pixel EP1 includes the emission device E and a pixel circuit 2A for supplying a current to the emission device E. The dummy pixel DP includes the pixel circuit 2A excluding the emission device E. The emission device E includes an anode, a cathode, and an emission layer formed or located between the anode and the cathode, and may be an OLED having a structure in which the anode is split or separated into a plurality of anodes. The emission device E may include first through nth OLEDs OLED1 through OLEDn that are coupled in parallel to each other by the plurality of anodes resulting from the splitting of the anode. Accordingly, a driving current of the pixel circuit 2A is separately provided to the first through nth OLEDs OLED1 through OLEDn. If a defective OLED is separated or electrically isolated from the corresponding pixel circuit, because the driving current is separately provided to the other OLEDs, the OLEDs may emit light without any perceivable brightness loss. The circuit connection wiring 12 coupled to the emission device E is disconnected from the circuit wiring 15 coupled to the pixel circuit 2A by cutting the circuit wiring 15, and thus the pixel circuit 2A and the emission device E may be separated or electrically isolated from each other.

[0067] The pixel circuit 2A may include first through fourth transistors TA1 through TA4, and first and second capacitors C1 and C2.

[0068] A gate electrode of the first transistor TA1 receives a scan signal S from a scan line. A first electrode of the first transistor TA1 receives a data signal D from a data line. A second electrode of the first transistor TA1 is coupled to a first node N1.

[0069] A gate electrode of the second transistor TA2 is coupled to a second node N2. A first electrode of the second transistor TA2 receives a first power voltage ELVDD from a first power source. A second electrode of the second transistor TA2 is coupled to the anode of the OLED. The second transistor TA2 functions as a driving transistor.

[0070] The first capacitor C1 is coupled between the first node N1, and the second electrode of the second transistor TA2 and the first power source. The second capacitor C2 is coupled between the first node N1 and the second node N2.

[0071] A gate electrode of the third transistor TA3 receives a first control signal GC. A first electrode of the third transistor TA3 is coupled to the gate electrode of the second transistor TA2. A second electrode of the third transistor TA3 is coupled to the anode of the OLED and the second electrode of the second transistor TA2.

[0072] A gate electrode of the fourth transistor TA4 receives a second control signal SUS_ENB. A first electrode of the fourth transistor TA4 receives an auxiliary voltage Vsus. A second electrode of the fourth transistor TA4 is coupled to the data line and receives the data signal D.

[0073] In an initialization period, the scan signal S having a low level is provided to the scan line, and a second control signal SUS_ENB having a low level is provided to the gate electrode of the fourth transistor TA4. In this case, the data line is in a high impedance (Hi-Z) state. As such, the first transistor TA1 and the fourth transistor TA4 are turned on and thus the auxiliary voltage Vsus having a high level is provided to the first node N1, a voltage of the second node N2 is reduced, and the second node N2 is maintained at an initialization voltage (e.g., a predetermined initialization voltage).

[0074] In a compensation period, the auxiliary voltage Vsus having a high level is provided to the first node N1 through the data line. The first control signal GC is provided at a low level and thus the third transistor TA3 is

turned on. As such, the second transistor TA2 is diode-connected and thus a current flows until a voltage corresponding to a threshold voltage of the second transistor TA2 is stored in the second capacitor C2. After that, the second transistor TA2 is turned off.

[0075] In a scan/data input period, the scan signal S having a low level is provided to the scan line and thus the first transistor TA1 is turned on, and the data signal D is provided through the data line. As such, a voltage difference between the driving voltage ELVDD and a voltage of the first node N1 is stored in the first capacitor C1.

[0076] In an emission period, the first power voltage ELVDD is provided at a high level, and the second power voltage ELVSS is provided at a low level. A current path from the first power voltage ELVDD to the cathode of the OLED is formed via the second transistor TA2, and the emission devices E of all the emission pixels EP1 emit light at a brightness corresponding to the data signal.

[0077] FIG. 34 is a circuit diagram of an emission pixel EP2 according to another embodiment of the present invention.

[0078] Referring to FIG. 34, the emission pixel EP2 includes the emission device E and a pixel circuit 2B for supplying a current to the emission device E. The dummy pixel DP includes the pixel circuit 2B excluding the emission device E. The emission device E includes an anode, a cathode, and an emission layer formed or located between the anode and the cathode, and may be an OLED having a structure in which the anode is split or physically separated into a plurality of anodes having a gap or space between the separated anodes. The emission device E may include the first through nth OLEDs OLED1 through OLEDn that are coupled in parallel to each other through the plurality of anodes resulting from the splitting of the anode. Accordingly, a driving current of the pixel circuit 2B is separately provided to the first through nth OLEDs OLED1 through OLEDn. If a defective OLED is separated or electrically isolated, because the driving current is separately provided to the other OLEDs, the OLEDs may emit light without any perceivable brightness loss. The circuit connection wiring 12 coupled to the emission device E is disconnected from the circuit wiring 15 coupled to the pixel circuit 2B by cutting the circuit wiring 15, and thus the pixel circuit 2B and the emission device E may be separated or electrically isolated from each other.

[0079] The pixel circuit 2B includes first through fifth transistors TB1 through TB5, and first through third capacitors C1 through C3.

[0080] A gate electrode of the first transistor TB1 receives the scan signal S from a scan line. A first electrode of the first transistor TB1 is coupled to a data line and receives the data signal D from the data line. A second electrode of the first transistor TB1 is coupled to the first node N1.

[0081] A gate electrode of the second transistor TB2 receives a first control signal GW. A first electrode of the second transistor TB2 is coupled to the first node N1. A second electrode of the second transistor TB2 is coupled to the second node N2.

[0082] A gate electrode of the third transistor TB3 is coupled to a third node N3. A first electrode of the third transistor TB3 receives a first power voltage ELVDD from a first power source. A second electrode of the third transistor TB3 is coupled to the anode of the OLED. The third transistor TB3 functions as a driving transistor.

[0083] A gate electrode of the fourth transistor TB4 receives a second control signal GC. A first electrode of the fourth transistor TB4 is coupled to the third node N3 and the gate electrode of the third transistor TB3. A second electrode of the fourth transistor TB4 is coupled to the anode of the OLED.

[0084] A gate electrode of the fifth transistor TB5 receives the second control signal GC. A first electrode of the fifth transistor TB5 is coupled to the data line and receives the data signal D from the data line. A second electrode of the fifth transistor TB5 is coupled to the second node N2.

[0085] The first capacitor C1 is coupled between the first node N1 and the gate electrode of the fifth transistor TB5. The second capacitor C2 is coupled between the second node N2 and the first power source providing the first power voltage ELVDD. The third capacitor C3 is coupled between the second node N2, and the third node N3, and the gate electrode of the third transistor TB3. When the first transistor TB1 is turned on, the first capacitor C1 is charged with a voltage corresponding to the data signal D provided from the data line.

[0086] In an initialization period, the first power voltage ELVDD and the second control signal GC are provided at a low level. The data line is in a high impedance (Hi-Z) state. As such, the fifth transistor TB5 and the fourth transistor TB4 are sequentially turned on and thus the third transistor TB3 is diode-connected, and a voltage of the anode of the OLED and a voltage of the third node N3 are initialized to a level of the driving voltage ELVDD.

[0087] In a compensation period, the second control signal GC is provided at a low level, and an auxiliary voltage Vsus having a high level is provided to the data line. As such, the fifth transistor TB5 is turned on and thus the auxiliary voltage Vsus is provided to the second node N2. Also, the fourth transistor TB4 is turned on and thus the third transistor TB3 is diode-connected, and a current flows until a voltage corresponding to a threshold voltage of the third transistor TB3 is stored in the third capacitor C3. Thereafter, the third transistor TB3 is turned off.

[0088] In a data transmission period, the first power voltage ELVDD and the second power voltage ELVSS are provided at a high level, and the first control signal GW is provided at a low level. As such, the second transistor TB2 is turned on and thus the data signal D written in the emission pixel EP2 in a scan period of an (N-1)th frame stored in the first capacitor C1 moves to the second node N2. Accordingly, a voltage difference between the driving voltage ELVDD and a voltage of the second node N2 is stored in the second capacitor C2.

[0089] In a scan/emission period Scan/Emission, a scan period and an emission period are concurrently (e.g., simultaneously) performed. In the scan/emission period Scan/Emission, the first power voltage ELVDD is provided at a high level, and the second power voltage ELVSS is provided at a low level. Also, the scan signal S at a low level is input to the scan line and thus the first transistor TB1 is turned on, and a data signal is input to the emission pixel EP2 coupled to the scan line. As such, a voltage corresponding to a data signal of an Nth frame is stored in the first capacitor C1.

[0090] The second transistor TB2 is turned off to block the first node N1 and the second node N2. Also, a current path from the first power voltage ELVDD to the cathode of the OLED is formed via the turned-on third transistor TB3, and the OLED emits light to a brightness corresponding to the data signal written in the emission pixel EP2 in the scan period of the (N-1)th frame stored in the second capacitor C2. In this regard, all emission pixels EP2 in the display area AA concurrently (e.g., simultaneously) emit light. That is, in the scan/emission period Scan/Emission, data signals of the Nth frame are sequentially input according to scan signals and, at the same time, all emission pixels EP2 in the display area AA concurrently (e.g., simultaneously) emit light in correspondence with data signals of the (N-1)th frame.

[0091] FIG. 35 is a circuit diagram of an emission pixel EP3 according to another embodiment of the present invention.

[0092] Referring to FIG. 35, the emission pixel EP3 includes the emission device E and a pixel circuit 2C for supplying a current to the emission device E. The dummy pixel DP includes the pixel circuit 2C excluding the emission device E. The emission device E includes an anode, a cathode, and an emission layer formed or located between the anode and the cathode, and may be an OLED having a structure in which the anode is split into a plurality of anodes. The emission device E may include the first through nth OLEDs OLED1 through OLEDn that are coupled in parallel to each other according to the plurality of anodes resulting from the splitting of the anode. Accordingly, a driving current of the pixel circuit 2B is separately provided to the first through nth OLEDs OLED1 through OLEDn. If a defective OLED is separated or electrically isolated from the corresponding pixel circuit, because the driving current is separately provided to the other OLEDs, the OLEDs may emit light without any perceivable brightness loss. The circuit connection wiring 12 coupled to the emission device E is disconnected from the circuit wiring 15 coupled to the pixel circuit 2C by cutting the circuit wiring 15, and thus the pixel circuit 2C and the emission device E may be separated or electrically isolated from each other.

[0093] The pixel circuit 2C includes first through eighth transistors TC1 through TC8, and the first and second capacitors C1 and C2.

[0094] A gate electrode of the first transistor TC1 receives the scan signal S from a scan line. A first electrode of the first transistor TC1 is coupled to a data line and receives a data signal D from the data line. A second electrode of the first transistor TC1 is coupled to the first node N1.

[0095] A gate electrode of the second transistor TC2 receives the first control signal GW. A first electrode of the second transistor TC2 is coupled to the first node N1. A second electrode of the second transistor TC2 is coupled to the second node N2.

[0096] A gate electrode of the third transistor TC3 receives a second control signal GI. A first electrode of the third transistor TC3 is coupled to an initialization power source and receives an initialization voltage Vint from the initialization power source. A second electrode of the third transistor TC3 is coupled to the third node N3.

[0097] A gate electrode of the fourth transistor TC4 receives the first control signal GW. A first electrode of the fourth transistor TC4 is coupled to the third node N3. A second electrode of the fourth transistor TC4 is coupled to a fourth node N4.

[0098] A gate electrode of the fifth transistor TC5 receives the second control signal GI. A first electrode of the fifth transistor TC5 is coupled to a first power source and receives the first power voltage ELVDD from the first power source. A second electrode of the fifth transistor TC5 is coupled to the second node N2.

[0099] A gate electrode of the sixth transistor TC6 is coupled to the third node N3. A first electrode of the sixth transistor TC6 is coupled to the second node N2. A second electrode of the sixth transistor TC6 is coupled to the fourth node N4. The sixth transistor TC6 functions as a driving transistor.

[0100] A gate electrode of the seventh transistor TC7 receives a third control signal GE. A first electrode of the seventh transistor TC7 is coupled to the fourth node N4. A second electrode of the seventh transistor TC7 is coupled to the anode of the OLED.

[0101] A gate electrode of the eighth transistor TC8 receives the third control signal GE. A first electrode of the eighth transistor TC8 is coupled to the first power source and receives the first power voltage ELVDD from the first power source. A second electrode of the eighth transistor TC8 is coupled to the second node N2.

[0102] The first capacitor C1 is coupled between the first node N1 and a third power source for providing a third power voltage Vhold. When the first transistor TC1 is turned on, the first capacitor C1 is charged with a voltage corresponding to the data signal D provided from the data line. The third power source may be set as a power source fixed to a voltage (e.g., a predetermined voltage, for example, a direct current (DC) power source). For example, the third power source may be set as the first power source for providing the first power voltage ELVDD or the initialization power source for providing the initialization voltage Vint. The second capacitor C2 is coupled between the third node N3 and the first power source.

[0103] In an initialization period, the first power voltage ELVDD is provided at a high level, and the second power

voltage ELVSS and the second control signal GI are provided at a low level. As such, the third transistor TC3 and the fifth transistor TC5 are turned on, and thus the first power voltage ELVDD is provided to the second node N2 and the initialization voltage Vint is provided to the third node N3.

[0104] In a compensation/data transmission period, the first power voltage ELVDD, the second power voltage ELVSS, and the first control signal GW are provided at a low level. As such, the second transistor TC2 is turned on, and thus the data signal D, written in the emission pixel EP3 in a scan period of an (N-1)th frame stored in the first capacitor C1, moves to the second node N2. Also, the fourth transistor TC4 is turned on and thus the sixth transistor TC6 is diode-connected, and a current flows through the diode-connected sixth transistor TC6, and thus a threshold voltage of the sixth transistor TC6 is compensated, and a voltage difference between the driving voltage ELVDD and a voltage of the second node N2 is stored in the second capacitor C2.

[0105] In a scan/emission period, a scan period and an emission period are concurrently (e.g., simultaneously) performed. In the scan/emission period, the first power voltage ELVDD is provided at a high level, and the second power voltage ELVSS and the third control signal GE are provided at a low level. Also, the scan signal S having a low level is input to the scan line and thus the first transistor TC1 is turned on, and a data signal of an Nth frame is input to the emission pixels EP3 coupled to the scan line. As such, a voltage corresponding to the data signal of the Nth frame is stored in the first capacitor C1.

[0106] The second transistor TC2 is turned off to block the first node N1 and the second node N2. Also, the seventh and eighth transistors TC7 and TC8 are turned on and thus a current path from the first power voltage ELVDD to the cathode of the OLED is formed via the turned-on sixth transistor TC6, and the OLED emits light at a brightness corresponding to a data signal written in the emission pixel EP3 in the scan period of the (N-1)th frame stored in the second capacitor C2. In this regard, all emission pixels EP3 in the display area AA concurrently (e.g., simultaneously) emit light. That is, in the scan/emission period, data signals of the Nth frame are sequentially input according to scan signals and, at the same time, all emission pixels EP3 in the display area AA concurrently (e.g., simultaneously) emit light in correspondence with data signals of the (N-1)th frame. The emission period may partially overlap with the scan period and may be shorter than the scan period.

[0107] FIG. 36 is a circuit diagram of an emission pixel EP4 according to another embodiment of the present invention.

[0108] Referring to FIG. 36, the emission pixel EP4 includes the emission device E and a pixel circuit 2D for supplying a current to the emission device E. The dummy pixel DP includes the pixel circuit 2D excluding the emission device E. The emission device E includes an anode, a cathode, and an emission layer formed or located between the anode and the cathode, and may be an OLED having a structure in which the anode is split into a plurality of anodes. The emission device E may include the first through nth OLEDs OLED1 through OLEDn that are coupled in parallel to each other according to the plurality of anodes resulting from the splitting of the anode. Accordingly, a driving current of the pixel circuit 2D is separately provided to the first through nth OLEDs OLED1 through OLEDn. If a defective OLED is separated or electrically isolated, because the driving current is separately provided to the other OLEDs, the OLEDs may emit light without any perceivable brightness loss. The circuit connection wiring 12 coupled to the emission device E is disconnected from the circuit wiring 15 coupled to the pixel circuit 2D by cutting the circuit wiring 15, and thus the pixel circuit 2D and the emission device E may be separated or electrically isolated from each other.

[0109] The pixel circuit 2D includes first and second transistors TD1 and TD2, and a first capacitor C.

[0110] A gate electrode of the first transistor TD1 is coupled to a scan line. A first electrode of the first transistor TD1 is coupled to a data line. A second electrode of the first transistor TD1 is coupled to the first node N1.

[0111] A gate electrode of the second transistor TD2 is coupled to the first node N1. A first electrode of the second transistor TD2 receives the first power voltage ELVDD from a first power source. A second electrode of the second transistor TD2 is coupled to the anode of the OLED.

[0112] A first electrode of the capacitor C is coupled between the first node N1. A second electrode of the capacitor C receives (e.g., is coupled to) the first power voltage ELVDD from the first power source.

[0113] When the scan signal S is provided from the scan line, the first transistor TD1 transfers the data signal D provided from the data line to the first electrode of the capacitor C. As such, a voltage corresponding to the data signal D is charged in the capacitor C, and a driving current corresponding to the voltage charged in the capacitor C is transferred to the emission device E through the second transistor TD2, and thus the emission device E emits light.

[0114] Although the emission pixel EP4 of FIG. 36 has a 2Tr-1 Cap structure including two transistors and one capacitor in one pixel, the present invention is not limited thereto. That is, the emission pixel EP4 may have various structures including two or more transistors and one or more capacitors by forming additional wirings or omitting the existing wirings.

[0115] FIG. 37 is a schematic diagram of a display panel 10d according to another embodiment of the present invention.

[0116] Referring to FIG. 37, a plurality of pixels P aligned in a matrix-like shape where the plurality of scan lines SL, the plurality of data lines DL, and the plurality of repair lines RL cross each other are formed on the display panel 10d. The pixels P include emission pixels EP formed on the display area AA, and dummy pixels

DP formed on the non-display area NA. The non-display area NA may be formed on at least one of top and bottom regions of the display area AA. As such, one or more dummy pixels DP may be formed in each pixel column on at least one of top and bottom regions of the pixel column. FIG. 37 shows an example that the dummy pixel DP is formed on the bottom region of the pixel column.

[0117] One emission pixel EP includes first through third sub-emission pixels SEP1, SEP2, and SEP3 aligned in a column direction. Each of the first through third sub-emission pixels SEP1, SEP2, and SEP3 includes the pixel circuit PC, and the emission device E coupled to the pixel circuit PC. The emission device E may be an OLED including an anode, a cathode, and an emission layer between the anode and the cathode. The anode of the emission device E may be split into at least two anodes and thus the emission device E may include at least two sub-emission devices.

[0118] The pixel circuits PC and/or the emission devices E of the first through third sub-emission pixels SEP1, SEP2, and SEP3 may differ in size. The first through third sub-emission pixels SEP1, SEP2, and SEP3 are commonly coupled to one scan line, for example, an ith scan line SLi, and are respectively coupled to first through third data lines DLj_1, DLj_2, and DLj_3. Accordingly, if a scan signal is provided to the ith scan line SLi, data signals are provided via the first through third data lines DLj_1, DLj_2, and DLj_3 respectively to the first through third sub-emission pixels SEP1, SEP2, and SEP3, and thus each of the first through third sub-emission pixels SEP1, SEP2, and SEP3 is charged with a voltage corresponding to the provided data signal and emits light at a brightness corresponding to the charged voltage.

[0119] The dummy pixel DP includes first through third sub-dummy pixels SDP1, SDP2, and SDP3 aligned in a column direction. Each of the first through third sub-dummy pixels SDP1, SDP2, and SDP3 includes only a pixel circuit PC excluding an emission device E. The pixel circuit PC of each of the first through third sub dummy pixels SDP1, SDP2, and SDP3 may have the same or substantially the same design and function as the pixel circuit PC of each of the first through third sub-emission pixels SEP1, SEP2, and SEP3. The first through third sub-dummy pixels SDP1, SDP2, and SDP3 are commonly coupled to one scan line, for example, an (n+1)th scan line SLn+1, and are respectively coupled to the first through third data lines DLj_1, DLj_2, and DLj_3. Accordingly, if a scan signal is provided to the (n+1)th scan line SLn+1, data signals are provided via the first through third data lines DLj_1, DLj_2, and DLj_3 respectively to the first through third sub-dummy pixels SDP1, SDP2, and SDP3.

[0120] From among the first through third sub-emission pixels SEP1, SEP2, and SEP3, if the pixel circuit PC of the second sub-emission pixel SEP2 is defective, the pixel circuit PC of the second sub-emission pixel SEP2 is separated or electrically isolated from the second sub-emission device SE2, and the second sub-emission device SE2 is coupled to the repair line RLj. Also, from among the first through third sub-dummy pixels SDP1, SDP2, and SDP3, the pixel circuit PC of the second sub-dummy pixel SDP2 corresponding to the second sub-emission pixel SEP2 is coupled to the repair line RLj.

[0121] FIG. 37 shows an example that a dummy pixel is formed as a plurality of sub-pixels when a plurality of sub-pixels included in one pixel have different characteristics. However, even in this case, the same driving principal may also be applied by forming a dummy pixel as one sub-pixel and correcting a gamma value of a data signal provided to the dummy pixel.

[0122] FIG. 38 is a circuit diagram of an emission pixel EP5 according to another embodiment of the present invention.

[0123] Referring to FIG. 38, the emission pixel EP5 includes the emission device E and a pixel circuit 2E for supplying a current to the emission device E. The dummy pixel DP includes the pixel circuit 2E excluding the emission device E. The emission device E includes an anode, a cathode, and an emission layer formed or located between the anode and the cathode, and may be an OLED having a structure in which the anode is split into a plurality of anodes. The emission device E may include the first through nth OLEDs OLED1 through OLEDn that are coupled in parallel to each other through the plurality of anodes resulting from the splitting of the anode. Accordingly, a driving current of the pixel circuit 2E is separately provided to the first through nth OLEDs OLED1 through OLEDn. If a defective OLED is separated or electrically isolated from the corresponding pixel circuit, because the driving current is separately provided to the other OLEDs, the OLEDs may emit light without any perceivable brightness loss. The circuit connection wiring 12 coupled to the emission device E is disconnected from the circuit wirings 15 and 19 coupled to the pixel circuit 2E by cutting the circuit wirings 15 and 19, and thus the pixel circuit 2E and the emission device E may be separated or electrically isolated from each other.

[0124] The pixel circuit 2E of FIG. 38 which further includes a ninth transistor TC9 and accordingly further includes the circuit wiring 19 coupled to the emission device E is the same as the pixel circuit 2C of FIG. 35 in terms of structure and operation, and thus a detailed description thereof will be omitted here.

[0125] A gate electrode of the ninth transistor TC9 receives the second control signal GI. A first electrode of the ninth transistor TC9 is coupled to an initialization power line and receives the initialization voltage Vint from the initialization power line. A second electrode of the ninth transistor TC9 is coupled to the anode of the emission device E. The ninth transistor TC9 is turned on by the second control signal GI and provides the initialization voltage Vint to the anode.

[0126] FIG. 39 is a plan view of the emission pixel EP including the pixel circuit 2E of FIG. 38.

[0127] FIG. 39 shows the emission pixel EP including three emission sub-pixels SEP_R, SEP_G, and SEP_B

that are coupled to the scan line SL and a plurality of data lines DL_R, DL_G, and DL_B, respectively. The red sub-pixel SEP_R includes two red sub-emission devices OLED_R1 and OLED_R2 by an anode split and a red pixel circuit PC_R. The green sub-pixel SEP_G includes two green sub-emission devices OLED_G1 and OLED_G2 by the anode split and a green pixel circuit PC_G. The blue sub-pixel SEP_B includes two blue sub-emission devices OLED_B1 and OLED_B2 by the anode split and a blue pixel circuit PC_B. For convenience of explanation and understanding, FIG. 39 shows only an anode of each sub-emission device.

[0128] Referring to FIG. 39, the repair line RL is formed or located in a pixel column direction to the left of the three emission sub-pixels SEP_R, SEP_G, and SEP_B, and a first signal line GWL providing the first control signal GW, a second signal line GIL providing the second control signal GI, a third signal line GEL providing the third control signal GE, the power voltage line ELVDDL, an initialization voltage line VL, and the data lines DL_R, DL_G, and DL_B are formed or located in the pixel column direction to the right of the three emission sub-pixels SEP_R, SEP_G, and SEP_B.

[0129] Each of the emission sub-pixels SEP_R, SEP_G, and SEP_B includes short nodes SN1_R, SN1_G, and SN1_B that are provisionally coupled to the repair line RL, and cut nodes CN1_R, CN2_R, CN1_G, CN2_G, CN1_B, and CN2_B formed in electrode connection wirings coupling the red sub-emission devices OLED_R1 and OLED_R2, the green sub-emission devices OLED_G1 and OLED_G2, and the blue sub-emission devices OLED_B1 and OLED_B2. The red sub-emission devices OLED_R1 and OLED_R2, the green sub-emission devices OLED_G1 and OLED_G2, and the blue sub-emission devices OLED_B1 and OLED_B2 may be separated or electrically isolated from the red pixel circuit PC_R, the green pixel circuit PC_G, and the blue pixel circuit PC_B by cutting the circuit wirings 15 and 19 coupled to the red pixel circuit PC_R, the green pixel circuit PC_G, and the blue pixel circuit PC_B.

[0130] FIG. 40 is a plan view of the dummy pixel DP including the pixel circuit 2E of FIG. 38.

[0131] FIG. 40 shows the dummy pixel DP including the three dummy sub-pixels SDP_R, SDP_G, and SDP_B that are coupled to the scan line SL and the plurality of data lines DL_R, DL_G, and DL_B, respectively. The red dummy sub-pixel SDP_R includes the red pixel circuit PC_R. The green dummy sub-pixel SDP_G includes the green pixel circuit PC_G. The blue dummy sub-pixel SDP_B includes the blue pixel circuit PC_B.

[0132] Referring to FIG. 40, the repair line RL is formed or located in a pixel column direction to the left of the three dummy sub-pixels SDP_R, SDP_G, and SDP_B. The first signal line GWL providing the first control signal GW, the second signal line GIL providing the second control signal GI, the third signal line GEL providing the third control signal GE, the power voltage line ELVDDL, the initialization voltage line VL, and the data lines DL_R, DL_G, and DL_B are formed or located in the pixel column direction to the right of the three dummy sub-pixels SDP_R, SDP_G, and SDP_B.

[0133] Each of the dummy sub-pixels SDP_R, SDP_G, and SDP_B includes short nodes SN2_R, SN2_G, and SN2_B that are provisionally coupled to the repair line RL. The repair line RL is coupled to the power voltage line ELVDDL, and when a defective pixel is repaired by using the repair line RL in the future, the power voltage line ELVDDL and the repair line RL may be separated or electrically isolated from each other by cutting a region X of the power connection wiring 18.

[0134] FIG. 41 is a plan view of the emission device E of the emission pixel EP according to another embodiment of the present invention. FIG. 42 is a cross-sectional view taken along a line C-C' of FIG. 41.

[0135] Referring to FIG. 41, split electrodes of the emission device E according to an embodiment of the present invention, i.e., the first and second anodes AD1 and AD2, the electrode connection wiring 11, and the circuit connection wiring 12, may be integrally formed. The electrode connection wiring 11 may include the first connection units CU1 coupled to the first and second anodes AD1 and AD2 and the second connection unit CU2 coupled to the circuit connection wiring 12. The first and second cut nodes CN1 and CN2 are formed between the first connection unit CU1 and the second connection unit CU2. As such, the first and second cut nodes CN1 and CN2 may be cut by irradiating a laser beam onto the first and second cut nodes CN1 and CN2 in the future. The electrode connection wiring 11 contacts the short wiring 14 that overlaps with a part of the repair connection wiring 13 in the first short node SN1 and is provisionally coupled to the repair connection wiring 13. The repair line RL is coupled to the repair connection wiring 13 through a contact hole. As such, the short wiring 14 and the repair connection wiring 13 may be coupled to each other by irradiating the laser beam onto the first short node SN1 in the future.

[0136] The repair line RL and the short wiring 14 may be formed on the same layer and of the same material as a conductive electrode included in a TFT of the pixel circuit PC, for example, a source electrode and a drain electrode. The third insulating layer 105 is formed on the repair line RL and the short wiring 14. The first and second anodes AD1 and AD2, the electrode connection wiring 11, and the circuit connection wiring 12 are integrally formed on the third insulating layer 105. The fourth insulating layer 106 covering edges of the first and second anodes AD1 and AD2 is formed on the first and second anodes AD1 and AD2.

[0137] FIG. 43 is a cross-sectional diagram of an organic light emitting display apparatus including the emission pixels EP, according to an embodiment of the present invention.

[0138] Referring to FIG. 43, the display area AA that includes the emission pixels EP and displays an image are provided on the substrate 101 of the organic light

emitting display apparatus according to an embodiment of the present invention. In the non-display area NA outside the display area AA, the dummy pixel DP and a pad unit PAD that transfers a plurality of driving signals and control signals to the display area AA are formed. The emission pixels EP and the pad unit PAD are only shown in FIG. 43.

[0139] The organic light emitting display apparatus includes the emission devices E including a plurality of sub-emission devices, the pixel circuit PC including at least one TFT TR and at least one capacitor CAP and supplying a driving current to the emission device E, and the pad unit PAD.

[0140] The emission device E includes an anode AD including the split first and second anodes AD1 and AD2, a cathode CD facing the anode AD, and an organic layer OL including an emission layer formed or located between the anode AD and the cathode CD.

[0141] The anode AD may have a three layer structure including semitransparent metal and a transparent conductive oxide formed on top and bottom portions of the semitransparent metal and protecting the semitransparent metal. The semitransparent metal may include silver (Ag) or a silver alloy. The transparent conductive oxide may include at least one selected from the group consisting of ITO, IZO, ZnO, In_2O_3, IGO, and AZO. The semitransparent metal forms a micro-cavity structure along with the cathode CD, thereby increasing light efficiency of the organic light emitting display apparatus. The fourth insulating layer 106 that is a pixel definition layer covering the split first and second anodes AD1 and AD2 may be formed in edges of the split first and second anodes AD1 and AD2. One of the split first and second anodes AD1 and AD2 may be coupled to one of a source electrode 217a and a drain electrode 217b of the transistor TR through a contact metal 117.

[0142] Although not shown, the split first and second anodes AD1 and AD2 may be coupled to each other by the electrode connection wiring 11 (see FIGS. 15 and 41). The electrode connection wiring 11 may be formed on the same layer and of the same material as the anode AD or may be formed on the same layer and of the same material as an active layer 212 of the transistor TR and contact the anode AD. The electrode connection wiring 11 may contact one of the source electrode 217a and the drain electrode 217b of the transistor TR. The transistor TR coupled to the electrode connection wiring 11 may be different from the transistor TR coupled to one of the split first and second anodes AD1 and AD2.

[0143] The cathode CD may be configured as a reflective electrode including a reflective material. In this regard, the cathode CD may include at least one selected from the group consisting of Al, Mg, Li, Ca, LiF/Ca, and LiF/Al. The cathode CD may be configured as a reflective electrode so that light emitted from the organic layer OL is reflected from the cathode CD, and is transmitted through the anode AD formed of semitransparent metal, and then is emitted through the substrate 101.

[0144] The transistor TR may include the active layer 212 formed on the buffer layer 102 of the substrate 101, a gate electrode 215 formed on the active layer 212 with the first insulating layer 103 that is a gate insulating layer formed therebetween and located at a location corresponding to a channel region 212c of the active layer 212, the source electrode 217a and the drain electrode 217b disposed on the gate electrode 215 with the second insulating layer 104 that is an interlayer insulating layer formed or located therebetween and respectively coupled to a source region 212a and a drain region 212b.

[0145] The active layer 212 may be formed of a semiconductor containing amorphous or crystalline silicon, or an oxide semiconductor. The active layer 212 may include the channel region 212c and the source region 212a and the drain region 212b that are doped with ion impurities and located at opposite sides of the channel region 212c. The gate electrode 215 may be formed from a single layer or a plurality of layers including at least one metal selected from the group consisting of aluminium (Al), platinum (Pt), palladium (Pd), silver (Ag), magnesium (Mg), gold (Au), nickel (Ni), neodymium (Nd), iridium (Ir), chromium (Cr), lithium (Li), nickel (Ni), calcium (Ca), molybdenum (Mo), titanium (Ti), tungsten (W), and copper (Cu). The source electrode 217a and the drain electrode 217b may be formed from two or more layers of two different metals with different electron mobilities. For example, the two different metals may be selected from the group consisting of Al, Pt, Pd, Ag, Mg, Au, Ni, Nd, Ir, Cr, Li, Ni, Ca, Mo, Ti, W, Cu, or an alloy thereof.

[0146] The capacitor CAP may include a first electrode 312 formed on the same layer as the active layer 212, a second electrode 314 formed on the same layer as the gate electrode 215, and a third electrode 317 formed on the same layer as the source electrode 217a and the drain electrode 217b.

[0147] The first electrode 312 of the capacitor CAP may be formed of a semiconductor doped with ion impurities like the source region 212a and the drain region 212b of the active layer 212. The second electrode 314 of the capacitor CAP is formed on the first insulating layer 103 where the gate electrode 215 is formed or located, but of a different material than the gate electrode 215. The second electrode 314 may include a transparent conductive oxide. The capacitor CAP may have a metal-insulator-metal (MIM) structure by forming a semiconductor doped with ion impurities as the first electrode 312 through the second electrode 314.

[0148] First and second pad electrodes 417 and 418 that are connection terminals of an external driver may be formed in the pad unit PAD.

[0149] The first pad layer 417 may include a plurality of metal layers with different electron mobilities. For example, the first pad layer 417 may be formed from multiple layers of at least one metal selected from the group consisting of Al, Pt, Pd, Ag, Mg, Au, Ni, Nd, Ir, Cr, Li, Ni, Ca, Mo, Ti, W, and Cu.

[0150] The second pad layer 418 may be formed of a

transparent conductive oxide containing at least one material selected from the group consisting of ITO, IZO, ZnO, In_2O_3, IGO, and AZO. The second pad layer 418 may prevent exposure of the first pad layer 417 to moisture and oxygen, thereby preventing degradation in reliability of a pad.

[0151] In the above-described embodiments, a pixel circuit is formed as a p-channel metal-oxide semiconductor (PMOS) transistor and a low-level signal is an enable signal while a high-level signal is a disable signal. However, the present invention may also be applied by forming the pixel circuit as an n-channel metal-oxide semiconductor (NMOS) transistor and inverting the provided signals. In this case, a high-level signal is an enable signal and a low-level signal is a disable signal.

[0152] In the above-described embodiments, an emission pixel circuit and a dummy pixel circuit may be the same (e.g., having a same component structure or functionality), or the dummy pixel circuit may be different (e.g., having a different component structure or functionality) from the emission pixel circuit of which TFTs and/or capacitors are partially omitted and/or added.

[0153] In the above-described embodiments, although an anode has a two split structure, the anode may have a plural split structure, for example, three split anodes, four split anodes, etc., as described above.

[0154] According to embodiments of the present invention, an operating point of a TFT is included in a saturation range and, if an anode of a defective pixel has a high resistance, a current of the defective pixel may be corrected by predicting a resistance value.

In the above-described embodiments, a pixel circuit is formed as a p-channel metal-oxide semiconductor (PMOS) transistor and a low-level signal is an enable signal while a high-level signal is a disable signal. However, the present invention may also be applied by forming the pixel circuit as an n-channel metal-oxide semiconductor (NMOS) transistor and inverting the provided signals. In this case, a high-level signal is an enable signal and a low-level signal is a disable signal.

In the above-described embodiments, an emission pixel circuit and a dummy pixel circuit may be the same (e.g., having a same component structure or functionality), or the dummy pixel circuit may be different (e.g., having a different component structure or functionality) from the emission pixel circuit of which TFTs and/or capacitors are partially omitted and/or added.

In the above-described embodiments, although an anode has a two split structure, the anode may have a plural split structure, for example, three split anodes, four split anodes, etc., as described above.

According to embodiments of the present invention, an operating point of a TFT is included in a saturation range and, if an anode of a defective pixel has a high resistance, a current of the defective pixel may be corrected by predicting a resistance value.

The embodiments of the present invention are not limited to the above-described pixel structure, may be applied to various pixels for emitting light, and may achieve light emission without any perceivable brightness reduction by repairing a bright spot or a dark spot of a defective pixel due to a defect of a pixel circuit or an emission device. A dark spot or a dark spot caused by a defective pixel circuit or emission device is relatively easily repaired by using a dummy pixel of a display apparatus of the present invention, thereby improving yield and reliability of a panel.

Claims

1. An organic light-emitting display apparatus (100) comprising:

a display panel (10a, 10b, 10c) that comprises a plurality of pixels (P), a scan driving unit (20), a data driving unit (30) and a control unit (40), wherein a plurality of n scan lines (SL), n being a natural number, extending in a horizontal direction, and a plurality of the data lines (DL) extending in a vertical direction and perpendicularly crossing the scan lines (SL) are formed on the display panel (10), wherein a plurality of repair lines (RL) extending parallel with and spaced apart from the data lines (DL) and perpendicularly crossing the scan lines SL are formed on the display panel (10), and the plurality of pixels (P) aligned in a matrix-like shape are formed where the scan lines (SL), the data lines (DL), and the repair lines (RL) cross each other, wherein at least one repair line is formed in each pixel column,

wherein the plurality of pixels (P) comprises a plurality of emission pixels (EP) in a display area (AA), each emission pixel (EP) comprising an emission device (E) that comprises an emission pixel circuit (PCi) coupled to and configured to supply a driving current to the emission device (E), , and

one row of dummy pixels (DP), each comprising a dummy pixel circuit (PCn+1), formed in a non-display are (NA) on the top and/or bottom regions of the display area (AA), the dummy pixel circuits (PCn+1) of the row being connected to a further scan line (SL), wherein each of the plurality of repair lines (RL) is configured to be electrically coupled to one of the emission devices (E) having a defective emission pixel circuit (PCi) and to a dummy pixel circuit (PCn+1) in the same column, and

wherein the scan driving unit (20) is configured to sequentially provide or activate first through nth scan signals (S1 through Sn) to the first through nth scan line (SL1 through SLn) and to provide a further scan signal (Sn+1 to the (n+1)th) to the further scan line (SLn+1) at the

same time as the scan signal (Si) is provided to the scan line (SL) connected to the defective emission pixel circuit (PCi), and
wherein the data driving unit (30) is configured to sequentially provide or activate first through nth data signals (D1 through Dn) to the data line (DL1) connected to the defective emission pixel circuit (PCi) in synchronization with the scan signals (S1 through Sn+1), wherein a data signal (Di) that is the same as the data signal (Di) provided to the defective emission pixel circuit (PCi) is concurrently provided to the dummy pixel circuit (PCn+1).

2. The organic light-emitting display apparatus of claim 1, wherein the emission device (E) comprises a first sub-emission device (SE1) and a second sub-emission device (SE2), wherein the first sub-emission device (SE1) comprising a first lower electrode, an upper electrode (AD1) facing the first lower electrode, and a first emission layer between the first lower electrode and the upper electrode (AD1); and the second sub-emission device (SE2) comprising a second lower electrode, the upper electrode (AD2) facing the second lower electrode, and a second emission layer between the second lower electrode and the upper electrode (AD2), wherein the first lower electrode and the second lower electrode are coupled to each other through an electrode connection wiring (11).

3. The organic light-emitting display apparatus of claim 2, wherein the electrode connection wiring (11) comprises at least one of metal, amorphous silicon, crystalline silicon, and an oxide semiconductor.

4. The organic light-emitting display apparatus of claim 2 or 3, wherein the electrode connection wiring (11) is at a same layer and of a same material as an active layer of the emission pixel circuit (PCi).

5. The organic light-emitting display apparatus of claim 2 or 3, wherein the electrode connection wiring (11) is integrally formed with the plurality of separated lower electrodes.

6. The organic light-emitting display apparatus of claim 2, wherein the electrode connection wiring comprises:

a first connection unit (CU1) coupled to the first lower electrode;
a second connection unit (CU2) coupled to the second lower electrode;
a third connection unit (CU3) coupled to the emission pixel circuit; a first node (CN1) between the first connection unit (CU1) and the third connection unit (CU3) and configured to be cut to electrically isolate the first submission device (SE1) from the emission pixel circuit (PCi); and
a second node (CN2) between the second connection unit (CU2) and the third connection unit (CU3) and configured to be cut to electrically isolate the second submission (SE2) device from the emission pixel circuit (PCi).

7. The organic light-emitting display apparatus of claim 6, further comprising:
at least one circuit wiring (15) having one end coupled to the emission pixel circuit (PCi) and another end coupled to the second connection unit (CU2), wherein the at least one circuit wiring is configured to be cut to electrically isolate the emission pixel (PCi) circuit from the emission device (E).

8. The organic light-emitting display apparatus of claim 6 or 7, further comprising:

a first repair connection wiring (13) having one end coupled to the repair line (RL) and another end insulated from, and configured to be electrically coupled to a first short wiring (14), in the display area (AA), the first short wiring electrically coupled to the emission device (E), and
a second repair connection wiring (16) having one end coupled to the first repair line (RL) and another end insulated from, and configured to be electrically coupled to a second short wiring (17), in the non-display area (NA), the second short wiring coupled to the dummy pixel circuit (PCn+1).

9. The organic light-emitting display apparatus of claim 8, wherein the first repair connection wiring (13) and the second repair connection wiring (16) are at a same layer as a first conductive layer of the emission pixel circuit (PCi) and the first short wiring (14) and the second short wiring (17) are at a same layer as a second conductive layer of the emission pixel circuit (PCi).

10. The organic light-emitting display apparatus of one of claims 1 to 9, wherein the first repair connection wiring is coupled to the first short wiring, and the second repair connection wiring is coupled to the second short wiring

11. The organic light-emitting display apparatus of one of claims 1 to 10, wherein the first and second sub-emission devices (SE1, SE2) are separated each other such that the first sub-emission device (SE1) is coupled to the dummy pixel circuit (PCn+1) and separated from the emission pixel circuit (PCi), and the second sub-emission device (SE2) is coupled to the emission pixel circuit (PCi) and separated from

the dummy pixel circuit (PCn+1).

12. The organic light-emitting display apparatus of one of claims 1 to 11, wherein the emission pixel circuit (E) comprises:

a first transistor (TA1) configured to transfer a data signal in response to a scan signal;
a capacitor (C1) configured to be charged with a voltage corresponding to the data signal; and
a second transistor (TA2) configured to transfer a driving current corresponding to the voltage charged in the capacitor to the emission device (E).

13. The organic light-emitting display apparatus of one of claims 1 to 12, wherein the emission pixel circuit (PCi) further comprises:

a first transistor (TA1) configured to receive a data signal from a data line (DL) in response to a scan signal;
a second transistor (TA2) configured to transfer a driving current corresponding to the data signal to the emission device (E);
a third transistor (TA3) configured to diode-connect the second transistor (TA1);
a first capacitor (C1) configured to be charged with a voltage corresponding to the data signal; and
a second capacitor (C2) connected to one electrode of the first capacitor (C1) and a gate electrode of the second transistor (TA2).

14. The organic light-emitting display apparatus of claim 13, wherein the emission pixel circuit (PCi) further comprises:

a fourth transistor (TA4) connected to between the first transistor (TA1) and the one electrode of the first capacitor (C1);
a fifth transistor (TA5) connected to between the data line (DL) and the one electrode of the first capacitor (C1); and
a third capacitor (C3) having one electrode connected to a node between the first transistor (TA1) and the fourth transistor (TA4) and another electrode connected to a gate electrode of the fifth transistor (TA5).

15. The organic light-emitting display apparatus of one of claims 1 to 11, wherein the emission pixel circuit (PCi) further comprises:

a first transistor (TA1) configured to receive a data signal from a data line (DL) in response to a scan signal;
a second transistor (TA2) configured to transfer a driving current corresponding to the data signal to the emission device (PCi);
a third transistor (TA3) configured to diode-connect the second transistor (TA2);
a fourth transistor (TA4) connected to between the first transistor (TA1) and the second transistor (TA2);
a fifth transistor (TA5) connected to between the second transistor (TA2) and the emission device (E);
a sixth transistor (TA6) connected to between a gate electrode of the second transistor (TA2) and an initial power;
a first capacitor (C1) connected to between the gate electrode of the second transistor (TA2) and a first power source; and
a second capacitor (C2) having one electrode connected to a node between the first transistor (TA1) and the fourth transistor (TA4) and another electrode connected to a second power source.

Patentansprüche

1. Eine organische lichtemittierende Anzeigevorrichtung (100), aufweisend:

eine Anzeigetafel (10a, 10b, 10c), die eine Vielzahl von Pixeln (P), eine Abtastansteuereinheit (20), eine Datenansteuereinheit (30) und eine Steuereinheit (40) aufweist, wobei eine Vielzahl von n-Abtastleitungen (SL), wobei n eine natürliche Zahl ist, die in eine horizontale Richtung verlaufen, und eine Vielzahl der Datenleitungen (DL), die in eine vertikale Richtung verlaufen und die Abtastleitungen (SL) perpendikulär kreuzen, auf der Anzeigetafel (10) ausgebildet sind, wobei eine Vielzahl von Reparaturleitungen (RL), die parallel zu und beabstandet von den Datenleitungen (DL) verlaufen und die Abtastleitungen SL perpendikulär kreuzen, auf der Anzeigetafel (10) ausgebildet sind, und wobei die Vielzahl der Pixel (P), die in einer matrixartigen Form ausgerichtet sind, dort ausgebildet sind, wo sich die Abtastleitungen (SL), die Datenleitungen (DL) und die Reparaturleitungen (RL) kreuzen, wobei zumindest eine Reparaturleitung in jeder Pixelspalte ausgebildet ist,
wobei die Vielzahl der Pixel (P) eine Vielzahl von Emissionspixeln (EP) in einem Anzeigebereich (AA) aufweist, wobei jeder Emissionspixel (EP) eine Emissionsvorrichtung (E), die eine Emissionspixelschaltung (PCi), die mit der Emissionsvorrichtung (E) gekoppelt ist und konfiguriert ist, um die Emissionsvorrichtung (E) mit einem Ansteuerstrom zu versorgen, aufweist, aufweist, und

eine Zeile von Dummy-Pixeln (DP), von denen jeder eine Dummy-Pixelschaltung (PCn+1), die in einem Nicht-Anzeigebereich (NA) im oberen und/oder unteren Bereich des Anzeigebereichs (AA) ausgebildet ist, aufweist, wobei die Dummy-Pixelschaltungen (PCn+1) der Zeile mit einer weiteren Abtastleitung (SL) verbunden sind, wobei jede der Vielzahl der Reparaturleitungen (RL) konfiguriert ist, um mit einer der Emissionsvorrichtungen (E), die eine defekte Emissionspixelschaltung (PCi) aufweisen, und mit einer Dummy-Pixelschaltung (PCn+1) in derselben Spalte gekoppelt zu sein, und
wobei die Abtastansteuereinheit (20) konfiguriert ist, um nacheinander erste bis n-te Abtastsignale (S1 bis Sn) zur ersten bis n-ten Abtastleitung (SL1 bis SLn) zu liefern oder zu aktivieren und um zeitgleich mit dem Liefern des Abtastsignals (Si) zu der Abtastleitung (SL), die mit der defekten Emissionspixelschaltung (PCi) verbunden ist, ein weiteres Abtastsignal (Sn+1 bis zum (n+1)ten) zur weiteren Abtastleitung (SLn+1) zu liefern, und
wobei die Datenansteuereinheit (30) konfiguriert ist, um nacheinander synchron mit den Abtastsignalen (S1 bis Sn+1) erste bis n-te Datensignale (D1 bis Dn) zu der Datenleitung (DL1), die mit der defekten Emissionspixelschaltung (PCi) verbunden ist, zu liefern oder zu aktiveren, wobei ein Datensignal (Di), das gleich dem Datensignal (Di), das zur defekten Emissionspixelschaltung (PCi) geliefert wird, ist, gleichzeitig zur Dummy-Pixelschaltung (PCn+1) geliefert wird.

2. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 1, wobei die Emissionsvorrichtung (E) eine erste Sub-Emissionsvorrichtung (SE1) und eine zweite Sub-Emissionsvorrichtung (SE2) aufweist, wobei die erste Sub-Emissionsvorrichtung (SE1) eine erste untere Elektrode, eine obere Elektrode (AD1), die der ersten unteren Elektrode zugewandt ist, und eine erste Emissionsschicht zwischen der ersten unteren Elektrode und der oberen Elektrode (AD1) aufweist; und wobei die zweite Sub-Emissionsvorrichtung (SE2) eine zweite untere Elektrode, wobei die obere Elektrode (AD2) der zweiten unteren Elektrode zugewandt ist, und eine zweite Emissionsschicht zwischen der zweiten unteren Elektrode und der oberen Elektrode (AD2) aufweist, wobei die erste untere Elektrode und die zweite untere Elektrode durch eine Elektrodenverbindungsverdrahtung (11) miteinander gekoppelt sind.

3. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 2, wobei die Elektrodenverbindungsverdrahtung (11) zumindest eines von Metall, amorphem Silizium, kristallinem Silizium und einem Oxidhalbleiter aufweist.

4. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 2 oder 3, wobei die Elektrodenverbindungsverdrahtung (11) auf einer selben Schicht und aus einem selben Material wie eine Aktivschicht der Emissionspixelschaltung (PCi) ist.

5. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 2 oder 3, wobei die Elektrodenverbindungsverdrahtung (11) einstückig mit der Vielzahl getrennter unterer Elektroden ausgebildet ist.

6. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 2, wobei die Elektrodenverbindungsverdrahtung aufweist:

eine erste Verbindungseinheit (CU1), die mit der ersten unteren Elektrode gekoppelt ist;
eine zweite Verbindungseinheit (CU2), die mit der zweiten unteren Elektrode gekoppelt ist;
eine dritte Verbindungseinheit (CU3), die mit der Emissionspixelschaltung gekoppelt ist; einen ersten Knoten (CN1) zwischen der ersten Verbindungseinheit (CU1) und der dritten Verbindungseinheit (CU3), der konfiguriert ist, um durchtrennt zu werden, um die erste Sub-Emissionsvorrichtung (SE1) von der Emissionspixelschaltung (PCi) elektrisch zu isolieren; und
einen zweiten Knoten (CN2) zwischen der zweiten Verbindungseinheit (CU2) und der dritten Verbindungseinheit (CU3), der konfiguriert ist, um durchtrennt zu werden, um die zweite Sub-Emissions (SE2)-vorrichtung von der Emissionspixelschaltung (PCi) elektrisch zu isolieren.

7. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 6, ferner aufweisend:
zumindest eine Schaltungsverdrahtung (15), die ein Ende, das mit der Emissionspixelschaltung (PCi) gekoppelt ist, und ein anderes Ende, das mit der zweiten Verbindungseinheit (CU2) gekoppelt ist, aufweist, wobei die zumindest eine Schaltungsverdrahtung konfiguriert ist, um durchtrennt zu werden, um die Emissionspixel (PCi)-Schaltung von der Emissionsvorrichtung (E) elektrisch zu isolieren.

8. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 6 oder 7, ferner aufweisend:

eine erste Reparaturverbindungsverdrahtung (13), die ein Ende, das mit der Reparaturleitung (RL) gekoppelt ist, und ein anderes Ende, das davon isoliert ist, aufweist und konfiguriert ist, um mit einer ersten Kurzschlussverdrahtung (14) im Anzeigebereich (AA) elektrisch gekoppelt zu werden, wobei die erste Kurzschlussverdrahtung mit der Emissionsvorrichtung (E) elek-

trisch gekoppelt ist, und
eine zweite Reparaturverbindungsverdrahtung (16), die ein Ende, das mit der ersten Reparaturleitung (RL) gekoppelt ist, und ein anderes Ende, das davon isoliert ist, aufweist und konfiguriert ist, um mit einer zweiten Kurzschlussverdrahtung (17) im Nicht-Anzeigebereich (NA) elektrisch gekoppelt zu werden, wobei die zweite Kurzschlussverdrahtung mit der Dummy-Pixelschaltung (PCn+1) gekoppelt ist.

9. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 8, wobei die erste Reparaturverbindungsverdrahtung (13) und die zweite Reparaturverbindungsverdrahtung (16) auf einer selben Schicht wie eine erste leitfähige Schicht der Emissionspixelschaltung (PCi) sind und die erste Kurzschlussverdrahtung (14) und die zweite Kurzschlussverdrahtung (17) auf einer selben Schicht wie eine zweite leitfähige Schicht der Emissionspixelschaltung (PCi) sind.

10. Die organische lichtemittierende Anzeigevorrichtung nach einem der Ansprüche 1 bis 9, wobei die erste Reparaturverbindungsverdrahtung mit der ersten Kurzschlussverdrahtung gekoppelt ist und die zweite Reparaturverbindungsverdrahtung mit der zweiten Kurzschlussverdrahtung gekoppelt ist.

11. Die organische lichtemittierende Anzeigevorrichtung nach einem der Ansprüche 1 bis 10, wobei die erste und zweite Sub-Emissionsvorrichtung (SE1, SE2) derart voneinander getrennt sind, dass die erste Sub-Emissionsvorrichtung (SE1) mit der Dummy-Pixelschaltung (PCn+1) gekoppelt ist und von der Emissionspixelschaltung (PCi) getrennt ist und die zweite Sub-Emissionsvorrichtung (SE2) mit der Emissionspixelschaltung (PCi) gekoppelt ist und von der Dummy-Pixelschaltung (PCn+1) getrennt ist.

12. Die organische lichtemittierende Anzeigevorrichtung nach einem der Ansprüche 1 bis 11, wobei die Emissionspixelschaltung (E) aufweist:

einen ersten Transistor (TA1), der konfiguriert ist, um ein Datensignal in Reaktion auf ein Abtastsignal zu übertragen;
einen Kondensator (C1), der konfiguriert ist, um mit einer Spannung entsprechend dem Datensignal geladen zu werden; und
einen zweiten Transistor (TA2), der konfiguriert ist, um einen Ansteuerstrom entsprechend der im Kondensator geladenen Spannung zur Emissionsvorrichtung (E) zu übertragen.

13. Die organische lichtemittierende Anzeigevorrichtung nach einem der Ansprüche 1 bis 12, wobei die Emissionspixelschaltung (PCi) ferner aufweist:

einen ersten Transistor (TA1), der konfiguriert ist, um ein Datensignal von einer Datenleitung (DL) in Reaktion auf ein Abtastsignal zu empfangen;
einen zweiten Transistor (TA2), der konfiguriert ist, um einen Ansteuerstrom entsprechend dem Datensignal zur Emissionsvorrichtung (E) zu übertragen;
einen dritten Transistor (TA3), der konfiguriert ist, um den zweiten Transistor (TA1) als Diode zu schalten;
einen ersten Kondensator (C1), der konfiguriert ist, um mit einer Spannung entsprechend dem Datensignal geladen zu werden; und
einen zweiten Kondensator (C2), der mit einer Elektrode des ersten Kondensators (C1) und einer Gate-Elektrode des zweiten Transistors (TA2) verbunden ist.

14. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 13, wobei die Emissionspixelschaltung (PCi) ferner aufweist:

einen vierten Transistor (TA4), der zwischen den ersten Transistor (TA1) und die eine Elektrode des ersten Transistors (C1) geschaltet ist;
einen fünften Transistor (TA5), der zwischen die Datenleitung (DL) und die eine Elektrode des ersten Kondensators (C1) geschaltet ist; und
einen dritten Kondensator (C3), der eine Elektrode, die mit einem Knoten zwischen dem ersten Transistor (TA1) und dem vierten Transistor (TA4) verbunden ist, und eine weitere Elektrode, die mit einer Gate-Elektrode des fünften Transistors (TA5) verbunden ist, aufweist.

15. Die organische lichtemittierende Anzeigevorrichtung nach einem der Ansprüche 1 bis 11, wobei die Emissionspixelschaltung (PCi) ferner aufweist:

einen ersten Transistor (TA1), der konfiguriert ist, um ein Datensignal von einer Datenleitung (DL) in Reaktion auf ein Abtastsignal zu empfangen;
einen zweiten Transistor (TA2), der konfiguriert ist, um einen Ansteuerstrom entsprechend dem Datensignal zur Emissionsvorrichtung (PCi) zu übertragen;
einen dritten Transistor (TA3), der konfiguriert ist, um den zweiten Transistor (TA2) als Diode zu schalten;
einen vierten Transistor (TA4), der zwischen den ersten Transistor (TA1) und den zweiten Transistor (TA2) geschaltet ist;
einen fünften Transistor (TA5), der zwischen den zweiten Transistor (TA2) und die Emissionsvorrichtung (E) geschaltet ist,
einen sechsten Transistor (TA6), der zwischen

eine Gate-Elektrode des zweiten Transistors (TA2) und eine Anfangsleistung geschaltet ist;
einen ersten Kondensator (C1), der zwischen die Gate-Elektrode des zweiten Transistors (TA2) und eine erste Energiequelle geschaltet ist; und
einen zweiten Kondensator (C2), der eine Elektrode, die mit einem Knoten zwischen dem ersten Transistor (TA1) und dem vierten Transistor (TA4) verbunden ist, und eine weitere Elektrode, die mit einer zweiten Energiequelle verbunden ist, aufweist.

Revendications

1. Appareil d'affichage électroluminescent organique (100) comprenant :

un panneau d'affichage (10a, 10b, 10c) qui comprend une pluralité de pixels (P), une unité de commande de balayage (20), une unité de commande de données (30) et une unité de contrôle (40), dans lequel une pluralité de n lignes de balayage (SL), n étant un nombre entier naturel, s'étendant dans une direction horizontale, et une pluralité des lignes de données (DL) s'étendant dans une direction verticale et croisant perpendiculairement les lignes de balayage (SL) sont formées sur le panneau d'affichage (10), dans lequel une pluralité de lignes de réparation (RL) s'étendant parallèlement aux et espacées des lignes de données (DL) et croisant perpendiculairement les lignes de balayage (SL) sont formées sur le panneau d'affichage (10), et la pluralité de pixels (P) alignés en une forme semblable à une matrice sont formés là où les lignes de balayage (SL), les lignes de données (DL) et les lignes de réparation (RL) se croisent, dans lequel au moins une ligne de réparation est formée dans chaque colonne de pixels,
dans lequel la pluralité de pixels (P) comprend une pluralité de pixels d'émission (EP) dans une zone d'affichage (AA), chaque pixel d'émission (EP) comprenant un dispositif d'émission (E) qui comprend un circuit de pixel d'émission (PCi) couplé au et configuré pour fournir un courant de commande au dispositif d'émission (E), et
une rangée de pixels fictifs (DP), comprenant chacun un circuit de pixel fictif (PCn+1), formée dans une zone de non-affichage (NA) sur les régions supérieure et/ou inférieure de la zone d'affichage (AA), les circuits de pixels fictifs (PCn+1) de la rangée étant connectés à une ligne de balayage supplémentaire (SL), où chacune de la pluralité de lignes de réparation (RL) est configurée pour être couplée électriquement à l'un des dispositifs d'émission (E) ayant un circuit de pixel d'émission défectueux (PCi) et à un circuit de pixel fictif (PCn+1) dans la même colonne, et
dans lequel l'unité de commande de balayage (20) est configurée pour fournir, ou activer, séquentiellement des premier à nième signaux de balayage (S1 à Sn) aux première à nième lignes de balayage (SL1 à SLn) et pour fournir un signal de balayage supplémentaire (Sn+1 à (n+1)ème) à la ligne de balayage supplémentaire (SLn+1) simultanément à la fourniture du signal de balayage (Si) à la ligne de balayage (SL) connectée au circuit de pixel d'émission défectueux (PCi), et
dans lequel l'unité de commande de données (30) est configurée pour fournir, ou activer, séquentiellement des premier à nième signaux de données (D1 à Dn) à la ligne de données (DL1) connectée au circuit de pixel d'émission défectueux (PCi) en synchronisation avec les signaux de balayage (S1 à Sn+1), où un signal de données (Di) qui est le même que le signal de données (Di) fourni au circuit de pixel d'émission défectueux (PCi) est fourni simultanément au circuit de pixel fictif (PCn+1).

2. Appareil d'affichage électroluminescent organique selon la revendication 1, dans lequel le dispositif d'émission (E) comprend un premier dispositif d'émission secondaire (SE1) et un deuxième dispositif d'émission secondaire (SE2), dans lequel le premier dispositif d'émission secondaire (SE1) comprend une première électrode inférieure, une électrode supérieure (AD1) faisant face à la première électrode inférieure, et une première couche d'émission entre la première électrode inférieure et l'électrode supérieure (AD1) ; et le deuxième dispositif d'émission secondaire (SE2) comprend une deuxième électrode inférieure, l'électrode supérieure (AD2) faisant face à la deuxième électrode inférieure, et une deuxième couche d'émission entre la deuxième électrode inférieure et l'électrode supérieure (AD2), la première électrode inférieure et la deuxième électrode inférieure étant couplées l'une à l'autre par un câblage de connexion d'électrodes (11).

3. Appareil d'affichage électroluminescent organique selon la revendication 2, dans lequel le câblage de connexion d'électrodes (11) comprend au moins l'un d'un métal, d'un silicium amorphe, d'un silicium cristallin et d'un semi-conducteur à oxyde.

4. Appareil d'affichage électroluminescent organique selon la revendication 2 ou 3, dans lequel le câblage de connexion d'électrodes (11) est au niveau d'une même couche et en un même matériau qu'une couche active du circuit de pixel d'émission (PCi).

5. Appareil d'affichage électroluminescent organique selon la revendication 2 ou 3, dans lequel le câblage de connexion d'électrodes (11) est formé d'un seul tenant avec la pluralité d'électrodes inférieures séparées.

6. Appareil d'affichage électroluminescent organique selon la revendication 2, dans lequel le câblage de connexion d'électrodes comprend :

une première unité de connexion (CU1) couplée à la première électrode inférieure ;
une deuxième unité de connexion (CU2) couplée à la deuxième électrode inférieure ;
une troisième unité de connexion (CU3) couplée au circuit de pixel d'émission ;
un premier noeud (CN1) entre la première unité de connexion (CU1) et la troisième unité de connexion (CU3) et configuré pour être coupé pour isoler électriquement le premier dispositif d'émission secondaire (SE1) du circuit de pixel d'émission (PCi) ; et
un deuxième noeud (CN2) entre la deuxième unité de connexion (CU2) et la troisième unité de connexion (CU3) et configuré pour être coupé pour isoler électriquement le deuxième dispositif d'émission secondaire (SE2) du circuit de pixel d'émission (PCi).

7. Appareil d'affichage électroluminescent organique selon la revendication 6, comprenant en outre :
au moins un câblage de circuit (15) ayant une extrémité couplée au circuit de pixel d'émission (PCi) et une autre extrémité couplée à la deuxième unité de connexion (CU2), ledit au moins un câblage de circuit étant configuré pour être coupé pour isoler électriquement le circuit de pixel d'émission (PCi) du dispositif d'émission (E).

8. Appareil d'affichage électroluminescent organique selon la revendication 6 ou 7, comprenant en outre :

un premier câblage de connexion de réparation (13) ayant une extrémité couplée à la ligne de réparation (RL) et une autre extrémité isolée de et configurée pour être couplée électriquement à un premier câblage de court-circuit (14), dans la zone d'affichage (AA), le premier câblage de court-circuit étant couplé électriquement au dispositif d'émission (E), et
un deuxième câblage de connexion de réparation (16) ayant une extrémité couplée à la première ligne de réparation (RL) et une autre extrémité isolée de et configurée pour être couplée électriquement à un deuxième câblage de court-circuit (17), dans la région de non-affichage (NA), le deuxième câblage de court-circuit étant couplé au circuit de pixel fictif (PCn+1).

9. Appareil d'affichage électroluminescent organique selon la revendication 8, dans lequel le premier câblage de connexion de réparation (13) et le deuxième câblage de connexion de réparation (16) sont au niveau d'une même couche qu'une première couche conductrice du circuit de pixel d'émission (PCi) et le premier câblage de court-circuit (14) et le deuxième câblage de court-circuit (17) sont au niveau d'une même couche qu'une deuxième couche conductrice du circuit de pixel d'émission (PCi).

10. Appareil d'affichage électroluminescent organique selon l'une des revendications 1 à 9, dans lequel le premier câblage de connexion de réparation est couplé au premier câblage de court-circuit, et le deuxième câblage de connexion de réparation est couplé au deuxième câblage de court-circuit.

11. Appareil d'affichage électroluminescent organique selon l'une des revendications 1 à 10, dans lequel les premier et deuxième dispositifs d'émission secondaire (SE1, SE2) sont séparés l'un de l'autre de sorte que le premier dispositif d'émission secondaire (SE1) est couplé au circuit de pixel fictif (PCn+1) et séparé du circuit de pixel d'émission (PCi), et le deuxième dispositif d'émission secondaire (SE2) est couplé au circuit de pixel d'émission (PCi) et séparé du circuit de pixel fictif (PCn+1).

12. Appareil d'affichage électroluminescent organique selon l'une des revendications 1 à 11, dans lequel le circuit de pixel d'émission (E) comprend :

un premier transistor (TA1) configuré pour transférer un signal de données en réponse à un signal de balayage ;
un condensateur (C1) configuré pour être chargé avec une tension correspondant au signal de données ; et
un deuxième transistor (TA2) configuré pour transférer un courant de commande correspondant à la tension chargée dans le condensateur au dispositif d'émission (E).

13. Appareil d'affichage électroluminescent organique selon l'une des revendications 1 à 12, dans lequel le circuit de pixel d'émission (PCi) comprend en outre :

un premier transistor (TA1) configuré pour recevoir un signal de données provenant d'une ligne de données (DL) en réponse à un signal de balayage ;
un deuxième transistor (TA2) configuré pour transférer un courant de commande correspondant au signal de données au dispositif d'émission (E) ;
un troisième transistor (TA3) configuré pour

connecter en diode le deuxième transistor (TA1) ;
un premier condensateur (C1) configuré pour être chargé avec une tension correspondant au signal de données ; et
un deuxième condensateur (C2) connecté à une électrode du premier condensateur (C1) et à une électrode de grille du deuxième transistor (TA2).

14. Appareil d'affichage électroluminescent organique selon la revendication 13, dans lequel le circuit de pixel d'émission (PCi) comprend en outre :

un quatrième transistor (TA4) connecté entre le premier transistor (TA1) et ladite une électrode du premier condensateur (C1) ;
un cinquième transistor (TA5) connecté entre la ligne de données (DL) et ladite une électrode du premier condensateur (C1) ; et
un troisième condensateur (C3) ayant une électrode connectée à un noeud entre le premier transistor (TA1) et le quatrième transistor (TA4) et une autre électrode connectée à une électrode de grille du cinquième transistor (TA5).

15. Appareil d'affichage électroluminescent organique selon l'une des revendications 1 à 11, dans lequel le circuit de pixel d'émission (PCi) comprend en outre :

un premier transistor (TA1) configuré pour recevoir un signal de données provenant d'une ligne de données (DL) en réponse à un signal de balayage ;
un deuxième transistor (TA2) configuré pour transférer un courant de commande correspondant au signal de données au dispositif d'émission (PCi) ;
un troisième transistor (TA3) configuré pour connecter en diode le deuxième transistor (TA2) ;
un quatrième transistor (TA4) connecté entre le premier transistor (TA1) et le deuxième transistor (TA2) ;
un cinquième transistor (TA5) connecté entre le deuxième transistor (TA2) et le dispositif d'émission (E) ;
un sixième transistor (TA6) connecté entre une électrode de grille du deuxième transistor (TA2) et une alimentation initiale ;
un premier condensateur (C1) connecté entre l'électrode de grille du deuxième transistor (TA2) et une première source de puissance ; et
un deuxième condensateur (C2) ayant une électrode connectée à un noeud entre le premier transistor (TA1) et le quatrième transistor (TA4) et une autre électrode connectée à une deuxième source de puissance.

FIG. 1

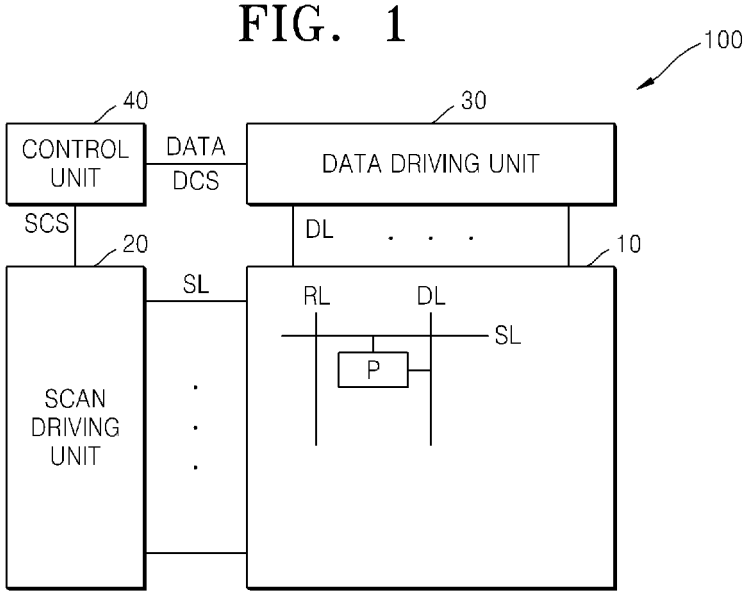

100
40
30
CONTROL UNIT
DATA
DCS
DATA DRIVING UNIT
SCS
DL
20
10
SL
RL
DL
SL
P
SCAN DRIVING UNIT

FIG. 2

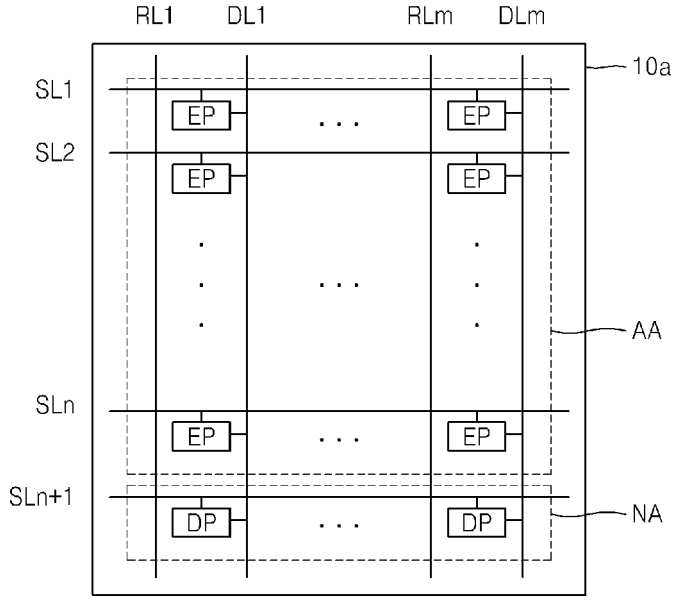

RL1
DL1
RLm
DLm
10a
SL1
SL2
SLn
SLn+1
EP
DP
AA
NA

FIG. 3

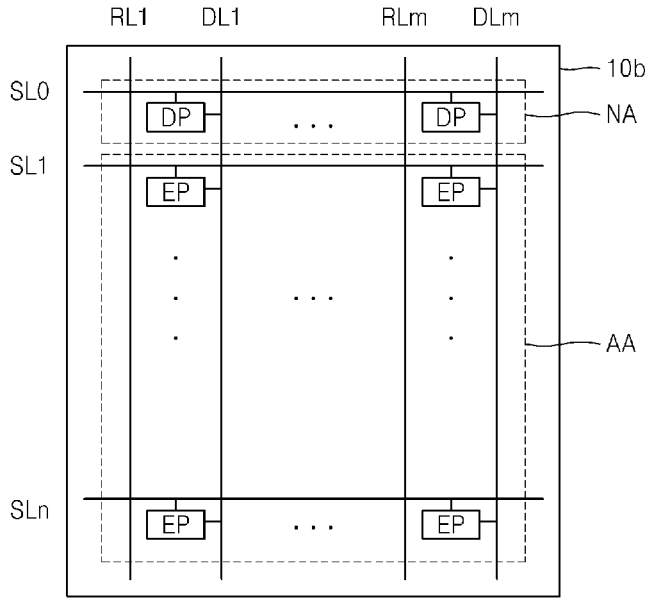

RL1
DL1
RLm
DLm
SL0
SL1
SLn
DP
EP
10b
NA
AA

FIG. 4

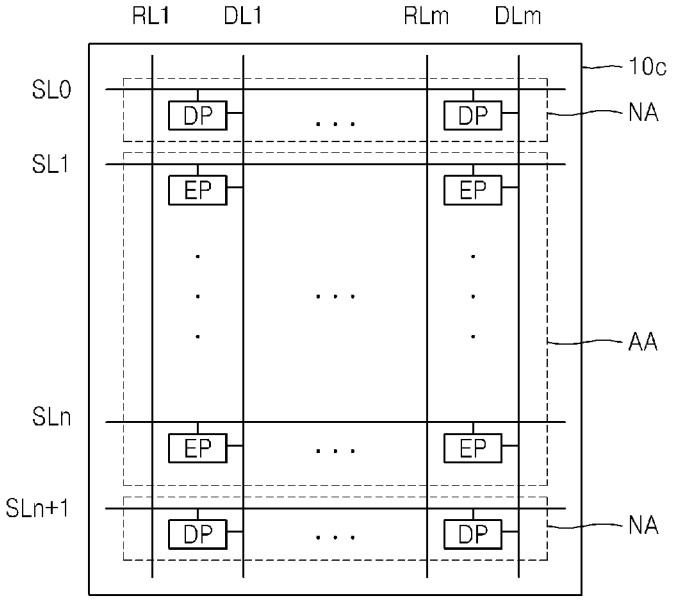

RL1
DL1
RLm
DLm
SL0
SL1
SLn
SLn+1
DP
EP
10c
NA
AA

FIG. 5

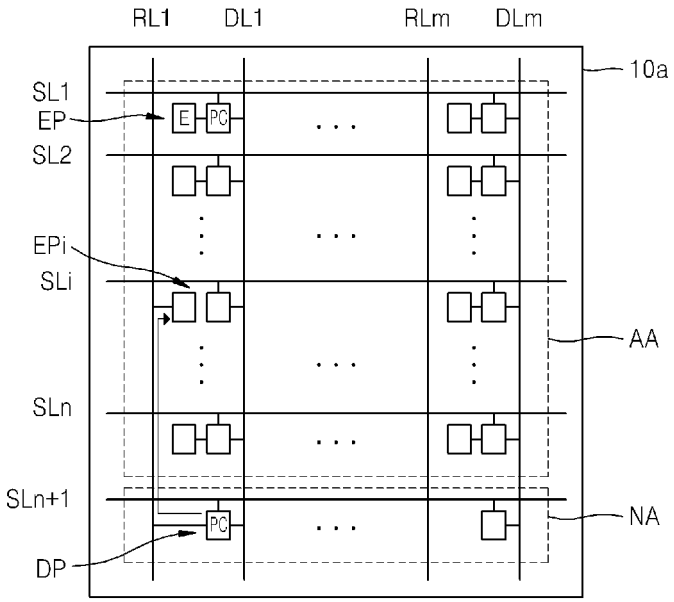

RL1
DL1
RLm
DLm
10a
SL1
EP
E
PC
SL2
EPi
SLi
AA
SLn
SLn+1
NA
PC
DP

FIG. 6

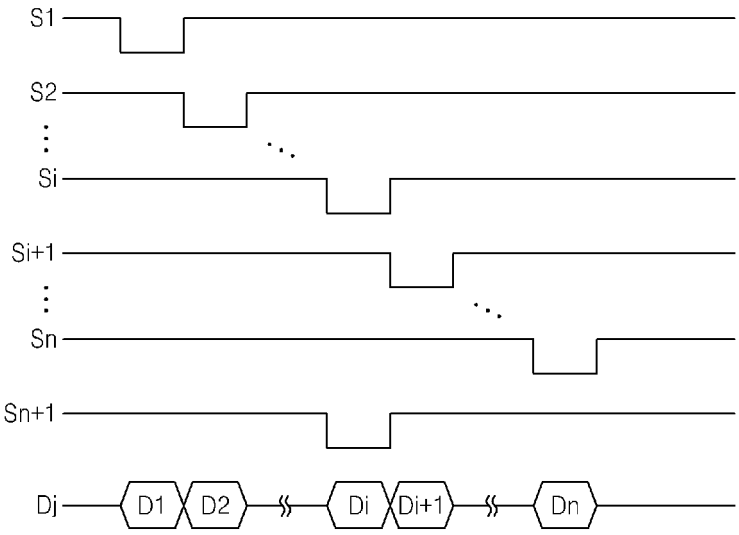

S1
S2
Si
Si+1
Sn
Sn+1
Dj
D1
D2
Di
Di+1
Dn

FIG. 7

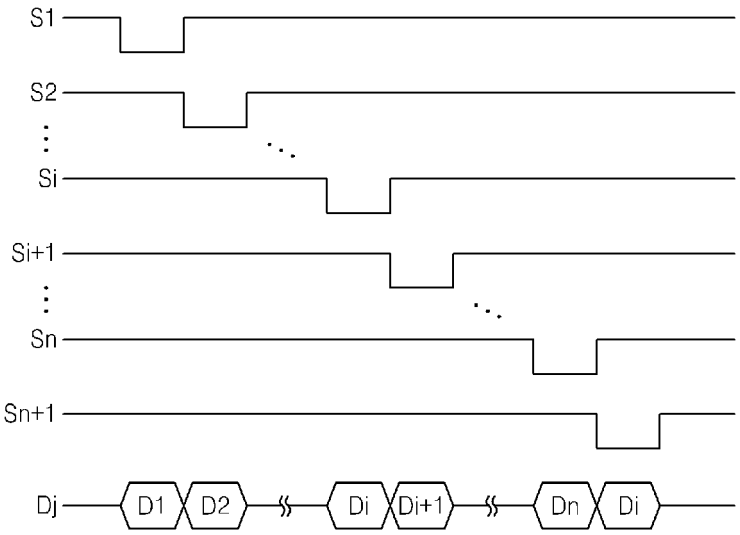

S1
S2
Si
Si+1
Sn
Sn+1
Dj
D1
D2
Di
Di+1
Dn
Di

FIG. 8

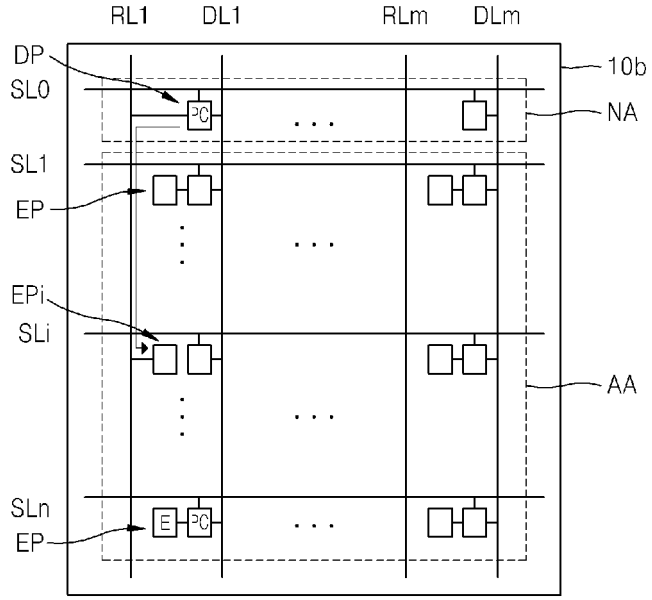

RL1
DL1
RLm
DLm
DP
SL0
SL1
EP
EPi
SLi
SLn
EP
10b
NA
AA

FIG. 9

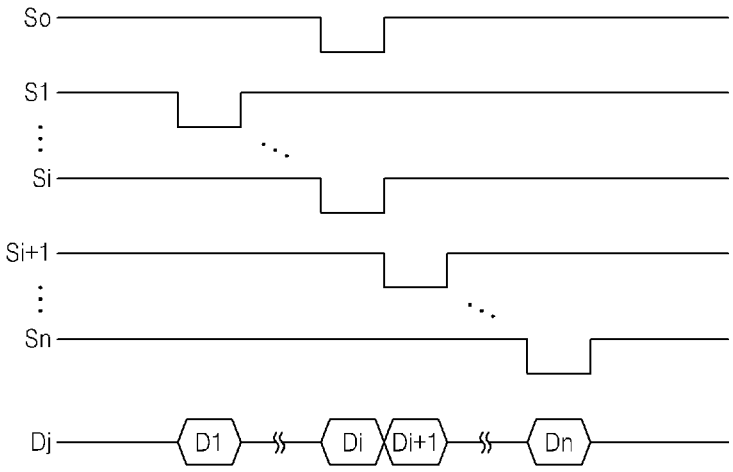


FIG. 10

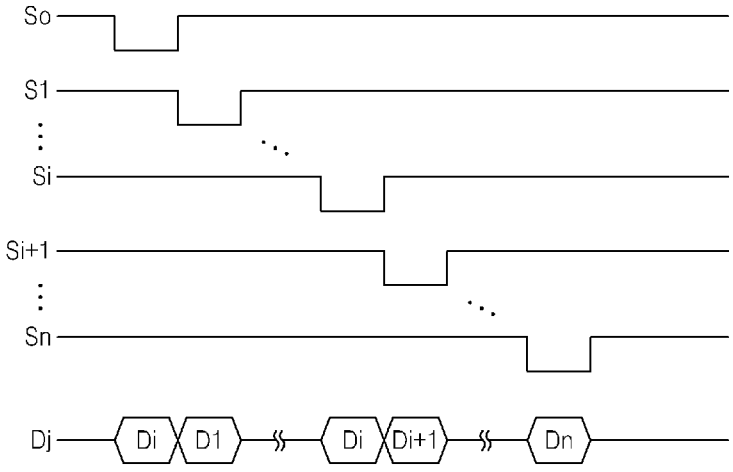


FIG. 11

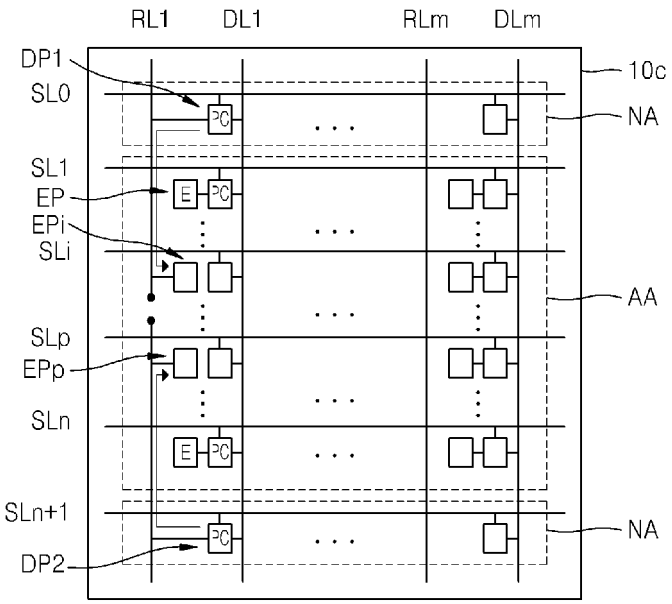

RL1
DL1
RLm
DLm
DP1
SL0
SL1
EP
EPi
SLi
SLp
EPp
SLn
SLn+1
DP2
10c
NA
AA
NA

FIG. 12

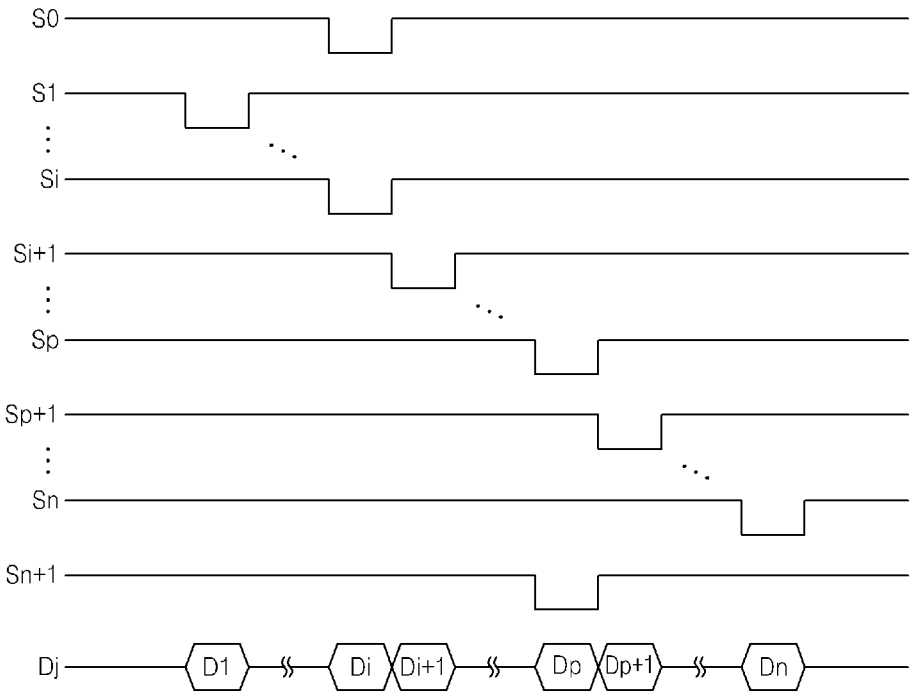


FIG. 13

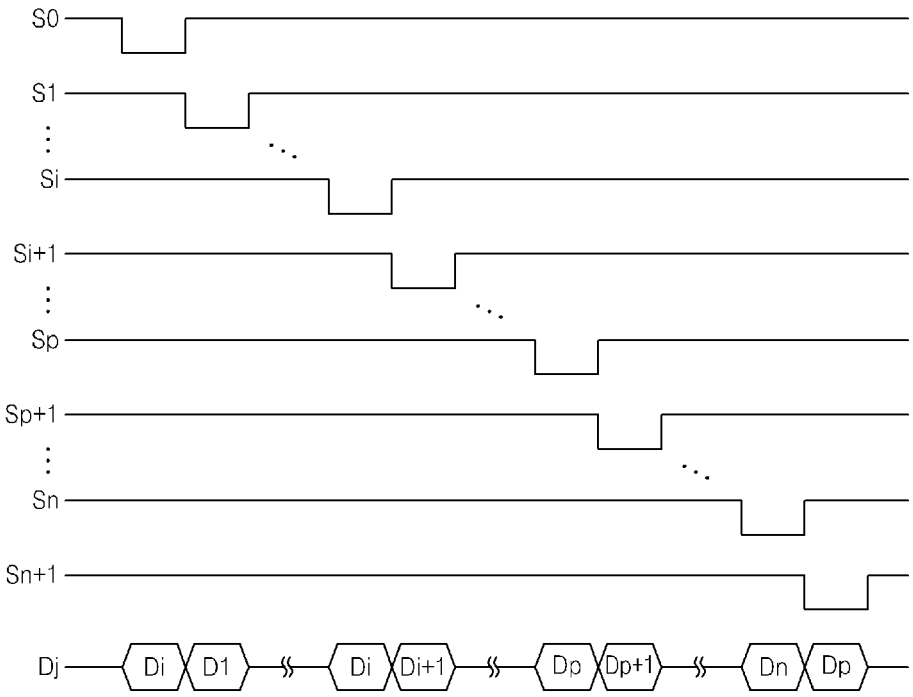


FIG. 14

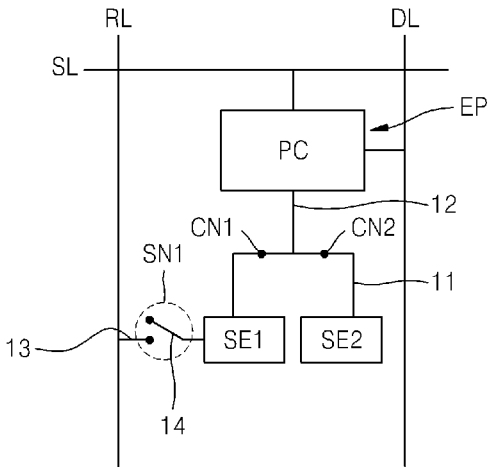


FIG. 15

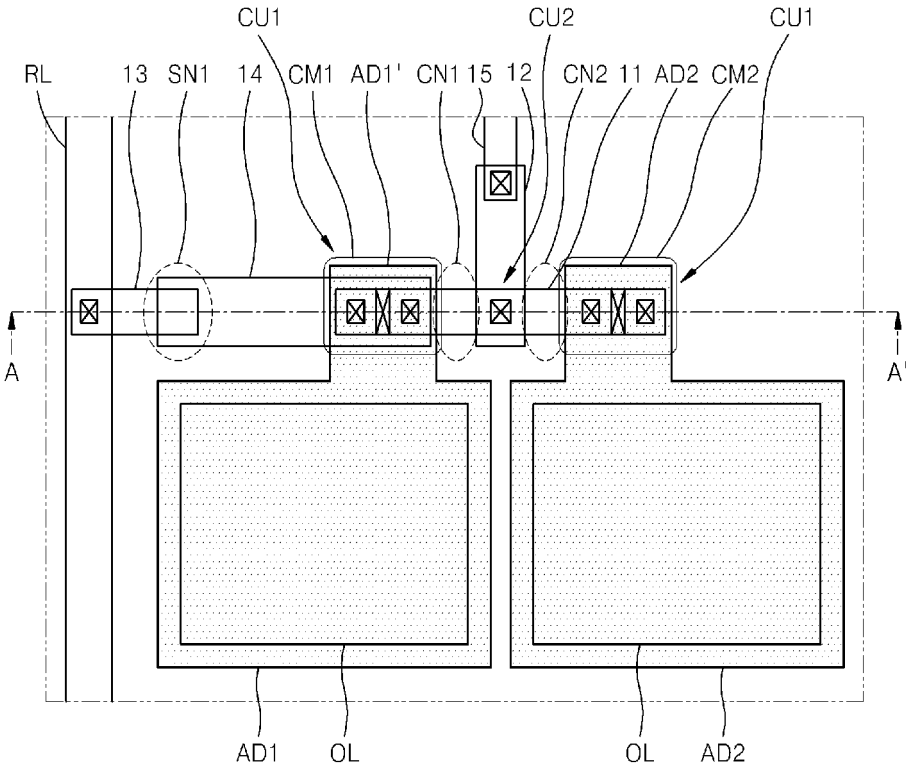

CU1
CU2
CU1
RL
13
SN1
14
CM1
AD1'
CN1
15
12
CN2
11
AD2
CM2
A
A'
AD1
OL
OL
AD2

FIG. 16

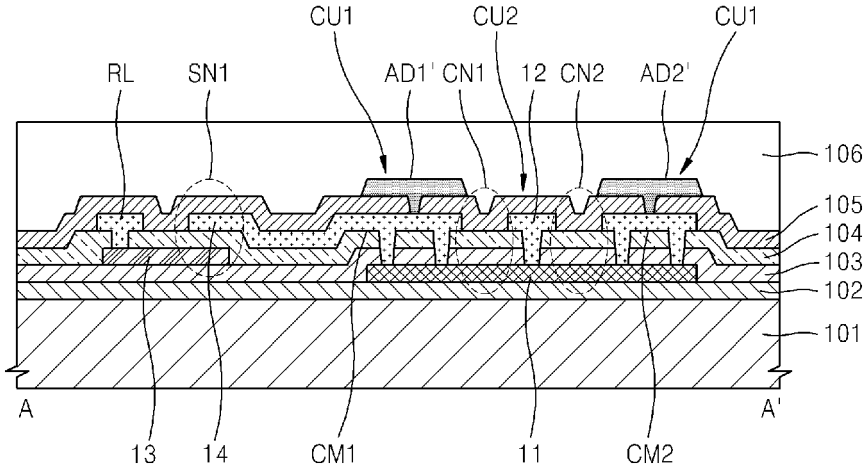

CU1
CU2
CU1
RL
SN1
AD1'
CN1
12
CN2
AD2'
106
105
104
103
102
101
A
A'
13
14
CM1
11
CM2

FIG. 17

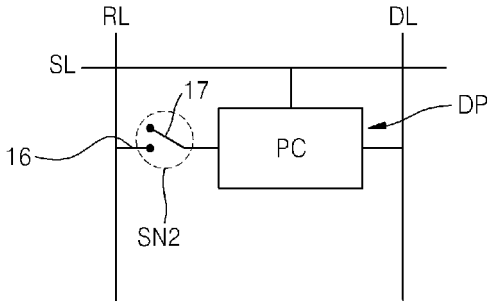


FIG. 18

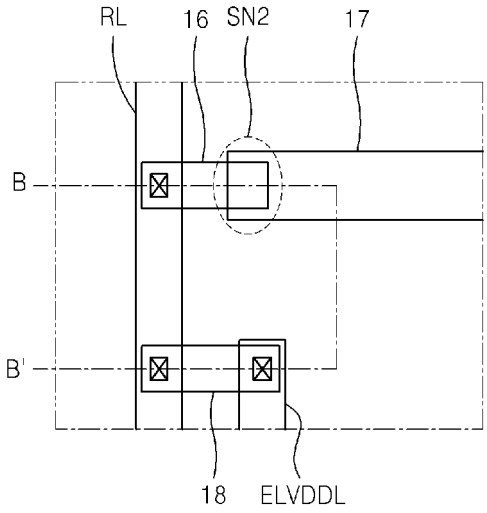

RL
16
SN2
17
B
B'
18
ELVDDL

FIG. 19

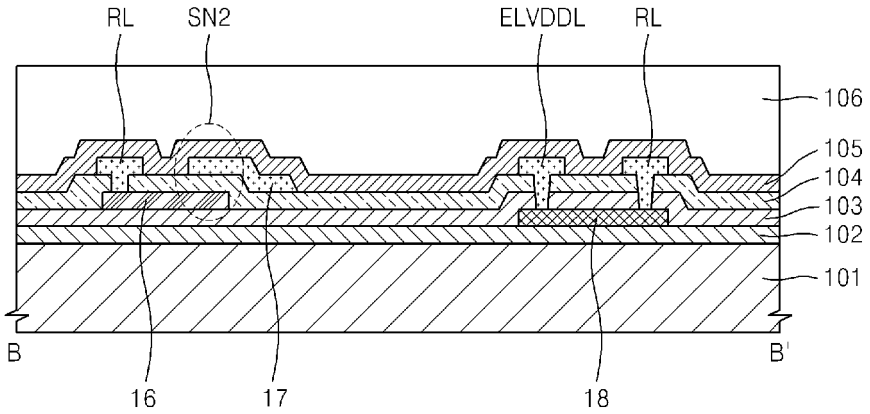

RL
SN2
ELVDDL
RL
106
105
104
103
102
101
B
B'
16
17
18

FIG. 20

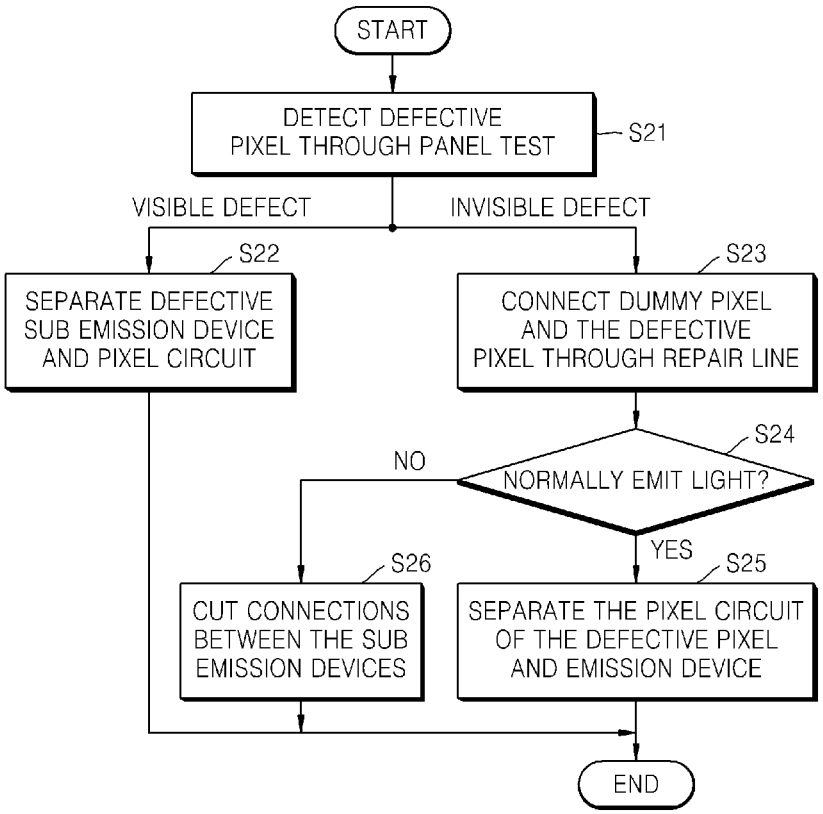

START
DETECT DEFECTIVE PIXEL THROUGH PANEL TEST
S21
VISIBLE DEFECT
INVISIBLE DEFECT
S22
SEPARATE DEFECTIVE SUB EMISSION DEVICE AND PIXEL CIRCUIT
S23
CONNECT DUMMY PIXEL AND THE DEFECTIVE PIXEL THROUGH REPAIR LINE
S24
NORMALLY EMIT LIGHT?
NO
YES
S26
CUT CONNECTIONS BETWEEN THE SUB EMISSION DEVICES
S25
SEPARATE THE PIXEL CIRCUIT OF THE DEFECTIVE PIXEL AND EMISSION DEVICE
END

FIG. 21

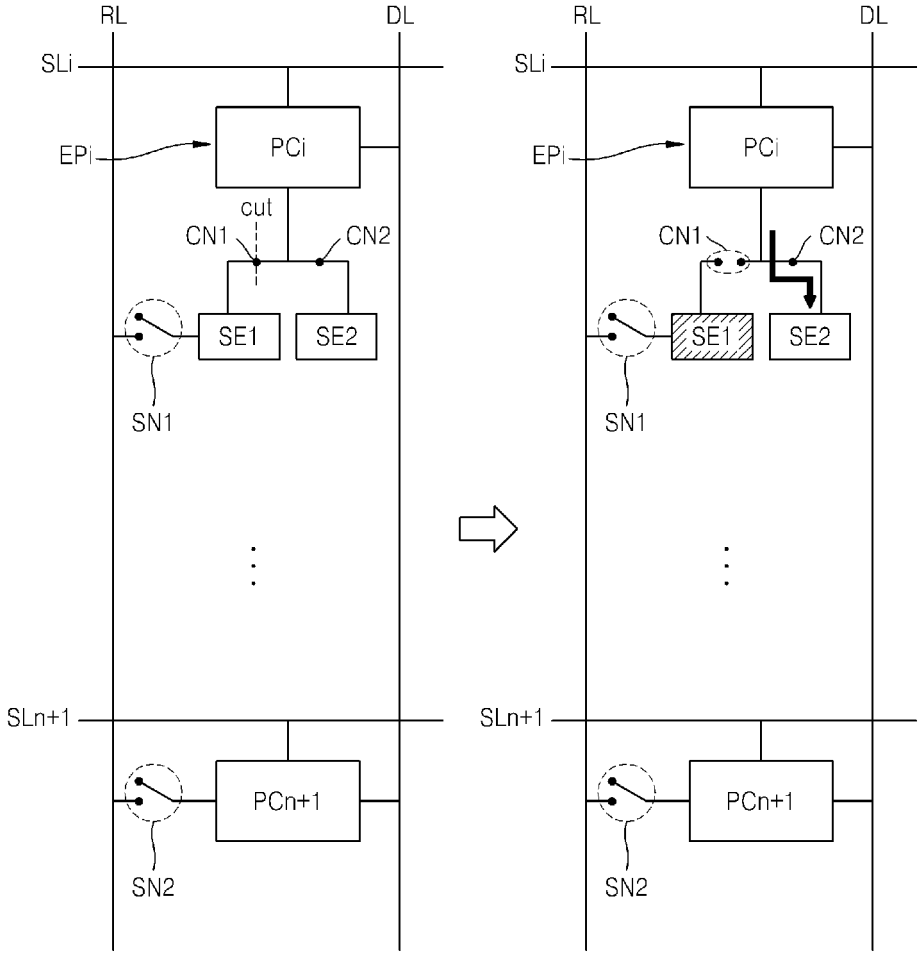


FIG. 22

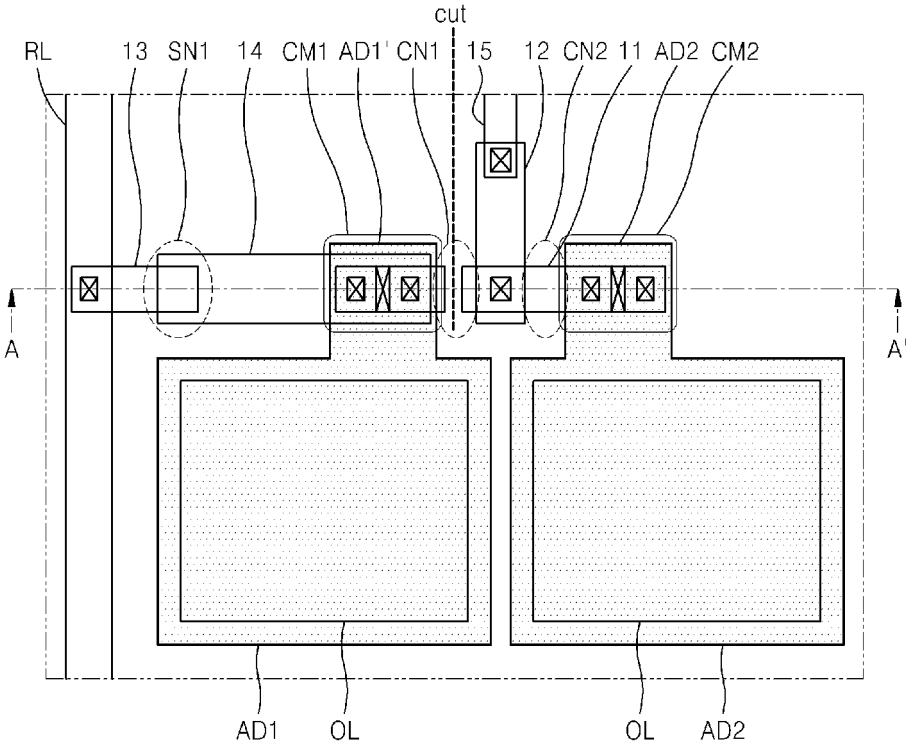

cut
RL
13
SN1
14
CM1
AD1'
CN1
15
12
CN2
11
AD2
CM2
A
A'
AD1
OL
OL
AD2

FIG. 23

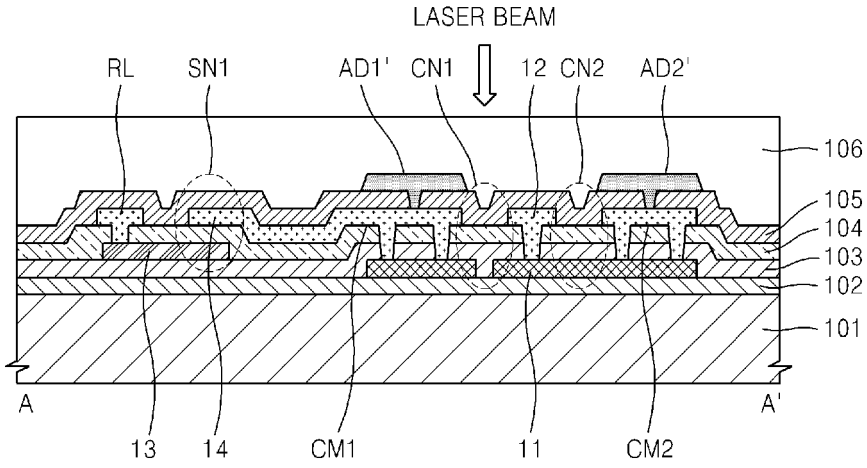

LASER BEAM
RL
SN1
AD1'
CN1
12
CN2
AD2'
106
105
104
103
102
101
A
A'
13
14
CM1
11
CM2

FIG. 24

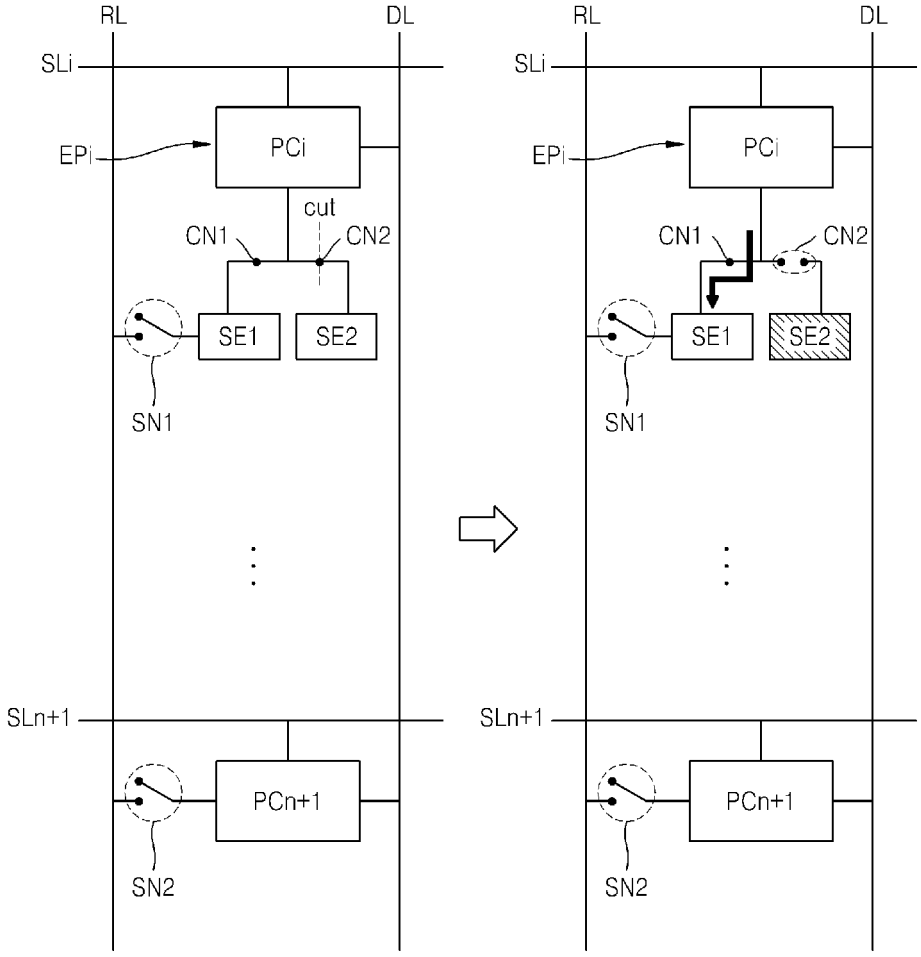


FIG. 25

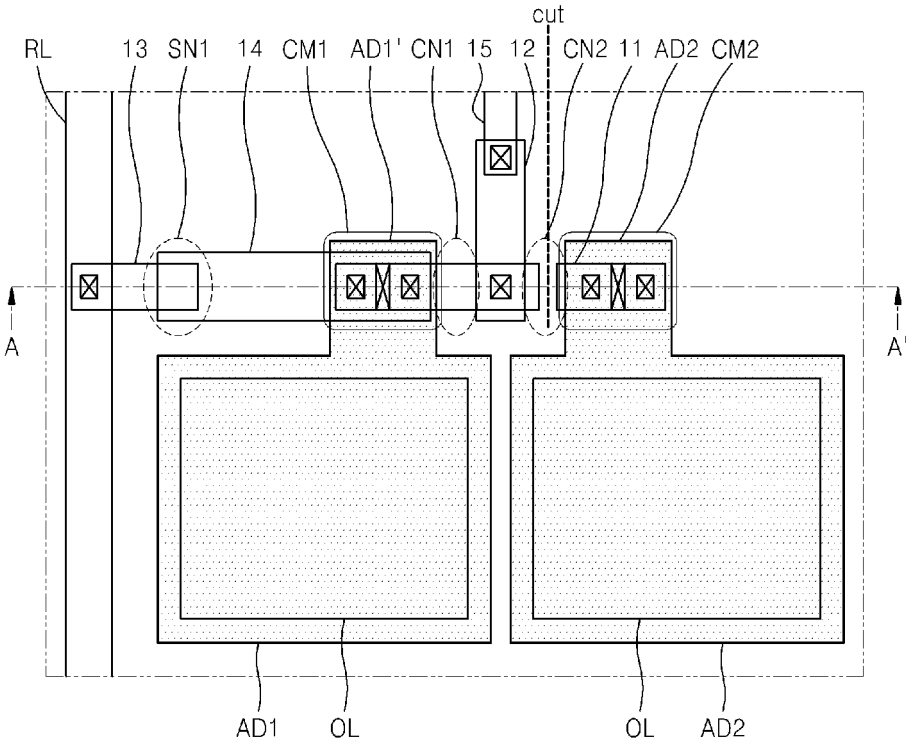

cut
RL
13
SN1
14
CM1
AD1'
CN1
15
12
CN2
11
AD2
CM2
A
A'
AD1
OL
OL
AD2

FIG. 26

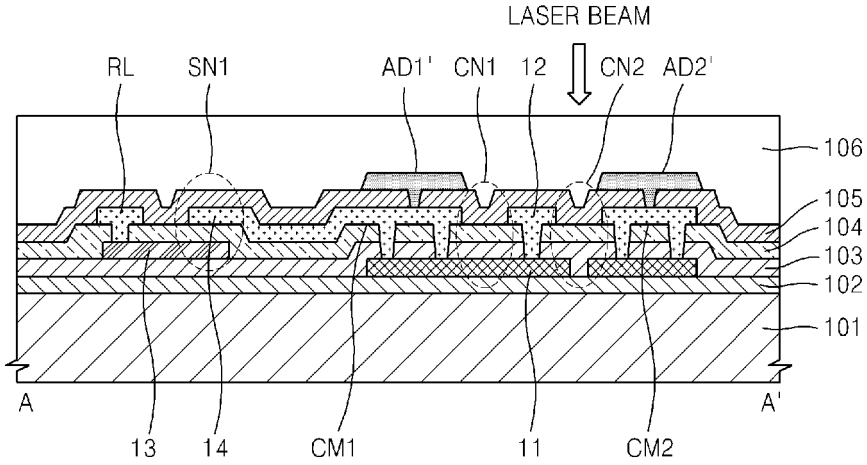

LASER BEAM
RL
SN1
AD1'
CN1
12
CN2
AD2'
106
105
104
103
102
101
A
A'
13
14
CM1
11
CM2

FIG. 27

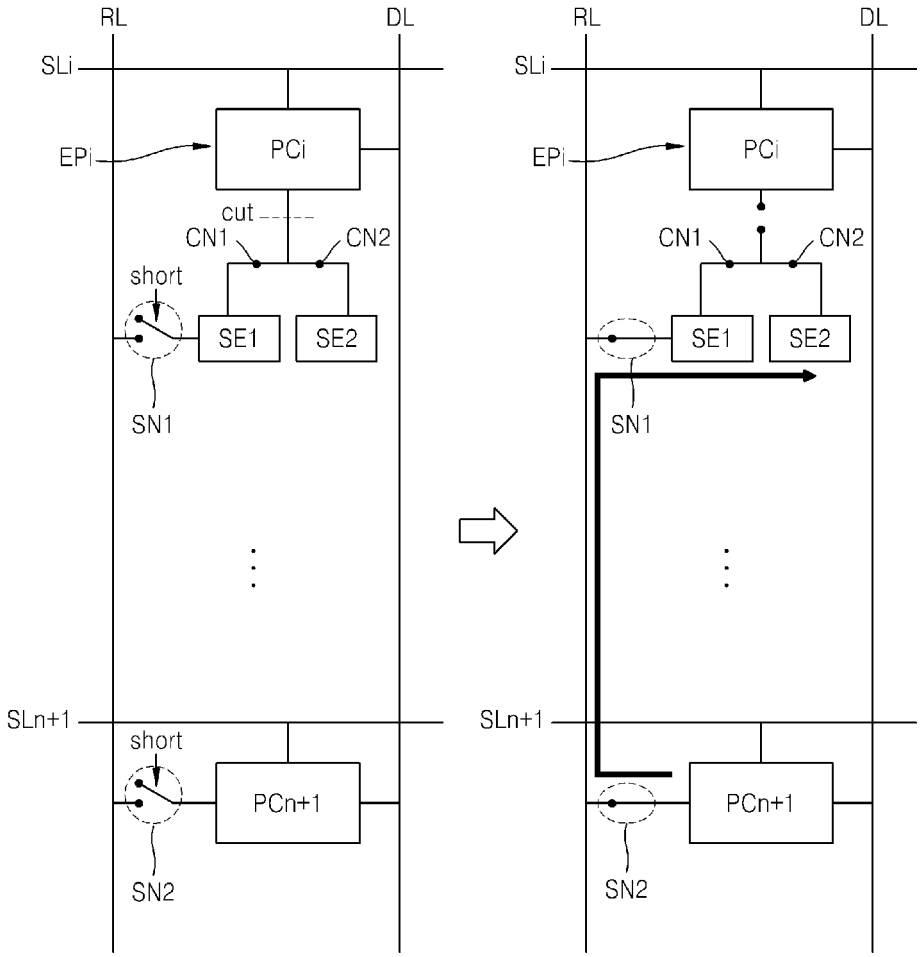

RL
DL
SLi
EPi
PCi
cut
CN1
CN2
short
SE1
SE2
SN1
SLn+1
short
PCn+1
SN2
RL
DL
SLi
EPi
PCi
CN1
CN2
SE1
SE2
SN1
SLn+1
PCn+1
SN2

FIG. 28A

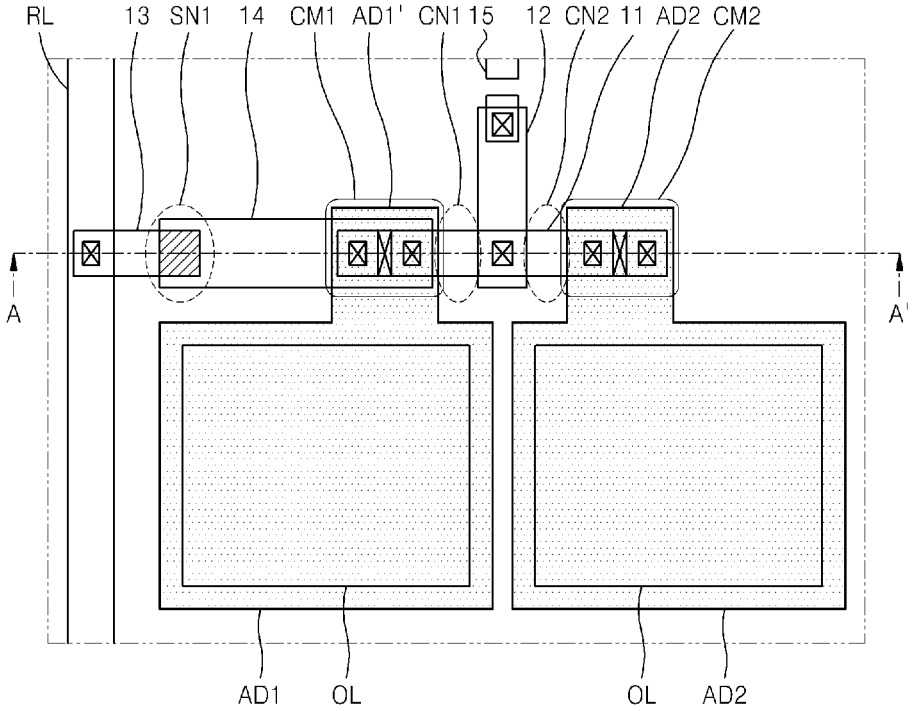


FIG. 28B

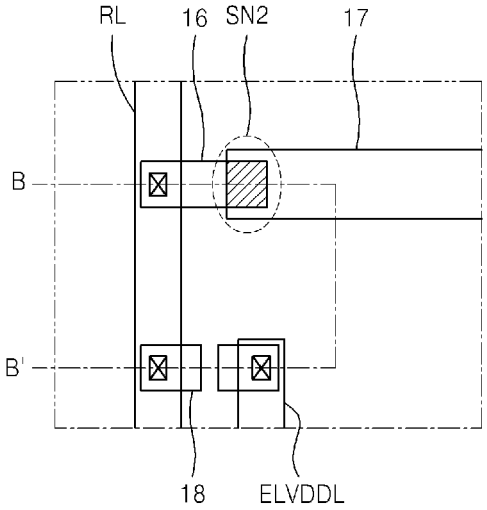


FIG. 29A

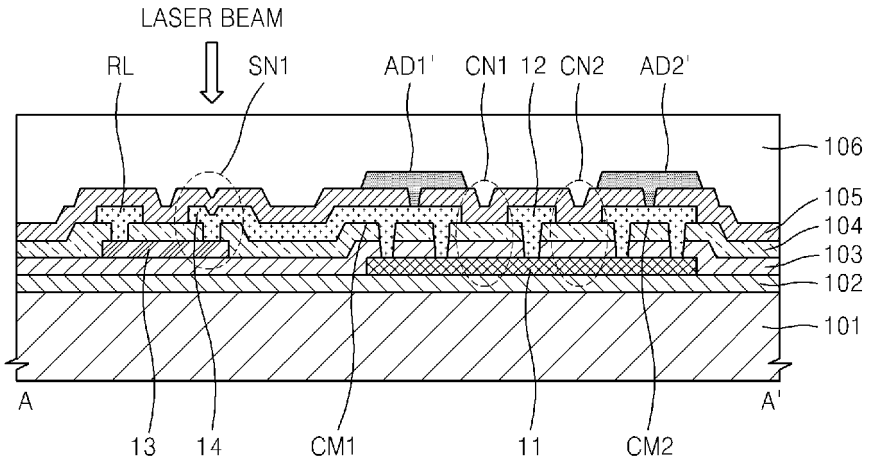


FIG. 29B

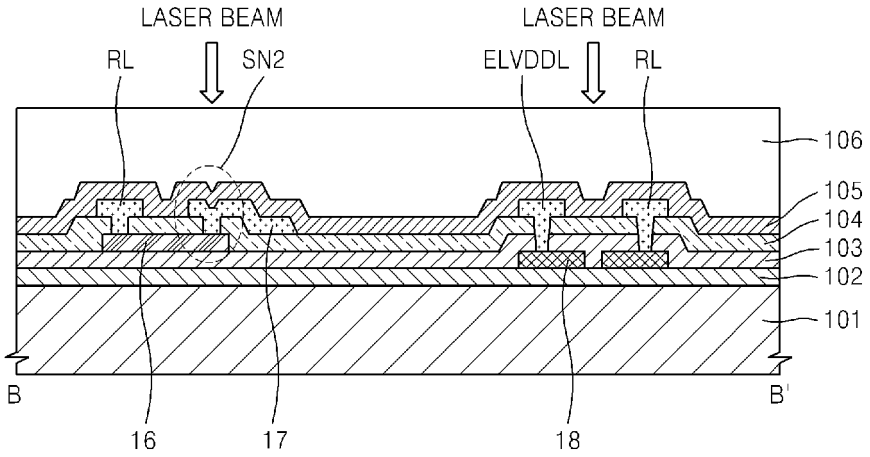


FIG. 30A

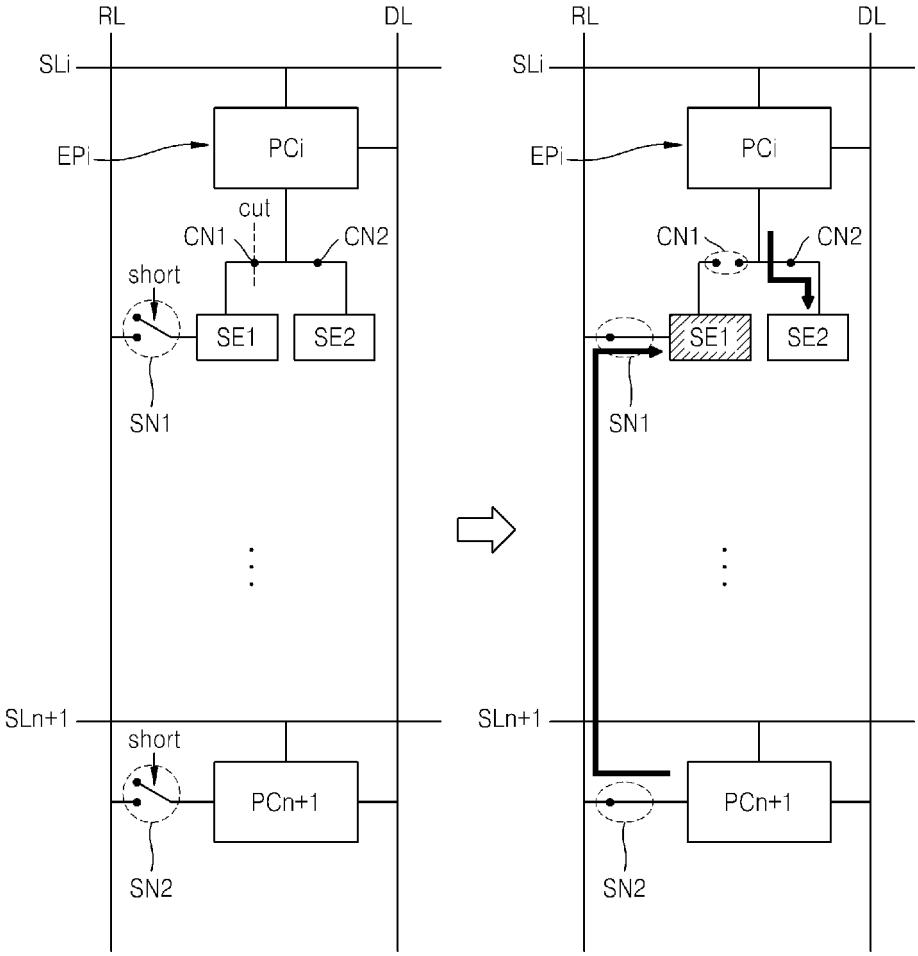

RL
DL
SLi
EPi
PCi
cut
CN1
CN2
short
SE1
SE2
SN1
SLn+1
short
PCn+1
SN2
RL
DL
SLi
EPi
PCi
CN1
CN2
SE1
SE2
SN1
SLn+1
PCn+1
SN2

FIG. 30B

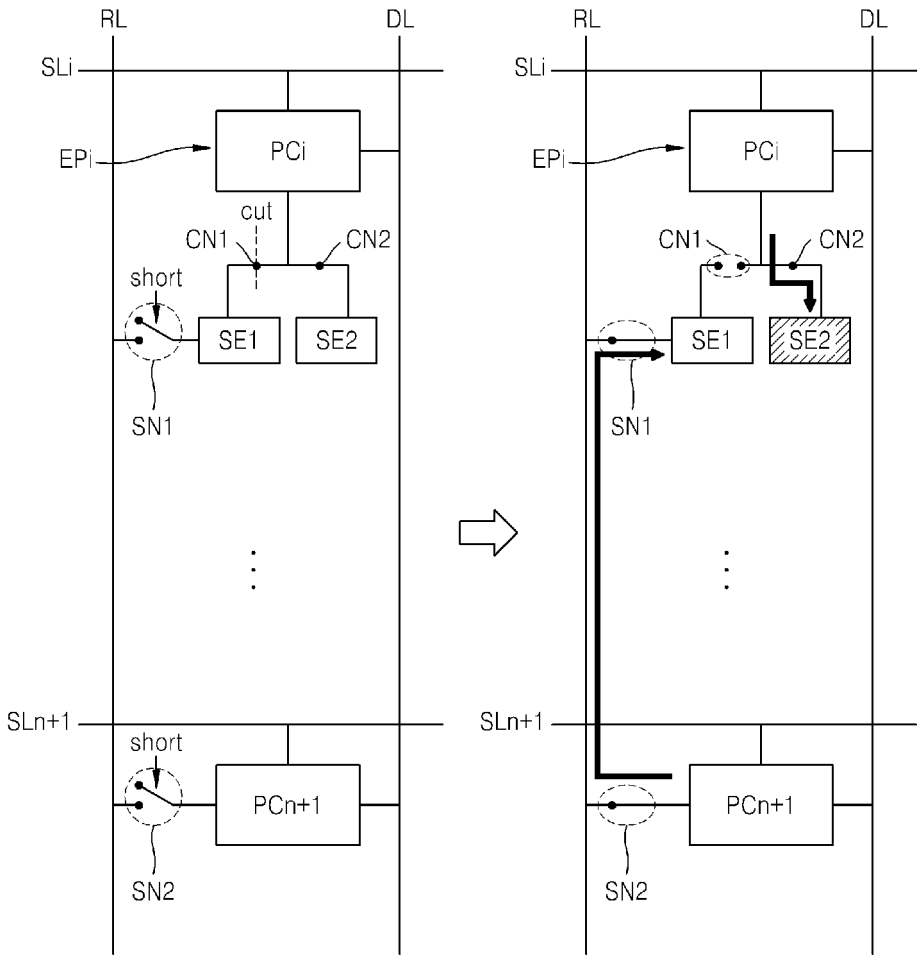

RL
DL
SLi
EPi
PCi
cut
CN1
CN2
short
SE1
SE2
SN1
SLn+1
short
PCn+1
SN2
RL
DL
SLi
EPi
PCi
CN1
CN2
SE1
SE2
SN1
SLn+1
PCn+1
SN2

FIG. 31

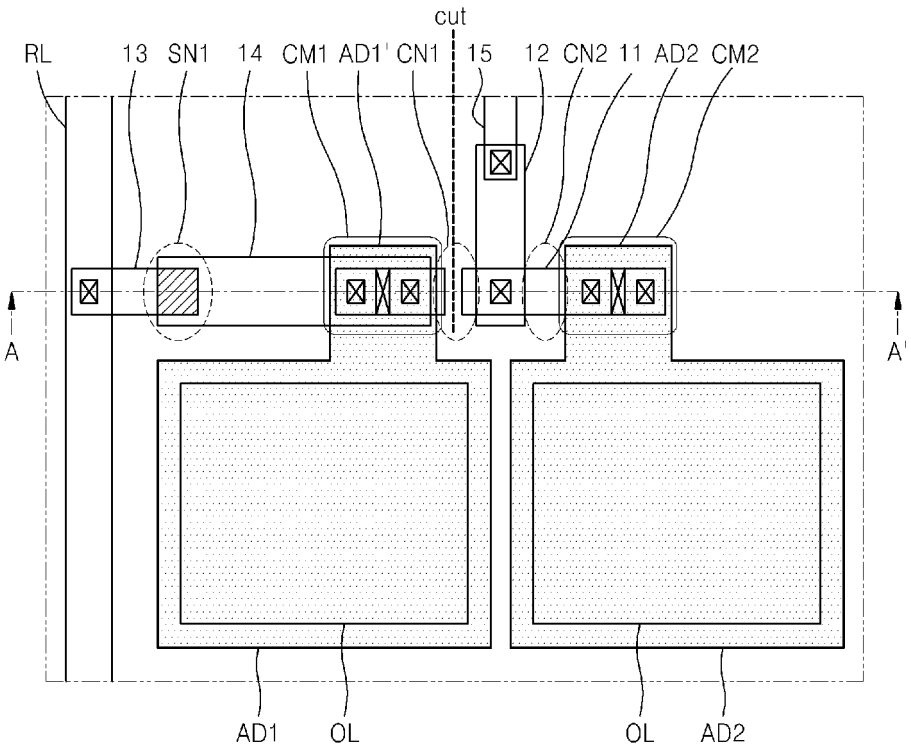

cut
RL
13
SN1
14
CM1
AD1'
CN1
15
12
CN2
11
AD2
CM2
A
A'
AD1
OL
OL
AD2

FIG. 32

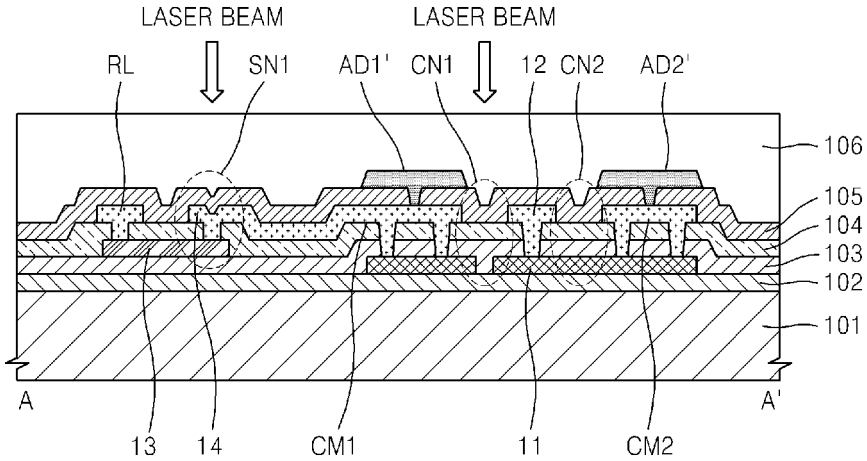

LASER BEAM
LASER BEAM
RL
SN1
AD1'
CN1
12
CN2
AD2'
106
105
104
103
102
101
A
A'
13
14
CM1
11
CM2

FIG. 33

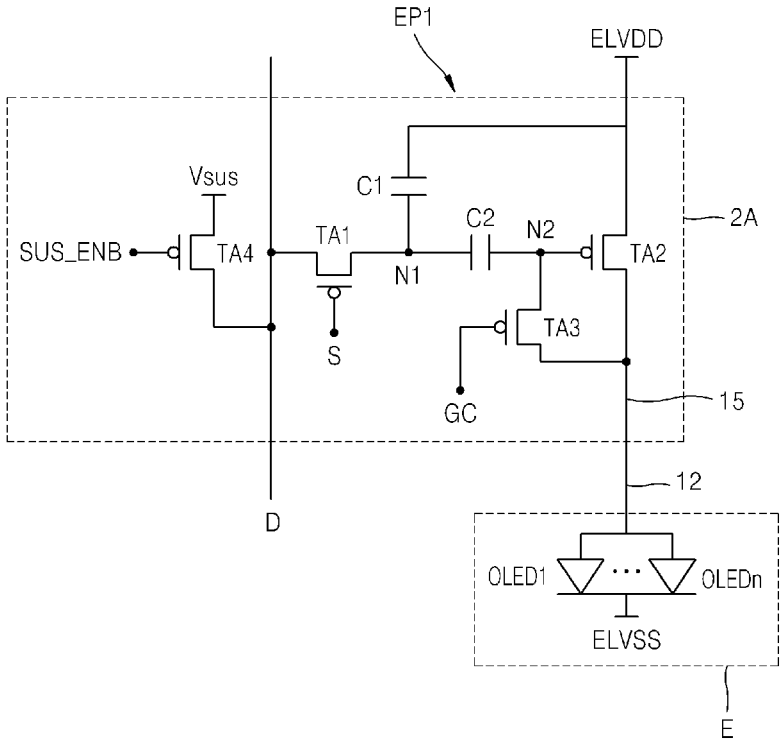

EP1
ELVDD
Vsus
C1
C2
N2
2A
SUS_ENB
TA4
TA1
N1
TA2
TA3
S
GC
15
12
D
OLED1
OLEDn
ELVSS
E

FIG. 34

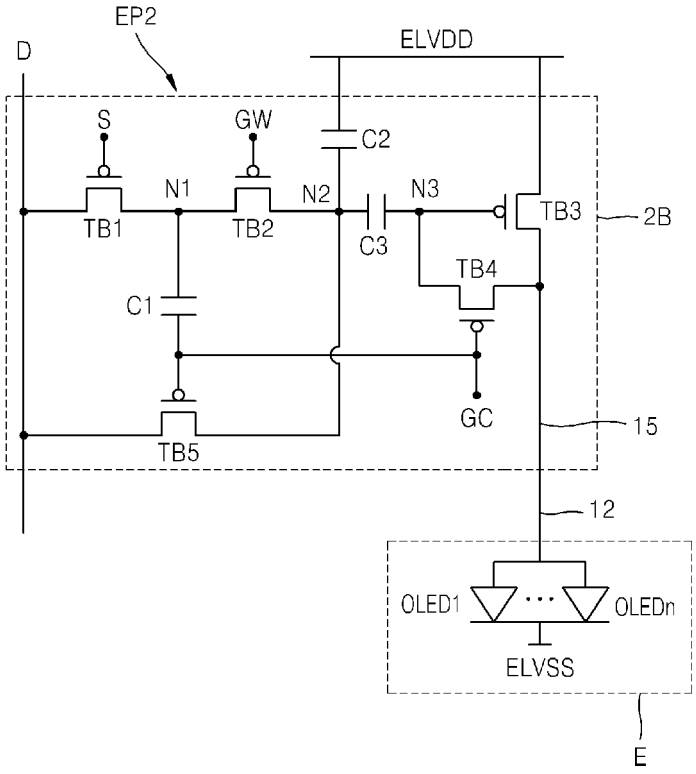

EP2
D
ELVDD
S
GW
C2
N1
N2
N3
TB3
2B
TB1
TB2
C3
TB4
C1
GC
15
TB5
12
OLED1
OLEDn
ELVSS
E

FIG. 35

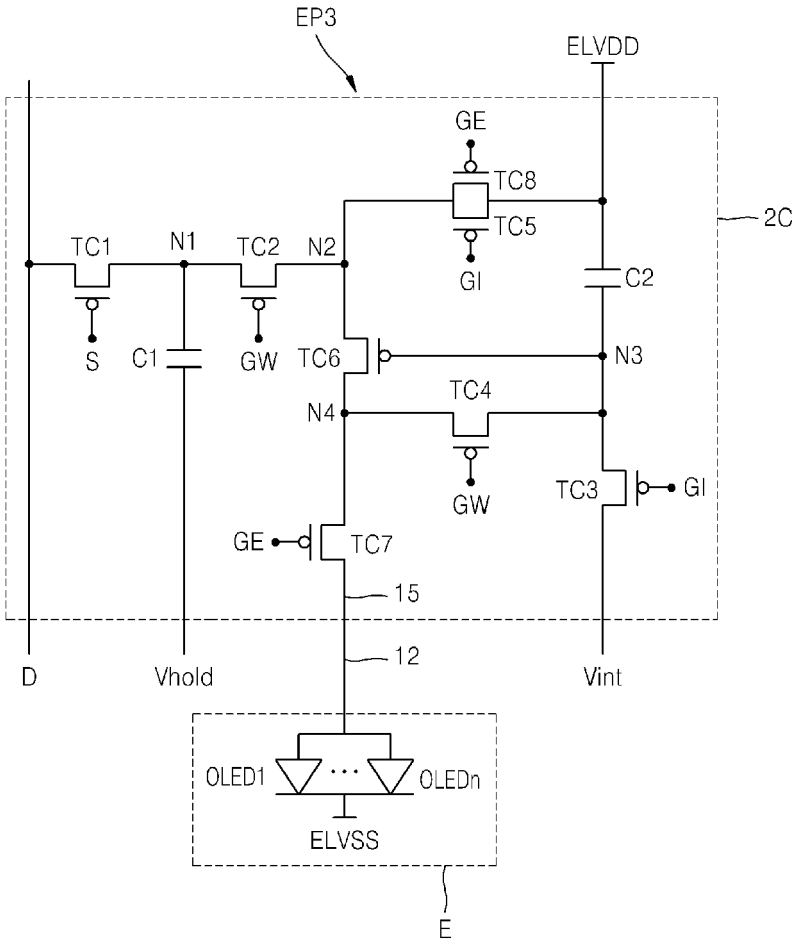

EP3
ELVDD
GE
TC8
TC5
2C
TC1
N1
TC2
N2
GI
C2
S
C1
GW
TC6
N3
TC4
N4
GW
TC3
GI
GE
TC7
15
12
D
Vhold
Vint
OLED1
OLEDn
ELVSS
E

FIG. 36

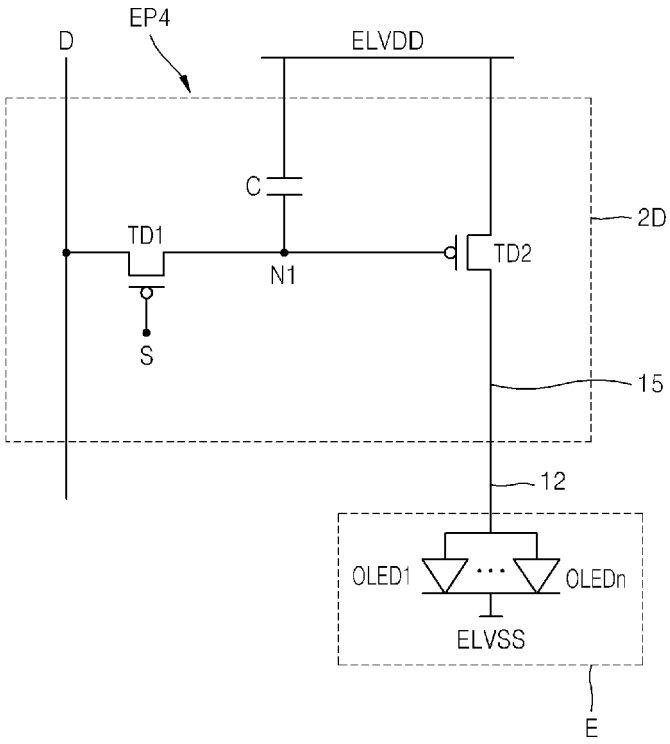


FIG. 37

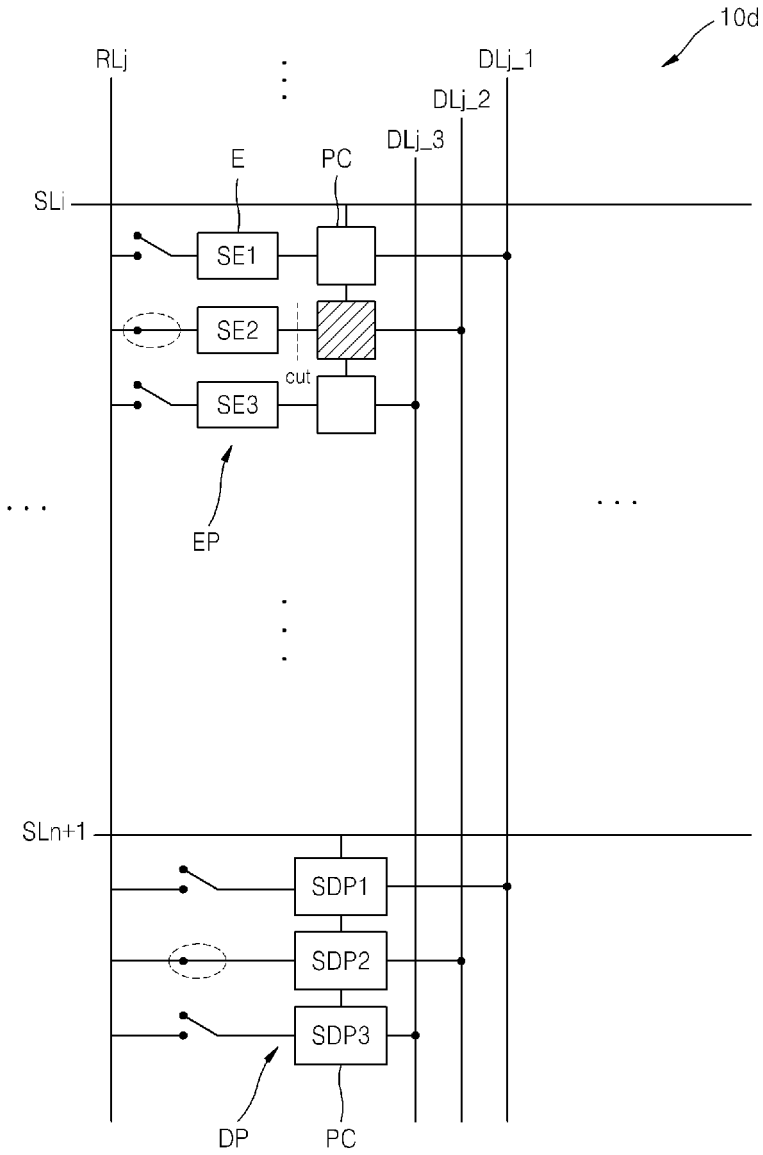

10d
RLj
DLj_1
DLj_2
DLj_3
E
PC
SLi
SE1
SE2
cut
SE3
EP
SLn+1
SDP1
SDP2
SDP3
DP
PC

FIG. 38

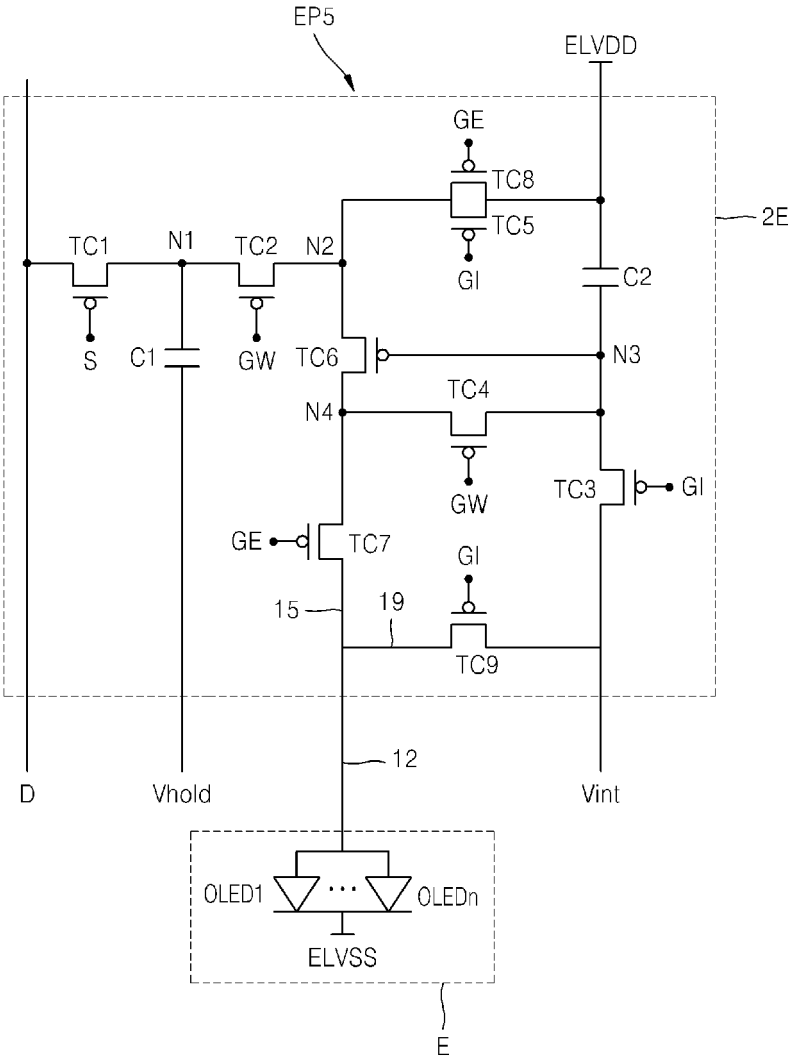

EP5
ELVDD
GE
TC8
TC5
2E
TC1
N1
TC2
N2
GI
C2
S
C1
GW
TC6
N3
TC4
N4
GW
TC3
GI
GE
TC7
GI
15
19
TC9
12
D
Vhold
Vint
OLED1
OLEDn
ELVSS
E

FIG. 39

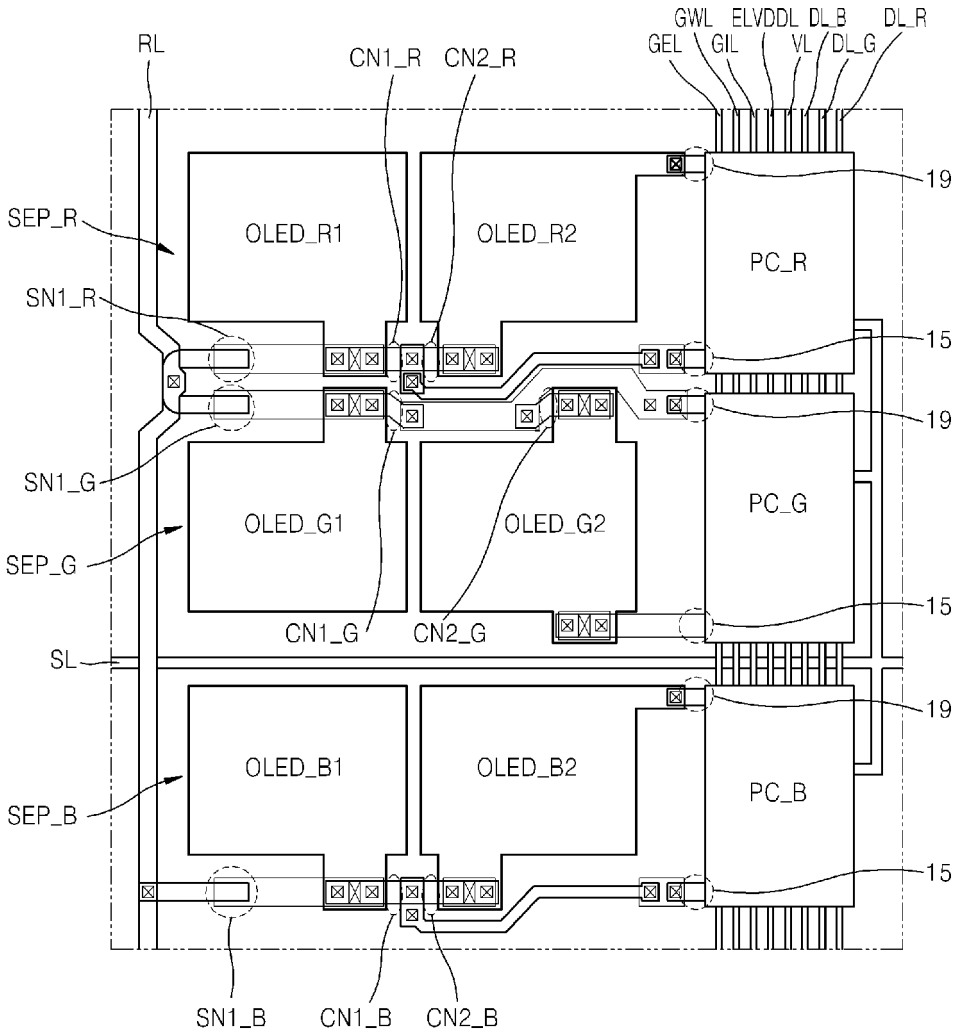

RL
CN1_R
CN2_R
GWL
ELVDDL
DL_B
DL_R
GEL
GIL
VL
DL_G
19
SEP_R
OLED_R1
OLED_R2
PC_R
SN1_R
15
19
SN1_G
OLED_G1
OLED_G2
PC_G
SEP_G
15
CN1_G
CN2_G
SL
19
OLED_B1
OLED_B2
PC_B
SEP_B
15
SN1_B
CN1_B
CN2_B

FIG. 40

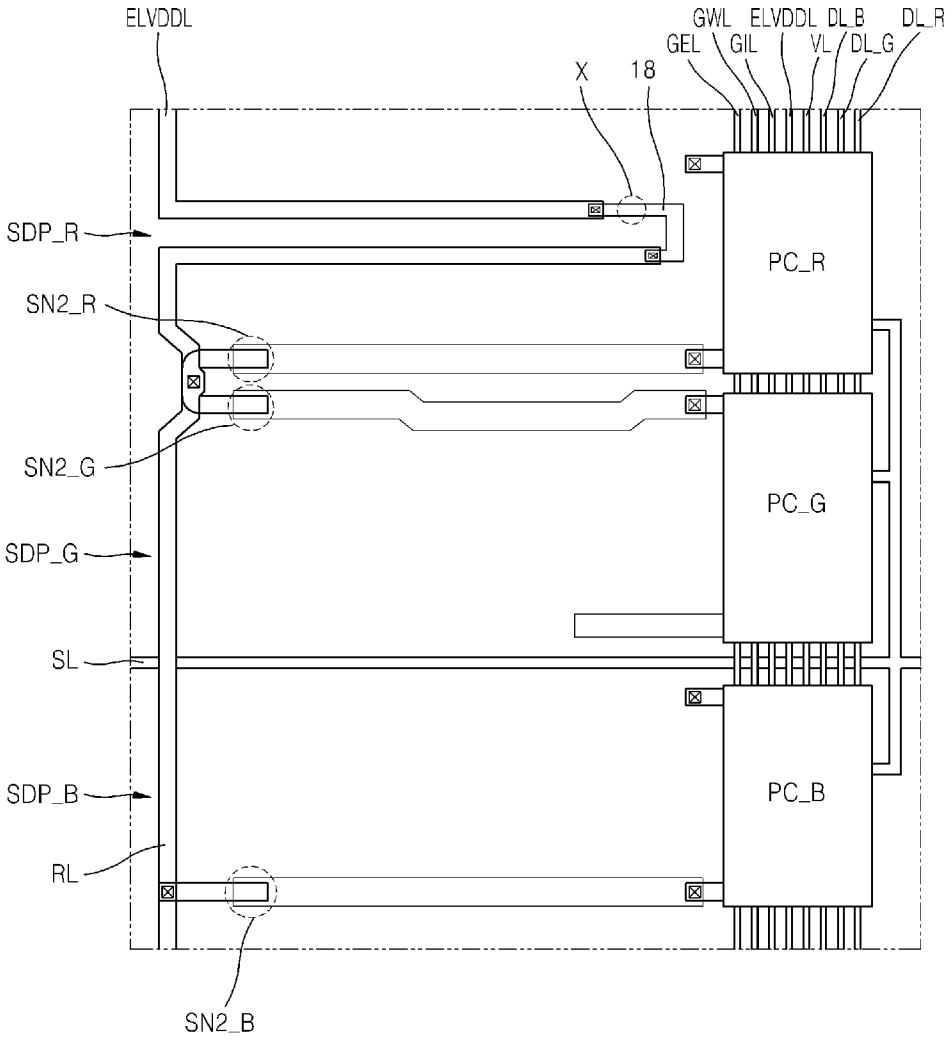

ELVDDL
GWL
ELVDDL
DL_B
DL_R
GEL
GIL
VL
DL_G
X
18
SDP_R
SN2_R
SN2_G
SDP_G
SL
SDP_B
RL
SN2_B
PC_R
PC_G
PC_B

FIG. 41

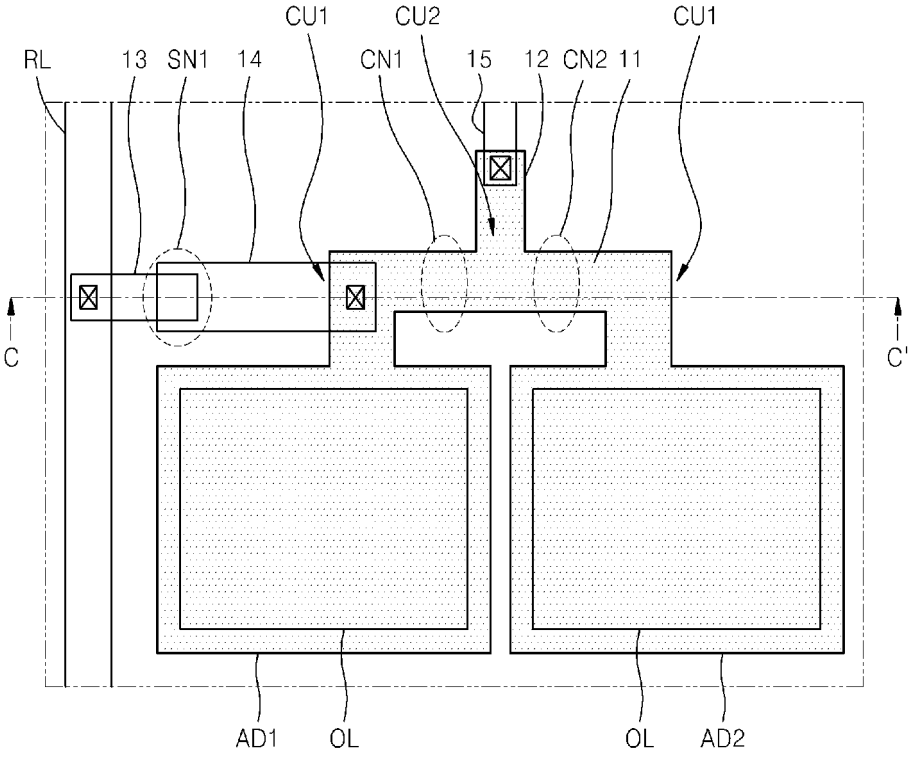

CU1
CU2
CU1
RL
13
SN1
14
CN1
15
12
CN2
11
C
C'
AD1
OL
OL
AD2

FIG. 42

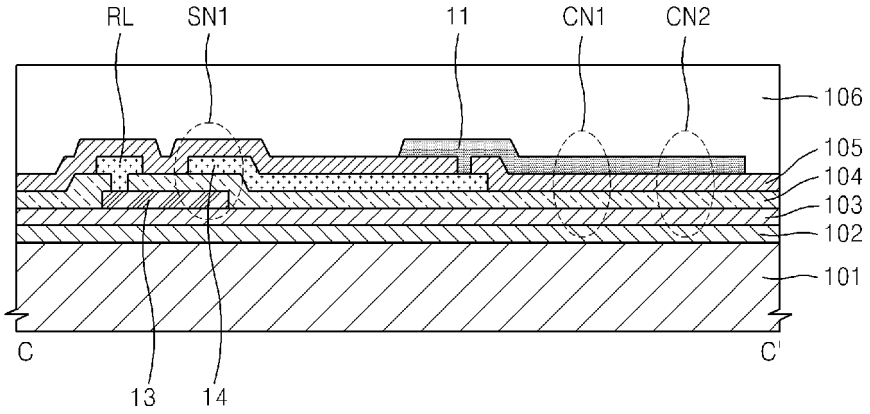
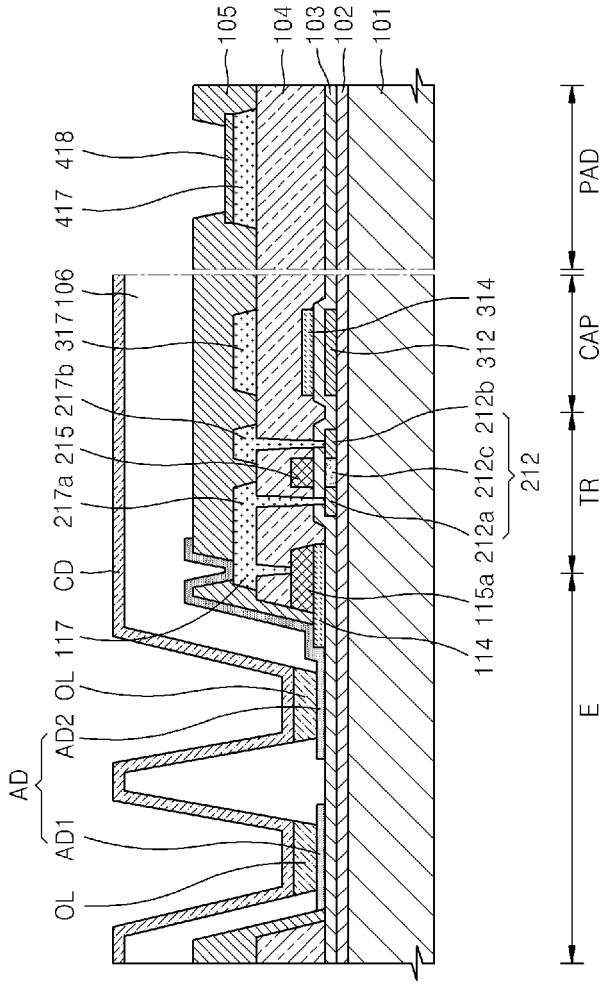

RL
SN1
11
CN1
CN2
106
105
104
103
102
101
C
C'
13
14

FIG. 43


105
104
103
102
101
418
417
106
317
217b
215
217a
CD
117
OL
AD2
AD
AD1
OL
314
312
212b
212c
212a
212
115a
114
PAD
CAP
TR
E

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 2007152567 A1 **[0002]**
- US 2008062096 A1 **[0002]**
- US 2007046186 A1 **[0002]**
- EP 2535888 A1 **[0002]**
- WO 2012001740 A1 **[0002]**
- US 2005173707 A1 **[0002]**
- US 2012146999 A1 **[0002]**
- US 2012113077 A1 **[0002]**
- US 2006017674 A1 **[0002]**
- US 2010001941 A1 **[0002]**
- US 2001028429 A1 **[0002]**

专利名称(译)	有机发光显示装置及其修复方法		
公开(公告)号	EP2806458B1	公开(公告)日	2018-07-04
申请号	EP2014169289	申请日	2014-05-21
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	CHO YOUNG JIN HWANG YOUNG IN KIM DONG GYU		
发明人	CHO, YOUNG-JIN HWANG, YOUNG-IN KIM, DONG-GYU		
IPC分类号	H01L27/32 H01L27/12 G09G3/32		
代理机构(译)	NIEPELT，CARSTEN		
优先权	1020130057959 2013-05-22 KR 1020130068638 2013-06-14 KR		
其他公开文献	EP2806458A2 EP2806458A3		
外部链接	Espacenet		

摘要(译)

提供一种有机发光显示装置（100）及其修复方法。有机发光显示装置（100）包括：发射装置（E），包括多个子发射装置（SE1，SE2）;发射像素电路（PCi），被配置为向发射装置提供驱动电流;虚设像素电路（PCn + 1），用于向发光装置（E）提供驱动电流;以及将发射装置（E）耦合到虚设像素电路（PCn + 1）的修复线（RL），其中发射装置（E）被配置为从发射像素电路（PCi）或虚设接收驱动电流像素电路（PCn + 1）。

FIG. 1

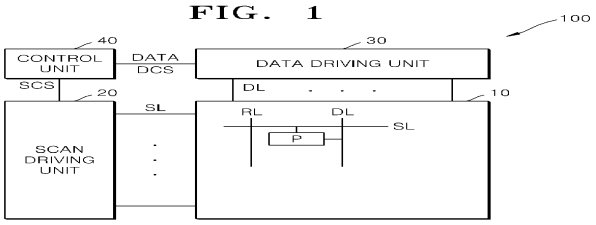


FIG. 2