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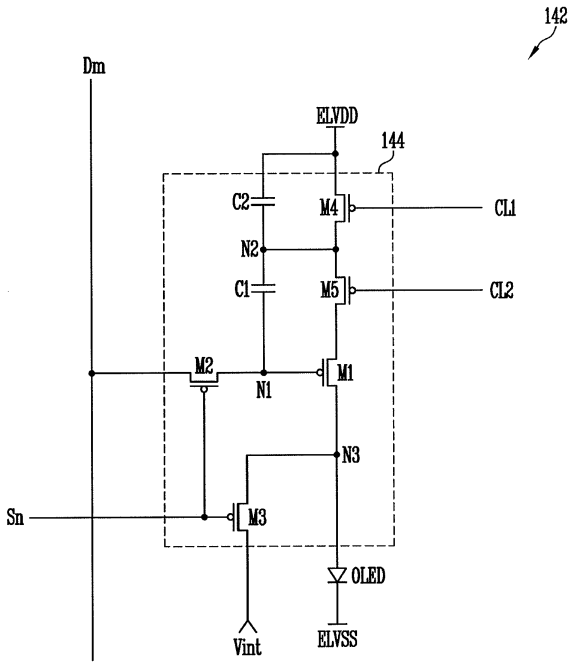
(54) Pixel and organic light emitting display using the same

(57) A pixel includes an organic light emitting diode and a pixel control circuit. The pixel control circuit includes a first transistor, a second transistor, and a third transistor. The first transistor controls an amount of current to the organic light emitting diode from a first power source based on a voltage applied to a first node. The second transistor is coupled between the first node and a data line and turns on when a scan signal is supplied to a scan line. The third transistor is coupled between the first power source and a second node that is a common terminal of first and second capacitors, which are coupled in series between the first node and the fist power source. In operation, the third transistor turns on when a first control signal is supplied to a first control line.

FIG. 2



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Description

BACKGROUND

1. Field

[0001] One or more embodiments described herein relate to a display device.

2. Description of the Related Art

[0002] Various types of flat panel displays have been developed. Examples include liquid crystal displays, field emission displays, plasma display panels, and organic light emitting displays. These displays are preferred by consumers because of their reduced weight and size compared with displays that use cathode ray tubes.

[0003] An organic light emitting display generates images using pixels that include organic light emitting diodes. Each diode emits light based on a recombination of electrons and holes in an active layer. Displays of this type have a fast response speed and may be driven with low power compared to other displays.

SUMMARY

[0004] In accordance with one embodiment, a pixel includes an organic light emitting diode; a first transistor configured to control an amount of current supplied to the organic light emitting diode from a first power source, the first power source coupled to a first electrode of the first transistor, the amount of current supplied to the organic light emitting diode being based on a voltage applied to a first node; a second transistor coupled between the first node and a data line, the second transistor being turned on when a scan signal is supplied to a scan line; first and second capacitors coupled in series between the first node and the first power source; and a third transistor coupled between the first power source and a second node that is a common terminal of the first and second capacitors, the third transistor being turned on when a first control signal is supplied to a first control line.

[0005] Also, the pixel may include a fourth transistor that may be coupled between an anode electrode of the organic light emitting diode and an initialization power source, and the fourth transistor may turn on when the scan signal is supplied to the scan line.

[0006] Also, the initialization power source may be set to a voltage at which the organic light emitting diode is turned off.

[0007] Also, the pixel may include a fourth transistor coupled between the second node and the first electrode of the first transistor, and the fourth transistor may turn on when a second control signal is supplied to a second control line.

[0008] Also, the third transistor and a fifth transistor may be progressively turned on after a data signal is supplied to the first node. The third and a fifth transistor may have turn-on periods that partially overlap a turn-on period of the second transistor.

[0009] Also, a fourth transistor may be coupled between a second electrode of the first transistor and the organic light emitting diode, and the fourth transistor may be turned on when a second control signal is supplied to a second control line.

[0010] Also, the third transistor and a fifth transistor may be progressively turned on after a data signal is supplied to the first node. The third transistor and a fifth transistor may have turn-on periods which partially overlap a turn-on period of the second transistor.

[0011] In accordance with another embodiment, an organic light emitting display includes pixels positioned in an area defined by scan lines and data lines; a scan driver configured to simultaneously supply a scan signal to the scan lines during first and second periods in one frame, and progressively control the supply of the scan signal to the scan lines during a third period in the one frame; a data driver configured to supply a data signal to the data lines synchronized with the scan signal during the third period; and a control driver configured to supply a first control signal to a first control line commonly coupled to the pixels, and to supply a second control signal to a second control line commonly coupled to the pixels.

[0012] Each pixel positioned on an i-th (i is a natural number) horizontal line may include an organic light emitting diode; a first transistor configured to control an amount of current supplied to the organic light emitting diode from a first power source, the first power source coupled to a first electrode of the first transistor, the amount of current supplied to the organic light emitting diode being based on a voltage applied to a first node; a second transistor coupled between the first node and a data line, the second transistor being turned on when a scan signal is supplied to an i-th scan line; first and second capacitors coupled in series between the first node and the first power source; a third transistor coupled between an anode electrode of the organic light emitting diode and an initialization power source, the third transistor being turned on when the scan signal is supplied to the i-th scan line; and a fourth transistor coupled between the first power source and a second node that is a common terminal of the first and second capacitors, the fourth transistor being turned on when the first control signal is supplied to the first control line.

[0013] Also, a fifth transistor may be coupled between the second node and the first electrode of the first transistor, and the fifth transistor may be turned on when the second control signal is supplied to the second control line.

[0014] Also, a fifth transistor may be coupled between a second electrode of the first transistor and the organic light emitting diode, and the fifth transistor may be turned on when the second control signal is supplied to the second control line.

[0015] Also, the initialization power source may be set to a voltage at which the organic light emitting diode is

turned off.

[0016] Also, the control driver may supply the first control signal during a first period and supplies the second control signal during a second period.

[0017] Also, the data driver may apply the voltage of a reference power source to the data lines during the first and second periods. The reference power source may be set to a voltage at which the first transistor is turned on.

[0018] Also, the data driver may apply the voltage of an off-power source to the data lines during a portion of the first period, and may apply the voltage of the reference power source to the data lines during the other of the first period and the second period.

[0019] Also, the off-power source may be set to a voltage to turn off the first transistor, and the reference power source may be set to a voltage to turn on the first transistor.

[0020] Also, the off-power source may be set to a voltage substantially equal to a voltage of the first power source, and the reference power source may be set to a voltage in the voltage range of the data signal.

[0021] Also, the control driver may supply the first control signal and then may supply the second control signal after a third period in the one frame. The scan driver may progressively stop the supply of the scan signal to the scan lines during the third period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] Features will become apparent to those of skill in the art by describing in detail exemplary embodiments with reference to the attached drawings in which:

FIG. 1 illustrates an embodiment of an organic light emitting display;

FIG. 2 illustrates a first embodiment of a pixel in FIG. 1;

FIG. 3 illustrates a waveform corresponding to a first embodiment of a method for driving the pixel in FIG. 2;

FIGS. 4A-4C illustrate an embodiment of a process for operating the pixel based on the driving waveform of FIG. 3;

FIG. 5 illustrates a waveform corresponding to a second embodiment of a method for driving the pixel in FIG. 2;

FIGS. 6A-6B illustrate an embodiment of a process for operating the pixel based on the driving waveform of FIG. 5;

FIG. 7 illustrates a second embodiment of the pixel in FIG. 1;

FIGS. 8A-8D illustrate another embodiment of a process for operating the pixel based on the driving waveform of FIG. 5;

FIG. 9 illustrates an example of a waveform of a scan signal supplied during a third period of operation.

DETAILED DESCRIPTION

[0023] Example embodiments are described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey exemplary implementations to those skilled in the art.

[0024] In the drawing figures, the dimensions of layers and regions may be exaggerated for clarity of illustration. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it may be the only layer between the two layers, or one or more intervening layers may also be present. Like reference numerals refer to like elements throughout.

[0025] FIG. 1 illustrates an embodiment of an organic light emitting display which includes a pixel unit 140, a scan driver 110, a control driver 120, a data driver 130, and a timing controller 150. The pixel unit 140 includes pixels 142 positioned at intersection portions of scan lines S1 to Sn and data lines D1 to Dm. The scan driver 110 drives the scan lines S1 to Sn. The control driver 120 drives first and second control lines CL1 and CL2 which are commonly coupled to the pixels 142. The data driver 130 drives the data lines D1 to Dm. The timing controller 150 controls the drivers 110, 120 and 130.

[0026] The scan driver 110 may supply a scan signal to the scan lines S1 to Sn. For example, the scan driver 110 may progressively supply a scan signal to the scan lines S1 to Sn during a third period in one frame. If the scan signal is progressively supplied to the scan lines S1 to Sn, pixels 142 are selected for each horizontal line.

[0027] The data driver 130 may supply a data signal to the data lines D1 to Dm so as to be synchronized with the scan signal. Then, the data signal is supplied to the pixels 142 selected by the scan signal. The data driver 130 applies a predetermined voltage, for example, the volatge of reference power source Vref (to be explained below) to the data lines D1 to Dm during the other periods except the third period in the one frame.

[0028] The control driver 120 supplies a first control signal to the first control line CL1 commonly coupled to the pixels 142, and supplies a second control signal to the second control line CL2 commonly coupled to the pixels 142. In accordance with one embodiment, the first and second control signals may be supplied during first and second periods, except a third period (to be discussed in greater detail below) in one frame.

[0029] The pixels 142 may be positioned in an area defined by the scan lines S1 to Sn and the data lines D1 to Dm. The pixels 142 may emit light with a predetermined luminance, by controlling the amount of current flowing from a first power source ELVDD to a second power source ELVSS via an organic light emitting diode, corresponding to the data signal.

[0030] Although the first and second control lines CL1

and CL2 were described above as being driven by the control driver 120, the first and second control lines CL1 and CL2 may be driven by the scan driver 110 in other embodiments.

[0031] In addition, although the first and second control lines CL1 and CL2 were described above as being commonly coupled to all the pixels 142, the pixel unit 140 may be divided into predetermined blocks in other embodiments. In these other embodiments, pixels 142 for each block may be coupled to different first and second control lines CL1 and CL2. In this case, the pixels 142 are driven for each block.

[0032] FIG. 2 illustrates a first embodiment of a pixel 142 in FIG. 1. For convenience of illustration, the pixel is shown to be coupled to an n-th scan line Sn and an m-th data line Dm. Referring to FIG. 2, in the first embodiment the pixel 142 includes an organic light emitting diode OLED and a pixel circuit 144 configured to control the amount of current supplied to the organic light emitting diode OLED.

[0033] An anode electrode of the organic light emitting diode OLED may be coupled to the pixel circuit 144, and a cathode electrode of the organic light emitting diode OLED is coupled to the second power source ELVSS. The organic light emitting diode OLED may generate light with a predetermined luminance corresponding to the amount of current supplied from the pixel circuit 144. The second power source ELVSS may be set to a voltage lower than that of the first power source ELVDD, so that current may flow through the organic light emitting diode OLED.

[0034] The pixel circuit 144 may control the amount of current supplied to the organic light emitting diode OLED, corresponding to a data signal. In accordance with the first embodiment, the pixel circuit 144 includes first to fifth transistors M1 to M5, a first capacitor C1, and a second capacitor C2. While these transistors are shown as PMOS transistors, one or more of the transistors may be NMOS transistors in other embodiments.

[0035] A first electrode of the first transistor (driving transistor) M1 is coupled to a second electrode of the fifth transistor M5, and a second electrode of the first transistor M1 is coupled to a third node N3. A gate electrode of the first transistor M1 may be coupled to a first node N1. The first transistor M1 may control the amount of current flowing from the first power source ELVDD to the second power source ELVSS via the organic light emitting diode OLED, corresponding to a voltage applied to the first node N1.

[0036] A first electrode of the second transistor M2 is coupled to the data line Dm, and a second electrode of the second transistor M2 is coupled to the first node N1. A gate electrode of the second transistor M2 is coupled to the scan line Sn. The second transistor M2 is turned on when a scan signal is supplied to the scan line Sn, so as to allow the data line Dm and the first node N1 to be electrically coupled to each other.

[0037] A first electrode of the third transistor M3 may be coupled to the third node N3, and a second electrode of the third transistor M3 may be coupled to an initialization power source Vint. A gate electrode of the third transistor M3 is coupled to the scan line Sn. The third transistor M3 is turned on when the scan signal is supplied to the scan line Sn, so as to apply the voltage of the initialization power source Vint to the third node N3. The initialization power source Vint may be set to a low voltage, so that the organic light emitting diode OLED may be turned off.

[0038] A first electrode of the fourth transistor M4 may be coupled to the first power source ELVDD, and a second electrode of the fourth transistor M4 is coupled to a second node N2. A gate electrode of the fourth transistor M4 may be coupled to the first control line CL1. The fourth transistor M4 is turned on when a first control signal is supplied to the first control line CL1, so as to supply the voltage of the first power source ELVDD to the second node N2.

[0039] A first electrode of the fifth transistor M5 may be coupled to the second node N2, and the second electrode of the fifth transistor M5 may be coupled to the first electrode of the first transistor M1. A gate electrode of the fifth transistor M5 is coupled to the second control line CL2. The fifth transistor M5 is turned on when a second control signal is supplied to the second control line CL2, so as to allow the second node N2 and the first transistor M1 to be electrically coupled to each other.

[0040] The first capacitor C1 may be coupled between the first and second nodes N1 and N2. The first capacitor C1 may store the threshold voltage of the first transistor M1 and a voltage corresponding to the data signal.

[0041] The second capacitor C2 may be coupled between the second node N2 and the first power source ELVDD. The second capacitor C2 may have a predetermined capacitance, so as to allow for storage of the threshold voltage of the first transistor M1 and the voltage corresponding to the data signal.

[0042] FIG. 3 illustrates a waveform corresponding to a first embodiment of a method for driving the pixel in FIG. 2. Referring to FIG. 3, during a first period T1, a first control signal is supplied to the first control line CL1, a scan signal is supplied to the scan lines S1 to Sn, and the voltage of a reference power source Vref is applied to the data line Dm. The reference power source Vref is set to a specific voltage in the voltage range of the data signal. Thus, the reference power source Vref may be set to a voltage at which current may flow through the first transistor M1.

[0043] When the first control signal is supplied to the first control line CL1, the fourth transistor M4 is turned on as shown in FIG. 4A. When the fourth transistor M4 is turned on, the voltage of the first power source ELVDD is applied to the second node N2.

[0044] When the scan signal is supplied to the scan line Sn, the second and third transistors M2 and M3 are turned on. When the second transistor M2 is turned on, the voltage of the reference power source Vref from the

data line Dm is applied to the first node N1.

[0045] When the third transistor M3 is turned on, the voltage of the initialization power source Vint is applied to the third node N3. When the voltage of the initialization power source Vint is applied to the third node N3, the organic light emitting diode OLED is initialized. For example, if the voltage of the initialization power source Vref is applied to the third node N3, an organic capacitor parasitically formed in the organic light emitting diode OLED may be discharged to be initialized.

[0046] During a second period T2, a second control signal may be supplied to the second control line CL2, the scan signal may be supplied to the scan lines S1 to Sn, and the voltage of the reference power source Vref may be applied to the data line Dm. When the second control signal is supplied to the second control line CL2, the fifth transistor M5 is turned on. When the fifth transistor M5 is turned on, the second node and the first electrode of the first transistor M1 are electrically coupled to each other.

[0047] Also, during the second period T2, the voltage of the reference power source Vref may be supplied to the first node N1 and the third transistor M3 may maintain a turn-on state. As a result, a predetermined current flows from the second node N2 to the initialization power source Vint via the fifth, first, and third transistors M5, M1 and M3.

[0048] When this occurs, the voltage at the second node N2 may be dropped from the voltage of the first power source ELVDD to a voltage obtained by adding the threshold voltage of the first transistor M1 to the voltage of the reference power source Vref. When the voltage at the second node N2 is set as the voltage obtained by adding the threshold voltage of the first transistor M1 to the voltage of the reference power source Vref, the first transistor M1 is turned off. Then, a voltage corresponding to the threshold voltage of the first transistor M1 may be charged in the first capacitor C1.

[0049] During a third period T3, a scan signal may be progressively supplied to the scan lines S1 to Sn, and a data signal may be supplied to the data lines D1 to Dm synchronized with the scan signal. When the scan signal is supplied to the n-th scan line Sn, the second and third transistors M2 and M3 are turned on as shown in FIG. 4C. When the second transistor M2 is turned on, the data signal from the data line Dm is supplied to the first node N1.

[0050] When the data signal is supplied to the first node N1, the voltage at the first node N1 is changed from the voltage of the reference power source Vref to the voltage of the data signal. Then, the voltage at the second node N2 may also be changed corresponding to the change in the voltage at the first node N1. Practically, the voltage at the second node N2 may be changed into a predetermined voltage, corresponding to a ratio of the capacitances of the first and second capacitors C1 and C2. Then, the threshold voltage of the first transistor M1 and a voltage corresponding to the data signal are charged in the first capacitor C1.

[0051] After the threshold voltage of the first transistor M1 and the voltage corresponding to the data signal are charged in the first capacitor C1, the first control signal is supplied to the first control line CL1 during a fourth period T4, so that the fourth transistor M4 is turned on. When the fourth transistor M4 is turned on, the voltage of the first power source ELVDD is applied to the second node N2. In this case, the first node N1 is set in a floating state, and hence the first capacitor C1 stably maintains the voltage charged in the previous period.

[0052] Subsequently, the second control signal may be supplied to the second control line CL2 during a fifth period T5 so that the fifth transistor M5 is turned on. If the fifth transistor M is turned on, the first electrode of the first transistor M1 is electrically coupled to the first power source ELVDD via the first node N1. Then, the first transistor M1 may control the amount of current supplied to the organic light emitting diode OLED, corresponding to the voltage stored in the first capacitor C1.

[0053] An organic light emitting display may display an image with a predetermined luminance by repeating the aforementioned procedure for the pixels in the pixel unit. In the first embodiment, the threshold voltages of the pixels may be simultaneously compensated during the second period T2. In this case, the second period T2 may be sufficiently assigned and, accordingly, the threshold voltage of the first transistor M1 may be stably compensated even when the organic light emitting display is driven at a high speed of 120Hz or more.

[0054] FIG. 5 illustrates another waveform corresponding to a second embodiment of a method for driving the pixel in FIG. 2. Referring to FIG. 5, during a first period T1', a first control signal is supplied to the first control line CL1, a second control signal is supplied to the second control line CL2, and a scan signal is supplied to the scan lines S1 to Sn. The voltage of an off-power source Voff is applied to the data line Dm during a first portion T1a' of the first period T1', and the voltage of a reference power source Vref is applied to the data line Dm during a second portion T1b' of the first period T1'.

[0055] When the first control signal is supplied to the first control line CL1, the fourth transistor M4 is turned on so that the first power source ELVDD and the second node N2 are electrically coupled to each other, as shown in FIG. 6A. When the second control signal is supplied to the second control line CL2, the fifth transistor M5 is turned on so that the first electrode of the first transistor M1 and the second node N2 is electrically coupled to each other.

[0056] When the scan signal is supplied to the scan line Sn, the second and third transistors M2 and M3 are turned on. When the second transistor M2 is turned on, the voltage of the off-power source Voff from the data line Dm is applied to the first node N1. When the voltage of the off-power source Voff is applied to the first node N1 during the T1a' portion of period T1', the first transistor M1 is turned off. The off-power source Voff may be set

to a voltage at which the first transistor M1 may be turned off, which, for example, may be a voltage identical to that of the first power source ELVDD or another voltage.

[0057] When the first transistor M1 is turned off, unnecessary current may be prevented from being supplied to the initialization power source Vint, even through the fourth and fifth transistors M4 and M5 are turned on. Accordingly, it may be possible to reduce power consumption and help secure operational reliability.

[0058] When the third transistor M3 is turned on, the voltage of the initialization power source Vint is applied to the third node N3. When the voltage of the initialization power source Vint is applied to the third node N3, the organic light emitting diode OLED is initialized.

[0059] Subsequently, the voltage of the reference power source Vref may be applied to the data line Dm during the second period T1b' of the first period T1'. When the voltage of the reference power source Vref is applied to the data line Dm, the first transistor M1 is set in a turn-on state as shown in FIG. 6B. In this case, an on-bias voltage is applied to the first transistor M1 during the second portion T1b' of the first period T1'. Accordingly, it may be possible to display an image with uniform luminance.

[0060] Specifically, the voltage characteristic of the first transistor M1 included in each pixel 142 may be set unequally, for example, based on a gray scale value of the previous period. Therefore, an image with a desired luminance may not be displayed.

[0061] In accordance with one embodiment, the voltage characteristic of the first transistor M1 is initialized by applying the on-bias voltage to the first transistor M1 during the second period T1b' of period T1'. Accordingly, it may be possible for a uniform image to be generated. Also, the current flowing through the first transistor M1 may be supplied to the initialization power source Vint during the second portion T1b' of the first period T1'. Accordingly, the organic light emitting diode OLED may be maintained in a non-emission state. In this embodiment, operations of the pixel during the second to fifth periods T2 to T5 may be similar to those in FIG. 3.

[0062] FIG. 7 illustrates a second embodiment of a pixel in FIG. 1. Referring to FIG. 7, the pixel 142 according to this embodiment includes a pixel circuit 144' and an organic light emitting diode OLED.

[0063] The pixel circuit 144' may include a fifth transistor M5' coupled between the second electrode and the third node N3. The fifth transistor M5' may be turned on when a second control signal is supplied to the second control line CL2 so as to allow the first transistor M1 and the third node N3 to be electrically coupled to each other. The pixel 142 may therefore have a structure similar to that of the pixel 142 of FIG. 2, except that the position of the fifth transistor M5' is changed. In operation, during a first period T1', a first control signal is supplied to the first control line CL1, a second control signal is supplied to the second control line CL2, and a scan signal is supplied to the scan lines S1 to Sn. The voltage of the off-power source Voff may be applied to the data line Dm during a first portion T1a' of the first period T1', and the voltage of the reference power source Vref may be applied to the data line Dm during the second portion T1b' of the first period T1'.

[0064] When the first control signal is supplied to the first control line CL1, the fourth transistor M4 is turned on so that the first power source ELVDD is electrically coupled to the first electrode of the first transistor M1 via the second node N2 as shown in FIG. 8A. When the second control signal is supplied to the second control line CL2, the fifth transistor M5' is turned on so that the second node of the first transistor M1 is electrically coupled to the third node N3.

[0065] When the scan signal is supplied to the scan line Sn, the second and third transistors M2 and M3 are turned on. When the second transistor M2 is turned on, the voltage of the off-power source Voff from the data line Dm is applied to the first node N1. When the voltage of the off-power source Voff is applied to the first node N1, the first transistor M1 is turned off. When the third transistor M3 is turned on, the voltage of the initialization power source Vint is applied to the third node N3. When the voltage of the initialization power source Vint is applied to the third node N3, the organic light emitting diode OLED is initialized.

[0066] Subsequently, the voltage of the reference power source Vref is applied to the data line Dm during the second portion T1b' of the first period T1', except the portion of the first period T1'. When the voltage of the reference power source Vref is applied to the data line Dm during the second portion T1b' of period T1', the first transistor M1 is set in a turn-on state as shown in FIG. 8B. Then, an on-bias voltage is applied to the first transistor M1 during the second portion T1b' of the first period T1'. Accordingly, it may be possible to display an image with uniform luminance.

[0067] During the second period T2, the second control signal may be supplied to the second control line CL2, the scan signal may be supplied to the scan lines S1 to Sn, and the voltage of the reference power source Vref may be applied to the data line Dm. When the second control signal is supplied to the second control line CL2, the fifth transistor M5' is turned on so that the first transistor M1 and the third node N3 are electrically coupled to each other as shown in FIG. 8C. In this case, the voltage of the reference power source Vref is applied to the first node N1, and the third transistor M3 maintains a turn-on state. Hence, a predetermined current flows from the second node N2 to the initialization power source Vref via the first, fifth and third transistors M1, M5' and M3. Then, the voltage at the second node N2 is dropped from the voltage of the first power source ELVDD to the voltage obtained by adding the threshold voltage of the first transistor M1 to the voltage of the reference power source Vref. Thus, a voltage corresponding to the threshold voltage of the first transistor M1 may be charged in the first capacitor C1 during the second period T2.

[0068] During the third period T3, a scan signal may be progressively supplied to the scan lines S1 to Sn, and a data signal may be supplied to the data lines D1 to Dm synchronized with the scan signal. When the scan signal is supplied to the n-th scan line Sn, the second and third transistors M2 and M3 are turned on as shown in FIG. 8D. When the second transistor M2 is turned on, the data signal from the data line Dm is supplied to the first node N1.

[0069] When the data signal is supplied to the first node N1, the voltage at the first node N1 is changed from the voltage of the reference power source Vref to the voltage of the data signal. Then, the voltage at the second node N2 is also changed corresponding to a change in the voltage at the first node N1. Practically, the voltage at the second node N2 is changed into a predetermined voltage, for example, based on a ratio of the capacitances of the first and second capacitors C1 and C2. Then, the threshold voltage of the first transistor M1 and a voltage corresponding to the data signal may be charged in the first capacitor C 1.

[0070] After the threshold voltage of the first transistor M1 and the voltage corresponding to the data signal are charged in the first capacitor C1, the first control signal may be supplied to the first control line CL1 so that the fourth transistor M4 is turned on during the fourth period T4. If the fourth transistor M4 is turned on, the voltage of the first power source ELVDD is applied to the second node N2. In this case, the first node N1 may be set in a floating state and, hence, the first capacitor C1 may stably maintain the voltage charged in the previous period.

[0071] Subsequently, the second control signal is supplied to the second control line CL2 so that the fifth transistor M5' is turned on during the fifth period T5. When the fifth transistor M5' is turned on, the first electrode of the first transistor M1 is electrically coupled to the first power source ELVDD via the first node N1. Then, the first transistor M1 controls the amount of current supplied to the organic light emitting diode OLED, corresponding to the voltage stored in the first capacitor C1.

[0072] Although it has been illustrated in FIGS. 3 and 5 that a scan signal is progressively supplied to the scan lines S1 to Sn during the third period T3, the scan signal may be supplied in a different manner in the third period T3 in other embodiments. For example, in one embodiment, a scan signal may be simultaneously supplied to the scan lines S1 to Sn during the third period T3 as shown in FIG. 9. In this case, the supply of the scan signal supplied to the scan lines S1 to Sn is progressively stopped. In a case where the scan signal is simultaneously supplied to the scan lines S1 to Sn and the supply of the scan signal is progressively stopped, the scan driver 110 may be briefly configured with a shift register.

[0073] Meanwhile, a specific pixel 142 positioned on an i-th (i is a natural number) horizontal line finally charges the voltage of a data signal corresponding to the i-th horizontal line, regardless of a data signal of the previous horizontal line. After the specific pixel 142 charges the voltage of the data signal corresponding to the i-th horizontal line, the supply of the scan signal to an i-th scan line Si may be stopped. Accordingly, the specific pixel 142 may stably maintain the voltage of a desired data signal.

[0074] Additionally, in the aforementioned embodiments, the transistors are shown as PMOS transistors. In other embodiments, the transistors in the pixel circuit may be NMOS transistors or a combination of PMOS and NMOS transistors.

[0075] Also, in accordance with one or more embodiments, an organic light emitting diode OLED may generate red, green and blue light corresponding to the amount of current supplied from the driving transistor. A combination of these OLEDs may correspond to subpixels emitting different color light in a pixel. In other embodiments, the organic light emitting diode OLED may generate white light corresponding to the amount of the current supplied from the driving transistor. In this case, a color image is implemented using a separate color filter or the like.

[0076] By way of summation and review, an organic light emitting display may include a plurality of pixels arranged in a matrix form at intersection portions of a plurality of data lines, a plurality of scan lines, and a plurality of power lines. Furthermore, each pixel may include an organic light emitting diode, two or more transistors including a driving transistor, and one or more capacitors. In general, an organic light emitting display has low power consumption. However, in some cases, the amount of current flowing through the organic light emitting diode may depend on a variation in threshold voltage of the driving transistor in each pixel. This may cause display inequality. Thus, the characteristic of the driving transistor may change depending on manufacturing process variables of the driving transistor included in each pixel. The manufacturing of the organic light emitting display so that all the transistors have the same characteristic may not be practical in the current process conditions. Accordingly, there may occur a variation in threshold voltage of the driving transistor.

[0077] In view of this, there has been considered a method of adding, to each pixel, a compensation circuit, including a plurality of transistors and a capacitor, that charges a voltage corresponding to the threshold voltage of a driving transistor during one horizontal period. Accordingly, a variation in the threshold voltage of the driving transistor may be compensated.

[0078] Also, a method has been considered in which the compensation circuit is driven at a driving frequency of 120Hz or more in order to prevent a motion blur phenomenon and/or to implement 3D images. However, in a case where the compensation circuit is driven at a high frequency of 120Hz or more, the period required to charge the threshold voltage of the driving transistor is shortened, which may complicate compensating for the threshold voltage of the driving transistor. In accordance with one or more embodiments of the pixel and organic

light emitting display described herein, the threshold voltages of the driving transistors in the pixels may be simultaneously compensated during a specific period in one frame. Accordingly, the period required to compensate for the threshold voltage of the driving transistor may be sufficiently secured, thereby improving display quality.

[0079] Also, in accordance with one or more embodiments, an on-bias voltage may be applied to the driving transistor. Accordingly, it may be possible to display an image with uniform luminance, regardless of a gray scale of the previous period.

[0080] It is clear for a person skilled in the art that the disclosed embodiments can also be combined where possible.

Claims

1. A pixel (142), comprising:

an organic light emitting diode (OLED);
a first transistor (M1) configured to control an amount of current supplied to the organic light emitting diode (OLED) from a first power source (EL VDD), the first power source (EL VDD) coupled to a first electrode of the first transistor (M1), the amount of current supplied to the organic light emitting diode (OLED) being based on a voltage applied to a first node (N1);
a second transistor (M2) coupled between the first node (N1) and a data line (D1 to Dm), the second transistor (M2) being turned on when a scan signal is supplied to a scan line (S1 to Sn);
first and second capacitors (C1,C2) coupled in series between the first node and (N1) the first power source (EL VDD); and
a fourth transistor (M4) coupled between the first power source and a second node (N2) that is a common terminal of the first and second capacitors (C1, C2), the fourth transistor (M4) being turned on when a first control signal is supplied to a first control line (CL1).

2. The pixel (142) as claimed in claim 1, further comprising:

a third transistor (M3) coupled between an anode electrode of the organic light emitting diode (OELD), and an initialization power source (Vint), the third transistor (M3) being turned on when the scan signal is supplied to the scan line (S1 to Sn).

3. The pixel as claimed in claim 2, wherein the initialization power source (Vint) is set to a voltage at which the organic light emitting diode (OLED) is turned off.

4. The pixel as claimed in one of claims 1 to 3, further comprising:

a fifth transistor (M5) coupled between the second node (N2) and the first electrode of the first transistor (M1), the fifth transistor (M5) being turned on when a second control signal is supplied to a second control line (CL2).

5. The pixel as claimed in claim 4, wherein the fourth transistor (M4) and the fifth transistor (M5) are progressively turned on after a data signal is supplied to the first node (N1), and/or.the fourth transistor (M4) and the fifth transistor(M5) have turn-on periods that partially overlap a turn-on period of the second transistor (M2).

6. The pixel as claimed in one of claims 1 to 3, further comprising:

a fifth transistor (M5') coupled between a second electrode of the first transistor (M1) and the organic light emitting diode (OLED), the fifth transistor (M5') being turned on when a second control signal is supplied to a second control line (CL2).

7. The pixel as claimed in claim 6, wherein the fourth transistor (M4) and the fifth transistor (M5') are progressively turned on after a data signal is supplied to the first node (M1), and/or. the fourth transistor (M4) and the fifth transistor (M5') have turn-on periods which partially overlap a turn-on period of the second transistor (M2).

8. An organic light emitting display, comprising:

pixels (142) positioned in an area defined by scan lines (S1 to Sn) and data lines (D1 to Dm);
a scan driver (110) configured to simultaneously supply a scan signal to the scan lines (S1 to Sn) during first and second periods(T1, T2) in one frame, and progressively control the supply of the scan signal to the scan lines (S1 to Sn) during a third period (T3) in the one frame;
a data driver (130) configured to supply a data signal to the data lines (D1 to Dm) synchronized with the scan signal during the third period; and
a control driver (120) configured to supply a first control signal to a first control line (CL1) commonly coupled to the pixels (142), and to supply a second control signal to a second control line (CL2) commonly coupled to the pixels (142), wherein each pixel (142) positioned on an i-th (i is a natural number) horizontal line includes:

an organic light emitting diode (OLED);
a first transistor (M1) configured to control an amount of current supplied to the organic

light emitting diode (OLED) from a first power source (EL VDD), the first power source (EL VDD) coupled to a first electrode of the first transistor (M1), the amount of current supplied to the organic light emitting diode (OLED) being based on a voltage applied to a first node (N1);
a second transistor (M2) coupled between the first node (N1) and a data line (D1 to Dm), the second transistor (M2) being turned on when a scan signal is supplied to an i-th scan line (Si);
first and second capacitors (C1 and C2) coupled in series between the first node (N1) and the first power source (EL VDD);
a third transistor (M3) coupled between an anode electrode of the organic light emitting diode (OLED) and an initialization power source (Vint), the third transistor (M3) being turned on when the scan signal is supplied to the i-th scan line (Si); and
a fourth transistor (M4) coupled between the first power source (EL VDD) and a second node (N2) that is a common terminal of the first and second capacitors (C1 and C2), the fourth transistor (M4) being turned on when the first control signal is supplied to the first control line (CL1).

9. The organic light emitting display as claimed in claim 8, further comprising a fifth transistor (M5) coupled between the second node (N2) and the first electrode of the first transistor (M1), the fifth transistor (M5) being turned on when the second control signal is supplied to the second control line (CL2), or
wherein the control driver (120) supplies the first control signal and then supplies the second control signal after a third period (T3) in the one frame.

10. The organic light emitting display as claimed in claim 8, further comprising a fifth transistor (M5') coupled between a second electrode of the first transistor (M1) and the organic light emitting diode (OLED), the fifth transistor (M5') being turned on when the second control signal is supplied to the second control line (CL2).

11. The organic light emitting display as claimed in one of claims 8 to 10 wherein the initialization power source (Vint) is set to a voltage at which the organic light emitting diode (OLED) is turned off, and/or.
the control driver (120) supplies the first control signal during a first period (T1) and supplies the second control signal during a second period (T2).

12. The organic light emitting display as claimed in one of claims 8 to 11, wherein the data driver (130) applies the voltage of a reference power source (Vref) to the data lines (D1 to Dm) during the first and second periods (T1, T2), and/or.
the reference power source (Vref) is set to a voltage at which the first transistor (M1) is turned on.

13. The organic light emitting display as claimed in claim 8 or 10, wherein the control driver (120) supplies the first control signal during the first period (T1'), and supplies the second control signal during the first period (T1') and second period (T2), and/or.
the data driver (130) applies the voltage of an off-power source (Voff') to the data lines (D1 to Dm) during a portion (T1a') of the first period (T1'), and applies the voltage of the reference power source (Vref) to the data lines (D1 to Dm) during the other (T1b') of the first period (T1') and the second period (T2).

14. The organic light emitting display as claimed in claim 13, wherein the off-power source (Voff') is set to a voltage substantially equal to a voltage of the first power source (EL VDD), and wherein the reference power source (Vref) is set to a voltage in the voltage range of the data signal.

15. The organic light emitting display as claimed in claim 8, wherein the scan driver (130) progressively stops the supply of the scan signal to the scan lines (S1 to Sn) during the third period (T3).

FIG. 1

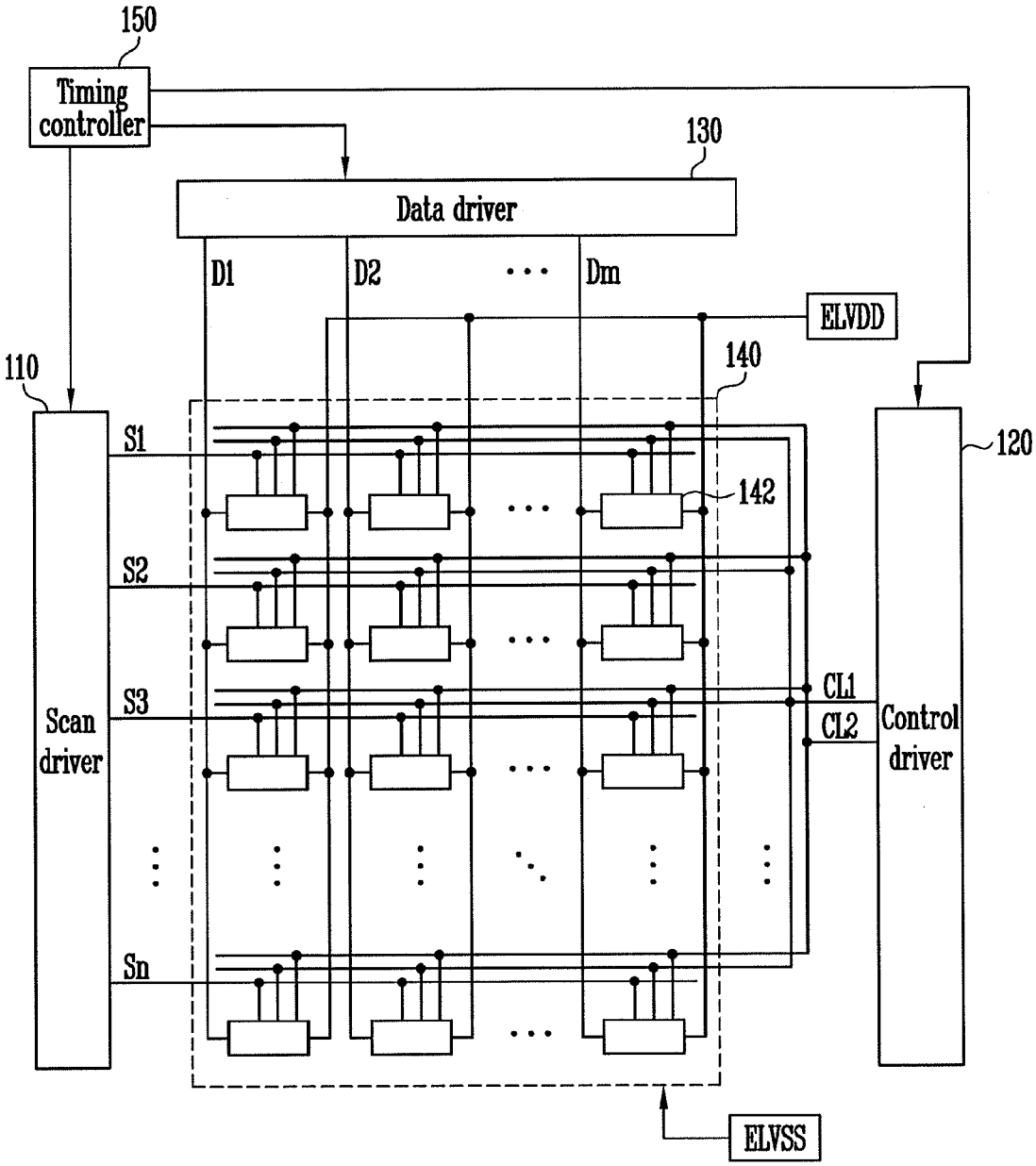
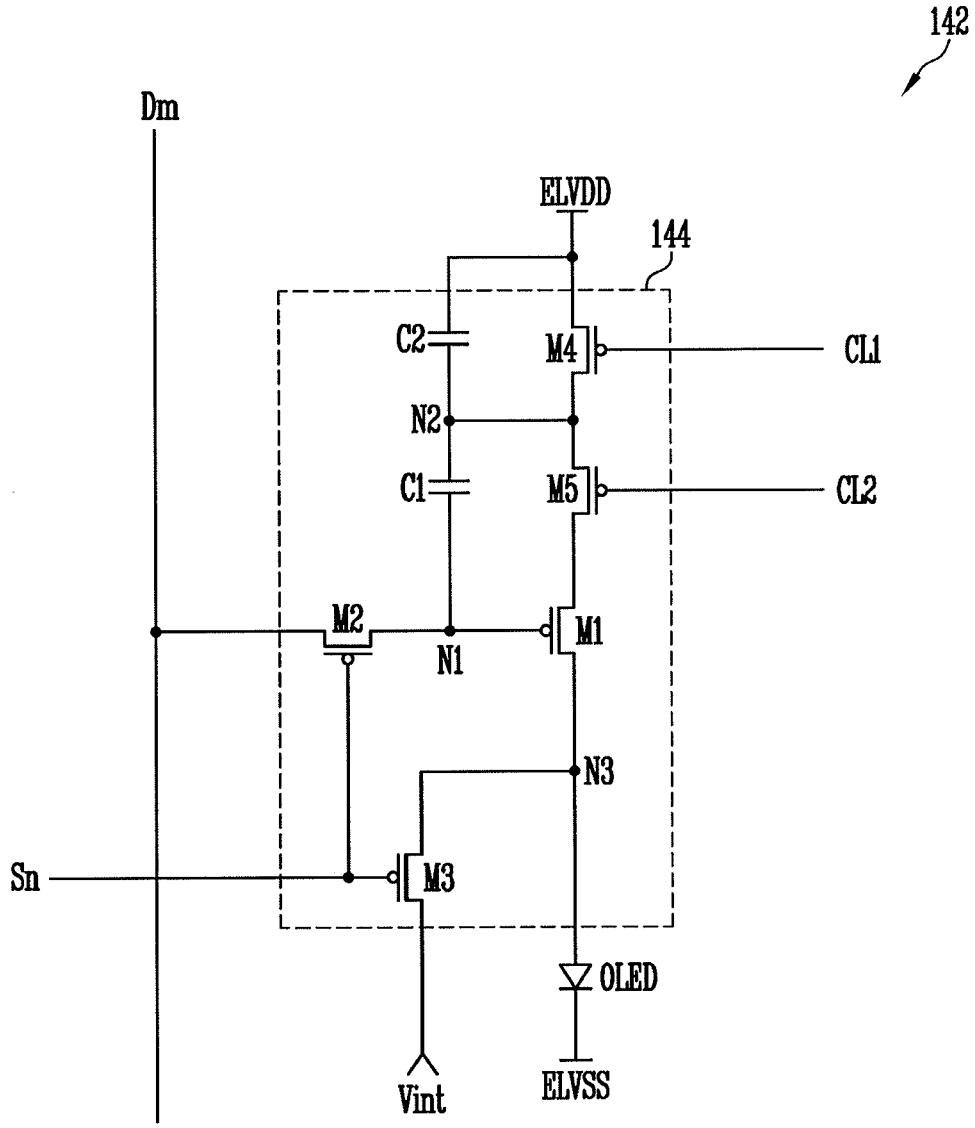

150
Timing controller
130
Data driver
D1
D2
Dm
ELVDD
110
140
120
S1
142
S2
S3
CL1
CL2
Scan driver
Control driver
Sn
ELVSS

FIG. 2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Dm
ELVDD
144
C2
M4
CL1
N2
C1
M5
CL2
M2
N1
M1
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 3

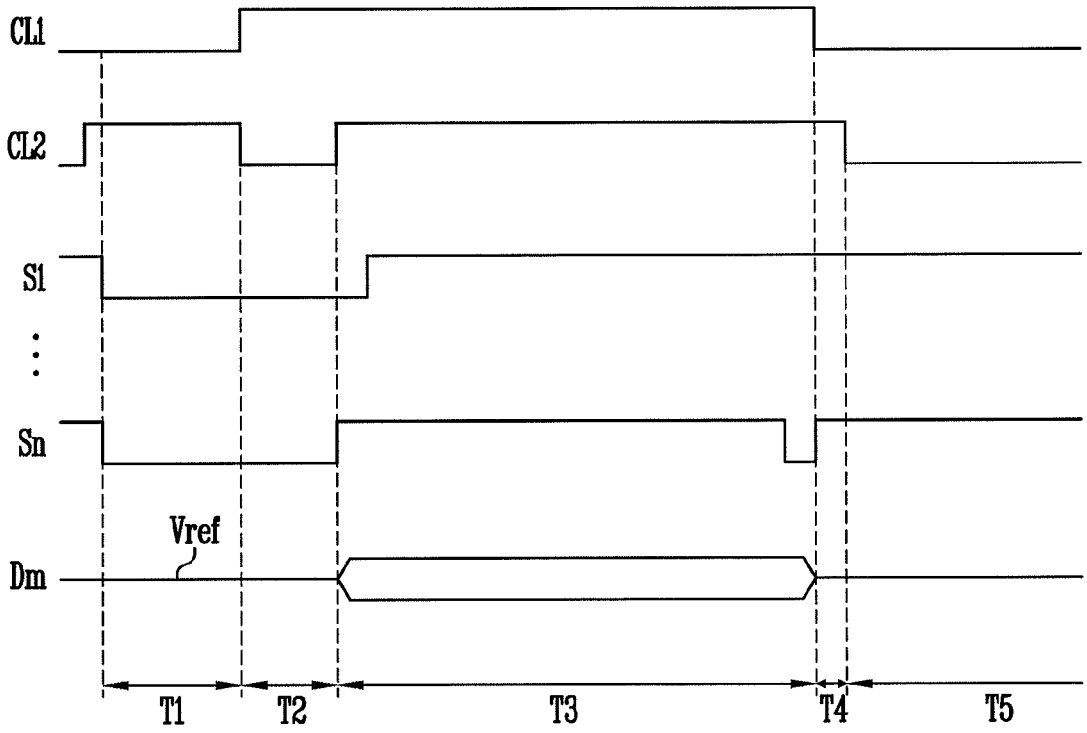
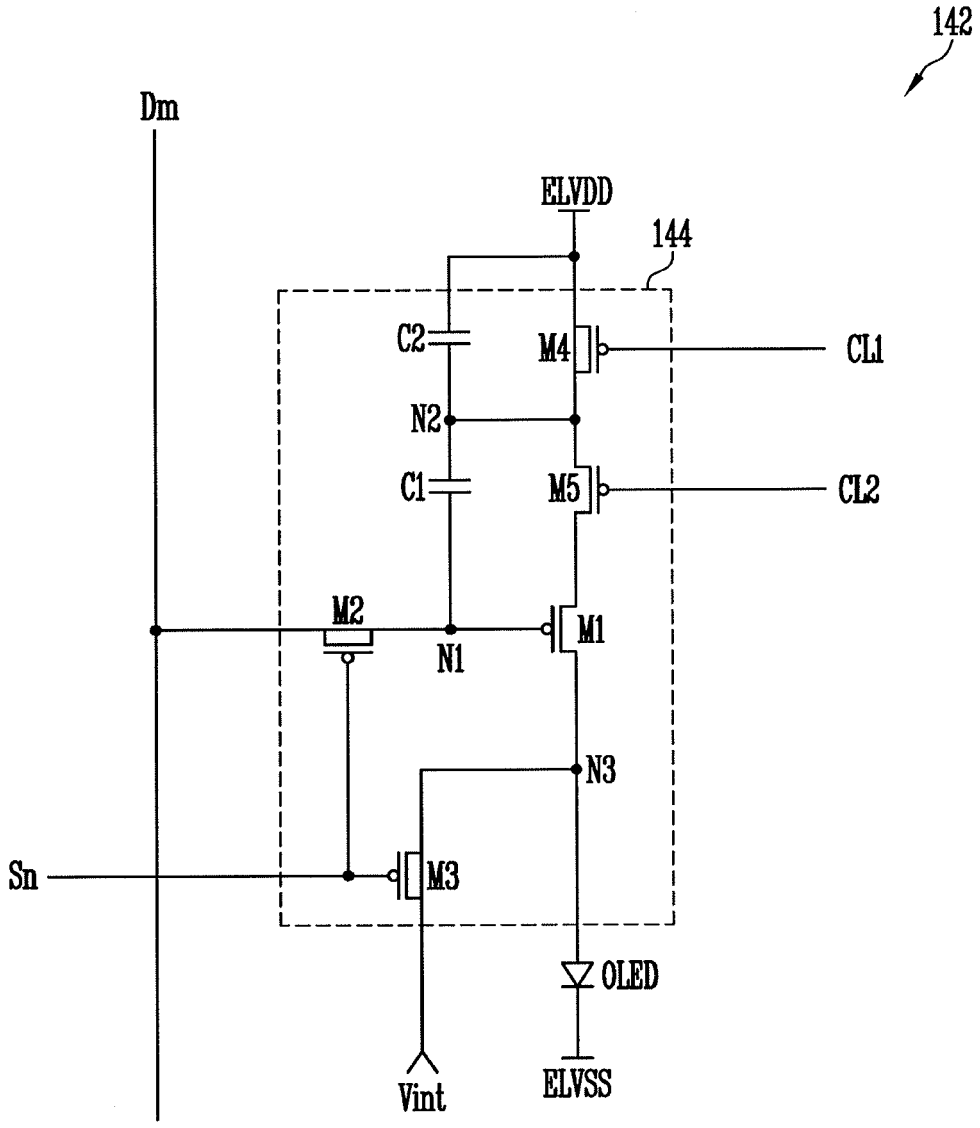


FIG. 4A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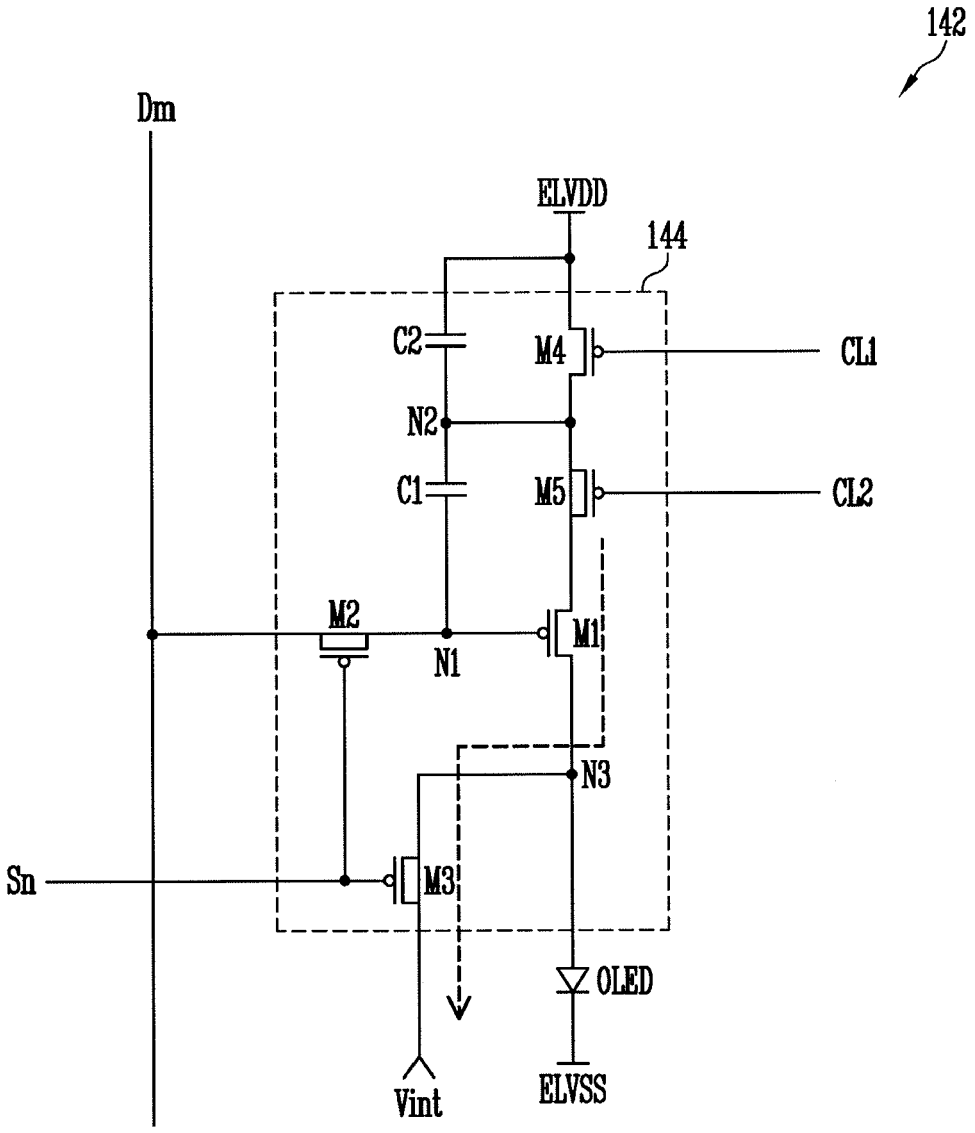
Dm
ELVDD
144
C2
M4
CL1
N2
C1
M5
CL2
M2
N1
M1
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 4B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144
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M4
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C1
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M2
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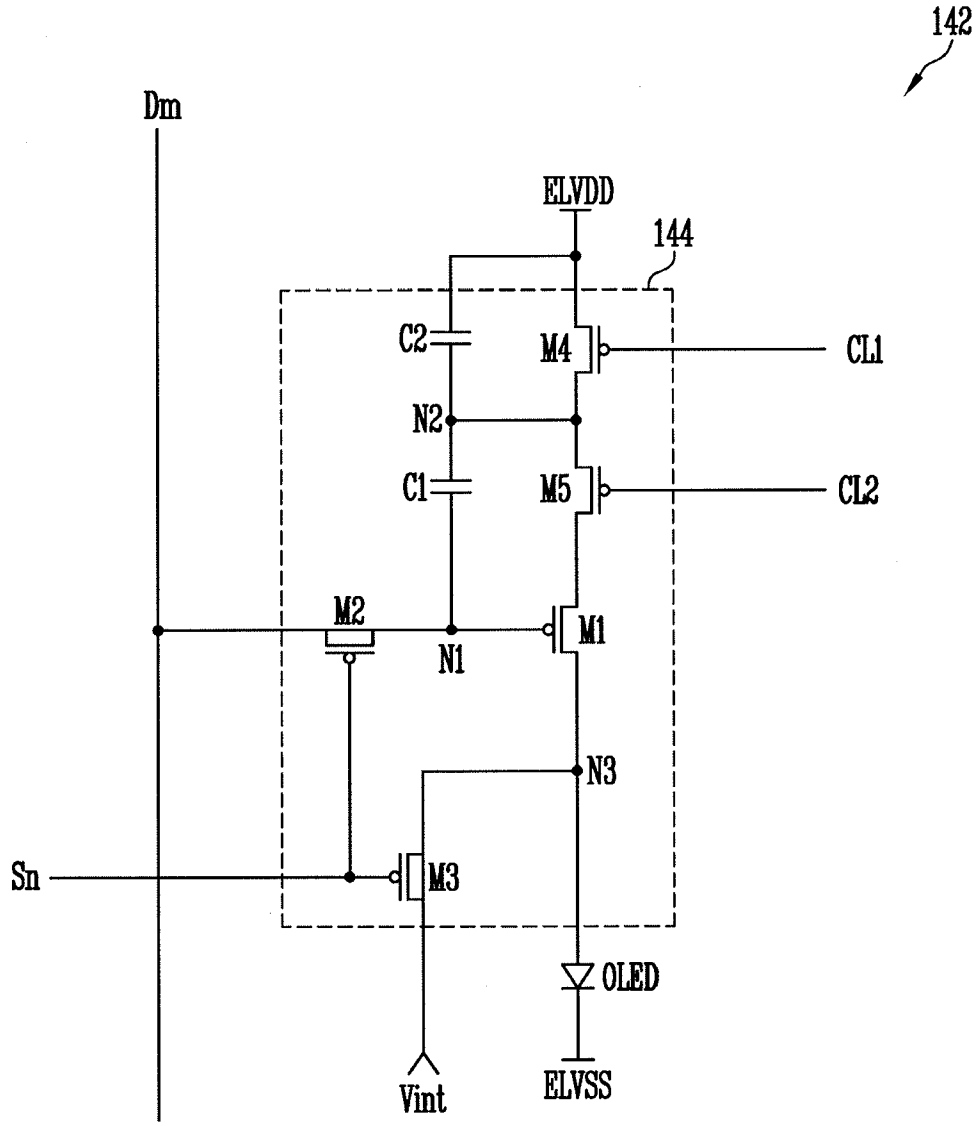
M1
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 4C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144
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CL1
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C1
M5
CL2
M2
N1
M1
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 5

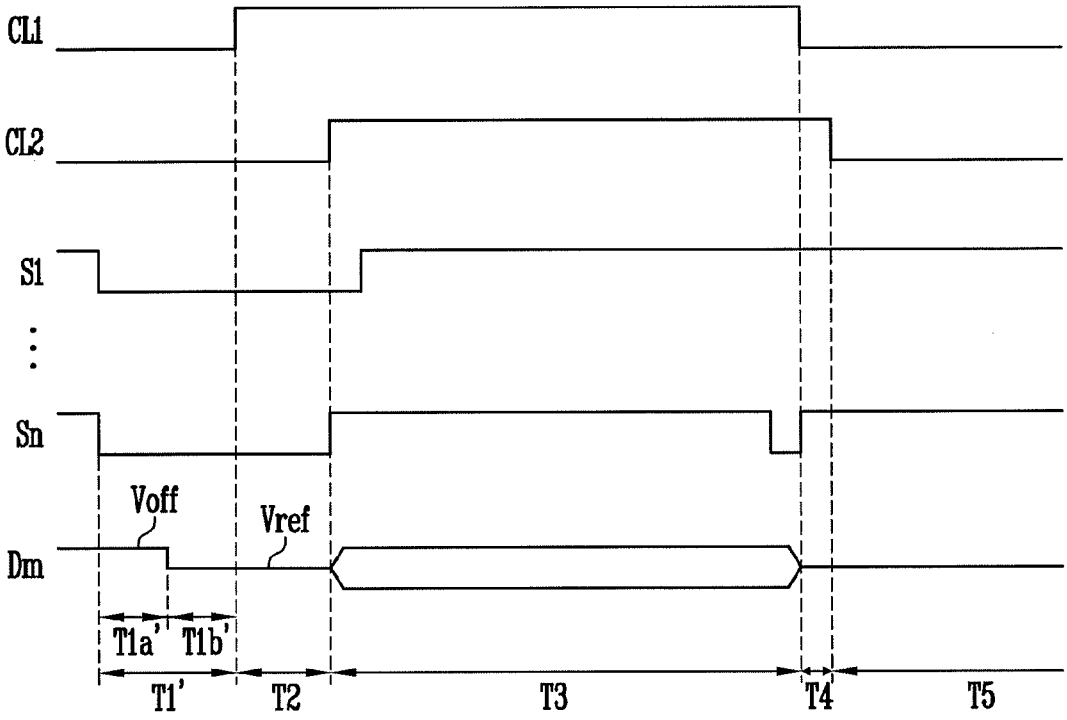


FIG. 6A

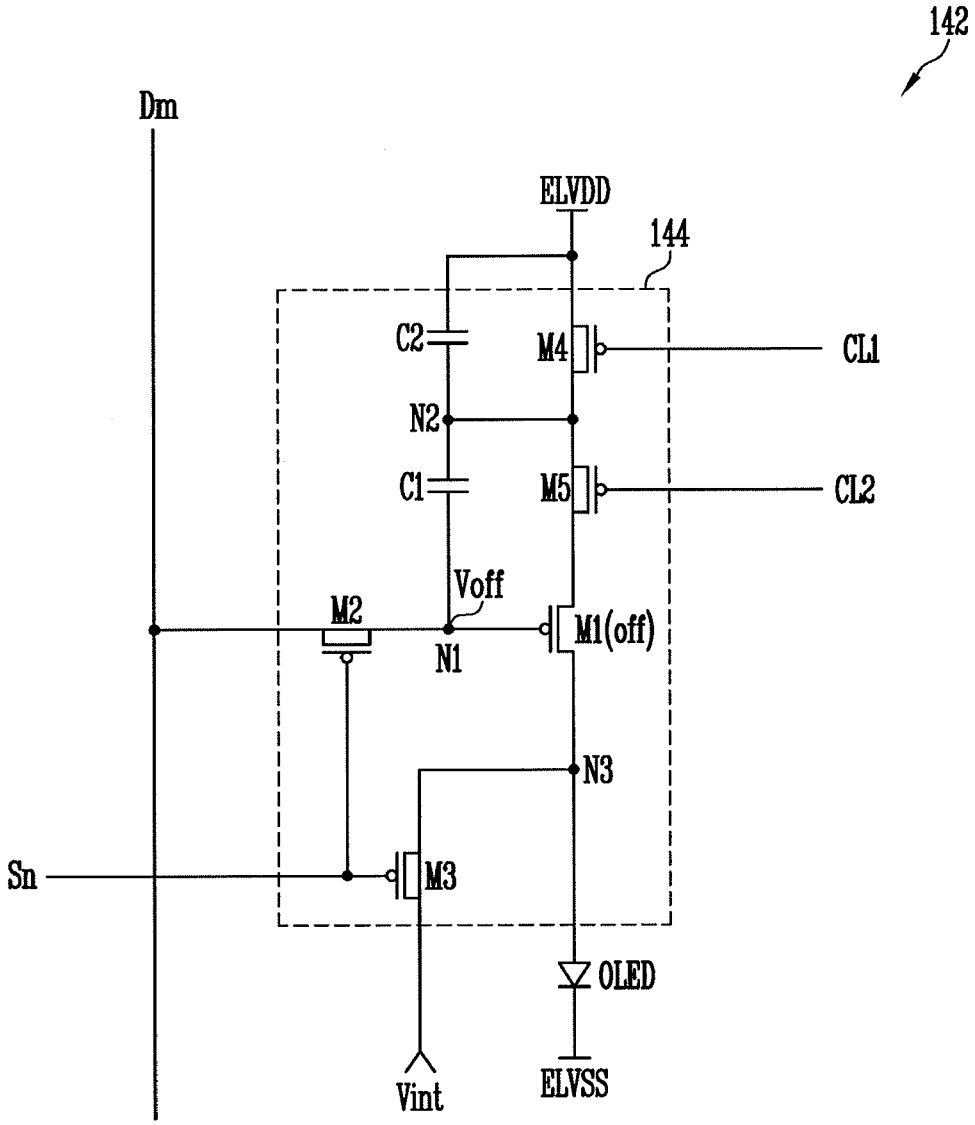
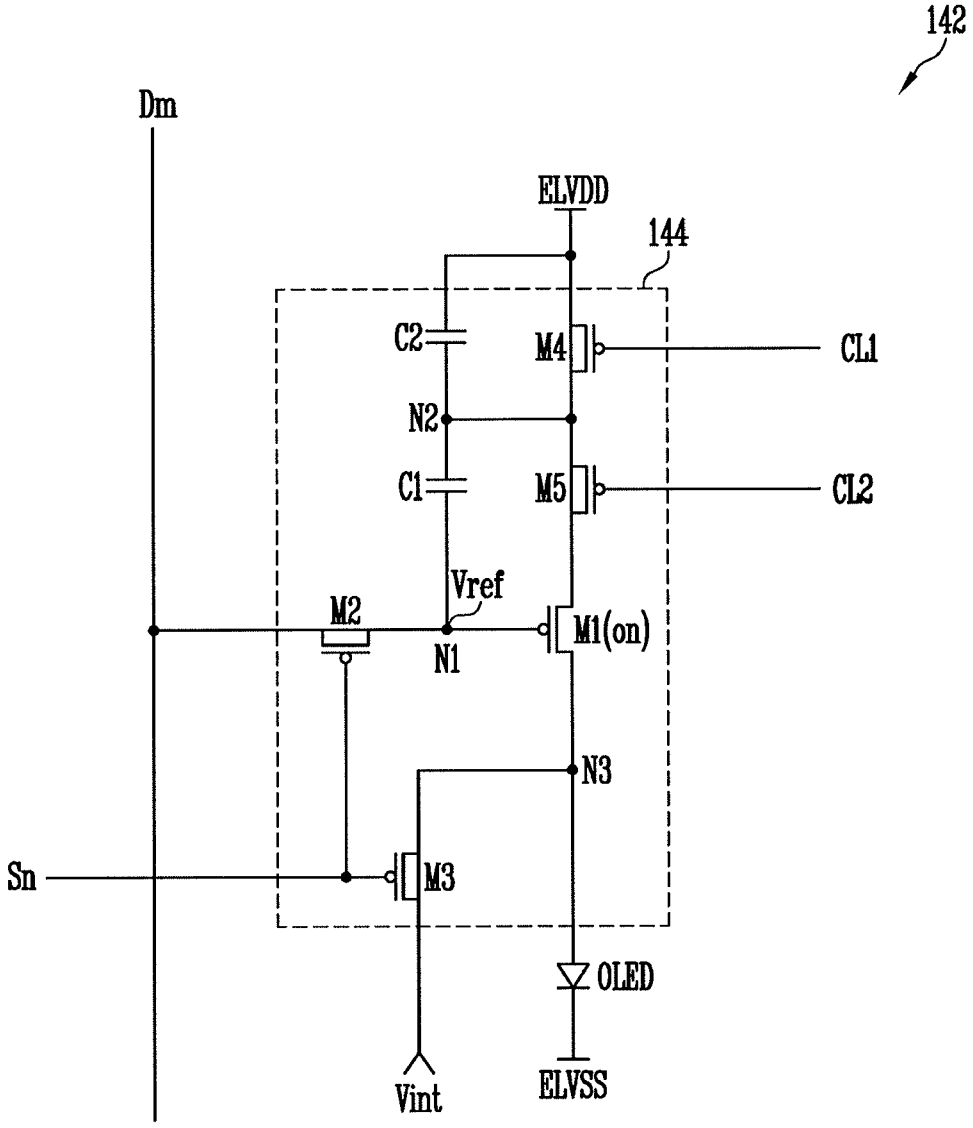

142
Dm
ELVDD
144
C2
M4
CL1
N2
C1
M5
CL2
Voff
M2
M1(off)
N1
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 6B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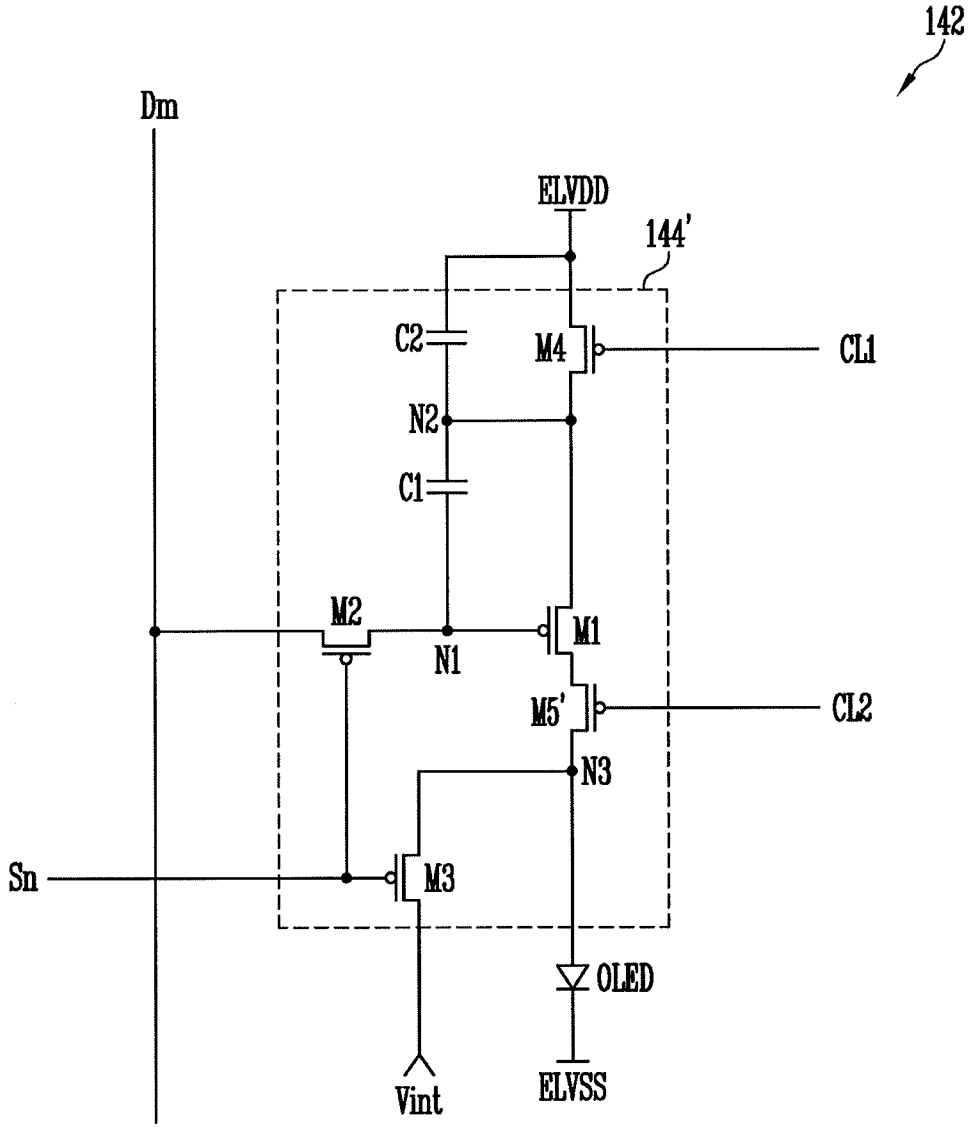
Dm
ELVDD
144
C2
M4
CL1
N2
C1
M5
CL2
Vref
M2
M1(on)
N1
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 7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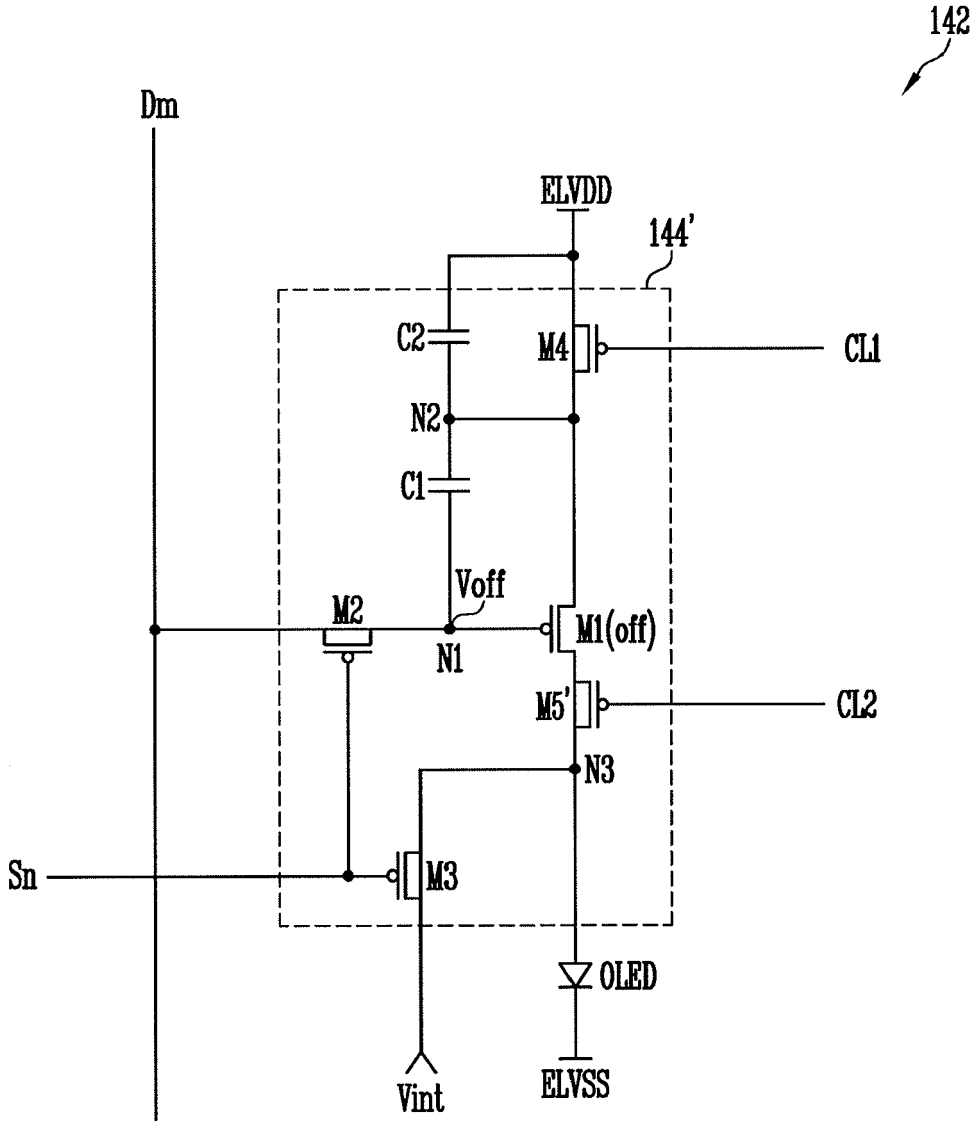
ELVDD
144'
C2
M4
CL1
N2
C1
M2
N1
M1
M5'
CL2
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 8A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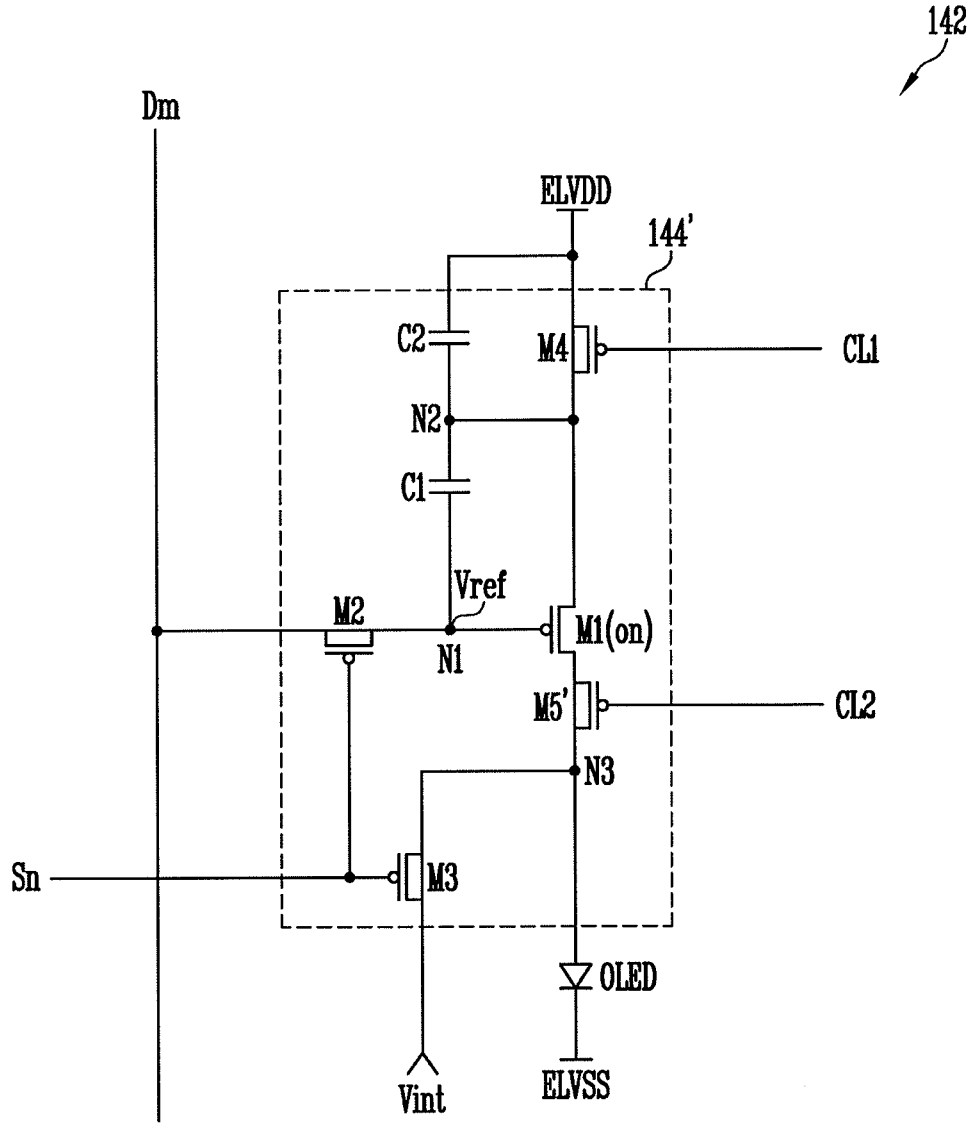
144'
C2
M4
CL1
N2
C1
Voff
M2
M1(off)
N1
M5'
CL2
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 8B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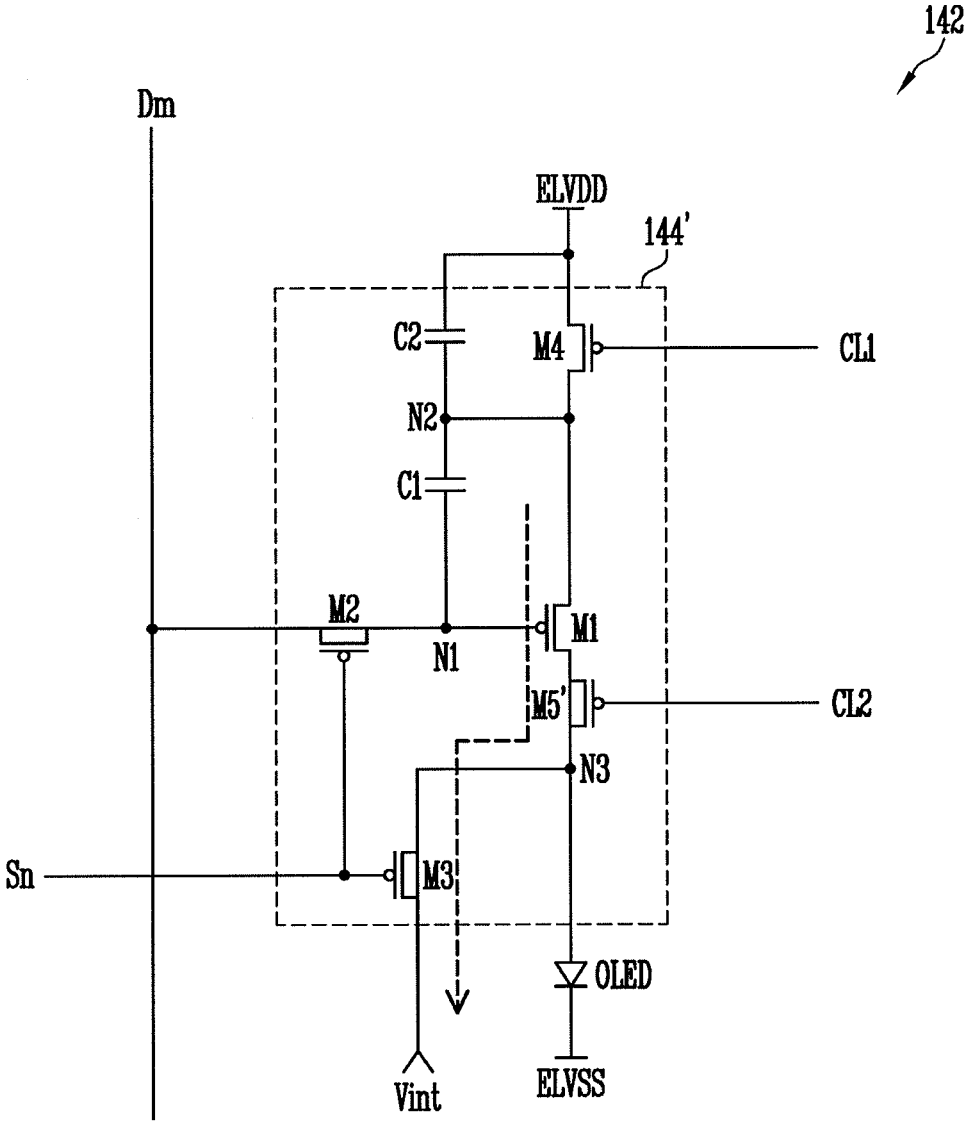
Dm
ELVDD
144'
C2
M4
CL1
N2
C1
Vref
M2
M1(on)
N1
M5'
CL2
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 8C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Dm
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144'
C2
M4
CL1
N2
C1
M2
N1
M1
M5'
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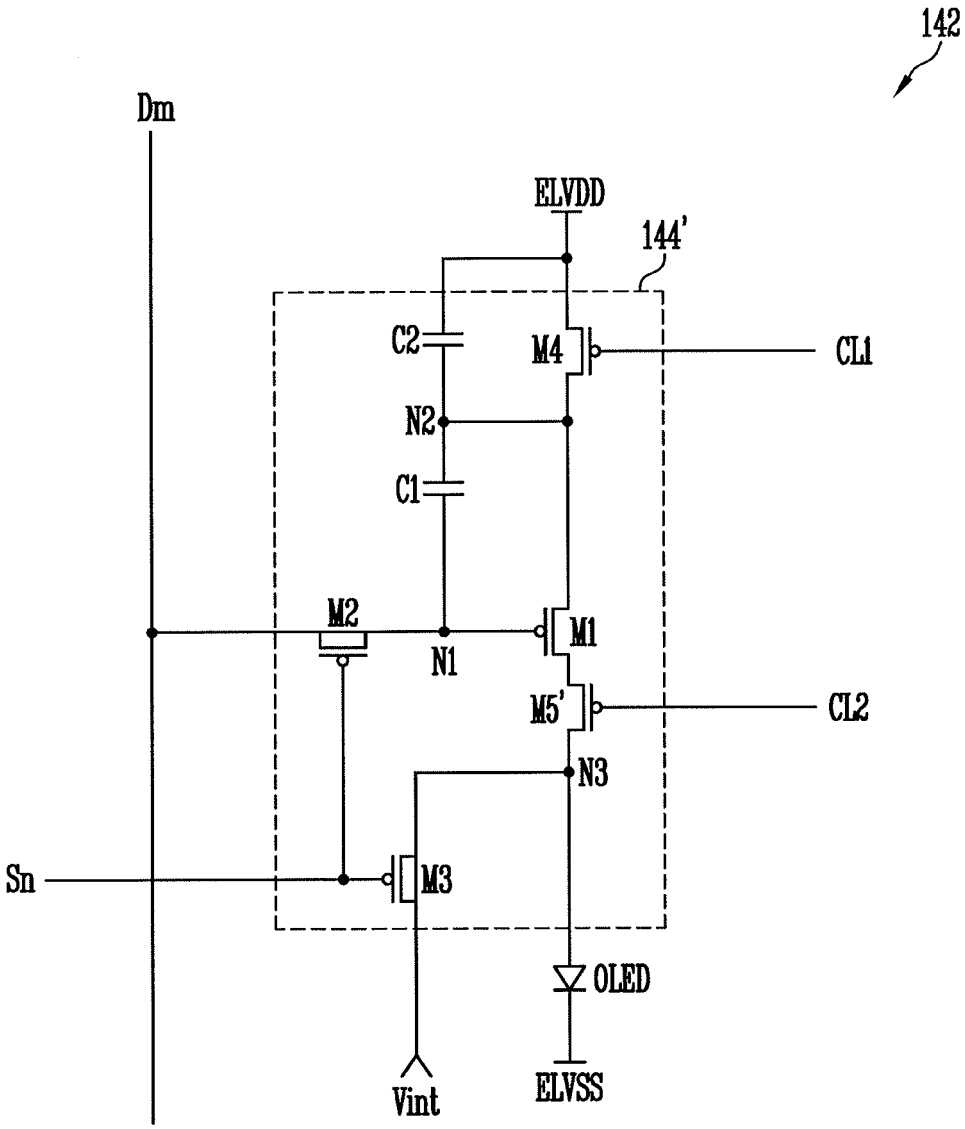
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 8D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ELVDD
144'
C2
M4
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M2
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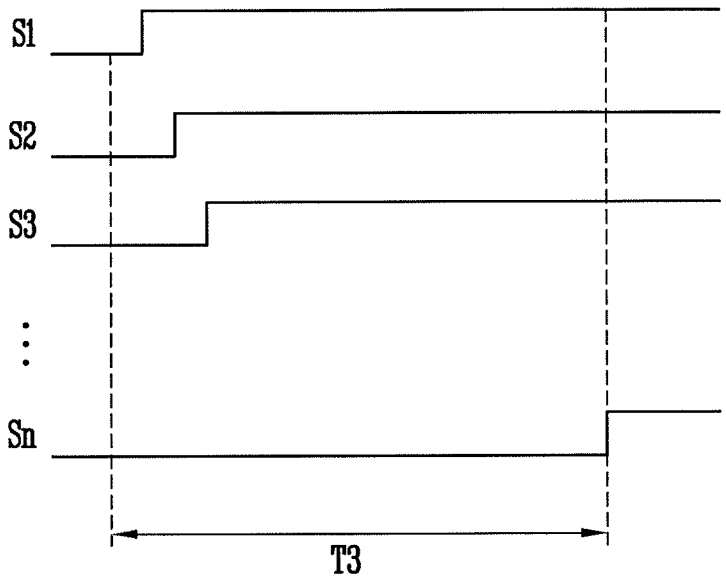
M5'
CL2
N3
Sn
M3
OLED
Vint
ELVSS

FIG. 9



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EUROPEAN SEARCH REPORT

Application Number
EP 14 16 8920

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X Y	US 2011/227903 A1 (CHOI SANG-MOO [KR]) 22 September 2011 (2011-09-22) * paragraphs [0060], [0068] - [0072]; figures 5,6 *	1,4-7 2,3, 8-12,15	INV. G09G3/32
X Y	CN 102 593 151 A (AU OPTRONICS CORP) 18 July 2012 (2012-07-18) * the whole document * & US 2013/169611 A1 (CHANG HUA-GANG [TW] ET AL) 4 July 2013 (2013-07-04) * paragraphs [0035], [0043] - [0054]; figures 1,4 *	1,6,7 2,3,8, 10-12,15	
X	US 2013/043802 A1 (HAN INHYO [KR] ET AL) 21 February 2013 (2013-02-21) * paragraphs [0041] - [0079], [0087] - [0091]; figures 4, 2 *	1-3,6-8, 10-15	
X	US 2012/019498 A1 (JEONG JIN-TAE [KR]) 26 January 2012 (2012-01-26) * paragraphs [0053] - [0115]; figures 2,3,5,6 *	1-3,8, 11,12,15	TECHNICAL FIELDS SEARCHED (IPC) G09G
Y	US 2008/169754 A1 (YANG SUN A [KR] ET AL) 17 July 2008 (2008-07-17) * paragraphs [0139], [0142]; figures 3,4,5,6, 21, 22, 23, ,24, 25, 26 *	2,3, 8-12,15	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	15 July 2014	Vázquez del Real, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 14 16 8920

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15-07-2014

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		US 2008169754 A1	17-07-2008

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	使用其的像素和有机发光显示器		
公开(公告)号	EP2806421A1	公开(公告)日	2014-11-26
申请号	EP2014168920	申请日	2014-05-20
[标]申请(专利权)人(译)	三星显示有限公司 汉阳大学校产学协力团		
申请(专利权)人(译)	三星DISPLAY CO.，LTD. IUCF-HYU（产学合作基金会汉阳大学）		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD. IUCF-HYU（产学合作基金会汉阳大学）		
[标]发明人	JEONG JIN TAE KWON OH KYONG		
发明人	JEONG, JIN-TAE KWON, OH-KYONG		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0852 G09G2300/0861 G09G2320/045 G09G3/30 H01L27/3237 H01L27/3246 H01L27/3248 H01L27/3262 G09G3/3208 G09G5/18 H01L27/3265		
优先权	1020130057871 2013-05-22 KR		
外部链接	Espacenet		

摘要(译)

像素包括有机发光二极管和像素控制电路。像素控制电路包括第一晶体管，第二晶体管和第三晶体管。第一晶体管基于施加到第一节点的电压来控制从第一电源到有机发光二极管的电流量。第二晶体管耦合在第一节点和数据线之间，并且当扫描信号被提供给扫描线时导通。第三晶体管耦合在第一电源和第二节点之间，第二节点是第一和第二电容器的公共端子，它们串联耦合在第一节点和第一电源之间。在操作中，当第一控制信号被提供给第一控制线时，第三晶体管导通。

FIG. 2