

(19)



(11)

**EP 2 592 617 B1**

(12)

**EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:  
**13.07.2016 Bulletin 2016/28**

(51) Int Cl.:  
**G09G 3/32<sup>(2006.01)</sup>**

(21) Application number: **12187449.9**

(22) Date of filing: **05.10.2012**

**(54) Organic light emitting diode display device**

Organische lichtemittierende Diodenanzeigevorrichtung

Dispositif d'affichage à diode électroluminescente organique

(84) Designated Contracting States:  
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR**

(30) Priority: **08.11.2011 KR 20110115577**

(43) Date of publication of application:  
**15.05.2013 Bulletin 2013/20**

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**Description****CROSS-REFERENCE TO RELATED APPLICATION**

5 **[0001]** This application claims priority under 35 U.S.C. § 119(a) of Korean Patent Application No. 10-2011-0115577, filed on Nov 8, 2011, which is incorporated by reference in its entirety.

**BACKGROUND**10 **Technical Field**

**[0002]** The following description relates to an organic light emitting diode display device which compensates a threshold voltage of a driving TFT.

15 **Discussion of the Related Art**

**[0003]** There has been an increasing demand for a display device for displaying an image together with the growth of an information-oriented society, and various flat panel displays such as liquid crystal displays (LCDs), plasma display panels (PDPs), and organic light emitting diodes (OLEDs) have been widely used in recent years. Among the flat panel displays, organic light emitting diode display devices are driven at a low voltage, are thin, have a wide viewing angle and a quick response speed. Among the organic light emitting diode display devices, active matrix type organic light emitting diode display devices have been widely used since they have a plurality of pixels disposed in a matrix form to display an image.

20 **[0004]** A display panel of the active matrix type organic light emitting diode display device comprises a plurality of pixels arranged in matrix. Each pixel includes a scan TFT (thin film transistor) supplying data voltage from data line in response to scan signal from the scan line and a driving TFT controlling the amount of current supplied to an organic light emitting diode in response to the data voltage supplied to a gate electrode. At this point, the current  $I_{ds}$  between a drain electrode and a source electrode of the driving TFT supplied to the organic light emitting diode can be represented by Equation 1:

30

[Equation 1]

35

$$I_{ds} = k' \cdot (V_{gs} - V_{th})^2$$

**[0005]** In equation 1,  $k'$  indicates a proportionality factor determined by the structure and physical properties of the driving TFT,  $V_{gs}$  indicates a voltage difference between the gate electrode and source electrode of the driving TFT, and  $V_{th}$  indicates a threshold voltage of the driving TFT.

40 **[0006]** Meanwhile, due to a threshold voltage shift caused by deterioration of the driving TFT, the threshold voltage  $V_{th}$  of the driving TFT of each of the pixels has a different value. The current  $I_{ds}$  between the drain electrode and source electrode of the driving TFT is dependent on the threshold voltage  $V_{th}$  of the driving TFT. Thus, the current  $I_{ds}$  - between the drain electrode and source electrode of the driving TFT of each pixel is varied even if the same data voltage is supplied to each of the pixels. Accordingly, there arises the problem that the luminance of light emitted from the organic light emitting diode of each of the pixels is varied even if the same data voltage is supplied to each of the pixels. To solve this problem, various types of pixel structures for compensating the threshold voltage of the driving TFT of each of the pixels have been proposed.

45 **[0007]** However, recently, the organic light emitting diode display device is driven by a high frequency in order to implement a 3D image or improve an image quality. Accuracy of sensing a threshold voltage gets lower because a period for sensing a threshold voltage is shortened due to the high frequency driving.

50 **[0008]** Also, recently, the organic light emitting diode display device has a big size and a high resolution. Due to a big size and a high resolution, line resistance increases because a length of the line becomes longer. Finally, RC delay can be occurred. The period for sensing a threshold voltage is shortened due to RC delay. Therefore, accuracy of sensing a threshold voltage gets lower.

55 JP2006023515A discloses an active-matrix OLED pixel circuit compensating for the drive transistor threshold voltage variations.

**SUMMARY**

[0009] One object of the embodiments of this application provides an organic light emitting diode display device which improves accuracy of sensing a threshold voltage of a driving TFT.

[0010] To achieve these objects and other advantages and in accordance with the purpose according to one aspect of the invention, an organic light emitting diode display device comprising: a display panel configured to include data lines, first scan lines, second scan lines, control lines, emission lines, and a plurality of pixels disposed in a matrix form, wherein each of the pixels including: a driving TFT configured to have a gate electrode coupled to a first node and a source electrode coupled to a second node; an organic light emitting diode configured to have an anode electrode coupled to a drain electrode of the driving TFT and a cathode electrode coupled to a first level voltage supply source supplying a first level voltage; a first TFT configured to supply a data voltage of the data line to the first node in response to a first scan signal of the first scan line; a second TFT configured to supply a reference voltage from a reference voltage supply source to the first node in response to a second scan signal of the second scan line; a third TFT configured to supply a second level voltage higher than the first level voltage to the second node in response to an emission signal of the emission line; a fourth TFT configured to couple the second node to a third node in response to a control signal of the control line; a first capacitor coupled between the first node and the third node; a second capacitor coupled between the third node and a second voltage supply source supplying the second level voltage, and wherein the control signal is inverted to a second logic level voltage from a first logic level voltage after the emission signal is inverted to the second logic level voltage from the first logic level voltage during a period for emitting the organic light emitting diode, and wherein the reference voltage is lower than a voltage subtracting a threshold voltage of the driving TFT from the second level voltage and is higher than the first level voltage.

[0011] The features and advantages described in this summary and the following detailed description are not intended to be limiting. Many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification and claims.

**BRIEF DESCRIPTION OF THE DRAWINGS****[0012]**

FIG. 1 illustrates an equivalent circuit diagram of a pixel of a display panel according to an exemplary embodiment of the present invention;

FIG. 2 illustrates waveform diagram showing signals input to the pixel of FIG. 1;

FIG. 3 illustrates a table showing voltage variation of nodes;

FIG. 4 illustrates a graph showing a compensation error in accordance with threshold voltage variation of a driving TFT;

FIG. 5 illustrates a block diagram schematically showing an organic light emitting diode display device according to an exemplary embodiment of the present invention.

**DETAILED DESCRIPTION**

[0013] The invention will be described more fully hereinafter with reference to the accompanying drawings, in which example embodiments of the inventions are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Like reference numerals designate like elements throughout the specification. In the following description, if it is decided that the detailed description of known function or configuration related to the invention makes the subject matter of the invention unclear, the detailed description is omitted.

[0014] FIG. 1 illustrates an equivalent circuit diagram of a pixel of a display panel according to an exemplary embodiment of the present invention. With reference to FIG. 1, the pixel of the display panel includes a driving TFT (Thin Film Transistor) DT, an organic light emitting diode OLED, a control circuit, and capacitors.

[0015] The driving TFT DT controls an amount of current  $I_{ds}$  between a source electrode and a drain electrode to vary depending on an amount of the voltage applied to a gate electrode. A gate electrode of the driving TFT DT is coupled to the first node N1, a source electrode thereof is coupled to the second node N2, and a drain electrode thereof is coupled to an anode electrode of the organic light emitting diode OLED.

[0016] The anode electrode of the organic light emitting diode OLED is coupled to the drain electrode of the driving

TFT DT, a cathode electrode of thereof is coupled to a first level voltage supply source. The organic light emitting diode OLED emits light depending on the current  $I_{ds}$  between the drain electrode and source electrode of the driving TFT Td.

**[0017]** The control circuit includes a first TFT T1, a second TFT T2, a third TFT T3, and a fourth TFT T4. The first TFT T1 supplies a data voltage DATA of a data line DL to the first node N1 in response to a first scan signal SCAN1 of a first scan line SL1. The data voltage DATA represents an intended intensity level of the OLED. A gate electrode of the first TFT T1 is coupled to the scan line SL1, a source electrode thereof is coupled to the data line DL, and a drain electrode thereof is coupled to the first node N1.

**[0018]** The second TFT T2 initializes a voltage of the first node N1 as a reference voltage from a reference voltage supply source REF\_S in response to a second scan signal SCAN2 of a second scan line SL2. A gate electrode of the second TFT T2 is coupled to the second scan line SL2, a source electrode thereof is coupled to the first node N1, and a drain electrode thereof is coupled to the reference voltage supply source REF\_S.

**[0019]** The third TFT T3 supplies a second level voltage from a second level voltage supply source to the second node N2 in response to an emission signal EM of an emission line EML. A gate electrode of the third TFT T3 is coupled to the emission line EML, a source electrode thereof is coupled to the second level voltage supply source, and a drain electrode thereof is coupled to the second node N2.

**[0020]** The fourth TFT T4 connects a third node N3 with the second node N2 in response to a control signal MG of a control line MGL. A gate electrode of the fourth TFT T4 is coupled to the control line MGL, a source electrode thereof is coupled to the second node N2, and a drain electrode thereof is coupled to the third node N3.

**[0021]** A first capacitor C1 is coupled between the first node N1 and the third node N3. A second capacitor C2 is coupled between the third node N3 and the second level voltage supply source.

**[0022]** The first node N1 is a contact between the gate electrode of the driving TFT Td, the drain electrode of the first TFT T1, and an electrode of the first capacitor C1. The second node N2 is a contact between the source electrode of the driving TFT Td, the drain electrode of the third TFT T3, and the source electrode of the fourth TFT T4. The third node N3 is a contact between the drain electrode of the fourth TFT T4, the other electrode of the first capacitor C1, and an electrode of the second capacitor C2. The other electrode of the second capacitor is coupled to the second level voltage supply source.

**[0023]** Each of the first to fourth TFTs T1, T2, T3, and T4 and the driving TFT Td of the pixel according to the exemplary embodiment may be composed of a thin film transistor. Semiconductor layers of the first to fourth TFTs T1, T2, T3, and T4 and the driving TFT Td each may be composed of any one of amorphous silicon (a-Si), polycrystalline silicon (poly-Si), and oxide semiconductor. Moreover, the exemplary embodiment has been described focusing on an example in which the first to fourth TFTs T1, T2, T3, and T4 and the driving TFT Td each are implemented as a P-type. In other embodiments, one or more of the TFTs may be implemented with N-type.

**[0024]** The first level voltage supply source may be set to a low potential voltage supply source VSS\_S and the second level voltage supply source may be set to a high potential voltage supply source VDD\_S. The low potential voltage supply source VSS\_S supplies a low potential voltage VSS, and the high potential voltage supply source VDD\_S supplies a high potential voltage VDD higher than the low potential voltage VSS. The low supply voltage VSS and the high supply voltage VDD may be set in accordance with characteristics of the driving TFT DT and the organic light emitting diode OLED. The reference voltage REF is a voltage for initializing the first node N1. The reference voltage REF may be set to a voltage lower than a voltage subtracting a threshold voltage of the driving TFT DT from the high potential voltage VDD. Also, the reference voltage REF may be set to a voltage higher than the low potential voltage VSS.

**[0025]** FIG. 2 illustrates waveform diagram showing signals input to the pixel of FIG.1. The first scan signal SCAN1, the second scan signal SCAN2, the control signal MG, the emission signal EM input to the pixel of the display panel is illustrated in FIG 2. Also, the data voltage DATA of the data line DL is illustrated in FIG. 2.

**[0026]** With reference to FIG.2, the first scan signal SCAN1, the second scan signal SCAN2, the control signal MG, and the emission signal EM are signals for controlling the first to fourth TFTs (T1, T2, T3, T4). Each cycle of the first scan signal SCAN1, the second scan signal SCAN2, the control signal MG, and the emission signal EM may be one frame period. One frame period indicates a period in which data voltages are supplied to all pixels of the display panel. Each of the first scan signal SCAN1, the second scan signal SCAN2, the control signal MG, and the emission signal EM swings between a first logic level voltage and a second logic level voltage. In FIG.2, the first logic level voltage may be a gate high voltage VGH and the second level voltage may be a gate low voltage VGL lower than the gate high voltage.

**[0027]** One frame period includes first to fourth periods t1, t2, t3, t4. The first period t1 is a period for initializing the first node N1, the second node N2, and the third node N3. The second period t2 is a period for sensing the threshold voltage of the driving TFT DT. The third period t3 is a period for supplying the data voltage to the first node N1. The fourth period t4 is a period for emitting the organic light emitting diode OLED.

**[0028]** The first scan signal SCAN1 is generated at the gate high voltage VGH during the first period t1. Also, the second scan signal SCAN2, the control signal MG, and the emission signal EM are generated at the gate low voltage VGL during the first period t1. The first scan signal SCAN1 and the emission signal EM are generated at the gate high voltage VGH during the second period t2. Also, the second scan signal SCAN2 and the control signal MG are generated

at the gate low voltage VGL during the second period t2. The second scan signal SCAN2, the control signal MG, and the emission signal EM are generated at the gate high voltage VGH during the third period t3. Also, the first scan signal SCAN1 is generated at the gate low voltage VGL during the third period t3. The first scan signal SCAN1 and the second scan signal SCAN2 are generated at the gate high voltage VGH during the fourth period t4. Also, the control signal MG and the emission signal EM are generated at the gate low voltage VGL during the fourth period t4. Especially, during the fourth period t4, the control signal MG is inverted to the gate low voltage VGL from the gate high voltage VGH after the emission signal EM is inverted to the gate low voltage VGL from the gate high voltage VGH.

**[0029]** A cycle of the data voltage DATA is one horizontal period. Accordingly, the third period t3 in which the data voltage DATA is supplied may be one horizontal period in FIG. 2. One horizontal period indicates a period in which data voltages are supplied to pixels of one horizontal line of the display panel. However, each of the first period t1, the second period t2, the third period t3, and the fourth period t4 may be a few horizontal periods or dozen(s) of horizontal periods in order to improve picture quality of the pixel, and may be predetermined by an experiment.

**[0030]** FIG 3 illustrates a table showing voltage variation of nodes. Hereinafter, the operation of the pixel according to the exemplary embodiment during the first to fourth periods t1, t2, t3, t4 will be described in detail with reference to FIGS. 1 to 3. In FIG. 4, the first node voltage Vn1 indicates a voltage at the first node N1, the second node voltage Vn2 indicates a voltage at the second node N2, and the third node voltage Vn3 indicates a voltage at the third node N3.

**[0031]** Firstly, during the first period t1, the first scan signal SCAN1 having the gate high voltage VGH is supplied to the pixel through the first scan line SL1. The second scan signal SCAN2 having the gate low voltage VGL is supplied to the pixel through the second scan line SL2. The control signal MG having the gate low voltage VGL is supplied to the pixel through the control line MG. The emission signal EM having the gate low voltage VGL is supplied to the pixel through the emission line EM.

**[0032]** The first TFT T1 is turned off by the first scan signal SCAN1 having the gate high voltage VGH. The second TFT T2 is turned on in response to the second scan signal SCAN2 having the gate low voltage VGL. The first node N1 is coupled to the reference voltage supply source REF\_S due to turn-on of the second TFT T2. Thus, a first node voltage Vn1 is discharged to the reference voltage REF. The third TFT T3 is turned on in response to the emission signal EM having the gate low voltage VGL. The second node N2 is coupled to the high potential voltage supply source VDD\_S due to turn-on of the third TFT T3. Thus, a second node voltage Vn2 is charged to the high potential voltage VDD. The fourth TFT T4 is turned on in response to the control signal having the gate low voltage VGL. The third node N3 is coupled to the second node N2 due to turn-on of the fourth TFT T4. Thus, a third node voltage Vn3 is charged to the high potential voltage VDD.

**[0033]** Secondly, during the second period t2, the first scan signal SCAN1 having the gate high voltage VGH is supplied to the pixel through the first scan line SL1. The second scan signal SCAN2 having the gate low voltage VGL is supplied to the pixel through the second scan line SL2. The control signal MG having the gate low voltage VGL is supplied to the pixel through the control line MG. The emission signal EM having the gate high voltage VGH is supplied to the pixel through the emission line EM.

**[0034]** The first TFT T1 is turned off by the first scan signal SCAN1 having the gate high voltage VGH. The second TFT T2 is turned on in response to the second scan signal SCAN2 having the gate low voltage VGL. The first node N1 is coupled to the reference voltage supply source REF\_S due to turn-on of the second TFT T2. Thus, the first node voltage Vn1 is discharged to the reference voltage REF. The third TFT T3 is turned off by the emission signal EM having the gate high voltage VGH. The second node N2 is floated due to turn-off of the third TFT T3. The fourth TFT T4 is turned on in response to the control signal having the gate low voltage VGL. The third node N3 is coupled to the second node N2 due to turn-on of the fourth TFT T4. Thus, the second node voltage Vn2 and the third node voltage Vn3 are substantially same.

**[0035]** The second node N2 and the third node N3 may sense the threshold voltage Vth of the driving TFT DT because the second node N2 is floated during the second period t2. The difference between the first node voltage Vn1 and the second node voltage Vn2 is greater than the threshold voltage Vth of the driving TFT DT during the second period t2. The difference between the first node voltage Vn1 and the second node voltage Vn2 indicates the difference between the gate electrode of the driving TFT DT and the source electrode thereof. Thus, current flows through the driving TFT DT until the difference between the first node voltage Vn1 and the second node voltage Vn2 reaches the threshold voltage Vth of the driving TFT DT. Accordingly, the second node voltage Vn2 would be lowered to the difference voltage REF-Vth between the reference voltage REF and the threshold voltage Vth of the driving TFT DT during the second period t2. Also, the third node voltage Vn3 would be lowered to the difference voltage REF-Vth between the reference voltage REF and the threshold voltage Vth of the driving TFT DT during the second period t2 because the third node N3 is coupled to the second node N2.

**[0036]** In FIG.2, the second period t2 may be two horizontal periods. However, the second period t2 may be a few horizontal periods or dozen(s) of horizontal periods, and may be predetermined by an experiment. The embodiments described herein may improve accuracy of sensing the threshold voltage Vth of the driving TFT DT even though an organic light emitting diode display device drives high frequency such as 240Hz because sensing periods are long

enough to sense the threshold voltage  $V_{th}$  of the driving TFT DT.

**[0037]** Thirdly, during the third period  $t_3$ , the first scan signal SCAN1 having the gate low voltage VGL is supplied to the pixel through the first scan line SL1. The second scan signal SCAN2 having the gate high voltage VGH is supplied to the pixel through the second scan line SL2. The control signal MG having the gate high voltage VGH is supplied to the pixel through the control line MG. The emission signal EM having the gate high voltage VGH is supplied to the pixel through the emission line EM.

**[0038]** The first TFT T1 is turned on in response to the first scan signal SCAN1 having the gate low voltage VGL. The first node N1 is coupled to the data line DL due to turn-on of the first TFT T1. The second TFT T2 is turned off by to the second scan signal SCAN2 having the gate high voltage VGH. Thus, the first node voltage  $V_{n1}$  is charged to the data voltage DATA. The third TFT T3 is turned off by the emission signal EM having the gate high voltage VGH. The second node N2 is floated due to turn-off of the third TFT T3. The fourth TFT T4 is turned off by the control signal having the gate high voltage VGH. The third node N3 is not coupled to the second node N2 due to turn-off of the fourth TFT T4. Thus, the third node N3 is floated.

**[0039]** The amount of voltage variation of the first node N1 during the third period  $t_3$  is applied to the third node N3 through the first capacitor C1. That is, "REF-DATA" which corresponds to the amount of the voltage variation of the first node N1 during the third period  $t_3$  is applied to the third node N3 through the first capacitor C1. The third node N3 is located between the first capacitor C1 and the second capacitor C2 that are coupled in series. Hence, the amount of voltage variation in the third node N3 is based on the ratio of  $C'$  as shown in Equation 2:

[equation 2]

$$C' = \frac{CA1}{CA1+CA2}$$

**[0040]** In Equation 2, CA1 indicates the capacitance of the first capacitor C1, and CA2 indicates the capacitance of the second capacitor C2. Consequently, the second node voltage  $V_{n2}$  is lowered to 'REF-Vth-C'(REF-DATA)' during period  $t_3$ .

**[0041]** The fourthly, during the fourth period  $t_4$ , the first scan signal SCAN1 having the gate high voltage VGH is supplied to the pixel through the first scan line SL1. The second scan signal SCAN2 having the gate high voltage VGH is supplied to the pixel through the second scan line SL2. The control signal MG having the gate low voltage VGL is supplied to the pixel through the control line MG. The emission signal EM having the gate low voltage VGL is supplied to the pixel through the emission line EM. Especially, during the fourth period  $t_4$ , the control signal MG is inverted to the gate low voltage VGL from the gate high voltage VGH after the emission signal EM is inverted to the gate low voltage VGL from the gate high voltage VGH.

**[0042]** The first TFT T1 is turned off by the first scan signal SCAN1 having the gate high voltage VGH. The second TFT T2 is turned off by to the second scan signal SCAN2 having the gate high voltage VGH. Thus, the first node is floated due to turn-off of the first TFT T1 and turn-off of the second TFT T2. The third TFT T3 is turned on in response to the emission signal EM having the gate low voltage VGL. The second node N2 is coupled to the high potential voltage supply source VDD\_S due to turn-on off the third TFT T3. Thus, the second node voltage  $V_{n2}$  is charged to high potential voltage VDD. The fourth TFT T4 is turned on in response to the control signal having the gate low voltage VGL. The third node N3 is coupled to the second node N2 due to turn-on of the fourth TFT T4. Thus, a third node voltage  $V_{n3}$  is charged to the high potential voltage VDD.

**[0043]** The amount of voltage variation of the third node N3 during the fourth period  $t_4$  is applied to the first node N1 through the first capacitor C1. That is, "REF-Vth-C'(REF-DATA)-VDD" which corresponds to the amount of the voltage variation of the third node N3 during the fourth period  $t_4$  is applied to the first node N1 through the first capacitor C1. Therefore, the first node voltage  $V_{n1}$  is changed to "DATA-{REF-Vth-C'(REF-DATA)-VDD}".

**[0044]** The current  $I_{ds}$  between the drain and source of the driving TFT Td is supplied to the organic light emitting diode OLED. The current  $I_{ds}$  between the drain and source of the driving TFT Td is represented by Equation 3:

[Equation 3]

$$I_{ds} = k' \cdot (V_{gs} - V_{th})^2$$

[0045] In equation 3,  $k'$  indicates a proportionality factor determined by the structure and physical properties of the driving TFT DT, which is determined by the mobility, channel width, channel length, etc. of the driving TFT Td.  $V_{gs}$  indicates the voltage difference between the gate electrode and source electrode of the driving TFT Td.  $V_{th}$  indicates the threshold voltage of the driving TFT Td. " $V_{gs} - V_{th}$ " during the fourth period  $t_4$  is as shown in Equation 4:

[Equation 4]

$$V_{gs} - V_{th} = [DATA - \{REF - V_{th} - C'(REF - DATA) - VDD\} - VDD] - V_{th}$$

[0046] In Equation 4, the current  $I_{ds}$  between the drain and source of the driving TFT Td is derived as shown in Equation 5:

[Equation 5]

$$I_{ds} = k' [(C' - 1) \cdot (REF - DATA)]^2$$

[0047] As shown in equation 5, the current  $I_{ds}$  between the drain and source of the driving TFT Td supplied to the organic light emitting diode OLED during the fourth period  $t_4$  is dependent only on proportionality factor  $k'$ , the capacitance of the first capacitor  $C_1$ , the capacitance of the second capacitor  $C_2$ , the data voltage  $DATA$ , and the reference voltage  $REF$ . The current  $I_{ds}$  between the drain and source of the driving TFT Td is not dependent on the threshold voltage  $V_{th}$  of the driving TFT Td. Therefore, the threshold voltage  $V_{th}$  of the driving TFT Td is compensated for.

[0048] Additionally, the high potential voltage supply source  $VDD\_S$  supplies the high potential voltage  $VDD$  to all pixels of the display panel. However, the high potential voltage  $VDD$  is dropped because the driving TFT DT and the organic light emitting diode display OLED of each pixel existing according to a current path from the high potential voltage supply source  $VDD\_S$  to the low potential voltage supply source  $VSS\_S$  function as resistances. The current  $I_{ds}$  between the drain and source of the driving TFT Td is not dependent on the high potential voltage  $VDD$  because the high potential voltage  $VDD$  applied at the gate electrode of the driving TFT DT and the high potential voltage  $VDD$  applied at the source electrode thereof during the fourth period  $t_4$  is a voltage dropped. Therefore, any drop in the high potential voltage  $VDD$  is also compensated for.

[0049] FIG. 4 illustrates a graph showing a compensation error in accordance with threshold voltage variation of a driving TFT. With reference to FIG. 4, the threshold variation  $V_{th}$  Variation [V] of the driving TFT DT is shown in a horizontal axis, the current Pixel current [ $\mu A$ ] between the drain and source of the driving TFT Td is shown in a left-vertical axis, and an error Error (%) of the current between the drain and source of the driving TFT Td is shown in right-vertical axis.

[0050] The threshold voltage shift of the driving TFT DT of each pixel may be caused by deterioration of the driving TFT DT. Thus, organic light emitting diode display device compensate the threshold voltage  $V_{th}$  of the driving TFT DT by sensing the threshold voltage  $V_{th}$  thereof. However, the current  $I_{ds}$  between the drain and source of the driving TFT Td may have an error when accuracy of sensing the threshold voltage  $V_{th}$  of the driving TFT TD is low.

[0051] As shown in FIG. 4, when the threshold voltage variation  $V_{th}$  Variation [V] is -1.0V to 1.0V, the current  $I_{ds}$  between the drain and source of the driving TFT Td is approximately 1.26  $\mu A$  to 1.36  $\mu A$ , and the error Error (%) of the current  $I_{ds}$  between the drain and source of the driving TFT Td is approximately -5% to +2.5%. That is, the embodiments described herein may decrease the error Error(%) of the current  $I_{ds}$  between the drain and source of the driving TFT Td into -5% to +2.5%.

[0052] FIG. 5 illustrates a block diagram schematically showing an organic light emitting diode display device according

to an exemplary embodiment of the present invention. Referring to FIG. 5, the organic light emitting diode display device according to the exemplary embodiment comprises a display panel 10, a data driving circuit 20, a gate driving circuit 30, a timing controller 40, and a host system 50.

**[0053]** The display panel 10 has data lines DL and first scan lines SL1 crossing each other. Also, the display panel 10 has second scan lines SL2, control lines MGL, and emission lines EML in parallel with the first scan lines SL1. The display panel 10 comprises a pixel array having pixels P disposed in a matrix form in. A detailed description of each pixel P of the display panel 10 was previously described by reference to FIGs. 1-4.

**[0054]** The data driving circuit 20 comprises a plurality of source drive ICs. The source drive ICs receive digital video data from the timing controller 40. The source drive ICs convert the digital video data into gamma correction voltages to generate data voltages, in response to source timing control signals from the timing controller 40. And then, the source drive ICs supply the data voltages to the data lines DL of the display panel 10 in synchronization with the first scan signals from the gate driving circuit 30.

**[0055]** The gate driving circuit 30 comprises a first scan signal output unit (not shown), a second scan signal output unit (not shown), a control signal output unit (not shown), and an emission signal output unit (not shown). The first scan signal output unit supplies sequentially the first scan signals SCAN1 to the first scan lines SL1 of the display panel 10. The second scan signal output unit supplies sequentially the second scan signals SCAN2 to the second scan lines SL2 of the display panel 10. The control signal output unit supplies sequentially the control signals MG to the control lines MGL of the display panel 10. The emission signal output unit supplies sequentially the emission signals EM to the emission lines EML of the display panel 10. A detailed description of the first scan signal SCAN1, the second scan signal SCAN2, the control signal MG, and the emission signal EM was previously described by reference to FIGs. 1-4.

**[0056]** The timing controller 40 receives the digital video data from the host system 50 via an interface such as an LVDS (low voltage differential signaling) interface, a TMDS (transition minimized differential signaling) interface or the like. The timing controller 40 transmits the digital video data input from the host system 50 to the data driving circuit 20.

**[0057]** The timing controller 40 receives timing signals such as a vertical synchronization signal, a horizontal synchronization signal, a data enable signal, a main clock, and so forth from the host system 50. The timing controller 40 generates timing control signals for controlling operation timings of the data driving circuit 20 and the gate driving circuit 30 based on the timing signals from the host system 50. The timing control signals comprise gate timing control signals for controlling operation timings of the gate driving circuit 30, and data timing signals for controlling operation timings of the data driving circuit 20.

**[0058]** The embodiments described herein may improve accuracy of sensing a threshold voltage  $V_{th}$  of a driving TFT DT even though an organic light emitting diode display device drives high frequency such as 240Hz because sensing periods are long enough to sense the threshold voltage  $V_{th}$  of the driving TFT DT. Also, the embodiments described herein may compensate a drop of a high potential voltage VDD due to compensating the current  $I_{ds}$  between a drain electrode and a source electrode of the driving TFT DT by using the high potential voltage VDD dropped.

**[0059]** Although the embodiments of this application have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments of this application can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

## Claims

1. An organic light emitting diode display device comprising:

a display panel (10) configured to include data lines (DL), first scan lines (SL1), second scan lines (SL2), control lines (MGL), emission lines (EML), and a plurality of pixels (P) disposed in a matrix form,

wherein each of the pixels (P) including:

a driving TFT (DT) configured to have a gate electrode coupled to a first node (N1) and a source electrode coupled to a second node (N2);

an organic light emitting diode (OLED) configured to have an anode electrode coupled to a drain electrode of the driving TFT (DT) and a cathode electrode coupled to a first level voltage supply source supplying a first level voltage;

a first TFT (T1) configured to supply a data voltage of the data line (DL) to the first node (N1) in response to a first scan signal (SCAN1) of the first scan line (SL1);

a second TFT (T2) configured to supply a reference voltage from a reference voltage supply source (REF\_S) to the first node (N1) in response to a second scan signal (SCAN2) of the second scan line (SL2) ;  
 a third TFT (T3) configured to supply a second level voltage higher than the first level voltage to the second node (N2) in response to a emission signal (EM) of the emission line (EML);  
 5 a fourth TFT (T4) configured to couple the second node (N2) to a third node (N3) in response to a control signal (MG) of the control line (MGL);  
 a first capacitor (C1) coupled between the first node (N1) and the third node (N3);  
 a second capacitor (C2) coupled between the third node (N3) and a second voltage supply source supplying the second level voltage, and  
 10 wherein the control signal (MG) is inverted to a second logic level voltage from a first logic level voltage after the emission signal (EM) is inverted to the second logic level voltage from the first logic level voltage during a period for emitting the organic light emitting diode (OLED), and  
 wherein the reference voltage is lower than a voltage subtracting a threshold voltage of the driving TFT (DT) from the second level voltage and is higher than the first level voltage.

2. The organic light emitting diode display device of claim 1, wherein during a first period (t1) in which the reference voltage is supplied to the first node (N1) and the second level voltage is supplied to the second (N2) and third node (N3) for initialization, the first scan signal (SCAN1) is generated as the first logic level voltage, and the second scan signal (SCAN2), the control signal (MG), and the emission signal (EM) are generated as the second logic level voltage.  
 20
3. The organic light emitting diode display device of claim 2, wherein during a second period (t2) for sensing a threshold voltage of the driving TFT (DT), the first scan signal (SCAN1) and the emission signal (EM) are generated as the first logic level voltage, and the second scan signal (SCAN2) and the control signal (MG) are generated as the second logic level voltage.  
 25
4. The organic light emitting diode display device of claim 3, wherein during a third period (t3) for supplying the data voltage to the pixel (P), the second scan signal (SCAN2), the control signal (MG), and the emission signal (EM) are generated in the first logic level voltage, and the first scan signal (SCAN1) is generated in the second logic level voltage.  
 30
5. The organic light emitting diode display device of claim 4, wherein during the period for emitting the organic light emitting diode (OLED), the first scan signal (SCAN1) and the second scan signal (SCAN2) are generated as the first logic level voltage.
- 35 6. The organic light emitting diode display device of claim 5, wherein the first logic level voltage is higher than the second logic level voltage.
7. The organic light emitting diode display device of claim 6, wherein each of the first to the fourth TFTs (T1-T4) is P-type transistor.  
 40
8. The organic light emitting diode display device of claim 1, wherein a gate electrode of the first TFT (T1) is coupled to the first scan line (SL1), a source electrode thereof is coupled to the data line (DL), and a drain electrode thereof is coupled to the first node (N1),  
 a gate electrode of the second TFT (T2) is coupled to the second scan line (SL2), a source electrode thereof is coupled to the first node (N1), and a drain electrode thereof is coupled to the reference voltage supply source (REF\_S) supplying the reference voltage,  
 45 a gate electrode of the third TFT (T3) is coupled to the emission line (EML), a source electrode thereof is coupled to the second level voltage supply source, and a drain electrode thereof is coupled to the second node (N2),  
 a gate electrode of the fourth TFT (T4) is coupled to the control line (MGL), a source electrode thereof is coupled to the second node (N2), and a drain electrode thereof is coupled to the third node (N3) .  
 50
9. The organic light emitting diode display device of claim 1, wherein the reference voltage is lower than a difference voltage between the second level voltage and a threshold voltage of the driving TFT (DT), and is greater than the first logic level voltage.  
 55
10. The organic light emitting diode display device of claim 1, wherein the first level voltage is a low potential voltage and the second level voltage is a high potential voltage.

## Patentansprüche

### 1. Eine Organische-Lichtemittierende-Diode-Anzeigevorrichtung aufweisend:

5 ein Anzeige-Panel (10), das ausgebildet ist, um Datenleitungen (DL), erste Scanleitungen (SL1), zweite Scanleitungen (SL2), Steuerleitungen (MGL), Emissionsleitungen (EML) und eine Mehrzahl von Pixeln (P), die in einer Matrixform angeordnet sind, aufzuweisen,

10 wobei jedes der Pixel (P) aufweist:

einen Treiber-Dünnschichttransistor (DT), der ausgebildet ist, um eine Gate-Elektrode, die mit einem ersten Knoten (N1) verbunden ist, und eine Source-Elektrode, die mit einem zweiten Knoten (N2) verbunden ist, aufzuweisen;

15 eine organische lichtemittierende Diode (OLED), die ausgebildet ist, um eine Anodenelektrode, die mit einer Drain-Elektrode des Treiber-TFT (DT) verbunden ist, und eine Kathodenelektrode, die mit einer Erster-Pegel-Spannungszufuhrquelle, die eine Erster-Pegel-Spannung zuführt, verbunden ist, aufzuweisen;

einen ersten TFT (T1), der ausgebildet ist, um eine Datenspannung der Datenleitung (DL) an den ersten Knoten (N1) zuzuführen, in Antwort auf ein erstes Scansignal (SCAN1) der ersten Scanleitung (SL1);

20 einen zweiten TFT (T2), der ausgebildet ist, um eine Referenzspannung von einer Referenzspannung-Zufuhrquelle (REF\_S) an den ersten Knoten (N1) zuzuführen, in Antwort auf ein zweites Scansignal (SCAN2) der zweiten Scanleitung (SL2);

einen dritten TFT (T3), der ausgebildet ist, um eine Zweiter-Pegel-Spannung, die höher ist als die Erster-Pegel-Spannung an den zweiten Knoten (N2) zuzuführen, in Antwort auf ein Emissionssignal (EM) der Emissionsleitung (EML);

25 einen vierten TFT (T4), der ausgebildet ist, um den zweiten Knoten (N2) mit einem dritten Knoten (N3) zu verbinden, in Antwort auf ein Steuersignal (MG) der Steuerleitung (MGL);

einen ersten Kondensator (C1), der zwischen dem ersten Knoten (N1) und dem dritten Knoten (N3) geschaltet ist; einen zweiten Kondensator (C2), der zwischen dem dritten Knoten (N3) und einer zweiten Spannungszufuhrquelle, die die Zweiter-Pegel-Spannung zuführt, geschaltet ist, und

30 wobei das Steuersignal (MG) von einer Erster-Logischer-Pegel-Spannung zu einer Zweiter-Logischer-Pegel-Spannung invertiert wird, nachdem das Emissions-Signal (EM) von der Erster-Logischer-Pegel-Spannung in die Zweiter-Logischer-Pegel-Spannung invertiert wird, während einer Periode zum Emittieren der organischen lichtemittierenden Diode (OLED), und

35 wobei die Referenzspannung geringer ist als eine Spannung beim Subtrahieren einer Schwellenspannung des Treiber-TFT (DT) von der Zweiter-Pegel-Spannung und höher ist als die Erster-Pegel-Spannung.

2. Die Organische-Lichtemittierende-Diode-Anzeigevorrichtung gemäß Anspruch 1, wobei während einer ersten Periode ( $t_1$ ), in welcher zur Initialisierung die Referenzspannung an den ersten Knoten (N1) und die Zweiter-Pegel-Spannung an den zweiten Knoten (N2) und den dritten Knoten (N3) zugeführt wird, das erste Scansignal (SCAN1) als die Erster-Logischer-Pegel-Spannung erzeugt wird, und das zweite Scansignal (SCAN2), das Steuersignal (MG) und das Emissionssignal (EM) als die Zweiter-Logischer-Pegel-Spannung erzeugt werden.

3. Die Organische-Lichtemittierende-Diode-Anzeigevorrichtung gemäß Anspruch 2, wobei während einer zweiten Periode ( $t_2$ ) zum Abfühlen einer Schwellenspannung des Treiber-TFT (DT), das erste Scansignal (SCAN1) und das Emissionssignal (EM) als die Erster-Logischer-Pegel-Spannung erzeugt werden, und das zweite Scansignal (SCAN2) und das Steuersignal (MG) als die Zweiter-Logischer-Pegel-Spannung erzeugt werden.

4. Die Organische-Lichtemittierende-Diode-Anzeigevorrichtung gemäß Anspruch 3, wobei während einer dritten Periode ( $t_3$ ) zum Zuführen der Datenspannung an das Pixel (P), das zweite Scansignal (SCAN2), das Steuersignal (MG) und das Emissionssignal (EM) in der Erster-Logischer-Pegel-Spannung erzeugt werden, und das erste Scansignal (SCAN1) in der Zweiter-Logischer-Pegel-Spannung erzeugt wird.

5. Die Organische-Lichtemittierende-Diode-Anzeigevorrichtung gemäß Anspruch 4, wobei während der Periode zum Emittieren der organischen lichtemittierende Diode (OLED), das erste Scansignal (SCAN1) und das zweite Scansignal (SCAN2) als die Erster-Logischer-Pegel-Spannung erzeugt werden.

6. Die Organische-Lichtemittierende-Diode-Anzeigevorrichtung gemäß Anspruch 5, wobei die Erster-Logischer-Pegel-Spannung höher ist als die Zweiter-Logischer-Pegel-Spannung.

7. Die Organische-Lichtemittierende-Diode-Anzeigevorrichtung gemäß Anspruch 6, wobei jeder von dem ersten bis zu dem vierten TFT (T1-T4) ein P-Typ-Transistor ist.
8. Die Organische-Lichtemittierende-Diode-Anzeigevorrichtung gemäß Anspruch 1, wobei eine Gate-Elektrode des ersten TFT (T1) mit der ersten Scanleitung (SL1) verbunden ist, eine Source-Elektrode davon mit der Datenleitung (DL) verbunden ist, und eine Drain-Elektrode davon mit dem ersten Knoten (N1) verbunden ist, eine Gate-Elektrode des zweiten TFT (T2) mit der zweiten Scanleitung (SL2) verbunden ist, eine Source-Elektrode davon mit dem ersten Knoten (N1) verbunden ist, und eine Drain-Elektrode davon mit der Referenzspannung-Zufuhrquelle (REF\_S), die die Referenzspannung zuführt, verbunden ist, eine Gate-Elektrode des dritten TFT (T3) mit der Emissionsleitung (EML) verbunden ist, eine Source-Elektrode davon mit der Zweiter-Pegel-Spannung-Zufuhrquelle verbunden ist, und eine Drain-Elektrode davon mit dem zweiten Knoten (N2) verbunden ist, eine Gate-Elektrode des vierten TFT (T4) mit der Steuerleitung (MGL) verbunden ist, eine Source-Elektrode davon mit dem zweiten Knoten (N2) verbunden ist, und eine Drain-Elektrode davon mit dem dritten Knoten (N3) verbunden ist.
9. Die Organische-Lichtemittierende-Diode-Anzeigevorrichtung gemäß Anspruch 1, wobei die Referenzspannung geringer ist als eine Differenzspannung zwischen der Zweiter-Pegel-Spannung und einer Schwellenspannung des Treiber-TFT (DT), und größer ist als die Erster-Logischer-Pegel-Spannung.
10. Die Organische-Lichtemittierende-Diode-Anzeigevorrichtung gemäß Anspruch 1, wobei die Erster-Pegel-Spannung eine Niedrig-Potential-Spannung ist und die Zweiter-Pegel-Spannung eine Hoch-Potential-Spannung ist.

## Revendications

1. Dispositif d'affichage à diode électroluminescente organique comprenant :

un panneau d'affichage (10) configuré de façon à inclure des lignes de données (DL), des premières lignes de balayage (SL1), des secondes lignes de balayage (SL2), des lignes de commande (MGL), des lignes d'émission (EML), et une pluralité de pixels (P) disposés sous une forme de matrice ;

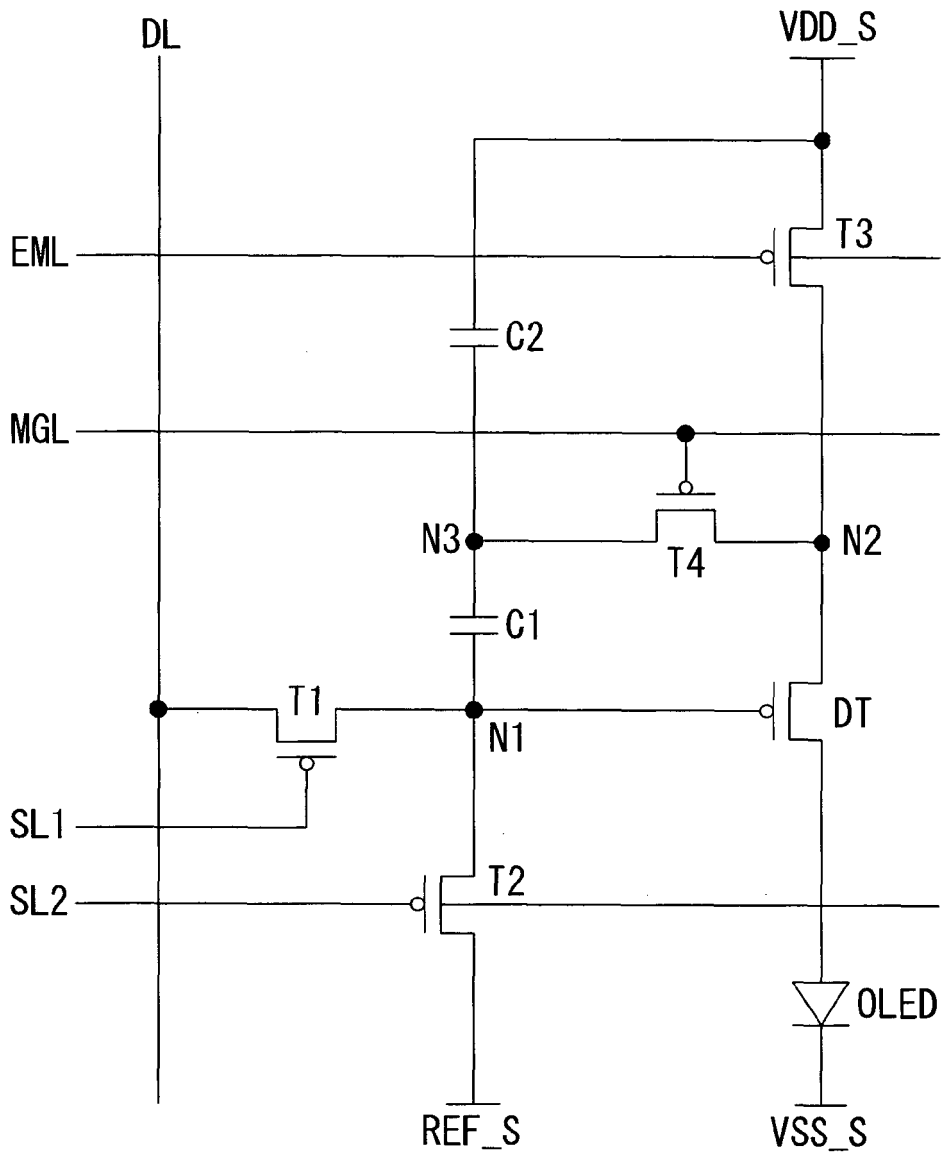
dans lequel chacun des pixels (P) comprend :

un TFT de commande (DT) configuré de façon à présenter une électrode de grille couplée à un premier noeud (N1) et une électrode de source couplée à un deuxième noeud (N2) ;  
 une diode électroluminescente organique (OLED) configurée de façon à présenter une électrode d'anode couplée à l'électrode de drain du TFT de commande (DT), et une électrode de cathode couplée à une source d'alimentation d'un premier niveau de tension qui fournit un premier niveau de tension ;  
 un premier TFT (T1) configuré de façon à fournir une tension de données de la ligne de données (DL) au premier noeud (N1) en réponse à un premier signal de balayage (SCAN1) de la première ligne de balayage (SL1) ;  
 un deuxième TFT (T2) configuré de façon à fournir une tension de référence à partir d'une source d'alimentation de tension de référence (REF\_S) au premier noeud (N1) en réponse à un deuxième signal de balayage (SCAN2) de la deuxième ligne de balayage (SL2) ;  
 un troisième TFT (T3) configuré de façon à fournir au deuxième noeud (N2) un deuxième niveau de tension supérieur au premier niveau de tension en réponse à un signal d'émission (EM) de la ligne d'émission (EML) ;  
 un quatrième TFT (T4) configuré de façon à coupler le deuxième noeud (N2) à un troisième noeud (N3) en réponse à un signal de commande (MG) de la ligne de commande (MGL) ;  
 un premier condensateur (C1) couplé entre le premier noeud (N1) et le troisième noeud (N3) ;  
 un second condensateur (C2) couplé entre le troisième noeud (N3) et une source d'alimentation d'un second niveau de tension qui fournit le second niveau de tension ; et  
 dans lequel le signal de commande (MG) est inversé à un second niveau de tension logique à partir d'un premier niveau de tension logique une fois que le signal d'émission (EM) a été inversé au second niveau de tension logique à partir du premier niveau de tension logique au cours d'une période pour faire émettre la diode électroluminescente organique (OLED) ; et  
 dans lequel la tension de référence est inférieure à une tension en soustrayant une tension de seuil du TFT de commande (DT) du second niveau de tension, et est supérieure au premier niveau de tension.

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- 5
2. Dispositif d'affichage à diode électroluminescente organique selon la revendication 1, dans lequel, au cours d'une première période (t1) pendant laquelle la tension de référence est fournie au premier noeud (N1), et le second niveau de tension est fourni au deuxième noeud (N2) et au troisième noeud (N3) pour une initialisation, le premier signal de balayage (SCAN1) est généré en tant que premier niveau de tension logique, et le second signal de balayage (SCAN2), le signal de commande (MG), et le signal d'émission (EM) sont générés en tant que second niveau de tension logique.
- 10
3. Dispositif d'affichage à diode électroluminescente organique selon la revendication 2, dans lequel, au cours d'une seconde période (t2) pour détecter une tension de seuil du TFT de commande (DT), le premier signal de balayage (SCAN1) et le signal d'émission (EM) sont générés en tant que premier niveau de tension logique, et le second signal de balayage (SCAN2) et le signal de commande (MG) sont générés en tant que second niveau de tension logique.
- 15
4. Dispositif d'affichage à diode électroluminescente organique selon la revendication 3, dans lequel, au cours d'une troisième période (t3) pour fournir la tension de données au pixel (P), le second signal de balayage (SCAN2), le signal de commande (MG), et le signal d'émission (EM) sont générés dans le premier niveau de tension logique, et le premier signal de balayage (SCAN1) est généré dans le second niveau de tension logique.
- 20
5. Dispositif d'affichage à diode électroluminescente organique selon la revendication 4, dans lequel, au cours de la période pour faire émettre la diode électroluminescente organique (OLED), le premier signal de balayage (SCAN1) et le second signal de balayage (SCAN2) sont générés en tant que premier niveau de tension logique.
- 25
6. Dispositif d'affichage à diode électroluminescente organique selon la revendication 5, dans lequel le premier niveau de tension logique est supérieur au second niveau de tension logique.
- 30
7. Dispositif d'affichage à diode électroluminescente organique selon la revendication 6, dans lequel chacun des quatre premiers TFT (T1 - T4) est un transistor de type P.
- 35
8. Dispositif d'affichage à diode électroluminescente organique selon la revendication 1, dans lequel l'électrode de grille du premier TFT (T1) est couplée à la première ligne de balayage (SL1), son électrode de source est couplée à la ligne de données (DL), et son électrode de drain est couplée au premier noeud (N1) ; l'électrode de grille du deuxième TFT (T2) est couplée à la seconde ligne de balayage (SL2), son électrode de source est couplée au premier noeud (N1), et son électrode de drain est couplée à la source d'alimentation de tension de référence (REF\_S) qui fournit la tension de référence ; l'électrode de grille du troisième TFT (T3) est couplée à la ligne d'émission (EML), son électrode de source est couplée à la source d'alimentation d'un second niveau de tension, et son électrode de drain est couplée au deuxième noeud (N2) ; l'électrode de grille du quatrième TFT (T4) est couplée à la ligne de commande (MGL), son électrode de source est couplée au deuxième noeud (N2), et son électrode de drain est couplée au troisième noeud (N3).
- 40
9. Dispositif d'affichage à diode électroluminescente organique selon la revendication 1, dans lequel la tension de référence est inférieure à la différence de tension entre le second niveau de tension et une tension de seuil du TFT de commande (DT), et est supérieure au premier niveau de tension logique.
- 45
10. Dispositif d'affichage à diode électroluminescente organique selon la revendication 1, dans lequel le premier niveau de tension est une tension qui présente un potentiel faible, et le second niveau de tension est une tension qui présente un potentiel élevé.
- 50
- 55

FIG. 1



**FIG. 2**

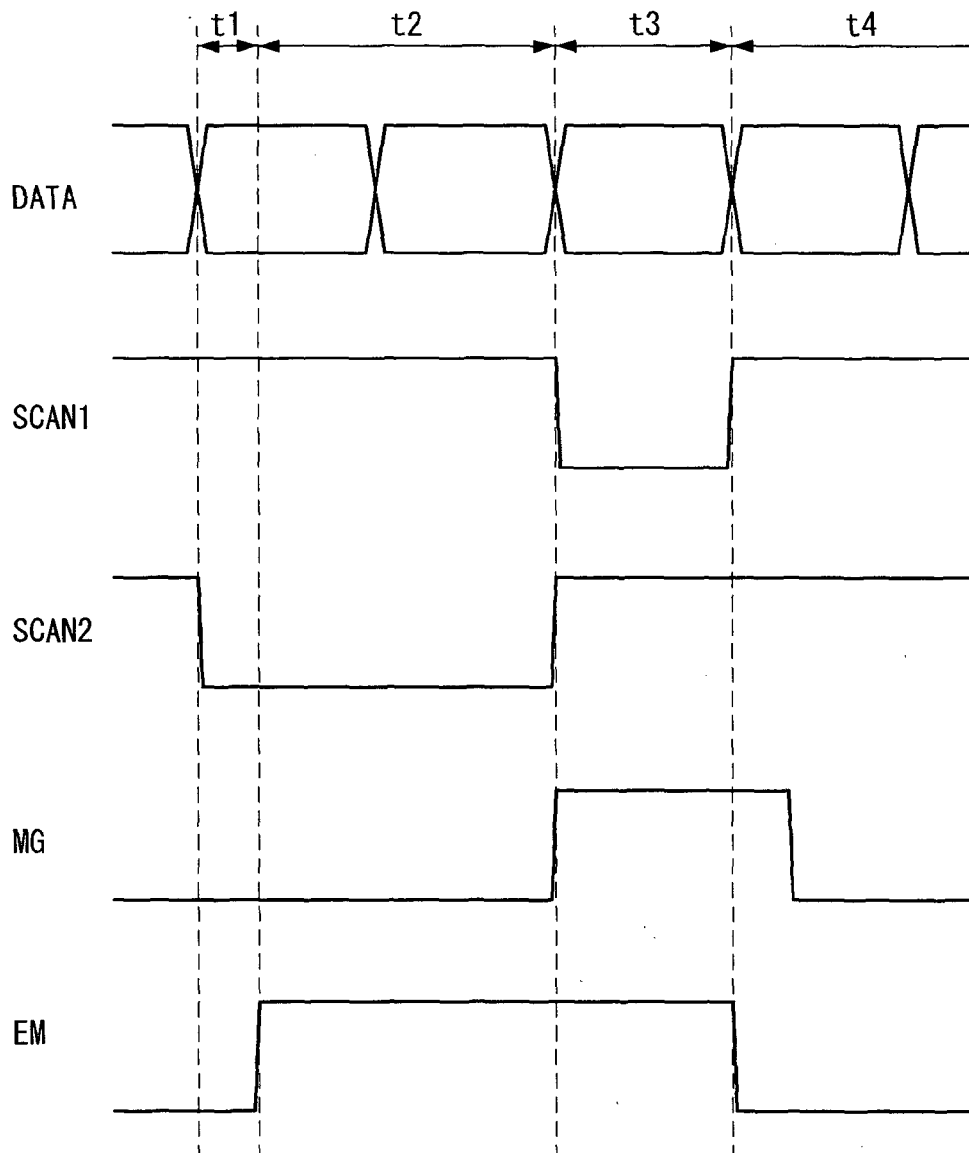


FIG. 3

period	Vn1	Vn2	Vn3
t1	REF	VDD	VDD
t2	REF	REF-Vth	REF-Vth
t3	DATA	REF-Vth	REF-Vth -C' (REF-DATA)
t4	DATA-[REF-Vth -C' (REF-DATA)-VDD]	VDD	VDD

FIG. 4

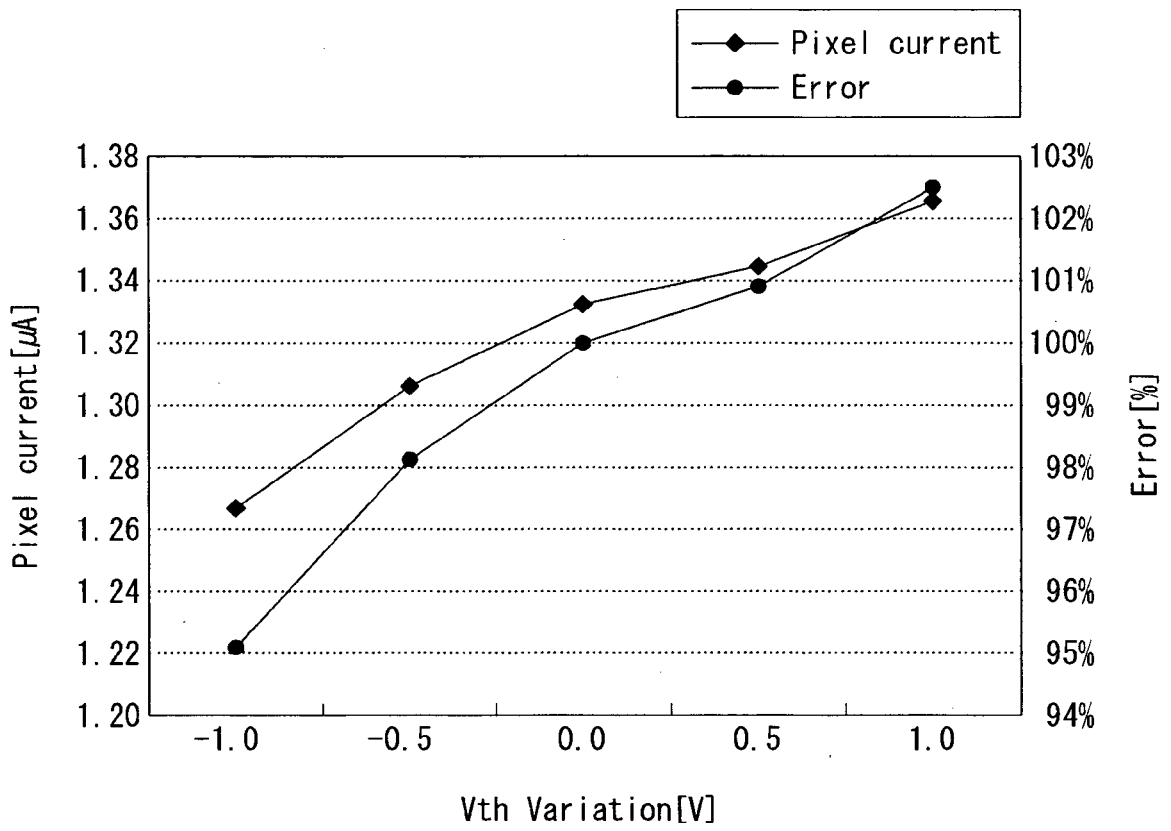
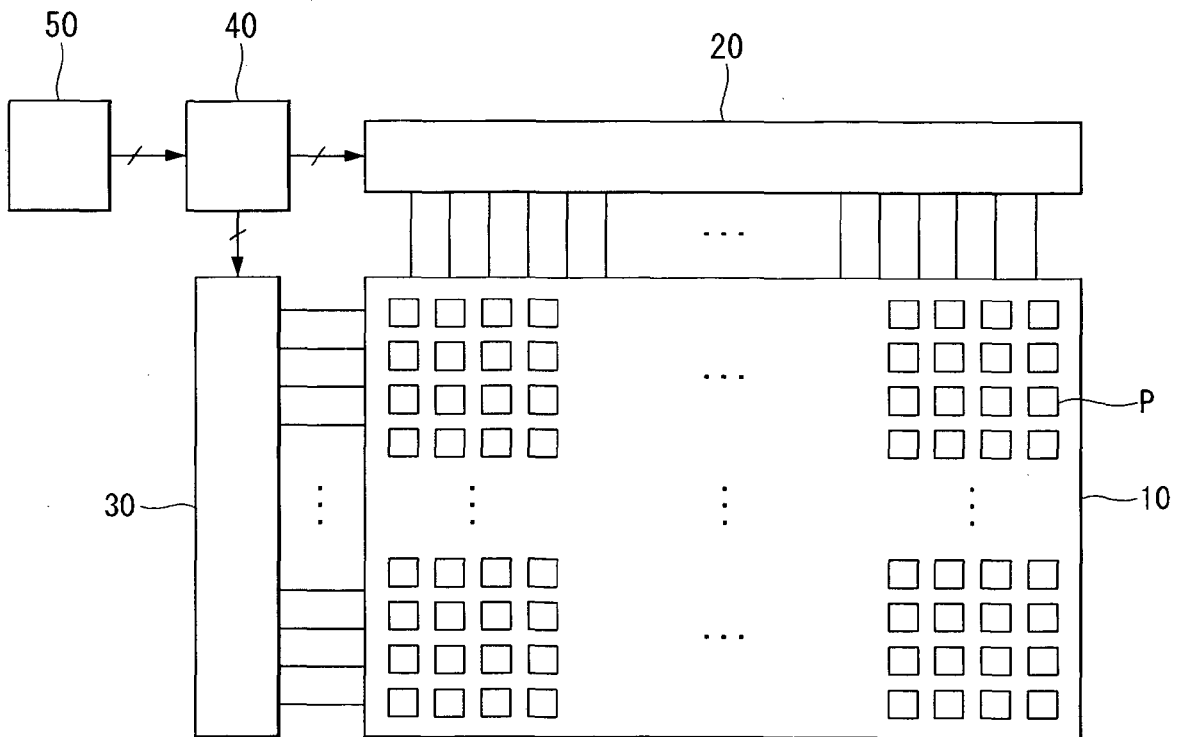


FIG. 5



**REFERENCES CITED IN THE DESCRIPTION**

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**Patent documents cited in the description**

- KR 1020110115577 [0001]
- JP 2006023515 A [0008]

专利名称(译)	有机发光二极管显示装置		
公开(公告)号	<a href="#">EP2592617B1</a>	公开(公告)日	2016-07-13
申请号	EP2012187449	申请日	2012-10-05
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	YOON JOONGSUN KANG JIHYUN		
发明人	YOON, JOONGSUN KANG, JIHYUN		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0852 G09G2300/0861 G09G2320/0223 G09G2320/043		
优先权	1020110115577 2011-11-08 KR		
其他公开文献	EP2592617A1		
外部链接	<a href="#">Espacenet</a>		

摘要(译)

本实施例涉及一种有机发光二极管显示装置，包括：显示面板，被配置为包括以矩阵形式设置的多个像素，其中每个像素包括：驱动TFT，有机发光二极管，控制电路包括第一至第四TFT，电容器。这里描述的实施例可以提高感测驱动TFT的阈值电压的准确度，即使有机发光二极管显示装置驱动诸如240Hz的高频，因为感测周期足够长以感测驱动TFT的阈值电压。而且，这里描述的实施例可以通过使用下降的高电位电压来补偿由于补偿驱动TFT的漏电极和源电极之间的电流而导致的高电位电压的下降。

[Equation 1]

$$I_{ds} = k' \cdot (V_{gs} - V_{th})^2$$