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(54) **Organic light emitting display device and driving method thereof**

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Dispositif d'affichage électroluminescent organique et son procédé de commande

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**Description****CROSS-REFERENCE TO RELATED APPLICATIONS**

**[0001]** This application claims priority to and the benefit of Korean Patent Application No. 10-2009-0082451, filed on September 2, 2009, in the Korean Intellectual Property Office.

**BACKGROUND****1. Field**

**[0002]** An aspect of an embodiment of the present invention relates to an organic light emitting display device and a driving method thereof.

**2. Description of Related Art**

**[0003]** Various flat panel display devices with reduced weight and volume in comparison to a cathode ray tube have been developed. Examples of the flat panel display devices include a liquid crystal display device, a field emission display device, a plasma display panel, an organic light emitting display device, etc.

**[0004]** Among the flat panel display devices, the organic light emitting display device displays an image by using organic light emitting diodes that emit light by recombining holes with electrons. The organic light emitting display device has low power consumption while having high response speed.

**[0005]** FIG. 1 is a circuit diagram showing a pixel of an organic light emitting display device according to the related art.

**[0006]** Referring to FIG. 1, a pixel 4 includes a pixel circuit 2 for controlling an organic light emitting diode (OLED) connected to the pixel circuit 2, a data line Dm, and a scan line Sn.

**[0007]** An anode electrode of the OLED is connected to the pixel circuit 2, and a cathode electrode of the OLED is connected to a second power supply ELVSS. The OLED generates light having a luminance (e.g., a predetermined luminance) corresponding to the amount of current supplied from the pixel circuit 2.

**[0008]** The pixel circuit 2 controls the amount of current supplied to the OLED to correspond to a data signal provided from the data line Dm when a scan signal is provided to the scan line Sn. Here, the pixel circuit 2 includes a second transistor M2 connected to a first power supply ELVDD and the OLED, a first transistor M1 connected to the second transistor M2, the data line Dm, and the scan line Sn, and a storage capacitor Cst connected between a gate electrode and a first electrode of the second transistor M2.

**[0009]** A gate electrode of the first transistor M1 is connected to the scan line Sn, and a first electrode of the first transistor M1 is connected to the data line Dm. In addition, a second electrode of the first transistor M1 is connected to one terminal of the storage capacitor Cst. Here, the first electrode is one of a source electrode or a drain electrode, and the second electrode is an electrode other than the first electrode. For example, when the first electrode is the source electrode, the second electrode is a drain electrode. The first transistor M1 connected to the scan line Sn and the data line Dm is turned on and provides the data signal provided from the data line Dm to the storage capacitor Cst when a scan signal is provided from the scan line Sn. Here, the storage capacitor Cst is charged with a voltage corresponding to the data signal.

**[0010]** The gate electrode of the second transistor M2 is connected to one terminal of the storage capacitor Cst, and the first electrode of the second transistor M2 is connected to the other terminal of the storage capacitor Cst and the first power supply ELVDD. In addition, a second electrode of the second transistor M2 is connected to the anode electrode of the OLED. The second transistor M2 controls the amount of current that flows to the second power supply ELVSS via the OLED from the first power supply ELVDD to correspond to a voltage value stored in the storage capacitor Cst. Here, the OLED generates light corresponding to the amount of current supplied from the second transistor M2.

**[0011]** The pixel circuit 2 supplies a current corresponding to the voltage charged in the storage capacitor Cst to the OLED to display an image having a luminance (e.g., a predetermined luminance). However, the above described organic light emitting display device cannot display an image having uniform luminance due to a variation in threshold voltage of the second transistor M2.

**[0012]** In the related art, additional circuits such as a plurality of transistors are included in the pixel 4 for compensating for the variation of the threshold voltage of the second transistor M2. However, when the plurality of transistors (for example, 6 transistors) are included in the pixel 4 in order to compensate for the variation of the threshold voltage of the second transistor M2, reliability is deteriorated.

**[0013]** Further, in the related art, a voltage value of the first power supply ELVDD varies due to a voltage drop depending on the position of the pixel 4, and as a result, an image having desired luminance cannot be displayed.

**[0014]** The document EP2093748A1 discloses an active matrix OLED display, wherein a common circuit (20) is

provided between the data driver and the pixel circuit (10). The pixel circuit comprises an OLED (15), a light emission control transistor (14), a drive transistor (11), a storage capacitor (16), a scan transistor (12) and a transistor (13) for diode connecting the drive transistor. The pixel is controlled using three scan signals (Ri, Wi, Gi). The common circuit (20) comprises a capacitor (26), switching transistors (21-25) and an analog buffer (27). The common circuit can apply a reset voltage (Vreset) to the data line (Sj), connect the data line directly (21) to one end of the capacitor (26) or via the analog buffer (24, 27), and can connect the other end of the capacitor to either a supply voltage (Vp) or a data voltage (Vdata). The display compensates for threshold voltage variations of the drive transistor (11) by storing a compensation voltage in the capacitor (26) of the common circuit (20). Both electrodes of the capacitor (26) of the common circuit (20) are connected to the respective power supplies (Vreset, Vp) at the same time as the drive transistor (11) is diode-connected by a transistor (13).

**[0015]** The document JP 2005352411 discloses an active matrix OLED, wherein a common circuit (OS1) is provided between the data driver and the pixel circuit (A<sub>ij</sub>). The pixel circuit comprises an OLED (OLED), a light emission control transistor (T4), a drive transistor (T3), a storage capacitor (Cs), a scan transistor (T2) and a transistor (T1) for diode connecting the drive transistor. The pixel is controlled using two scan signals (G1j, G2j) only. The common circuit (OS1) comprises a capacitor (C1) and switching transistors (T5-T7). The common circuit can apply a precharge voltage (V<sub>pre</sub>) to the data line (Si) connected to one end of the capacitor (C1) of the common circuit, and can connect the other end of the capacitor (C1) of the common circuit to either a supply voltage (VO) or a data voltage (Vdata). The display compensates for threshold voltage variations of the drive transistor by storing a compensation voltage in the capacitor (C1) of the common circuit (OS1). Both electrodes of the capacitor (C1) of the common circuit (OS1) are connected to the respective power supplies (Vpre, VO) at the same time as the drive transistor (T3) is diode-connected by a transistor (T1).

**[0016]** The document EP1755104A2 discloses an active matrix OLED display comprising a demultiplexer (151) between one source driver output (D<sub>1</sub>) and a plurality of data lines (D<sub>11</sub> - D<sub>13</sub>).

## SUMMARY

**[0017]** An aspect of an embodiment of the present invention provides an organic light emitting display device that may compensate for a threshold voltage of a driving transistor and a voltage drop of a first voltage supplied to the driving transistor.

**[0018]** According to an embodiment of the present invention, there is provided an organic light emitting display device as defined in the independent claim 1.

**[0019]** According to an embodiment of the present invention, there is provided a driving method of an organic light emitting display device as defined in the independent claim 6.

**[0020]** According to the above described embodiments of the present invention, an organic light emitting display device can display an image having a desired luminance irrespective of the voltage drop of a first power supply and the threshold voltage of a driving transistor. According to the embodiments of the present invention, it is possible to compensate for the voltage drop of the first power supply and the threshold voltage of the driving transistor by using a relatively simple structure in which four transistors and one capacitor are included in a pixel, thereby improving reliability. Further, the embodiments of the present invention may be applied to an organic light emitting display device using a demultiplexer.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0021]** The accompanying drawings, together with the specification, illustrate exemplary embodiments of the present invention and, together with the description, serve to explain the principles of the present invention.

**[0022]** FIG. 1 is a circuit diagram showing a pixel of an organic light emitting display device according to the related art.

**[0023]** FIG. 2 is a block diagram showing an organic light emitting display device according to an embodiment of the present invention.

**[0024]** FIG. 3 is a circuit diagram showing an embodiment of a pixel shown in FIG. 2.

**[0025]** FIG. 4 is a circuit diagram showing an embodiment of a common circuit unit shown in FIG. 2.

**[0026]** FIG. 5 is a circuit diagram showing a demultiplexer shown in FIG. 2.

**[0027]** FIG. 6 is a circuit diagram showing a connection structure of a demultiplexer, a common circuit unit, and pixels.

**[0028]** FIG. 7 is a waveform diagram for showing driving methods of a demultiplexer, a common circuit unit, and pixels shown in FIG. 6.

**[0029]** FIGS. 8A, 8B, 8C, 8D, and 8E are circuit diagrams for showing a driving process according to the waveform diagram of FIG. 7.

## DETAILED DESCRIPTION

**[0030]** Hereinafter, certain exemplary embodiments according to the present invention will be described with reference

to the accompanying drawings. Here, when a first element is described as being connected or coupled to a second element, the first element may be directly coupled to the second element or indirectly coupled to the second element via a third element. Further, some of the elements that are not essential to a complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

**[0031]** Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to FIGS. 2 to 8E.

**[0032]** FIG. 2 is a block diagram showing an organic light emitting display device according to an embodiment of the present invention. In FIG. 2, a demultiplexer (hereinafter, referred to as "DEMUX") 170 is connected to  $j$  ( $j$  is a natural number of 2 or more) data lines, but it is assumed that  $j$  is 3 for the convenience of description.

**[0033]** Referring to FIG. 2, the organic light emitting display device according to one embodiment of the present invention includes a display unit 130 that includes pixels 140 positioned at regions where first scan lines  $S11$  to  $S1n$  and second scan lines  $S21$  to  $S2n$  cross second data lines  $D21$  to  $D2m$ , common circuit units 160, which are connected between first data lines  $D11$  to  $D1m$  and the second data lines  $D21$  to  $D2m$  and are connected to the DEMUXs 170 through the first data lines  $D11$  to  $D1m$ , a scan driver 110 for driving the first scan lines  $S11$  to  $S1n$ , the second scan lines  $S21$  to  $S2n$ , and emission control lines  $E1$  to  $En$ , a data driver 120 for providing  $j$  data signals to each of output lines  $O1$  to  $Oj$ , respectively, during a horizontal period, and a timing controller 150 for controlling the scan driver 110 and the data driver 120.

**[0034]** In addition, according to one embodiment of the present invention, each of the DEMUXs 170 is connected to a corresponding one of the output lines  $O1$  to  $Oj$ . Each of the output lines  $O1$  to  $Oj$  provides  $j$  data signals to a connected one of the DEMUXs 170 during a horizontal period. The organic light emitting display device according to one embodiment of the present invention includes a switch control unit 180 for controlling the common circuit units 160.

**[0035]** The scan driver 110 receives a scan driving control signal SCS from the timing controller 150. The scan driver 110 that receives the scan driving control signal SCS generates and sequentially provides first scan signals to the first scan lines  $S11$  to  $S1n$  and generates and sequentially provides second scan signals to the second scan lines  $S21$  to  $S2n$ . In addition, the scan driver 110 generates and sequentially provides emission control signals to the emission control lines  $E1$  to  $En$ .

**[0036]** Here, the first scan signals and the second scan signals are set to a voltage (e.g., low voltage) at which transistors included in the pixel 140 may be turned on, and the emission control signals are set to a voltage (e.g., high voltage) at which the transistors included in the pixel 140 may be turned off. In addition, a second scan signal provided to a  $k$ -th ( $k$  is a natural number) second scan line  $S2k$  is provided earlier than a first scan signal provided to a  $k$ -th first scan line  $S1k$  and stops to be provided after the first scan signal stops to be provided. Further, the emission control signal provided to the emission control line ( $E1$  to  $En$ ) is provided to be overlapped with two second scan signals. For example, the emission control signal provided to the  $k$ -th emission control line  $Ek$  overlaps with the second scan signals provided to a  $k$ -th second scan line  $S2k$  and a  $(k+1)$ -th second scan line  $S2k+1$ .

**[0037]** The data driver 120 receives a data driving control signal DCS from the timing controller 150. The data driver 120 that receives the data driving control signal DCS provides  $j$  data signals to each of the output lines  $O1$  to  $Oj$  in every horizontal period. Here, the data driver 120 provides the data signals to the output lines  $O1$  to  $Oj$  during a period when the first scan signal is not provided and the second scan signal is provided.

**[0038]** The timing controller 150 generates the data driving control signal DCS and the scan driving control signal SCS to correspond to externally provided synchronization signals. The data driving control signal DCS generated by the timing controller 150 is provided to the data driver 120, and the scan driving control signal SCS is provided to the scan driver 110. In addition, the timing controller 150 provides externally provided data Data to the data driver 120.

**[0039]** Each of the DEMUXs 170 is connected between a corresponding one of the output lines  $O1$  to  $Oj$  and  $j$  first data lines. Each of the DEMUXs 170 distributes  $j$  data signals supplied from each of the output lines  $O1$  to  $Oj$  to  $j$  first data lines  $D11$  to  $D1m$  in response to control signals CS1, CS2, and CS3 provided from the switch control unit 180.

**[0040]** The common circuit units 160 are formed between the first data lines  $D11$  to  $D1m$  and the second data lines  $D21$  to  $D2m$ , respectively. The common circuit units 160 receive an initial voltage  $V_{int}$  and a reference voltage  $V_{ref}$  supplied from the outside. Each of the common circuit units 160 that receives the initial voltage  $V_{int}$  and the reference voltage  $V_{ref}$  controls voltage of a first data line to which the common circuit unit 160 is connected in accordance with the control of the switch control unit 180.

**[0041]** The switch control unit 180 controls turn-on and turn-off of transistors included in the DEMUXs 170 and the common circuit units 160 while providing control signals CS3 to CS5 to the DEMUXs 170 and control signals CS1 to CS2 to the common circuit units 160. Here, the switch control unit 180 provides the third control signal CS3 to the fifth control signal CS5 in order to control three transistors included in the DEMUX 170 and provides the first control signal CS1 and the second control signal CS2 in order to control two transistors included in the common circuit unit 160.

**[0042]** In FIG. 2, the switch control unit 180 is additionally shown for the convenience of description according to one embodiment, but the present invention is not limited thereto. As one example, the switch control unit 180 may be included in the timing controller 150. In this case, the timing controller 150 generates the first control signal CS1 to the fifth control

signal CS5 to control driving of the DEMUXs 170 and the common circuit units 160.

**[0043]** Each of the pixels 140 receives a first power supply ELVDD and a second power supply ELVSS from the outside. The pixels 140 that receive the first power supply ELVDD and the second power supply ELVSS generate light having a luminance (e.g., a predetermined luminance) while controlling the amount of current that flows to the second power supply ELVSS from the first power supply ELVDD to correspond to the data signals.

**[0044]** FIG. 3 is a circuit diagram showing an embodiment of a pixel shown in FIG. 2. In FIG. 3, a pixel 140 connected to a 2m-th data line D2m and a 1 n-th scan line S1 n is shown.

**[0045]** Referring to FIG. 3, the pixel 140 according to one embodiment of the present invention includes an organic light emitting diode OLED and a pixel circuit 142 for supplying current to the OLED.

**[0046]** An anode electrode of the OLED is connected to the pixel circuit 142 and a cathode electrode of the OLED is connected to the second power supply ELVSS. The OLED generates light having a luminance (e.g., a predetermined luminance) to correspond to the amount of current supplied from the pixel circuit 142.

**[0047]** The pixel circuit 142 receives a voltage (e.g., a predetermined voltage) corresponding to the data signal and supplies a current corresponding to the received voltage to the OLED. Here, the pixel circuit 142 includes first to fourth transistors M1 to M4 and a storage capacitor Cst.

**[0048]** A first electrode of the first transistor M1 is connected to the common circuit unit 160 through the second data line D2m and a second electrode of the first transistor M1 is connected to a gate electrode of the second transistor M2. In addition, a gate electrode of the first transistor M1 is connected to the second scan line S2n. The first transistor M1 is turned on when the scan signal is provided to the second scan line S2n.

**[0049]** A first electrode of the second transistor M2 is connected to the first power supply ELVDD, and a second electrode of the second transistor M2 is connected to a first electrode of the fourth transistor M4. In addition, the gate electrode of the second transistor M2 is connected to the second electrode of the first transistor M1. The second transistor M2 supplies a current corresponding to a voltage applied to its own gate electrode to the OLED through the fourth transistor M4.

**[0050]** A first electrode of the third transistor M3 is connected to the second electrode of the second transistor M2, and the second electrode of the third transistor M3 is connected to the gate electrode of the second transistor M2. In addition, a gate electrode of the third transistor M3 is connected to the first scan line S1 n. The third transistor M3 is turned on when the scan signal is provided to the first scan line S1 n.

In this case, the third transistor M3 remains turned off after the first transistor M1 is turned on and turned off before the first transistor M1 is turned off. Here, when the third transistor M3 is turned on, the second transistor M2 is connected in a diode-connected configuration.

**[0051]** A first electrode of the fourth transistor M4 is connected to the second electrode of the second transistor M2, and the second electrode of the fourth transistor M4 is connected to the anode electrode of the OLED. In addition, a gate electrode of the fourth transistor M4 is connected to the emission control line En. The fourth transistor M4 is turned off when the emission control signal is provided and turned on when the emission control signal is not provided.

**[0052]** The storage capacitor Cst is connected between the gate electrode and the first electrode of the second transistor M2. The storage capacitor Cst is charged with a voltage (e.g., a predetermined voltage) to correspond to the voltage applied to the gate electrode of the second transistor M2.

**[0053]** FIG. 4 is a circuit diagram showing an embodiment of a common circuit unit 160 shown in FIG. 2. In FIG. 4, the common circuit unit 160 is connected to a 1m-th data line D1m. In addition, the common circuit unit 160 is connected to a plurality of pixels 140 in a unit of a vertical line (e.g., a column of pixels), but only one pixel 140 is shown in FIG. 4.

**[0054]** Referring to FIG. 4, the common circuit unit 160 includes a first capacitor C1 having a first terminal connected to the first data line D1m and a second terminal connected to the second data line D2m, a first common transistor CM1 connected between the reference voltage Vref and the first terminal of the first capacitor C1, and a second common transistor CM2 connected between the initial voltage Vint and the second terminal of the first capacitor C1.

**[0055]** The first common transistor CM1 is connected between the reference voltage Vref and the first terminal of the first capacitor C1 and is turned on when the first control signal CS1 is provided. When the first common transistor CM1 is turned on, the voltage of the reference voltage Vref is supplied to the first terminal of the first capacitor C1.

**[0056]** The second common transistor CM2 is connected between the initial voltage Vint and the second terminal of the first capacitor C1 and is turned on when the second control signal CS2 is provided. When the second common transistor CM2 is turned on, the voltage of the initial voltage Vint is supplied to the second terminal of the second capacitor C2.

**[0057]** The first capacitor C1 is formed between the first data line D1m and the second data line D2m. The first capacitor C1 varies the voltage (i.e., the voltage of the second data line D2m) supplied to the pixel 140 to correspond to the data signal provided to the DEMUX 170.

**[0058]** FIG. 5 is a circuit diagram showing an embodiment of a DEMUX 170 shown in FIG. 2. In FIG. 5, a DEMUX 170 is connected to the i-th output line Oi.

**[0059]** Referring to FIG. 5, the DEMUX 170 includes a 10-th transistor M10, an 11-th transistor M11, and a 12-th

transistor M12.

**[0060]** The 10-th transistor M10 is connected between the output line Oi and a (1m-2)-th data line D1m-2. The 10-th transistor M10 is turned on when the third control signal CS3 is supplied to provide the data signal provided from the output line Oi to the (1m-2)-th data line D1m-2.

**[0061]** The 11-th transistor M11 is connected between the output line Oi and a (1m-1)-th data line D1m-1. The 11-th transistor M11 is turned on when the fourth control signal CS4 is supplied to provide the data signal provided from the output line Oi to the (1m-1)-th data line D1m-1.

**[0062]** The 12-th transistor M12 is connected between the output line Oi and the 1m-th data line D1m. The 12-th transistor M12 is turned on when the fifth control signal CS5 is supplied to provide the data signal provided from the output line Oi to the 1m-th data line D1m.

**[0063]** Here, the third control signal CS3 to the fifth control signal CS5 are sequentially supplied, and, as a result, the data signals are supplied to the (1m-2)-th data line D1m-2, the (1m-1)-th data line D1m-1, and the first data line D1m while the 10-th transistor M10 to the 12-th transistor M12 are sequentially turned on.

**[0064]** FIG. 6 is a circuit diagram showing a connection structure of a demultiplexer, a common circuit unit, and pixels. In FIG. 6, the DEMUX 170 connected to the i-th output line Oi, the common circuit units 160, and the pixels 140 are shown according to one embodiment of the present invention.

**[0065]** Referring to FIG. 6, the output line Oi is connected to the DEMUX 170, and the DEMUX 170 includes the 10-th transistor M10, the 11-th transistor M11, and the 12-th transistor M12 that are connected to the first data lines D1m-2, D1m-1, and D1m, respectively.

**[0066]** The common circuit units 160 are positioned between the first data lines D1m-2, D1m-1, and D1m and the second data lines D2m-2, D2m-1, and D2m, respectively. The common circuit units 160 control voltages of the second data lines D2m-2, D2m-1, and D2m to correspond to the initial voltage Vint, the reference voltage Vref, and the data signals.

**[0067]** In addition, in FIG. 6, a data capacitor Cdata represents an equivalent parasitic capacitor. Here, since a first terminal of the first capacitor C1 is positioned adjacent to the DEMUX 170, the parasitic capacitor formed by the first data line does not substantially influence driving. However, since the pixel 140 connected to a second terminal of the first capacitor C1 are separated from each other in a vertical direction by a distance (e.g., a predetermined distance), a parasitic capacitor of the second data line influences driving. As a panel becomes larger, the influence of the parasitic capacitor of the second data line becomes larger. Therefore, in one embodiment of the present invention, the parasitic capacitor of the second data line that influences driving is shown as the data capacitor Cdata in FIG. 6.

**[0068]** FIG. 7 is a waveform diagram for showing driving methods of a demultiplexer, a common circuit unit, and pixels shown in FIG. 6.

**[0069]** Referring to FIG. 7, a first horizontal period 1 H is divided into a first period t1 to a fifth period t5.

**[0070]** First, during the first period t1, the first control signal CS1 and the second control signal CS2 are provided. Here, the first control signal CS1 is provided during the first period t1 to the fourth period t4, and the second control signal CS2 is provided during the first period t1.

**[0071]** When the first control signal CS1 is provided, the first common transistor CM1 is turned on as shown in FIG. 8A. In FIGS. 8A to 8E, when a transistor is turned off, only its reference numeral is shown in the drawing without its circuit symbol. However, it should be understood that the transistor is not physically removed from the circuit shown in FIGS. 8A to 8E. When the first common transistor CM1 is turned on, the voltage of the reference voltage Vref is supplied to a second node N2 (i.e., the first terminal of the first capacitor C1). Here, the voltage of the reference voltage Vref is set to a voltage lower than the voltage of a black data signal Vdata(black). The detailed description thereof will be described below.

**[0072]** When the second control signal CS2 is provided, the second common transistor CM2 is turned on. When the second common transistor CM2 is turned on, the voltage of the initial voltage Vint is supplied to a third node N3 (i.e., the second terminal of the first capacitor C1). Here, the voltage of the initial voltage Vint is set to a voltage sufficiently lower than a voltage obtained by subtracting an absolute value of the threshold voltage of the second transistor M2 from the voltage of the first power supply ELVDD. Here, when the initial voltage Vint is electrically connected to the first node N3 and the first node N1, the voltage of the first node N1 is set to the voltage lower than the voltage obtained by subtracting the absolute value of the threshold voltage of the second transistor M2 from the voltage of the first power supply ELVDD.

**[0073]** Here, since the first transistor M1 maintains a turn-off state during the first period t1, the first node N1 (i.e., the gate electrode of the second transistor M2) maintains the voltage charged during a previous frame period.

**[0074]** The second scan signal is provided to the second scan line S2n during the second period t2. When the scan signal is provided to the second scan line S2n, the first transistor M1 is turned on as shown in FIG. 8B. When the first transistor M1 is turned on, the first node N1 and the third node N3 are electrically connected to each other. Here, the second scan signal is provided during the second period t2 to the fifth period t5.

**[0075]** The first scan signal is provided to the first scan line S1 n during the third period t3. When the first scan signal is provided to the first scan line S1 n, the third transistor M3 is turned on as shown in FIG. 8C. When the third transistor M3 is turned on, the second transistor M2 is connected in the diode-connected configuration. In this case, the voltages

of the first node N1 and the third node N3 are set to the voltage obtained by subtracting the absolute value of the threshold voltage of the second transistor M2 from the voltage of the first power supply ELVDD as shown in Equation 1.

### Equation 1

$$V_{N1} = V_{N3} = ELVDD - |V_{th}(M2)|$$

**[0076]** Here, in one embodiment of the present invention, after the second scan signal is provided to the second scan line S2n, the first scan signal is provided to the first scan line S1 n. That is, in the embodiment of the present invention, it is possible to secure the reliability of an operation by providing the first scan signal after initializing the voltage of the first node N1 by firstly providing the second scan signal.

**[0077]** During the fourth period t4, the first scan signal stops to be provided. When the first scan signal stops to be provided, the third transistor M3 is turned off.

**[0078]** During the fifth period t5, the third control signal CS3, the fourth control signal CS4, and the fifth control signal CS5 are sequentially provided while the first control signal CS1 is not provided. When the first control signal CS1 is not provided, the first common transistor CM1 is turned off as shown in FIG. 8E. Here, since the first control signal CS1 stops to be provided after the first scan signal stops to be provided, the second node N2 maintains the voltage of the reference voltage Vref irrespective of the turn-off of the third transistor M3.

**[0079]** When the third control signal CS3 is provided, the 10-th transistor M10 is turned on. When the 10-th transistor M10 is turned on, the data signal provided to the output line Oi is provided to the second node N2. In this case, the voltage of the second node N2 is changed to the voltage of the data signal from the voltage of the reference voltage Vref.

**[0080]** When the voltage of the second node N2 is changed to the voltage of the data signal from the voltage of the reference voltage Vref, the voltage of the first node N1 varies as shown in Equation 2 to correspond to the variation of the voltage of the second node N2 from a voltage of  $ELVDD - |V_{th}(M2)|$ .

### Equation 2

$$V_{N1} = ELVDD - |V_{th}(M2)| + \{(C1+Cdata+Cst)/C1\} \times (Vdata-Vref)$$

**[0081]** In Equation 2, Vdata represents the voltage of the data signal.

**[0082]** In Equation 2, the first power supply ELVDD, the threshold voltage of the second transistor M2, the first capacitor C1, the data capacitor Cdata, and the storage capacitor Cst have respective determined values in design. In addition, the voltage of the reference voltage Vref is set to a value corresponding to the capacitances of the data capacitor Cdata and the first capacitor C1. Here, the voltage value of the reference voltage Vref is experimentally set so as to charge the pixel 140 with the desired voltage irrespective of the capacitances of the data capacitor Cdata and the first capacitor C1.

**[0083]** The voltage value of the voltage Vdata of the data signal varies depending on a gray-level to be expressed. That is, in Equation 2, only the voltage Vdata of the data signal varies depending on the gray-level, and, as a result, the voltage of the first node N1 is determined by the voltage Vdata of the data signal.

**[0084]** Thereafter, the 11-th transistor M11 and the 12-th transistor M12 are sequentially turned on to correspond to the fourth control signal CS4 and the fifth control signal CS5, respectively. At this time, the voltage of the first node N1 of the pixel 140 connected to each of the 11-th transistor M11 and the 12-th transistor M12 is set as shown in Equation 2.

**[0085]** After the fifth period t5, the second scan signal stops to be provided to the second scan line S2n, such that the first transistor M1 is turned off. In this case, the storage capacitor Cst is charged with the voltage applied to the first node N1 and maintains the charged voltage during the fifth period t5.

**[0086]** Thereafter, the emission control signal stops to be provided to the emission control line En during a sixth period t6. When the emission control signal stops to be provided to the emission control line En, the fourth transistor M4 is turned on. When the fourth transistor M4 is turned on, the second transistor M2 and the anode electrode of the OLED are electrically connected to each other. In this case, the second transistor M2 supplies a current corresponding to the voltage applied to the first node N1 to the OLED to emit light corresponding to a gray-level.

**[0087]** Here, in one embodiment of the present invention, the voltage of the reference voltage Vref is set to a voltage lower than the voltage of the black data signal Vdata(black). When the voltage of the reference voltage Vref is set to the voltage lower than the voltage of the black data signal Vdata(black), the voltage of the first node N1 is set to a voltage higher than the voltage of  $ELVDD - |V_{th}(M2)|$  to express a full black color at the time of expressing a black gray-level.

**[0088]** In addition, as shown in Equation 2, when the voltage of the first node N1 is set, the current supplied to the

OLED is determined irrespective of the voltage drop of the first power supply ELVDD and the threshold voltage of the second transistor M2. In other words,  $ELVDD - |V_{th}(M2)|$  is removed from an equation for determining a current flowing on the OLED, and, as a result, it is possible to display an image having a desired luminance irrespective of the voltage drop of the first power supply ELVDD and the threshold voltage of the second transistor M2.

**[0089]** Further, in one embodiment of the present invention, a relatively simple structure in which each of the pixels 140 includes four transistors M1 to M4 and only one capacitor Cst is formed, thereby improving reliability and reducing manufacturing cost.

**[0090]** While the present invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims, and equivalents thereof.

## Claims

1. An organic light emitting display device adapted to be driven during a horizontal period comprising first, second, third, fourth, and fifth periods (t1, t2, t3, t4, t5), the first to fifth period being consecutive and non-overlapping, the organic light emitting device comprising:

a plurality of horizontal lines, extending along a horizontal direction of the organic light emitting display device, wherein each of the horizontal lines of the organic light emitting display device comprises, arranged in parallel next to each other, a first scan line (S11, S12, S13, S1n), a second scan line (S21, S22, S23, S2n) and an emission control line (E1, E2, E3, En);

a plurality of data lines extending along a vertical direction of the organic light emitting display device, each of the data lines comprising a first data line section (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m) and a second data line section (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m), the second data line section (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) crossing the scan lines (S11, S12, S13, S1n, S21, S22, S23, S2n);

a scan driver (110) adapted to drive the first and second scan lines (S11, S12, S13, S1n, S21, S22, S23, S2n) and the emission control lines (E1, E2, E3, En);

a data driver (120) adapted to sequentially provide j data signals to each of a plurality of output lines (O1, O2, Oi) of the data driver (120) in each horizontal period;

at least one demultiplexer (170) adapted to transmit the j data signals to j first data line sections (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m), the demultiplexer being directly connected to the plurality of output lines (O1, O2, Oi);

a plurality of pixels (140) at crossing regions of the scan lines (S11, S12, S13, S1n, S21, S22, S23, S2n) and second data line sections (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m);

at least one common circuit unit (160) adapted to control voltages of the second data line sections (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) connected to the pixels (140) by using a reference voltage (Vref), an initial voltage (Vint) and the data signals, the common circuit unit (160) being directly connected to one of the first data line sections (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m) and to a corresponding one of the second data line sections (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m); and

a switch control unit (180) adapted to control the at least one demultiplexer (170) and the at least one common circuit unit (160),

wherein each of the pixels (140) comprises:

an organic light emitting diode (OLED) having a cathode electrode directly connected to a second power supply (ELVSS);

a second transistor (M2) comprising a gate electrode, a first electrode and a second electrode, the first electrode of the second transistor (M2) being directly connected to a first power supply (ELVDD) and the second transistor (M2) being configured to control an amount of current supplied to the organic light emitting diode (OLED);

a first transistor (M1) comprising a gate electrode, a first electrode and a second electrode, the first electrode of the first transistor (M1) being directly connected to the gate electrode of the second transistor (M2) and the second electrode of the first transistor (M1) being directly connected to one second data line section (D2m) and the first transistor (M1) being configured to be turned on when the second scan signals are provided to one second scan line (S2n) directly connected to the gate electrode of the first transistor (M1);

a third transistor (M3) comprising a gate electrode, a first electrode and a second electrode, the first electrode



of the third transistor (M3) being directly connected to the gate electrode of the second transistor (M2) and the second electrode of the third transistor (M3) being directly connected to the second electrode of the second transistor (M2) and the third transistor (M3) being configured to be turned on to diode-connect the second transistor (M2) when first scan signals are provided to one first scan line (S1n) directly connected to the gate electrode of the third transistor (M3); and  
 a fourth transistor (M4) comprising a gate electrode, a first electrode and a second electrode, the first electrode of the fourth transistor (M4) being directly connected to the second electrode of the second transistor (M2) and the second electrode of the fourth transistor (M4) being directly connected to the anode electrode of the organic light emitting diode (OLED) and the fourth transistor (M4) being configured to be turned off when the emission control signals are provided to one emission control line (En) directly connected to the gate electrode of the fourth transistor (M4), and

wherein

each of the common circuit units (160) comprises:

a first capacitor (C1) directly connected to one first data line section (D1m) of the first data line sections (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m) by a first electrode and to one second data line section (D2m) of the second data line sections (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) by a second electrode;

a first common transistor (CM1) having first and second electrodes directly connected between said one (D1m) of the first data line sections (D11, D12, D13, D14, D16, D1m-2, D1m-1, D1m) and a voltage source providing the reference voltage (Vref), the first common transistor (CM1) being configured to be turned on in response to a first control signal (CS1) from the switch control unit (180); and

a second common transistor (CM2) having first and second electrodes directly connected between said one (D2m) of the second data line sections (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) and a voltage source providing the initial voltage (Vint), the second common transistor (CM2) being configured to be turned on in response to a second control signal (CS2) from the switch control unit (180), wherein the organic light emitting display device is configured to be driven such that

the first scan signal is not provided during the first, the second, the fourth and the fifth period and is continuously provided during the third period,

the second scan signal is not provided during the first period and is continuously provided during the second, the third, the fourth and the fifth period,

the emission control signal is not provided during the first, the second, the third, the fourth and the fifth period, the second control signal is continuously provided during the first period and is not provided during the second, the third, the fourth and the fifth period, and

the first control signal is continuously provided during the first, the second, the third and the fourth period and is not provided during the fifth period.

2. The organic light emitting display device of claim 1, wherein each demultiplexer (170) comprises j transistors (M10, M11, M12) having first and second electrodes, the first electrodes being directly connected to one of the output lines (Oi) and the second electrodes being directly connected to a respective one of the first data line sections (D1m-2, D1m-1, D1m), and the j transistors (M10, M11, M12) being configured to be sequentially turned on in response to j control signals (CS3, CS4, CS5) provided from the switch control unit (180).

3. The organic light emitting display device of one of the preceding claims, wherein the scan driver (110) is configured to sequentially provide first scan signals to the first scan lines (S11, S12, S13, S1n), sequentially provide second scan signals to the second scan lines (S21, S22, S23, S2n), and sequentially provide emission control signals to the emission control lines (E1, E2, E3, En).

4. The organic light emitting display device of one of the preceding claims, wherein the scan driver (110) is configured to provide emission control signals overlapping with at least two of the second scan signals.

5. The organic light emitting display device of one of the preceding claims, wherein the data driver (120) is configured to sequentially provide the j data signals during the fifth period (t5) of the horizontal period.

6. A driving method of an organic light emitting display device adapted to be driven during a horizontal period comprising first, second, third, fourth, and fifth periods (t1, t2, t3, t4, t5), the first to fifth period being consecutive and non-overlapping, wherein the organic light emitting display comprises a plurality of pixels (140) arranged in a matrix and

a plurality of common circuit units (160), each common circuit unit (160) comprising a first capacitor (C1) comprising a first electrode and a second electrode, the first electrode being directly connected to a first data line (D1m) for receiving a data signal and the second electrode being directly connected to a second data line (D2m), and the second data line (D2m) being directly connected to the pixels (140) arranged along a column, each pixel (140) comprising a second transistor (M2) comprising a gate electrode, a first electrode and a second electrode, the first electrode of the second transistor (M2) being directly connected to a first power supply (ELVDD), the second transistor (M2) controlling an amount of current flowing to a second power supply (ELVSS) from the first power supply (ELVDD) through an organic light emitting diode (OLED), a first transistor (M1) comprising a gate electrode, a first electrode and a second electrode, the first electrode of the first transistor (M1) being directly connected to the gate electrode of the second transistor (M2) and the second electrode of the first transistor (M1) being directly connected to one second data line (D2m) of the second data lines (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) and the first transistor (M1) being configured to be turned on when a second scan signal is provided to a corresponding second scan line (S2n) of second scan lines (S21, S22, S23, S2n), a third transistor (M3) comprising a gate electrode, a first electrode and a second electrode, the first electrode of the third transistor (M3) being directly connected to the gate electrode of the second transistor (M2) and the second electrode of the third transistor (M3) being directly connected to the second electrode of the second transistor (M2) and the third transistor (M3) being configured to be turned on when a first scan signal is provided to a corresponding first scan line (S1n) of first scan lines (S11, S12, S13, S1n); and a fourth transistor (M4) comprising a gate electrode, a first electrode and a second electrode, the first electrode of the fourth transistor (M4) being directly connected to the second electrode of the second transistor (M2) and the second electrode of the fourth transistor (M4) being directly connected to the anode electrode of the organic light emitting diode (OLED), the fourth transistor (M4) being configured to be turned off when an emission control signal is provided to a corresponding emission control line (En) of emission control lines (E1, E2, E3, En), the cathode electrode of the organic light emitting diode (OLED) being directly connected to the second power supply (ELVSS),

each of the common circuits (160) further comprising a first common transistor (CM1) having first and second electrodes directly connected between said one (D1m) of the first data lines (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m) and a voltage source providing a reference voltage (Vref), the first common transistor (CM1) being configured to be turned on in response to a first control signal (CS1) from the switch control unit (180); and a second common transistor (CM2) having first and second electrodes directly connected between said one (D2m) of the second data lines (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) and a voltage source providing an initial voltage (Vint), the second common transistor (CM2) being configured to be turned on in response to a second control signal (CS2) from the switch control unit (180), the method comprising:

supplying the reference voltage (Vref) to the first data line (D1m) during the first to fourth periods (t1, t2, t3, t4) and supplying the initial voltage (Vint) to the second data line (D2m) during the first period (t1); electrically coupling the second data line (D2m) to the gate electrode of the second transistor (M2) while supplying the reference voltage (Vref) to the first data line (D1m) during the second period (t2); increasing the voltage of the second data line (D2m) to a voltage obtained by subtracting an absolute value of a threshold voltage of the second transistor (M2) from the voltage of the first power supply (ELVDD) by electrically coupling the second transistor (M2) in a diode-connected configuration while supplying the reference voltage (Vref) to the first data line (D1m) during the third period (t3); and varying the voltage of the gate electrode of the second transistor (M2) by providing data signals to the first data line (D1m) during the fifth period (t5), wherein

the first scan signal is not provided during the first, the second, the fourth and the fifth period and is continuously provided during the third period,

the second scan signal is not provided during the first period and is continuously provided during the second, the third, the fourth and the fifth period,

the emission control signal is not provided during the first, the second, the third, the fourth and the fifth period,

the second control signal is continuously provided during the first period and is not provided during the second, the third, the fourth and the fifth period, and

the first control signal is continuously provided during the first, the second, the third and the fourth period and is not provided during the fifth period.

7. The driving method of an organic light emitting display device of claim 6, wherein the reference voltage (Vref) is lower than a voltage of a black data signal for expressing a black gray-level, and/or wherein the initial voltage (Vint) is lower than the voltage obtained by subtracting the absolute value of the threshold voltage of the second transistor (M2) from the voltage of the first power supply (ELVDD).

## Patentansprüche

1. Organische lichtemittierende Anzeigevorrichtung, die ausgeführt ist, während einer erste, zweite, dritte, vierte und fünfte Perioden ( $t_1$ ,  $t_2$ ,  $t_3$ ,  $t_4$ ,  $t_5$ ) umfassenden Horizontalperiode angesteuert zu werden, wobei die erste bis fünfte Periode aufeinanderfolgend sind und nicht überlappen, wobei die organische lichtemittierende Vorrichtung umfasst:

eine Vielzahl horizontaler Zeilen, die sich entlang einer horizontalen Richtung der organischen lichtemittierenden Anzeigevorrichtung erstrecken, wobei jede der horizontalen Zeilen der organischen lichtemittierenden Anzeigevorrichtung parallel nebeneinander angeordnet eine erste Abtastzeile ( $S_{11}$ ,  $S_{12}$ ,  $S_{13}$ ,  $S_{1n}$ ), eine zweite Abtastzeile ( $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{2n}$ ) und eine Emissionssteuerleitung ( $E_1$ ,  $E_2$ ,  $E_3$ ,  $E_n$ ) umfasst;

eine Vielzahl von Datenleitungen, die sich entlang einer senkrechten Richtung der organischen lichtemittierenden Anzeigevorrichtung erstrecken, wobei jede der Datenleitungen einen ersten Datenleitungsabschnitt ( $D_{11}$ ,  $D_{12}$ ,  $D_{13}$ ,  $D_{14}$ ,  $D_{15}$ ,  $D_{16}$ ,  $D_{1m-2}$ ,  $D_{1m-1}$ ,  $D_{1m}$ ) und einen zweiten Datenleitungsabschnitt ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ ) umfasst, wobei der zweite Datenleitungsabschnitt ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ ) die Abtastzeilen ( $S_{11}$ ,  $S_{12}$ ,  $S_{13}$ ,  $S_{1n}$ ,  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{2n}$ ) kreuzt;

einen Abtasttreiber (110), der ausgeführt ist, die ersten und zweiten Abtastzeilen ( $S_{11}$ ,  $S_{12}$ ,  $S_{13}$ ,  $S_{1n}$ ,  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{2n}$ ) und die Emissionssteuerleitungen ( $E_1$ ,  $E_2$ ,  $E_3$ ,  $E_n$ ) anzusteuern;

einen Datentreiber (120), der ausgeführt ist, in jeder Horizontalperiode jeder einer Vielzahl von Ausgangsleitungen ( $O_1$ ,  $O_2$ ,  $O_i$ ) des Datentreibers (120)  $j$  Datensignale sequentiell bereitzustellen;

mindestens einen Demultiplexer (170), der ausgeführt ist, die  $j$  Datensignale an  $j$  erste Datenleitungsabschnitte ( $D_{11}$ ,  $D_{12}$ ,  $D_{13}$ ,  $D_{14}$ ,  $D_{15}$ ,  $D_{16}$ ,  $D_{1m-2}$ ,  $D_{1m-1}$ ,  $D_{1m}$ ) zu übertragen, wobei der Demultiplexer direkt mit der Vielzahl von Ausgangsleitungen ( $O_1$ ,  $O_2$ ,  $O_i$ ) verbunden ist;

eine Vielzahl von Pixeln (140) an Kreuzungsbereichen der Abtastzeilen ( $S_{11}$ ,  $S_{12}$ ,  $S_{13}$ ,  $S_{1n}$ ,  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{2n}$ ) und zweiten Datenleitungsabschnitten ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ );

mindestens eine gemeinsame Schaltungseinheit (160), die ausgeführt ist, Spannungen der mit den Pixeln (140) verbundenen zweiten Datenleitungsabschnitte ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ ) durch Verwendung einer Referenzspannung ( $V_{ref}$ ), einer Anfangsspannung ( $V_{int}$ ) und der Datensignale zu steuern, wobei die gemeinsame Schaltungseinheit (160) direkt mit einem der ersten Datenleitungsabschnitte ( $D_{11}$ ,  $D_{12}$ ,  $D_{13}$ ,  $D_{14}$ ,  $D_{15}$ ,  $D_{16}$ ,  $D_{1m-2}$ ,  $D_{1m-1}$ ,  $D_{1m}$ ) und einem entsprechenden der zweiten Datenleitungsabschnitte ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ ) verbunden ist; und

eine Schaltsteuereinheit (180), die ausgeführt ist, den mindestens einen Demultiplexer (170) und die mindestens eine gemeinsame Schaltungseinheit (160) zu steuern,

wobei jedes der Pixel (140) umfasst:

eine organische lichtemittierende Diode (OLED) mit einer Kathodenelektrode, die direkt mit einer zweiten Stromversorgung (ELVSS) verbunden ist;

einen zweiten Transistor (M2), umfassend eine Gate-Elektrode, eine erste Elektrode und eine zweite Elektrode, wobei die erste Elektrode des zweiten Transistors (M2) direkt mit einer ersten Stromversorgung (ELVDD) verbunden ist und der zweite Transistor (M2) zum Steuern einer der organischen lichtemittierenden Diode (OLED) zugeführten Strommenge konfiguriert ist;

einen ersten Transistor (M1), umfassend eine Gate-Elektrode, eine erste Elektrode und eine zweite Elektrode, wobei die erste Elektrode des ersten Transistors (M1) direkt mit der Gate-Elektrode des zweiten Transistors (M2) verbunden ist und die zweite Elektrode des ersten Transistors (M1) direkt mit einem zweiten Datenleitungsabschnitt ( $D_{2m}$ ) verbunden ist und der erste Transistor (M1) zum Einschalten konfiguriert ist, wenn die zweiten Abtastsignale einer zweiten Abtastzeile ( $S_{2n}$ ) bereitgestellt werden, die direkt mit der Gate-Elektrode des ersten Transistors (M1) verbunden ist;

einen dritten Transistor (M3), umfassend eine Gate-Elektrode, eine erste Elektrode und eine zweite Elektrode, wobei die erste Elektrode des dritten Transistors (M3) direkt mit der Gate-Elektrode des zweiten Transistors (M2) verbunden ist und die zweite Elektrode des dritten Transistors (M3) direkt mit der zweiten Elektrode des zweiten Transistors (M2) verbunden ist und der dritte Transistor (M3) zum Einschalten konfiguriert ist, um den zweiten Transistor (M2) als Diode zu schalten, wenn erste Abtastsignale einer ersten Abtastzeile ( $S_{1n}$ ) bereitgestellt werden, die direkt mit der Gate-Elektrode des dritten Transistors (M3) verbunden ist; und

einen vierten Transistor (M4), umfassend eine Gate-Elektrode, eine erste Elektrode und eine zweite Elektrode, wobei die erste Elektrode des vierten Transistors (M4) direkt mit der zweiten Elektrode des zweiten Transistors (M2) verbunden ist und die zweite Elektrode des vierten Transistors (M4) direkt mit der Anodenelektrode der organischen lichtemittierenden Diode (OLED) verbunden ist und der vierte Transistor

(M4) zum Ausschalten konfiguriert ist, wenn die Emissionssteuersignale einer mit der Gate-Elektrode des vierten Transistors (M4) direkt verbundenen Emissionssteuerleitung (En) bereitgestellt werden, und

wobei jede der gemeinsamen Schaltungseinheiten (160) umfasst:

einen ersten Kondensator (C1), der über eine erste Elektrode direkt mit einem ersten Datenleitungsabschnitt (D1m) der ersten Datenleitungsabschnitte (D11, D12, D13, D14, D15, D16, D1 m-2, D1 m-1, D1 m) und über eine zweite Elektrode mit einem zweiten Datenleitungsabschnitt (D2m) der zweiten Datenleitungsabschnitte (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) verbunden ist;  
einen ersten gemeinsamen Transistor (CM1) mit ersten und zweiten Elektroden, der direkt zwischen den einen (D1 m) der ersten Datenleitungsabschnitte (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m) und eine die Referenzspannung (Vref) bereitstellende Spannungsquelle geschaltet ist, wobei der erste gemeinsame Transistor (CM1) zum Einschalten als Reaktion auf ein erstes Steuersignal (CS1) von der Schaltsteuereinheit (180) konfiguriert ist; und  
einen zweiten gemeinsamen Transistor (CM2) mit ersten und zweiten Elektroden, der direkt zwischen den einen (D2m) der zweiten Datenleitungsabschnitte (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) und eine die Anfangsspannung (Vint) bereitstellende Spannungsquelle geschaltet ist, wobei der zweite gemeinsame Transistor (CM2) zum Einschalten als Reaktion auf ein zweites Steuersignal (CS2) von der Schaltsteuereinheit (180) konfiguriert ist, wobei  
die organische lichtemittierende Anzeigevorrichtung derart zum Ansteuern konfiguriert ist, dass  
das erste Abtastsignal nicht während der ersten, der zweiten, der vierten und der fünften Periode bereitgestellt wird und kontinuierlich während der dritten Periode bereitgestellt wird,  
das zweite Abtastsignal nicht während der ersten Periode bereitgestellt wird und kontinuierlich während der zweiten, der dritten, der vierten und der fünften Periode bereitgestellt wird,  
dass Emissionssteuersignal nicht während der ersten, der zweiten, der dritten, der vierten und der fünften Periode bereitgestellt wird,  
das zweite Steuersignal kontinuierlich während der ersten Periode bereitgestellt wird und nicht während der zweiten, der dritten, der vierten und der fünften Periode bereitgestellt wird, und  
das erste Steuersignal kontinuierlich während der ersten, der zweiten, der dritten und der vierten Periode bereitgestellt wird und nicht während der fünften Periode bereitgestellt wird.

2. Organische lichtemittierende Anzeigevorrichtung nach Anspruch 1, wobei jeder Demultiplexer (170) j Transistoren (M10, M11, M12) mit ersten und zweiten Elektroden umfasst, wobei die ersten Elektroden direkt mit einer der Ausgangsleitungen (Oi) verbunden sind und die zweiten Elektroden direkt mit einer jeweiligen der j ersten Datenleitungsabschnitte (D1m-2, D1m-1, D1m) verbunden sind, und die j Transistoren (M10, M11, M12) so konfiguriert sind, dass sie als Reaktion auf j Steuersignale (CS3, CS4, CS5), die von der Schaltsteuereinheit (180) bereitgestellt werden, sequentiell eingeschaltet werden.
3. Organische lichtemittierende Anzeigevorrichtung nach einem der vorstehenden Ansprüche, wobei der Abtasttreiber (110) so konfiguriert ist, dass er den ersten Abtastzeilen (S11, S12, S13, S1 n) sequentiell erste Abtastsignale bereitstellt, den zweiten Abtastzeilen (S21, S22, S23, S2n) sequentiell zweite Abtastsignale bereitstellt und den Emissionssteuerleitungen (E1, E2, E3, En) sequentiell Emissionssteuersignale bereitstellt.
4. Organische lichtemittierende Anzeigevorrichtung nach einem der vorstehenden Ansprüche, wobei der Abtasttreiber (110) so konfiguriert ist, dass er Emissionssteuersignale bereitstellt, die mit mindestens zwei der zweiten Abtastsignale überlappen.
5. Organische lichtemittierende Anzeigevorrichtung nach einem der vorstehenden Ansprüche, wobei der Datentreiber (120) so konfiguriert ist, dass er die j Datensignale während der fünften Periode (t5) der Horizontalperiode sequentiell bereitstellt.
6. Verfahren zum Ansteuern einer organischen lichtemittierenden Anzeigevorrichtung, die ausgeführt ist, während einer ersten, zweiten, dritten, vierten und fünften Perioden (t1, t2, t3, t4, t5) umfassenden Horizontalperiode angesteuert zu werden, wobei die erste bis fünfte Periode aufeinanderfolgend sind und nicht überlappen, wobei die organische lichtemittierenden Anzeige eine in einer Matrix angeordnete Vielzahl von Pixeln (140) sowie eine Vielzahl von gemeinsamen Schaltungseinheiten (160) umfasst, wobei jede gemeinsame Schaltungseinheit (160) einen ersten Kondensator (C1) umfassend eine erste Elektrode und eine zweite Elektrode umfasst, wobei die erste Elektrode direkt mit einer ersten Datenleitung (D1m) zum Empfangen eines Datensignals verbunden ist und die zweite Elek-

trode direkt mit einer zweiten Datenleitung (D2m) verbunden ist, und die zweite Datenleitung (D2m) direkt mit den entlang einer Spalte angeordneten Pixeln (140) verbunden ist, wobei jedes Pixel (140) einen zweiten Transistor (M2) umfassend eine Gate-Elektrode, eine erste Elektrode und eine zweite Elektrode umfasst, wobei die erste Elektrode des zweiten Transistors (M2) direkt mit einer ersten Stromversorgung (ELVDD) verbunden ist, der zweite Transistor (M2) eine von der ersten Stromversorgung (ELVDD) durch eine organische lichtemittierende Diode (OLED) zu einer zweiten Stromversorgung (ELVSS) fließende Strommenge steuert, einen ersten Transistor (M1), umfassend eine Gate-Elektrode, eine erste Elektrode und eine zweite Elektrode, wobei die erste Elektrode des ersten Transistors (M1) direkt mit der Gate-Elektrode des zweiten Transistors (M2) verbunden ist und die zweite Elektrode des ersten Transistors (M1) direkt mit einer zweiten Datenleitung (D2m) der zweiten Datenleitungen (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) verbunden ist und der erste Transistor (M1) zum Einschalten konfiguriert ist, wenn ein zweites Abtastsignal einer entsprechenden zweiten Abtastzeile (S2n) von zweiten Abtastzeilen (S21, S22, S23, S2n) bereitgestellt wird, einen dritten Transistor (M3), umfassend eine Gate-Elektrode, eine erste Elektrode und eine zweite Elektrode, wobei die erste Elektrode des dritten Transistors (M3) direkt mit der Gate-Elektrode des zweiten Transistors (M2) verbunden ist und die zweite Elektrode des dritten Transistors (M3) direkt mit der zweiten Elektrode des zweiten Transistors (M2) verbunden ist und der dritte Transistor (M3) zum Einschalten konfiguriert ist, wenn ein erstes Abtastsignal einer entsprechenden ersten Abtastzeile (S1 n) von ersten Abtastzeilen (S11, S12, S13, S1n) bereitgestellt wird; und einen vierten Transistor (M4), umfassend eine Gate-Elektrode, eine erste Elektrode und eine zweite Elektrode, wobei die erste Elektrode des vierten Transistors (M4) direkt mit der zweiten Elektrode des zweiten Transistors (M2) verbunden ist und die zweite Elektrode des vierten Transistors (M4) direkt mit der Anodenelektrode der organischen lichtemittierenden Diode (OLED) verbunden ist, wobei der vierte Transistor (M4) zum Ausschalten konfiguriert ist, wenn ein Emissionssteuersignal einer entsprechenden Emissionssteuerleitung (En) von Emissionssteuerleitungen (E1, E2, E3, En) bereitgestellt wird, wobei die Kathodenelektrode der organischen lichtemittierenden Diode (OLED) direkt mit der zweiten Stromversorgung (ELVSS) verbunden ist,

wobei jeder der gemeinsamen Schaltungen ferner einen ersten gemeinsamen Transistor (CM1) mit ersten und zweiten Elektroden umfasst, der direkt zwischen die eine (D1m) der ersten Datenleitungen (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m) und eine eine Referenzspannung (Vref) bereitstellende Spannungsquelle geschaltet ist, wobei der erste gemeinsame Transistor (CM1) zum Einschalten als Reaktion auf ein erstes Steuersignal (CS1) von der Schaltsteuereinheit (180) konfiguriert ist; und

einen zweiten gemeinsamen Transistor (CM2) mit ersten und zweiten Elektroden, der direkt zwischen die eine (D2m) der zweiten Datenleitungen (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) und eine eine Anfangsspannung (Vint) bereitstellende Spannungsquelle geschaltet ist, wobei der zweite gemeinsame Transistor (CM2) zum Einschalten als Reaktion auf ein zweites Steuersignal (CS2) von der Schaltsteuereinheit (180) konfiguriert ist, das Verfahren umfassend:

Zuführen der Referenzspannung (Vref) zur ersten Datenleitung (D1m) während der ersten bis vierten Periode (t1, t2, t3, t4) sowie Zuführen der Anfangsspannung (Vint) zur zweiten Datenleitung (V2m) während der ersten Periode (t1);

elektrisches Verbinden der zweiten Datenleitung (D2m) mit der Gate-Elektrode des zweiten Transistors (M2) während des Zuführens der Referenzspannung (Vref) zur ersten Datenleitung (D1m) während der zweiten Periode (t2);

Erhöhen der Spannung der zweiten Datenleitung (D2m) auf eine Spannung, die durch Abziehen eines Absolutwertes einer Schwellenspannung des zweiten Transistor (M2) von der Spannung der ersten Stromversorgung (ELVDD) erhalten wird,

durch elektrisches Verbinden des zweiten Transistors (M2) in einer als Diode geschalteten Ausführung während des Zuführens der Referenzspannung (Vref) zur ersten Datenleitung (D1m) während der dritten Periode (t3); und Variieren der Spannung der Gate-Elektrode des zweiten Transistors (M2) durch Bereitstellen von Datensignalen an die erste Datenleitung (D1m) während der fünften Periode (t5), wobei

das erste Abtastsignal nicht während der ersten, der zweiten, der vierten und der fünften Periode bereitgestellt wird und kontinuierlich während der dritten Periode bereitgestellt wird,

das zweite Abtastsignal nicht während der ersten Periode bereitgestellt wird und kontinuierlich während der zweiten, der dritten, der vierten und der fünften Periode bereitgestellt wird,

das Emissionssteuersignal nicht während der ersten, der zweiten, der dritten, der vierten und der fünften Periode bereitgestellt wird,

das zweite Steuersignal kontinuierlich während der ersten Periode bereitgestellt wird und nicht während der zweiten, der dritten, der vierten und der fünften Periode bereitgestellt wird, und

das erste Steuersignal kontinuierlich während der ersten, der zweiten, der dritten und der vierten Periode bereitgestellt wird und nicht während der fünften Periode bereitgestellt wird.

7. Verfahren zum Ansteuern einer organischen lichtemittierenden Anzeigevorrichtung nach Anspruch 6, wobei die Referenzspannung ( $V_{ref}$ ) niedriger ist als eine Spannung eines schwarzen Datensignals zum Ausdrücken eines Schwarz-Grau-Pegels, und/oder wobei die Anfangsspannung ( $V_{int}$ ) niedriger ist als die Spannung, die durch das Abziehen des Absolutwertes der Schwellenspannung des zweiten Transistors (M2) von der Spannung der ersten Stromversorgung (ELVDD) erhalten wird.

## Revendications

1. Dispositif d'affichage électroluminescent organique adapté pour être piloté au cours d'une période horizontale comprenant des première, deuxième, troisième, quatrième, et cinquième périodes ( $t_1$ ,  $t_2$ ,  $t_3$ ,  $t_4$ ,  $t_5$ ), la première à la cinquième période étant consécutives et non chevauchantes, le dispositif électroluminescent organique comprenant :

une pluralité de lignes horizontales, s'étendant le long d'une direction horizontale du dispositif d'affichage électroluminescent organique, où chacune des lignes horizontales du dispositif d'affichage électroluminescent organique comprend, agencées en parallèle l'une à côté de l'autre, une première ligne de balayage ( $S_{11}$ ,  $S_{12}$ ,  $S_{13}$ ,  $S_{1n}$ ), une seconde ligne de balayage ( $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{2n}$ ) et une ligne de commande d'émission ( $E_1$ ,  $E_2$ ,  $E_3$ ,  $E_n$ ) ;

une pluralité de lignes de données s'étendant le long d'une direction verticale du dispositif d'affichage électroluminescent organique, chacune des lignes de données comprenant une première section de ligne de données ( $D_{11}$ ,  $D_{12}$ ,  $D_{13}$ ,  $D_{14}$ ,  $D_{15}$ ,  $D_{16}$ ,  $D_{1m-2}$ ,  $D_{1m-1}$ ,  $D_{1m}$ ) et une seconde section de ligne de données ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ ), la seconde section de ligne de données ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ ) croisant les lignes de balayage ( $S_{11}$ ,  $S_{12}$ ,  $S_{13}$ ,  $S_{1n}$ ,  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{2n}$ ) ; un pilote de balayage (110) adapté pour piloter les première et seconde lignes de balayage ( $S_{11}$ ,  $S_{12}$ ,  $S_{13}$ ,  $S_{1n}$ ,  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{2n}$ ) et les lignes de commande d'émission ( $E_1$ ,  $E_2$ ,  $E_3$ ,  $E_n$ ) ;

un pilote de données (120) adapté pour fournir séquentiellement  $j$  signaux de données à chacune d'une pluralité de lignes de sortie ( $O_1$ ,  $O_2$ ,  $O_i$ ) du pilote de données (120) dans chaque période horizontale ;

au moins un démultiplexeur (170) adapté pour transmettre les  $j$  signaux de données à  $j$  premières sections de ligne de données ( $D_{11}$ ,  $D_{12}$ ,  $D_{13}$ ,  $D_{14}$ ,  $D_{15}$ ,  $D_{16}$ ,  $D_{1m-2}$ ,  $D_{1m-1}$ ,  $D_{1m}$ ), le démultiplexeur étant connecté directement à la pluralité de lignes de sortie ( $O_1$ ,  $O_2$ ,  $O_i$ ) ;

une pluralité de pixels (140) au niveau de régions de croisement des lignes de balayage ( $S_{11}$ ,  $S_{12}$ ,  $S_{13}$ ,  $S_{1n}$ ,  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{2n}$ ) et de secondes sections de ligne de données ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ ) ;

au moins une unité de circuit commune (160) adaptée pour commander des tensions des secondes sections de ligne de données ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ ) connectées aux pixels (140) en utilisant une tension de référence ( $V_{ref}$ ), une tension initiale ( $V_{int}$ ) et les signaux de données, l'unité de circuit commune (160) étant connectée directement à une des premières sections de ligne de données ( $D_{11}$ ,  $D_{12}$ ,  $D_{13}$ ,  $D_{14}$ ,  $D_{15}$ ,  $D_{16}$ ,  $D_{1m-2}$ ,  $D_{1m-1}$ ,  $D_{1m}$ ) et à une section correspondante des secondes sections de ligne de données ( $D_{21}$ ,  $D_{22}$ ,  $D_{23}$ ,  $D_{24}$ ,  $D_{25}$ ,  $D_{26}$ ,  $D_{2m-2}$ ,  $D_{2m-1}$ ,  $D_{2m}$ ) ; et

une unité de commande de commutation (180) adaptée pour commander le au moins un démultiplexeur (170) et la au moins une unité de circuit commune (160), dans lequel chacun des pixels (140) comprend :

une diode électroluminescente organique (OLED) ayant une électrode de cathode connectée directement à une seconde alimentation (ELVSS) ;

un deuxième transistor (M2) comprenant une électrode de grille, une première électrode et une seconde électrode, la première électrode du deuxième transistor (M2) étant connectée directement à une première alimentation (ELVDD) et le deuxième transistor (M2) étant configuré pour commander une quantité de courant fournie à la diode électroluminescente organique (OLED) ;

un premier transistor (M1) comprenant une électrode de grille, une première électrode et une seconde électrode, la première électrode du premier transistor (M1) étant connectée directement à l'électrode de grille du deuxième transistor (M2) et la seconde électrode du premier transistor (M1) étant connectée directement à une seconde section de ligne de données ( $D_{2m}$ ) et le premier transistor (M1) étant configuré pour être débloqué lorsque les seconds signaux de balayage sont fournis à une seconde ligne de balayage ( $S_{2n}$ ) connectée directement à l'électrode de grille du premier transistor (M1) ;

un troisième transistor (M3) comprenant une électrode de grille, une première électrode et une seconde

électrode, la première électrode du troisième transistor (M3) étant connectée directement à l'électrode de grille du deuxième transistor (M2) et la seconde électrode du troisième transistor (M3) étant connectée directement à la seconde électrode du deuxième transistor (M2) et le troisième transistor (M3) étant configuré pour être débloqué afin de connecter en diode le deuxième transistor (M2) lorsque des premiers signaux de balayage sont fournis à une première ligne de balayage (S1n) connectée directement à l'électrode de grille du troisième transistor (M3) ; et

un quatrième transistor (M4) comprenant une électrode de grille, une première électrode et une seconde électrode, la première électrode du quatrième transistor (M4) étant connectée directement à la seconde électrode du deuxième transistor (M2) et la seconde électrode du quatrième transistor (M4) étant connectée directement à l'électrode d'anode de la diode électroluminescente organique (OLED) et le quatrième transistor (M4) étant configuré pour être bloqué lorsque les signaux de commande d'émission sont fournis à une ligne de commande d'émission (En) connectée directement à l'électrode de grille du quatrième transistor (M4), et

dans lequel  
chacune des unités de circuit communes (160) comprend :

un premier condensateur (C1) connecté directement à une première section de ligne de données (D1m) des premières sections de ligne de données (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m) par une première électrode et à une seconde section de ligne de données (D2m) des secondes sections de ligne de données (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) par une seconde électrode ;

un premier transistor commun (CM1) ayant des première et seconde électrodes connectées directement entre ladite une (D1m) des premières sections de ligne de données (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m) et une source de tension fournissant la tension de référence (Vref), le premier transistor commun (CM1) étant configuré pour être débloqué en réponse à un premier signal de commande (CS1) en provenance de l'unité de commande de commutation (180) ; et

un second transistor commun (CM2) ayant des première et seconde électrodes connectées directement entre ladite une (D2m) des secondes sections de ligne de données (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) et une source de tension fournissant la tension initiale (Vint), le second transistor commun (CM2) étant configuré pour être débloqué en réponse à un second signal de commande (CS2) en provenance de l'unité de commande de commutation (180), dans lequel

le dispositif d'affichage électroluminescent organique est configuré pour être piloté de sorte que

le premier signal de balayage ne soit pas fourni au cours de la première, la deuxième, la quatrième et la cinquième période et soit fourni de façon continue au cours de la troisième période,

le second signal de balayage ne soit pas fourni au cours de la première période et soit fourni de façon continue au cours de la deuxième, la troisième, la quatrième et la cinquième période,

le signal de commande d'émission ne soit pas fourni au cours de la première, la deuxième, la troisième, la quatrième et la cinquième période,

le second signal de commande soit fourni de façon continue au cours de la première période et ne soit pas fourni au cours de la deuxième, la troisième, la quatrième et la cinquième période, et

le premier signal de commande soit fourni de façon continue au cours de la première, la deuxième, la troisième et la quatrième période et ne soit pas fourni au cours de la cinquième période.

2. Dispositif d'affichage électroluminescent organique selon la revendication 1, dans lequel chaque démultiplexeur (170) comprend j transistors (M10, M11, M12) ayant des première et seconde électrodes, les premières électrodes étant connectées directement à une des lignes de sortie (Oi) et les secondes électrodes étant connectées directement à une section respective des j premières sections de ligne de données (D1m-2, D1m-1, D1m), et les j transistors (M10, M11, M12) étant configurés pour être débloqués séquentiellement en réponse à j signaux de commande (CS3, CS4, CS5) fournis depuis l'unité de commande de commutation (180).

3. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel le pilote de balayage (110) est configuré pour fournir séquentiellement des premiers signaux de balayage aux premières lignes de balayage (S11, S12, S13, S1n), fournir séquentiellement des seconds signaux de balayage aux secondes lignes de balayage (S21, S22, S23, S2n), et fournir séquentiellement des signaux de commande d'émission aux lignes de commande d'émission (E1, E2, E3, En).

4. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel le pilote de balayage (110) est configuré pour fournir des signaux de commande d'émission se chevauchant avec au moins

deux des seconds signaux de balayage.

5. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel le pilote de données (120) est configuré pour fournir séquentiellement les j signaux de données au cours de la cinquième période (t5) de la période horizontale.

6. Procédé de pilotage d'un dispositif d'affichage électroluminescent organique adapté pour être piloté au cours d'une période horizontale comprenant des première, deuxième, troisième, quatrième, et cinquième périodes (t1, t2, t3, t4, t5), la première à la cinquième période étant consécutives et non chevauchantes, dans lequel l'affichage électroluminescent organique comprend une pluralité de pixels (140) agencés dans une matrice et une pluralité d'unités de circuit communes (160), chaque unité de circuit commune (160) comprenant un premier condensateur (C1) comprenant une première électrode et une seconde électrode, la première électrode étant connectée directement à une première ligne de données (D1m) pour recevoir un signal de données et la seconde électrode étant connectée directement à une seconde ligne de données (D2m), et la seconde ligne de données (D2m) étant connectée directement aux pixels (140) agencés le long d'une colonne, chaque pixel (140) comprenant un deuxième transistor (M2) comprenant une électrode de grille, une première électrode et une seconde électrode, la première électrode du deuxième transistor (M2) étant connectée directement à une première alimentation (ELVDD), le deuxième transistor (M2) commandant une quantité de courant circulant vers une seconde alimentation (ELVSS) depuis la première alimentation (ELVDD) par l'intermédiaire d'une diode électroluminescente organique (OLED), un premier transistor (M1) comprenant une électrode de grille, une première électrode et une seconde électrode, la première électrode du premier transistor (M1) étant connectée directement à l'électrode de grille du deuxième transistor (M2) et la seconde électrode du premier transistor (M1) étant connectée directement à une seconde ligne de données (D2m) des secondes lignes de données (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) et le premier transistor (M1) étant configuré pour être débloqué lorsqu'un second signal de balayage est fourni à une seconde ligne de balayage correspondante (S2n) de secondes lignes de balayage (S21, S22, S23, S2n), un troisième transistor (M3) comprenant une électrode de grille, une première électrode et une seconde électrode, la première électrode du troisième transistor (M3) étant connectée directement à l'électrode de grille du deuxième transistor (M2) et la seconde électrode du troisième transistor (M3) étant connectée directement à la seconde électrode du deuxième transistor (M2) et le troisième transistor (M3) étant configuré pour être débloqué lorsqu'un premier signal de balayage est fourni à une première ligne de balayage correspondante (S1n) de premières lignes de balayage (S11, S12, S13, S1n) ; et un quatrième transistor (M4) comprenant une électrode de grille, une première électrode et une seconde électrode, la première électrode du quatrième transistor (M4) étant connectée directement à la seconde électrode du deuxième transistor (M2) et la seconde électrode du quatrième transistor (M4) étant connectée directement à l'électrode d'anode de la diode électroluminescente organique (OLED), le quatrième transistor (M4) étant configuré pour être bloqué lorsqu'un signal de commande d'émission est fourni à une ligne de commande d'émission correspondante (En) de lignes de commande d'émission (E1, E2, E3, En), l'électrode de cathode de la diode électroluminescente organique (OLED) étant connectée directement à la seconde alimentation (ELVSS), chacun des circuits communs (160) comprenant en outre un premier transistor commun (CM1) ayant des première et seconde électrodes connectées directement entre ladite une (D1m) des premières lignes de données (D11, D12, D13, D14, D15, D16, D1m-2, D1m-1, D1m) et une source de tension fournissant une tension de référence (Vref), le premier transistor commun (CM1) étant configuré pour être débloqué en réponse à un premier signal de commande (CS1) en provenance de l'unité de commande de commutation (180) ; et un second transistor commun (CM2) ayant des première et seconde électrodes connectées directement entre ladite une (D2m) des secondes lignes de données (D21, D22, D23, D24, D25, D26, D2m-2, D2m-1, D2m) et une source de tension fournissant une tension initiale (Vint), le second transistor commun (CM2) étant configuré pour être débloqué en réponse à un second signal de commande (CS2) en provenance de l'unité de commande de commutation (180), le procédé comprenant :

la fourniture de la tension de référence (Vref) à la première ligne de données (D1m) au cours des première à quatrième périodes (t1, t2, t3, t4) et la fourniture de la tension initiale (Vint) à la seconde ligne de données (D2m) au cours de la première période (t1) ;

le couplage électrique de la seconde ligne de données (D2m) à l'électrode de grille du deuxième transistor (M2) pendant la fourniture de la tension de référence (Vref) à la première ligne de données (D1m) au cours de la deuxième période (t2) ;

l'augmentation de la tension de la seconde ligne de données (D2m) à une tension obtenue en soustrayant une valeur absolue d'une tension de seuil du deuxième transistor (M2) de la tension de la première alimentation (ELVDD) en couplant électriquement le deuxième transistor (M2) dans une configuration connectée en diode pendant la fourniture de la tension de référence (Vref) à la première ligne de données (D1m) au cours de la



troisième période ( $t_3$ ) ; et

la variation de la tension de l'électrode de grille du deuxième transistor (M2) en fournissant des signaux de données à la première ligne de données (D1m) au cours de la cinquième période ( $t_5$ ), où

le premier signal de balayage n'est pas fourni au cours de la première, la deuxième, la quatrième et la cinquième

période et est fourni de façon continue au cours de la troisième période,

le second signal de balayage n'est pas fourni au cours de la première période et est fourni de façon continue au cours de la deuxième, la troisième, la quatrième et la cinquième période,

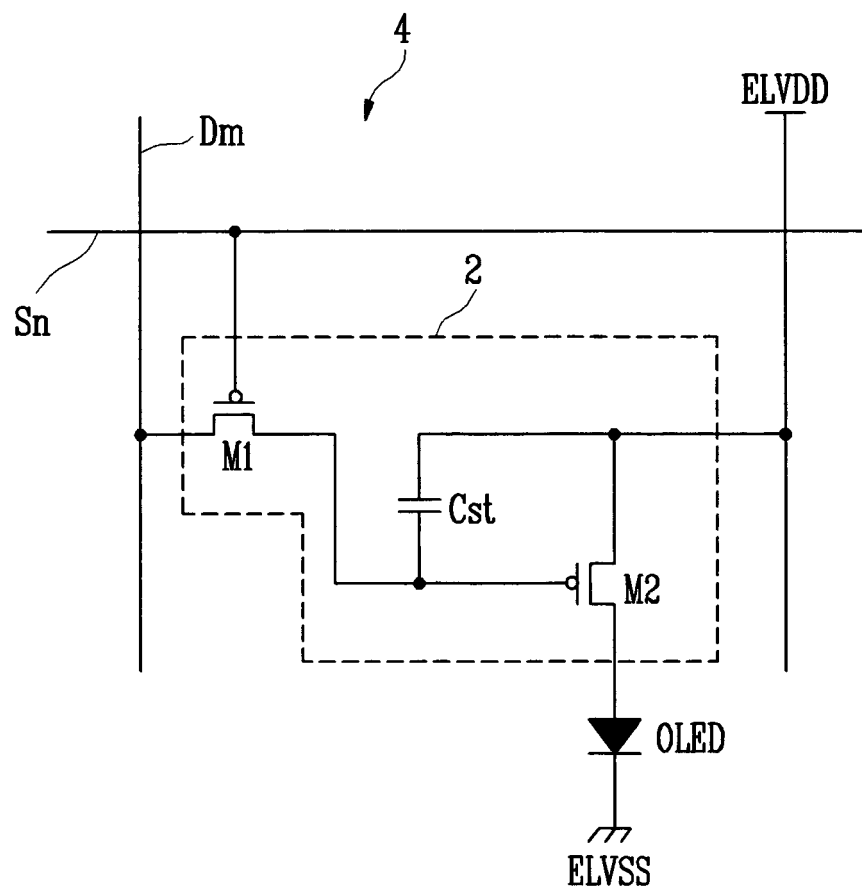
le signal de commande d'émission n'est pas fourni au cours de la première, la deuxième, la troisième, la quatrième et la cinquième période,

le second signal de commande est fourni de façon continue au cours de la première période et n'est pas fourni au cours de la deuxième, la troisième, la quatrième et la cinquième période, et

le premier signal de commande est fourni de façon continue au cours de la première, la deuxième, la troisième et la quatrième période et n'est pas fourni au cours de la cinquième période.

7. Procédé de pilotage d'un dispositif d'affichage électroluminescent organique selon la revendication 6, dans lequel la tension de référence ( $V_{ref}$ ) est inférieure à une tension d'un signal de données de noir pour exprimer un niveau de gris noir, et/ou dans lequel la tension initiale ( $V_{int}$ ) est inférieure à la tension obtenue en soustrayant la valeur absolue de la tension de seuil du deuxième transistor (M2) de la tension de la première alimentation (ELVDD).

FIG. 1  
(Related Art)



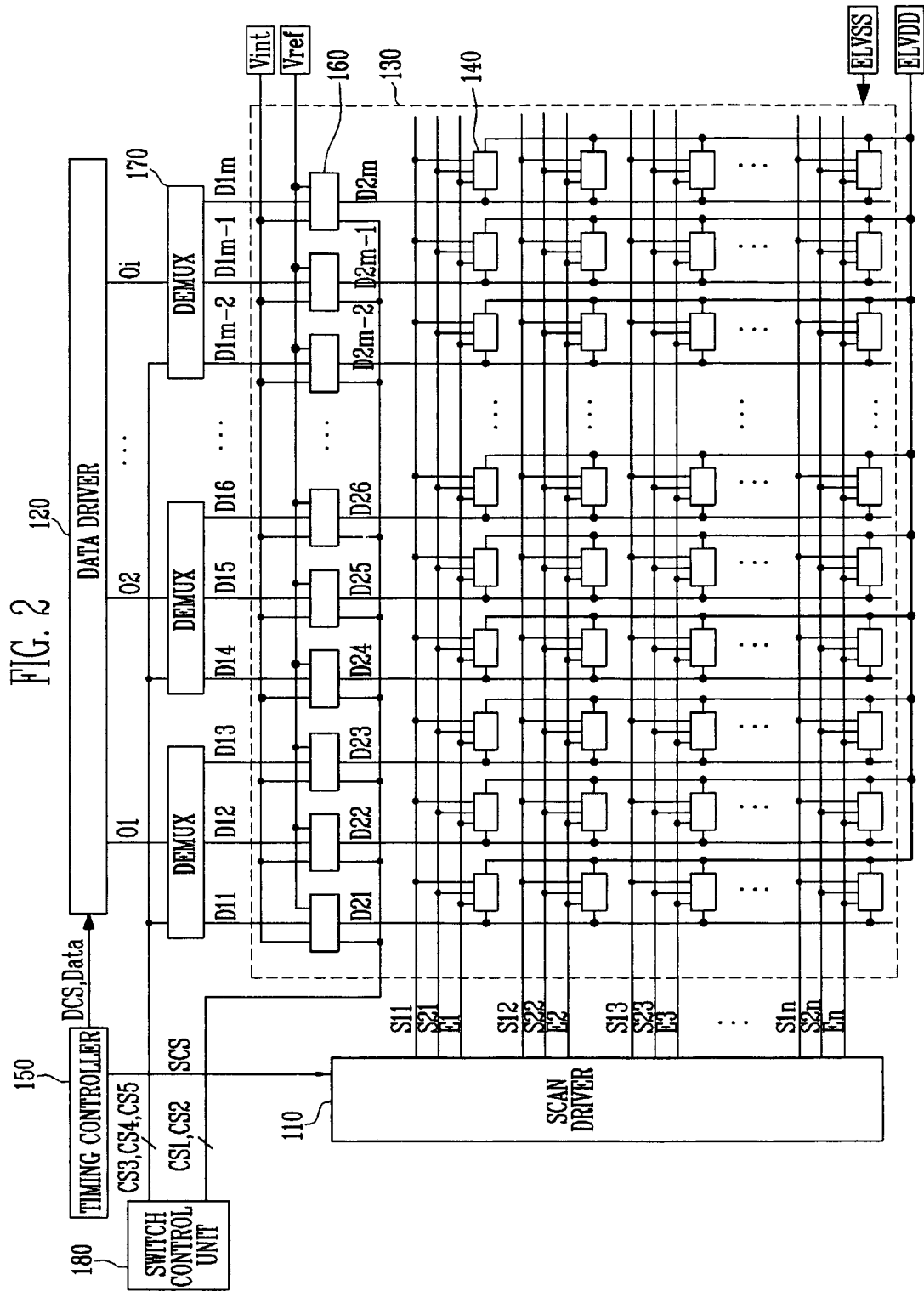


FIG. 3

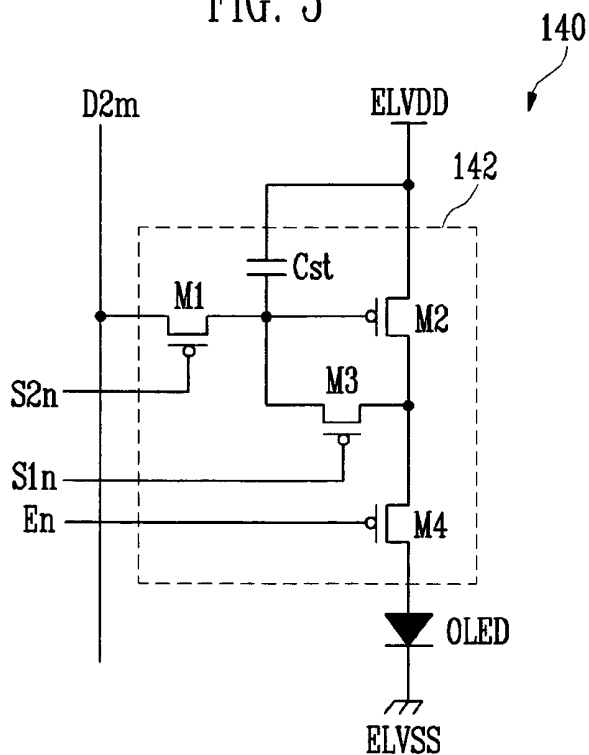


FIG. 4

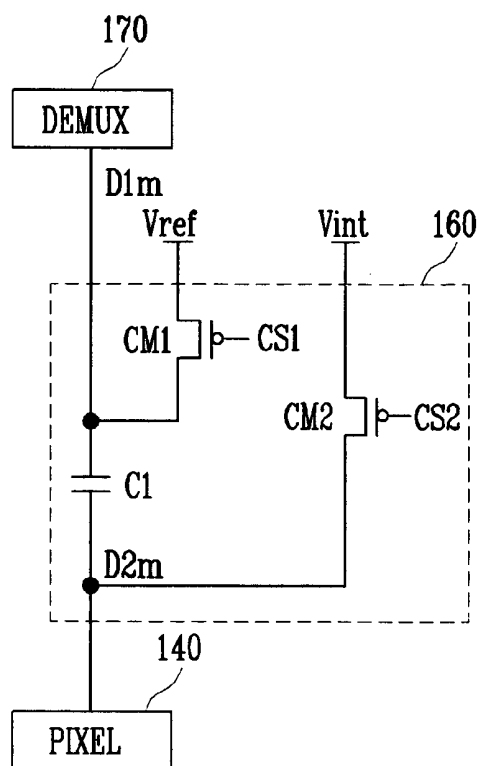


FIG. 5

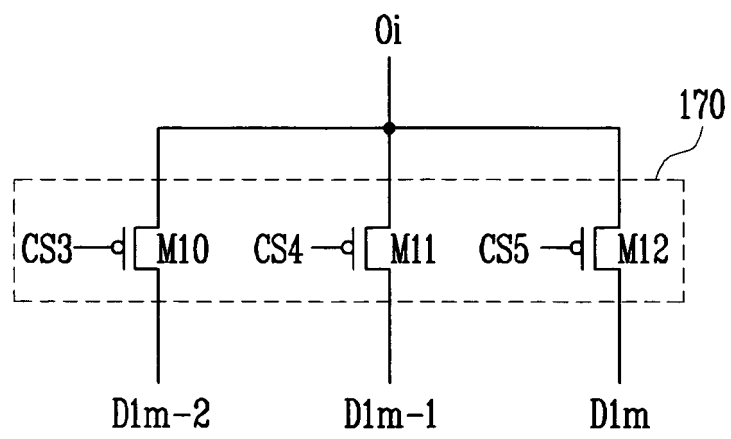


FIG. 6

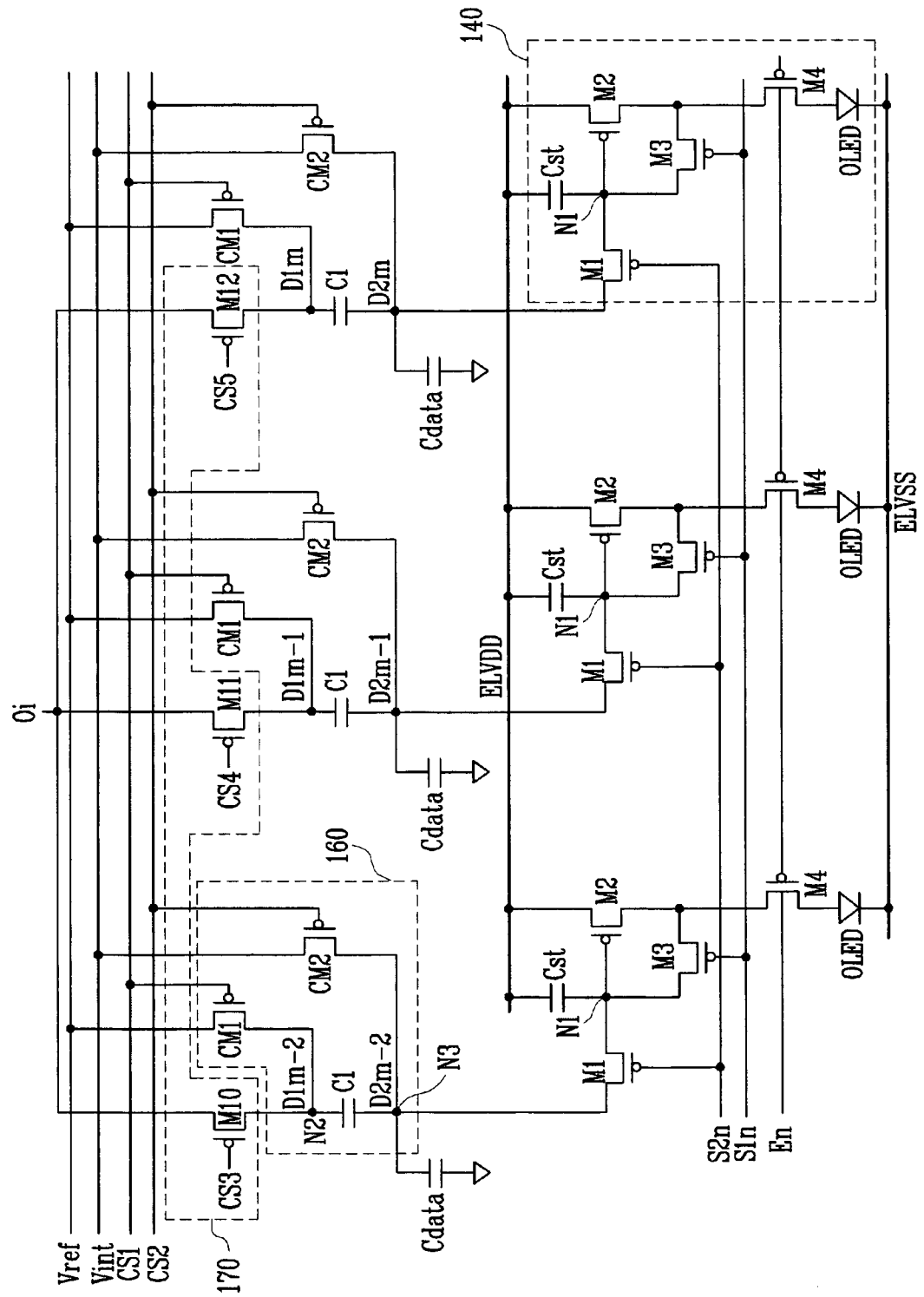


FIG. 7

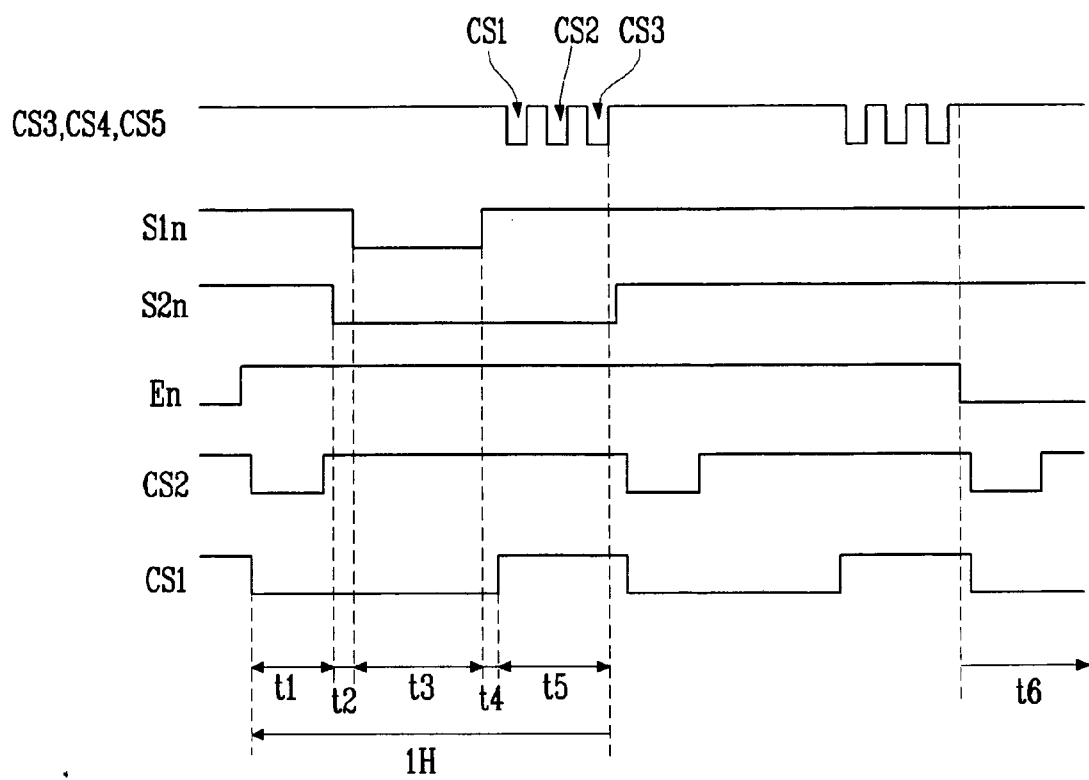


FIG. 8A

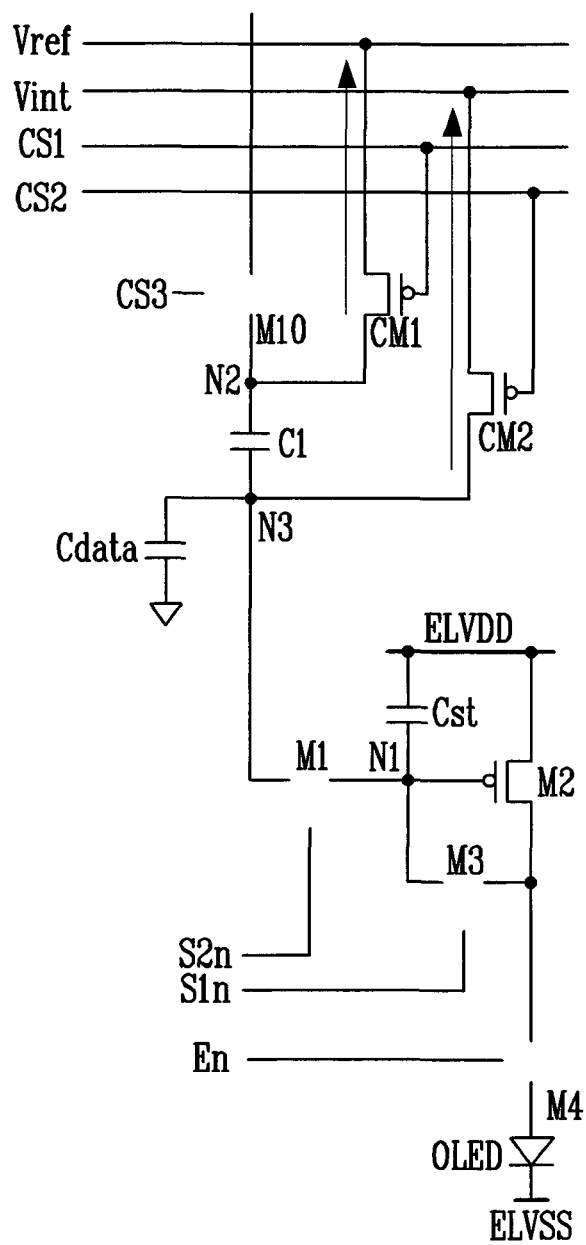




FIG. 8B

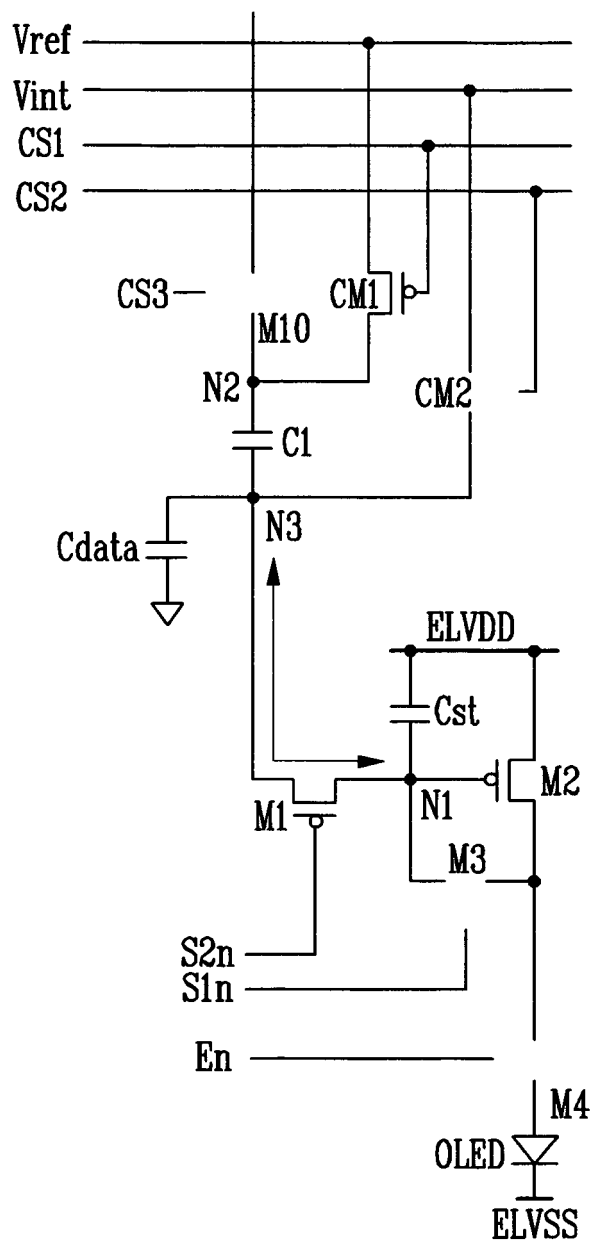


FIG. 8C

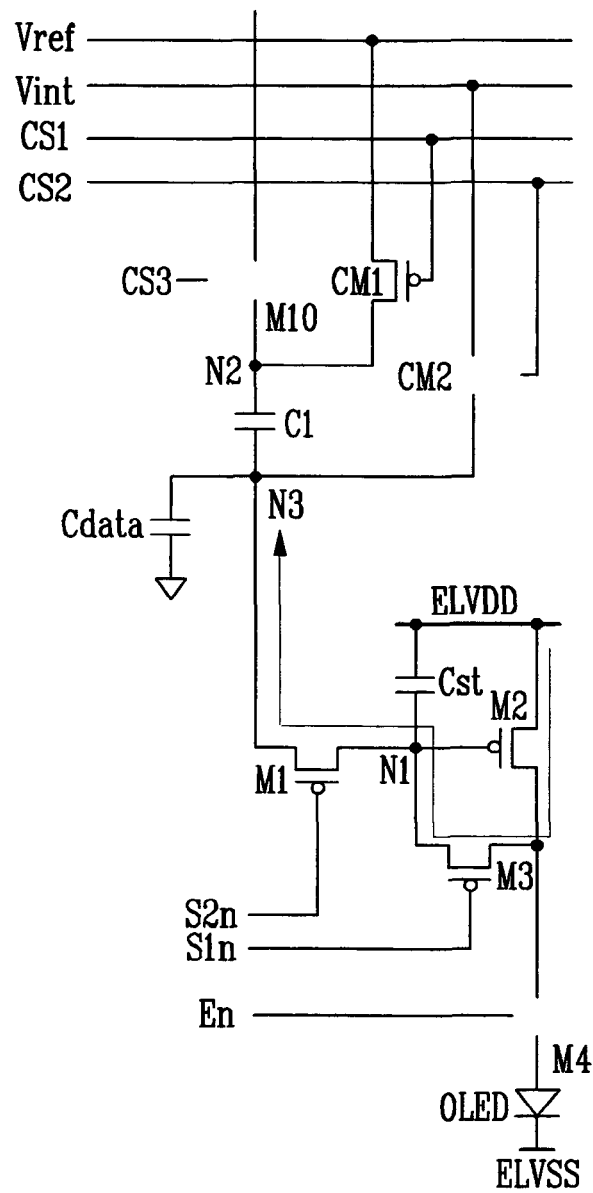


FIG. 8D

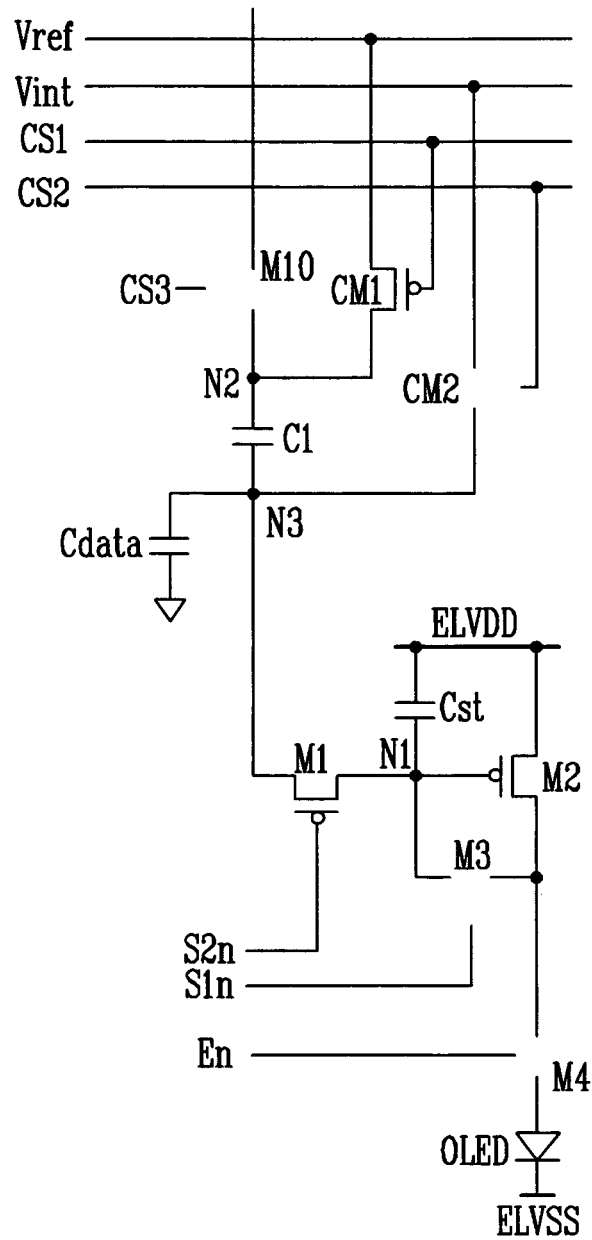
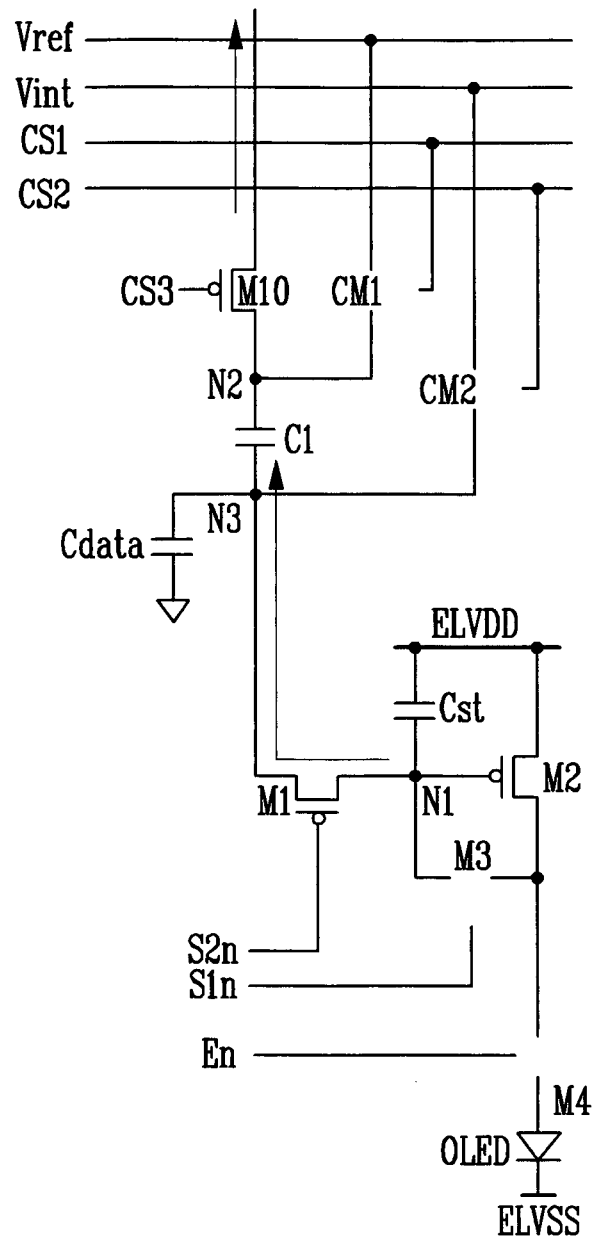


FIG. 8E



**REFERENCES CITED IN THE DESCRIPTION**

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|                |                                                                                                                        |         |            |
|----------------|------------------------------------------------------------------------------------------------------------------------|---------|------------|
| 专利名称(译)        | 有机发光显示装置及其驱动方法                                                                                                         |         |            |
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| [标]发明人         | JEONG JIN TAE                                                                                                          |         |            |
| 发明人            | JEONG, JIN-TAE                                                                                                         |         |            |
| IPC分类号         | G09G3/32                                                                                                               |         |            |
| CPC分类号         | G09G3/3233 G09G3/3291 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2310/0262 G09G2310/0297 G09G2320/0223 G09G2320/043 |         |            |
| 优先权            | 1020090082451 2009-09-02 KR                                                                                            |         |            |
| 其他公开文献         | EP2299430A1                                                                                                            |         |            |
| 外部链接           | <a href="#">Espacenet</a>                                                                                              |         |            |

#### 摘要(译)

一种有机发光显示装置，包括：扫描驱动器（110），用于驱动扫描线（S11，...，S1n，S21，...，S2n）和发射控制线（E1，...，En）；数据驱动器（120），用于在每个水平周期中向多个输出线（O1，...，Oi）中的每一个顺序提供j个数据信号；至少一个多路分解器（170），用于将j个数据信号发送到第一数据线（D11，...，D1m），所述至少一个多路分配器耦合到输出线（O1，...，Oi）；在扫描线（S11，...，S1n，S21，...，S2n）的交叉区域处的多个像素（140）和在与扫描线交叉的方向上延伸的第二数据线（D21，...，D2m）扫描线（S11，...，S1n，S21，...，S2n）；和至少一个共同的电路单元（160），用于通过使用参考电压（Vref）和初始电压（Vint）以及数据信号来控制耦合到像素（140）的第二数据线（D21，...，D2m）的电压，至少一个公共电路单元（160）耦合在第一数据线（D11，...，D1m）和第二数据线（D21，...，D2m）之间。公共电路（160）包括将第一数据线（D1m）耦合到第二数据线（D2m）的电容器（C1）。在阈值电压检测时段中，像素的驱动TFT（M2）是二极管连接（M3），并且公共电路电容器（C1）存储与驱动TFT（M2）的阈值电压对应的电压以执行后续写入中的阈值电压补偿期。

Equation 1

$$V_{W1} = V_{W3} = ELVDD - |V_{th}(M2)|$$