(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 2 093 749 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
28.10.2015 Bulletin 2015/44

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **08016568.1**

(22) Date of filing: **19.09.2008**

(54) **Organic light emitting diode display and method of driving the same**

Organische lichtemittierende Diodenanzeige und Ansteuerungsverfahren dafür

Affichage à diode électroluminescente organique et son procédé de commande

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR

(30) Priority: **22.02.2008 KR 20080016503**

(43) Date of publication of application:
26.08.2009 Bulletin 2009/35

(73) Proprietor: **LG Display Co., Ltd.**
Seoul 150-721 (KR)

(72) Inventor: **Nam, Woojin**
Seongnam-si
Gyeonggi-do (KR)

(74) Representative: **Ter Meer Steinmeister & Partner Patentanwälte mbB**
Nymphenburger Straße 4
80335 München (DE)

(56) References cited:
WO-A1-2005/015530
WO-A1-2006/053424
WO-A1-2007/037269
WO-A1-2008/018629
US-A1- 2005 212 445

EP 2 093 749 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates to an organic light emitting diode display, and more particularly to an organic light emitting diode display and a method of driving the same capable of increasing the display quality by preventing a driving current from becoming degraded by the degradation of a drive thin film transistor (TFT) depending on driving time.

DISCUSSION OF THE RELATED ART

[0002] Recently, various kinds of flat panel display devices with reduced weight and size have been developed as a replacement of cathode ray tubes. Examples of the flat panel display devices include liquid crystal displays (LCD), field emission displays (FED), plasma display panels (PDP), and electroluminescence devices. Because the structure and manufacturing process of plasma display panels are simple, the plasma display panels have been considered for large-sized display devices that are relatively light and thin. However, the emitting efficiency and luminance of the plasma display panel are low while its power consumption is high. As an alternative, thin film transistor (TFT) LCD using TFTs as a switching device is widely used. However, the TFT-LCD is a non-emitting device. Therefore, the TFT-LCD has a narrow viewing angle and a low response speed. The electroluminescence device, on the other hand, is a self-emitting device. The electroluminescence device may be classified into an inorganic light emitting diode display category and an organic light emitting diode (OLED) display category depending on the material of an emitting layer. Because the OLED display includes a self-emitting device, the OLED display has high response speed, high emitting efficiency, strong luminance, and wide viewing angle.

[0003] An OLED display includes an organic light emitting diode. As shown in FIG. 1, the organic light emitting diode includes organic compound layers 78a, 78b, 78c, 78d, and 78e between an anode electrode and a cathode electrode. The organic compound layers include an electron injection layer 78a, an electron transport layer 78b, an emitting layer 78c, a hole transport layer 78d, and a hole injection layer 78e. When a driving voltage is applied to the anode electrode and the cathode electrode, holes passing through the hole transport layer 78d and electrons passing through the electron transport layer 78b move to the emitting layer 78c to form an exciton. Hence, the emitting layer 78c generates visible light.

[0004] The OLED display is arranged with pixels including the organic light emitting diode in a matrix format and controls brightness of the pixels selected by a scan pulse depending on a gray level of digital video data. The OLED display may be classified into a passive matrix type OLED display and an active matrix type OLED display using a thin film transistor as a switching device. In particular, the active matrix type OLED display selectively turns on the thin film transistor used as the switching device to select the pixel and maintains an emission of the pixel using a voltage hold by a storage capacitor.

[0005] FIG. 2 is an equivalent circuit diagram showing one pixel in a related art active matrix type OLED display. As shown in FIG. 2, an pixel of the related art active matrix type OLED display includes an organic light emitting diode OLED, data lines DL and gate lines GL that cross each other, a switching thin film transistor SW, a drive thin film transistor DR, and a storage capacitor Cst. The switch TFT SW and the drive TFT DR may be an N-type metal-oxide semiconductor field effect transistor (MOSFET).

[0006] The switching TFT SW is turned on in response to a scan pulse received through the gate line GL, and thus a current path between a source electrode and a drain electrode of the switching TFT SW is turned on. During on-time of the switching TFT SW, a data voltage received from the data line DL is applied to a gate electrode of the drive TFT DR and the storage capacitor Cst via the source electrode and the drain electrode of the switching TFT SW. The drive TFT DR controls a current flowing in the organic light emitting diode OLED depending on a voltage difference Vgs between the gate electrode and a source electrode of the drive TFT DR. The storage capacitor Cst stores the data voltage applied to an electrode at one end of the storage capacitor Cst to keep a voltage applied to the gate electrode of the drive TFT DR constant during a frame period.

[0007] The organic light emitting diode OLED may have a structure shown in FIG. 1. The organic light emitting diode OLED is connected between the source electrode of the drive TFT DR and a low potential driving voltage source VSS. A brightness of the pixel shown in FIG. 2 is proportional to the current flowing in the organic light emitting diode OLED as indicated in the following Equation 1:

$$Vgs = Vg - Vs$$

$$Vg = Vdata, \quad Vs = Vss$$

$$Ioled = \frac{\beta}{2}(Vgs-Vth)^2 = \frac{\beta}{2}(Vdata-Vss-Vth)^2$$

[0008] In the above Equation 1, Vgs indicates a voltage difference between a gate voltage Vg and a source voltage Vs of the drive TFT DR, a data voltage Vdata, a low potential driving voltage Vss, a driving current Ioled, a threshold voltage of the TFT DR Vth, and a constant β determined by mobility and parasitic capacitance of the drive TFT DR.

[0009] As indicated in the above Equation 1, the driving current Ioled of the organic light emitting diode OLED is greatly affected by the threshold voltage Vth of the drive TFT DR. When the gate voltages with the same polarity are applied to the gate electrodes of the drive TFT DR for a long time, a gate-bias stress and the threshold voltage Vth of the drive TFT DR increases. Hence, operation characteristics of the drive TFT DR change over time. The changes in the operation characteristics of the drive TFT DR can be seen from an experimental result shown in FIG. 3.

[0010] FIG. 3 is a graph showing changes in operation characteristics of hydrogenated amorphous silicon TFT sample (A-Si:H TFT) when a positive gate-bias stress is applied to the hydrogenated amorphous silicon TFT sample (A-Si:H TFT) whose channel width to channel length ratio W/L is 120 μm/6 μm. In FIG. 3, the transverse axis indicates a gate voltage of the A-Si:H TFT, and the vertical axis indicates a current between a source electrode and a drain electrode of the A-Si:H TFT.

[0011] More specifically, FIG. 3 shows a threshold voltage of the A-Si:H TFT depending on voltage application time and a movement of the transmission characteristic curve when a voltage of 30 V is applied to a gate electrode of the A-Si:H TFT. As can be seen from FIG. 3, as application time of a positive voltage to the gate electrode of the A-Si:H TFT becomes longer, the transmission characteristic curve of the A-Si:H TFT moves to the right of the graph shown, and the threshold voltage of the A-Si:H TFT rises from a voltage Vth1 to a voltage Vth4.

[0012] A rise level of the threshold voltage of the A-Si:H TFT depending on the voltage application time changes in each pixel. For example, a rise width of a threshold voltage of a drive TFT in a first pixel to which a first data voltage is applied for a long time is smaller than a rise width of a threshold voltage of a drive TFT in a second pixel to which a second data voltage larger than the first data voltage is applied for a long time. In this case, the amount of driving current flowing in an organic light emitting diode generated by the same data voltage in the first pixel is more than that of the second pixel. Hence, the display quality is deteriorated.

[0013] A method in which a rise in the threshold voltage of the drive TFT is suppressed by applying a negative gate-bias stress to the drive TFT was recently proposed to prevent the deterioration of the display quality. However, it is difficult to completely compensate for a difference between driving currents of the pixels by only applying a negative voltage as pixel data to suppress the rise in the threshold voltage of the drive TFT. As indicated in the above Equation 1, the driving current Ioled flowing in the organic light emitting diode is affected by a potential value of a Vss supply line for supplying the low potential driving voltage Vss and the mobility of the drive TFT DR determining the constant β as well as the threshold voltage of the drive TFT DR. When the driving current flows in each pixel of an OLED display panel, the low potential driving voltage Vss changes depending on a location of the pixel because of a resistance of the Vss supply line. The mobility of the drive TFT DR is also degraded depending on the driving time. Therefore, a difference between the threshold voltages of the drive TFTs DR, a potential difference between the Vss supply lines, and a difference between the mobilities of the drive TFTs DR have to be compensated so that the display quality is improved by reducing a deviation of the driving current of each pixel.

[0014] WO 2006/053424 A1 describes an active matrix light emitting device display. A pixel of the display includes a light emitting device and a plurality of transistors. A capacitor is used to store a voltage applied to a driving transistor so that a current through the light emitting device is compensated for certain shifts of the transistor and is independent of characteristics of the light emitting device. A programming scheme includes first and second programming cycles and a driving cycle. During the first and second cycles both select lines are high. During the first cycle a bias current flows through a bias line and a bias voltage is applied to a signal line. In the second cycle a switch transistor is on, the bias current flowing through the bias line is zero, a programming voltage is applied to the signal line and the gate-source-voltage of the driving transistor is stored in the storage capacitor. In the third operation cycle the driving transistor is turned on and the OLED emits light.

[0015] WO 2005/015530 A1 discloses an electroluminescent display device comprising, in each pixel, a photo-sensor connected to a photo-sensor storage capacitor to measure the luminance of the respective OLED. Charge is accumulated on the photo-sensor storage capacitor over subsequent frames, the increase of which is dependent on pixel brightness. This data is provided to a compensation function unit that obtains a corrected threshold voltage and mobility data and

that corrects the data voltage to provide).

SUMMARY OF THE INVENTION

[0016] Accordingly, the present invention is directed to an organic light emitting diode (OLED) display and a method of driving the same that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0017] An object of the present invention is to provide an organic light emitting diode (OLED) display and a method of driving the same that increases the display quality by preventing the deterioration of a driving current caused by the deterioration of a drive thin film transistor (TFT) depending on driving time.

[0018] Another object of the present invention is to provide an OLED display and a method of driving the same that minimizes the deterioration of a threshold voltage of a drive TFT.

[0019] Yet another object of the present invention is to provide an OLED display and a method of driving the same that increases the display quality by compensating for a difference between threshold voltages of drive TFTs of pixels, a difference between mobilities of the drive TFTs, and a difference between potential values of Vss supply. The objects are solved by the features of the independent claims.

[0020] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is a diagram illustrating a light emitting principle of a general organic light emitting diode (OLED) display;
FIG. 2 is an equivalent circuit diagram showing one pixel in a related art active matrix type OLED display;
FIG. 3 is a graph showing a rise in a threshold voltage of a drive thin film transistor caused by a positive gate-bias stress;
FIG. 4 is a block diagram showing an OLED display according to an exemplary embodiment of the invention;
FIG. 5 is a circuit diagram of an exemplary data drive circuit of FIG. 4;
FIG. 6 is an equivalent circuit diagram of an exemplary pixel at a crossing of j-th gate, data, and sensing lines shown in FIG. 4;
FIG. 7 is an exemplary drive waveform diagram illustrating an operation of a pixel;
FIG. 8A is an equivalent circuit diagram of an exemplary pixel during a first period;
FIG. 8B is an equivalent circuit diagram of an exemplary pixel during a second period;
FIG. 8C is an equivalent circuit diagram of an exemplary pixel during a third period;
FIG. 9 is a diagram illustrating the calculation of a deviation amount of a mobility of a drive thin film transistor depending on driving time.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0022] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Exemplary embodiment

[0023] Because it is difficult to control current data depending on each gray level in an organic light emitting diode (OLED) display, a driving current actually flowing in an OLED is generated by setting a compensation voltage using a relatively high reference current and downscaling the set voltage in accordance with an exemplary embodiment of the present invention. In the OLED display according to the exemplary embodiment of the invention, a potential of a source electrode of a drive element is fixed at the set voltage, and a driving current is downscaled by reducing a potential of a gate electrode of the drive element from a reference voltage that is already supplied.

[0024] FIG. 4 is a block diagram showing an OLED display according to the exemplary embodiment of the invention. FIG. 5 is a circuit diagram of an exemplary data drive circuit of FIG. 4.

[0025] As shown in FIGs. 4 and 5, the OLED display according to the exemplary embodiment of the invention includes a display panel 116, a gate drive circuit 118, a data drive circuit 120, and a timing controller 124. The display panel 116 includes m×n pixels 122 at each crossing region of a pair of m data lines DL1 to DLm and m sensing lines SL1 to SLm that are in one-to-one correspondence with each other and n gate lines GL1 to GLn. Signal lines "a" supplying a high

potential driving voltage Vdd to each pixel 122 and signal lines "b" supplying a low potential driving voltage Vss to each pixel 122 are formed on the display panel 116. A high potential driving voltage source VDD and a low potential driving voltage source VSS generate the high potential driving voltage Vdd and the low potential driving voltage Vss, respectively.

[0026] The gate drive circuit 118 generates scan pulses Sp (FIG. 7) in response to a gate control signal GDC generated by the timing controller 124 to sequentially supply the scan pulses Sp to the gate lines GL1 to GLn. The data drive circuit 120 includes a first data driver 120a connected to the data lines DL1 to DLm and a second data driver 120b connected to the sensing lines SL1 to SLm. Although FIG. 4 shows the first and second data drivers 120a and 120b as being separate drivers formed on opposing ends of the display panel 116 for the convenience of explanation, the first and second data drivers 120a and 120b may be integrated into one data driver.

[0027] The first data driver 120a supplies a reference voltage Vref to the data lines DL1 to DLm during a first period T1, and then supplies a data voltage Vdata that is reduced from the reference voltage Vref by a data change amount ΔVdata to the data lines DL1 to DLm during a second period T2, as shown in FIG. 7. As shown in FIG. 5, the first data driver 120a includes a data generation unit 1201 a that generates the reference voltage Vref and the data voltage Vdata, and a first buffer 1202a that stabilizes the reference voltage Vref and the data voltage Vdata generated by the data generation unit 1201a to output the stabilized reference voltage Vref and the stabilized data voltage Vdata to the j-th data line DLj ($1 \leq j \leq m$). The data generation unit 1201 a includes a reference voltage source VREF, a data modulator DM, and a multiplexer MUX. The reference voltage source VREF generates the reference voltage Vref determined as a voltage between the high potential driving voltage Vdd and the low potential driving voltage Vss. The data modulator DM extracts the data change amount ΔVdata using digital video data RGB supplied by the timing controller 124 and an amount of mobility deviation MV of a drive thin film transistor (TFT) formed inside the pixel 122 depending on driving time. The data change amount ΔVdata is subtracted from the reference voltage Vref to generate the data voltage Vdata. The deviation amount of the mobility MV of the drive TFT in each pixel 122 depending on driving time is previously stored in an external memory. The multiplexer MUX selects and outputs the reference voltage Vref from the reference voltage source VREF in response to a switch control signal SC supplied by the timing controller 124 during the first period T1 and selects and outputs the data voltage Vdata from the data modulator DM during the second period T2. In the exemplary embodiment, the first period T1 is defined by a first half period of the scan pulse Sp maintained in a high logic voltage state, and the second period T2 is defined by a second half period of the scan pulse Sp maintained in the high logic voltage state.

[0028] The second data driver 120bk sinks a reference current Iref through the sensing lines SL1 to SLm to set a source voltage of the drive TFT to a sensing voltage Vsen during the first period T1, and keeps the set sensing voltage Vsen constant during the second period T2. As shown in FIG. 5, the second data driver 120b includes a reference current source IREF for sinking the reference current Iref, a second buffer 1202b for keeping the set sensing voltage Vsen constant, a first switch S 1, and a second switch S2. The first switch S1 switches on and off a current path between the reference current source IREF and an input terminal IN of the second buffer 1202b in response to the switch control signal SC supplied by the timing controller 124. The second switch S2 switches between a current path of the j-th sensing line SLj ($1 \leq j \leq m$) to the reference current source IREF and a current path of the sensing line SLj to an output terminal OUT of the second buffer 1202b in response to the switch control signal SC. During the first period T 1, the first switch S1 forms a current path between the reference current source IREF and the input terminal IN of the second buffer 1202b, and the second switch S2 forms the current path between the j-th sensing line SLj and the reference current source IREF. Hence, the set sensing voltage Vsen is applied to the input terminal IN of the second buffer 1202b. During the second period T2, the first switch S1 cuts off the current path between the reference current source IREF and the input terminal IN of the second buffer 1202b, and the second switch S2 forms the current path between the j-th sensing line SLj and the output terminal OUT of the second buffer 1202b. Hence, the sensing voltage Vsen is output through the j-th sensing line SLj with a voltage value equal to a voltage value applied to the input terminal IN of the second buffer 1202b.

[0029] The timing controller 124 supplies a digital video data RGB received from the outside to the data drive circuit 120. The timing controller 124 generates control signals GDC and DDC to control the operation timing of the gate drive circuit 118 and the data drive circuit 120, respectively, using vertical and horizontal sync signals Vsync and Hsync and a clock signal CLK. The timing controller 124 generates the switch control signal SC synchronizing the switches during the first and second periods T1 and T2. The timing controller 124 may include a memory for storing the deviation amount of mobility MV of the drive TFTs in each pixel 122 depending on driving time inside the timing controller 124.

[0030] As shown in FIG. 6, each pixel 122 includes an organic light emitting diode OLED, a drive TFT DR, two switch TFTs SW1 and SW2, and a storage capacitor Cst. FIG. 6 is an equivalent circuit diagram of an exemplary pixel 122 at a crossing of j-th gate, data, and sensing lines GLj, DLj, and SLj shown in FIG. 4. FIG. 7 is an exemplary drive waveform diagram for explaining an operation of the pixel 122. In FIG. 7, the first period T1 indicates an address period of the reference current Iref, the second period T2 indicates an address period of the data voltage Vdata, and the third period T3 indicates an emitting period.

[0031] As shown in FIGs. 6 and 7, the pixel 122 according to the exemplary embodiment of the invention includes an organic light emitting diode OLED at the crossing region of the j-th gate, data, and sensing lines GLj, DLj, and SLj, a

drive TFT DR, and a cell drive circuit 122a for driving the organic light emitting diode OLED and the drive TFT DR. The drive TFT DR includes a gate electrode G connected to the cell drive circuit 122a through a first node n1, a drain electrode D connected to the high potential driving voltage source VDD, and a source electrode S connected to the cell drive circuit 122a through a second node n2. The drive TFT DR controls a current flowing in the organic light emitting diode OLED depending on a voltage difference between a gate voltage applied to the gate electrode G and a source voltage applied to the source electrode S. The drive TFT DR may be an N-type metal-oxide semiconductor field effect transistor (MOSFET). A semiconductor layer of the drive TFT DR may include an amorphous silicon layer.

[0032] The organic light emitting diode OLED includes an anode electrode commonly connected to the drive TFT DR and the cell drive circuit 122a through the second node n2, and a cathode electrode connected to the low potential driving voltage source VSS. The organic light emitting diode OLED has the same structure as the structure shown in FIG. 1 and represents a gray scale of the OLED display by emitting light using the driving current controlled by the drive TFT DR.

[0033] The cell drive circuit 122a includes the first switch TFT SW1, the second switch TFT SW2, and the storage capacitor Cst. The cell drive circuit 122a and the data drive circuit 120 constitute a driving current stabilization circuit that prevents the driving current flowing in the organic light emitting diode OLED depending on driving time from becoming degraded.

[0034] During the first period T1, the driving current stabilization circuit including the cell drive circuit 122a applies the reference voltage Vref to the gate electrode G of the drive TFT DR to turn on the drive TFT DR and sinks the reference current Iref through the drive TFT DR to set the source voltage of the drive TFT DR to the sensing voltage Vsen. Then, during the second period T2, the driving current stabilization circuit fixes the source voltage of the drive TFT DR to the set sensing voltage Vsen and reduces a potential of the gate electrode G of the drive TFT DR to the data voltage Vdata obtained by subtracting the data change amount ΔVdata from the reference voltage Vref to reduce a voltage between the gate and source electrodes of the drive TFT DR. Then, during the third period T3, the driving current stabilization circuit downscales the current to be applied to the organic light emitting diode OLED.

[0035] In particular, the first switch TFT SW1 includes a gate electrode G connected to the j-th gate line GLj, a drain electrode D connected to the first data driver 120a through the j-th data line DLj, and a source electrode S connected to the first node n1. The first switch TFT SW1 switches on and off the current path between the j-th data line DLj and the first node n1 in response to the scan pulse Sp. Hence, the first switch TFT SW1 uniformly keeps the potential of the gate electrode G of the drive TFT DR at the reference voltage Vref during the first period T1 and then reduces the potential of the gate electrode G to the data voltage Vdata during the second period T2.

[0036] The second switch TFT SW2 includes a gate electrode G connected to the j-th gate line GLj, a drain electrode D connected to the second data driver 120b through the j-th sensing line SLj, and a source electrode S connected to the second node n2. The second switch TFT SW2 switches on and off the current path between the j-th sensing line SLj and the second node n2 in response to the scan pulse Sp. Thus, the reference current Iref is sunk through the drive TFT DR and the second switch TFT SW2 during the first period T1. After the source voltage of the drive TFT DR is set at the sensing voltage Vsen by the sink operation of the reference current Iref, the source voltage is kept at the sensing voltage Vsen during the second period T2.

[0037] The storage capacitor Cst includes a first electrode connected to the first node n1 and a second electrode connected to the second node n2. During the third period T3 during which the organic light emitting diode OLED emits light, the storage capacitor Cst keeps the voltage between the gate electrode G and the source electrode S of the drive TFT DR set during the first and second periods T1 and T2 constant.

[0038] A detailed operation of the pixel 122 will be described below with reference to FIGs. 7 and 8A to 8C. As shown in FIGs. 7 and 8A, the scan pulse Sp is generated as a high logic voltage during the first period T1. Thus, the first and second switch TFTs SW1 and SW2 are turned on. The reference voltage Vref is applied to the first node n1 by the turned-on first and second switch TFTs SW1 and SW2 Thus, the drive TFT DR is turned on. The reference current Iref is sunk from the high potential driving voltage source VDD to the data drive circuit 120 via the drive TFT DR and the second node n2 by the turned-on drive TFT DR. The reference current Iref is expressed by the following Equation 2:

$$Iref = \frac{\beta}{2}(Vref - Vsen - Vth)^2$$

[0039] In the above Equation 2, β indicates a constant determined by the mobility and parasitic capacitance of the drive TFT DR, Vsen indicates the sensing voltage at the second node n2, and Vth indicates a threshold voltage of the TFT DR.

[0040] The sensing voltage Vsen at the second node n2 are different in each pixel 122 depending on a characteristic deviation of the TFT DR and a location of the pixel 122. For example, the sensing voltage Vsen at the first pixel is smaller

than the sensing voltage Vsen at the second pixel whose threshold voltage Vth of the TFT DR is smaller than the threshold voltage Vth of the TFT DR of the first pixel. Further, the sensing voltage Vsen at the first pixel is smaller than the sensing voltage Vsen at the second pixel whose mobility of the TFT DR is higher than the mobility of the TFT DR of the first pixel. Still further, the sensing voltage Vsen at the first pixel is smaller than the sensing voltage Vsen at the second pixel whose potential of the Vss supply line is lower than a potential of the Vss supply line of the first pixel. As described above, because the sensing voltage Vsen has a different value in each pixel 122 depending on the characteristic deviation of the TFT DR and the location of the pixel 122 inside the display panel 116, a difference between the threshold voltages of the drive TFTs DR of the pixels 122, a difference between the mobilities of the drive TFTs DR, and a potential difference between the Vss supply lines can be compensated. Accordingly, all the pixels 122 are programmed so that the same current flows in the organic light emitting diode OLED in response to the same data voltage.

[0041] When the reference current Iref is sunk during the first period T1, the organic light emitting diode OLED has to be turned off. Therefore, a potential of the low potential driving voltage source VSS may be set to be larger than a voltage value obtained by subtracting the threshold voltage Vth of the TFT DR and a threshold voltage Voled of the organic light emitting diode OLED from the reference voltage Vref. The organic light emitting diode OLED remains in a turn-off state during the second period T2.

[0042] As shown in FIGs. 7 and 8B, the scan pulse Sp remains in a high logic voltage state during the second period T2, and thus the first and second switch TFTs SW1 and SW2 remain in a turn-on state. While the data drive circuit 120 uniformly maintains the potential of the second node n2 at the sensing voltage Vsen, the data drive circuit 120 allows the potential of the first node n1 to be the data voltage Vdata obtained by subtracting the data change amount ΔVdata from the reference voltage Vref. In other words, the potential of the first node n1 during the second period T2 is lower than the potential of the first node n1 during the first period T1. The reason why voltage between the gate and source electrodes of the drive TFT DR is reduced by lowering the potential of the first node n1 during the second period T2 is to change the current to be applied to the organic light emitting diode OLED from the reference current Iref to a driving current level corresponding to an actual gray level. The storage capacitor Cst keeps the downscaled voltage between the gate and source electrodes of the drive TFT DR constant, thereby keeping the programmed current constant.

[0043] As shown in FIGs. 7 and 8C, the scan pulse Sp is switched to a low logic voltage state during the third period T3. Thus, the first and second switch TFTs SW1 and SW2 are turned off. Although the first and second switch TFTs SW1 and SW2 are turned off, the programmed current, namely, the downscaled current still flows between the gate and source electrodes of the drive TFT DR. The downscaled current allows the potential at the second node n2 connected to the anode electrode of the organic light emitting diode OLED to increase from the sensing voltage Vsen by an amount equal to or larger than a sum of the threshold voltage Voled of the organic light emitting diode OLED and the low potential driving voltage Vss (i.e., Vsen+Vss+Voled). Thus, the organic light emitting diode OLED is turned on. When the potential of the second node n2 rises, the potential of the first node n1 also rises by the same amount (Vss+Voled) as a rise width of the potential of the second node n2 due to a boosting effect of the storage capacitor Cst. As a result, the current programmed during the second period T2 is continuously maintained during the third period T3.

[0044] The current Ioled flowing in the organic light emitting diode OLED during the third period T3 is expressed by the following Equation 3:

$$Ioled = \frac{\beta}{2}(Vref - \Delta Vdata - Vsen - Vth)^2$$

[0045] The current Ioled flowing in the organic light emitting diode OLED is expressed by the following Equation 4 by substituting Equation 2 in Equation 3.

$$Vref - Vsen - Vth = \sqrt{\frac{2}{\beta} Iref} \text{-------} (1)$$

$$Ioled = \frac{\beta}{2}\left(\sqrt{\frac{2}{\beta} Iref} - \Delta Vdata\right)^2 \text{----} (2)$$

[0046] As indicated in the above Equation 4(2), the current Ioled flowing in the organic light emitting diode OLED depends on the reference current Iref and the data change amount ΔVdata. In other words, the current Ioled is not

affected by a change in the threshold voltage Vth of the drive TFT DR. However, because the constant β determined by the mobility of the drive TFT DR remains in the above equation 4(2), the current Ioled flowing in the organic light emitting diode OLED is affected by a deviation of the mobility between the drive TFTs DR of the pixels. To compensate for the deviation, when the data change amount ΔVdata is extracted using the data drive circuit, the deviation amount of mobility MV of the drive TFT DR depending on driving time has to be considered. In other words, the constant β has to be eliminated from the data change amount ΔVdata.

[0047] Accordingly, Equation 4(1) may be abbreviated and expressed as the following Equation 5:

$$y = const. - \sqrt{\frac{2}{\beta}}\, x \quad , \quad (y = Vsen \, , \quad x = \sqrt{Iref})$$

[0048] As indicated in the above Equation 5, the deviation amount of mobility MV of the drive TFT DR depending on driving time results in a slope of a functional formula. Accordingly, as shown in FIG. 9, if two predetermined values on an X-axis are selected, values on the Y-axis can be obtained through the above Equation 5. As a result, a described slope can be calculated. Because the calculated slope may be different for each pixel, the slopes are stored in the memory in the form of a lookup table, and the slope lookup table is used to extract the data change amount ΔVdata using the data drive circuit during the second period T2. The current Ioled flowing in the organic light emitting diode OLED in which the slope is included in the data change amount ΔVdata is expressed by the following Equation 6, where A is a constant:

$$Ioled = Iref\left(1 - \frac{\Delta Vdata'}{A}\right)^2 \quad , \quad \left(\Delta Vdata' = \frac{A}{\sqrt{\frac{2}{\beta} Iref}}\, \Delta Vdata\right)$$

[0049] As indicated in the above Equation 6, the current Ioled flowing in the organic light emitting diode OLED is not affected by the deviation between the mobilities of the drive TFTs DR of the pixels since the constant β has been eliminated from the data change amount ΔVdata.

[0050] As described above, while it is difficult to control the current data depending on each gray level in the OLED display, the driving current actually flowing in the organic light emitting diode may be adjusted by setting a compensation voltage using a relatively high reference current and downscaling the set voltage according to the exemplary embodiment of the present invention.

[0051] As described above, the OLED display and the method of driving the same according to the exemplary embodiment of the present invention compensate for a difference between the threshold voltages of the drive TFTs, a difference between the mobilities of the drive TFTs, and a difference between the potentials of the Vss supply lines using a hybrid technique mixing current drive techniques with voltage drive technique, thereby preventing the degradation of the driving current and greatly improving the display quality.

[0052] Furthermore, the OLED display and the method of driving the same according to the exemplary embodiments of the present invention include a dual drive element inside each pixel that is alternately driven using two scan signals that alternate at every predetermined time interval, thereby minimizing the degradation of the threshold voltage of the drive element.

[0053] It will be apparent to those skilled in the art that various modifications and variations can be made in the OLED display of the present invention and the method of driving the same without departing scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims.

Claims

1. An organic light emitting diode display, comprising:

a data line (DLj);
a gate line (GLj) that crosses the data line (DLj) to receive a scan pulse;
a sensing line (SLj) positioned parallel to the data line (DLj);

a high potential driving voltage source adapted to generate a high potential driving voltage (VDD);
a low potential driving voltage source adapted to generate a low potential driving voltage (VSS);
a light emitting element (OLED) adapted to emit light due to a current flowing between the high potential driving voltage source and the low potential driving voltage source;
a drive element (DR) connected between the high potential driving voltage source and the light emitting element (OLED) adapted to control a current flowing in the light emitting element (OLED) depending on a voltage between a gate electrode (G) and a source electrode (S) of the drive element (DR); and
a driving current stabilization circuit adapted, in a first period (T1), to apply a stabilized first voltage (Vref) to the gate electrode (G) of the drive element (DR) to turn on the drive element (DR) and to sink a reference current (Iref) through the drive element (DR) to set a source voltage of the drive element (DR) at a sensing voltage (Vsen) and, in a second period (T2) subsequent to the first period, to reduce the voltage between the gate and source electrodes (G, S) of the drive element (DR) to scale a current to be applied to the light emitting element (OLED) from the reference current (Iref) by keeping potential of the source electrode (S) of the drive element (DR) fixed at the sensing voltage (Vsen) and reducing the potential of the gate electrode (G) of the drive element (DR) from the stabilized first voltage,
wherein the driving current stabilization circuit includes a cell drive circuit (122a) connected to the drive element (DR) and the light emitting element (OLED) at a crossing of the data line (DLj), the sensing line (SLj), and the gate line (GLj), and a data drive circuit (120) connected to the cell drive circuit (122a) through the data line (DLj) and the sensing line (SLj),
wherein the data drive circuit (120) includes a first data driver (120a) adapted to supply the stabilized first voltage to the data line (DLj) during the first period (T1) and to supply a stabilized data voltage (Vdata) that is reduced from the stabilized first voltage by a data change amount (ΔVdata) to the data line (DLj) during the second period (T2), and a second data driver (120b) adapted to sink the reference current (Iref) through the sensing line (SLj) to set the sensing voltage (Vsen) during the first period (T1); **characterised in that**:
the second data driver (120b) is further adapted to keep the set sensing voltage (Vsen) constant during the second period (T2), and
the first data driver (120a) includes a data generation unit (1201a) adapted to alternately generate a first voltage and a data voltage (Vdata) respectively in the first period (T1) and in the second period (T2) to extract the data change amount (ΔVdata) stored in a memory based on a deviation amount of a mobility of the drive element (DR) depending on driving time, and to subtract the data change amount (ΔVdata) from the first voltage to generate the data voltage (Vdata), and a first buffer (1202a) adapted to stabilize the first voltage and the data voltage (Vdata) generated by the data generation unit (1201a) to output the stabilized first voltage in the first period (T1) and the stabilized data voltage (Vdata) in the second period (T2) to the data line (DLj).

2. The organic light emitting diode display of claim 1, wherein the first voltage is a reference voltage (Vref).

3. The organic light emitting diode display of claim 1, wherein the drive current stabilization circuit is adapted to set the source voltage of the drive element (DR) at a sensing voltage (Vsens) during the first period (T1) and then to modify the voltage between the gate and source electrodes (G, S) of the drive element (DR) during the second period (T2), such that the light emitting element (OLED) is turned off during the first and second periods (T1, T2) and turned on during a third period (T3) following the second period (T2).

4. The organic light emitting diode display of claim 3, wherein the first period (T1) is a first half period of the scan pulse maintained in a high logic voltage state, the second period (T2) is a second half period of the scan pulse maintained in a high logic voltage state, and the third period is (T3) a period during which the scan pulse is maintained in a low logic voltage state.

5. The organic light emitting diode display of claim 1, wherein the cell drive circuit (122a) includes
a storage capacitor (Cst) including a first electrode connected to the gate electrode (G) of the drive element (DR) through a first node (n1) and a second electrode connected to the source electrode (S) of the drive element (DR) through a second node (n2),
a first switch thin film transistor (TFT) (SW1) adapted to switch on and off a current path between the data line (DLj) and the first node (n1) in response to the scan pulse, and
a second switch TFT (SW2) adapted to switch on and off a current path between the sensing line (SLj) and the second node (n2) in response to the scan pulse.

6. The organic light emitting diode display of claim 1, wherein the second data driver (120b) includes
a reference current source (IREF) adapted to sink the reference current (Iref),

a second buffer (1202b) adapted to keep the sensing voltage (Vsen) constant,
a first switch (S1) adapted to form a current path between the reference current source (IREF) and an input terminal (IN) of the second buffer (1202b) during the first period (T1) and to cut off the current path between the reference current source (IREF) and the input terminal (IN) of the second buffer (1202b) during the second period (T2), and
a second switch (S2) adapted to form a current path between the sensing line (SLj) and the reference current source (IREF) during the first period (T1) and to form a current path between the sensing line (SLj) and an output terminal (OUT) of the second buffer (1202b) during the second period (T2).

7. A method of driving a organic light emitting diode display according to one of the preceding claims, the method comprising:

in the first period (T1), applying the first voltage to the gate electrode (G) of the drive element (DR) to turn on the drive element (DR) and
sinking the reference current (Iref) through the drive element (DR) to set the source voltage of the drive element (DR) at the sensing voltage (Vsen); and
in the second period (T2), modifying the voltage between the gate and source electrodes (G, S) to scale the current to be applied to the light emitting element (OLED) from the reference current (Iref) **characterized in that**:

by the second data driver (120b), keeping the set sensing voltage (Vsen) constant during the second period (T2), and,
by data generation unit (1201 a), alternately generating the first voltage and the data voltage (Vdata) respectively in the first period (T1) and in the second period (T2), extracting the data change amount (ΔVdata) stored in the memory based on a deviation amount of the mobility of the drive element (DR) depending on driving time, subtracting the data change amount (ΔVdata) from the first voltage to generate the data voltage (Vdata), and,
by the first buffer (1202a), stabilizing the first voltage and the data voltage to output the stabilized first voltage in the first period (T1) and the stabilized data voltage (Vdata) in the second period (T2) to the data line (DLj).

Patentansprüche

1. Anzeige mit organischen Leuchtdioden, die umfasst:

eine Datenleitung (DLj);
eine Gate-Leitung (GLj), die die Datenleitung (DLj) kreuzt, um einen Abtastimpuls zu empfangen;
eine Abtastleitung (SLj), die parallel zu der Datenleitung (DLj) positioniert ist;
eine Ansteuerungsspannungsquelle mit hohem Potential, die beschaffen ist, eine Ansteuerungsspannung mit hohem Potential (VDD) zu erzeugen;
eine Ansteuerungsspannungsquelle mit tiefem Potential, die beschaffen ist, eine Ansteuerungsspannung mit tiefem Potential (VSS) zu erzeugen;
ein Lichtemissionselement (OLED), das beschaffen ist, Licht aufgrund eines Stroms, der zwischen der Ansteuerungsspannungsquelle mit hohem Potential und der Ansteuerungsspannungsquelle mit tiefem Potential fließt, zu emittieren;
ein Ansteuerelement (DR), das zwischen die Ansteuerungsspannungsquelle mit hohem Potential und das Lichtemissionselement (OLED) geschaltet ist und das beschaffen ist, einen Strom, der in dem Lichtemissionselement (OLED) fließt, in Abhängigkeit von einer Spannung zwischen einer Gate-Elektrode (G) und einer Source-Elektrode (S) des Ansteuerelements (DR) zu steuern; und
eine Ansteuerungsstrom-Stabilisierungsschaltung, die beschaffen ist, während eines ersten Zeitraums (T1) eine stabilisierte erste Spannung (Vref) an die Gate-Elektrode (G) des Ansteuerelements (DR) anzulegen, um das Ansteuerelement (DR) einzuschalten und um einen Bezugsstrom (Iref) durch das Ansteuerelement (DR) zu ziehen, um eine Quellenspannung des Ansteuerelements (DR) auf eine Abtastspannung (Vsen) festzulegen, und während eines zweiten Zeitraums (T1) nach dem ersten Zeitraum die Spannung zwischen der Gate- und der Source-Elektrode (G, S) des Ansteuerelements (DR) zu verringern, um durch das Halten eines Potentials der Source-Elektrode (S) des Ansteuerelements (DR) fest auf der Abtastspannung (Vsen) und das Verringern des Potentials der Gate-Elektrode (G) des Ansteuerelements (DR) von der stabilisierten ersten Spannung einen Strom, der in das Lichtemissionselement (OLED) einzuspeisen ist, von dem Bezugsstrom (Iref) zu skalieren,
wobei die Ansteuerungsstrom-Stabilisierungsschaltung eine Zellenansteuerschaltung (122a), die mit dem An-

steuerelement (DR) und dem Lichtemissionselement (OLED) an einer Kreuzung der Datenleitung (DLj), der Abtastleitung (SLj) und der Gate-Leitung (GLj) verbunden ist, und eine Datenansteuerschaltung (120), die mit der Zellenansteuerschaltung (122a) durch die Datenleitung (DLj) und die Abtastleitung (SLj) verbunden ist, enthält,

wobei die Datenansteuerschaltung (120) einen ersten Datentreiber (120a), der beschaffen ist, während des ersten Zeitraums (T1) die stabilisierte erste Spannung der Datenleitung (DLj) zuzuführen und während des zweiten Zeitraums (T2) eine stabilisierte Datenspannung (Vdata), die von der stabilisierten ersten Spannung um einen Datenänderungsbetrag (ΔVdata) verringert ist, der Datenleitung (Dlj) zuzuführen, und einen zweiten Datentreiber (120b), der beschaffen ist, während des ersten Zeitraums (T1) den Bezugsstrom (Iref) durch die Abtastleitung (SLj) zu ziehen, um die Abtastspannung (Vsen) festzulegen, enthält; **dadurch gekennzeichnet, dass**:

der zweite Datentreiber (120b) ferner beschaffen ist, während des zweiten Zeitraums (T2) die festgelegte Abtastspannung (Vsen) konstant zu halten, und

der erste Datentreiber (120a) eine Datenerzeugungseinheit (1201a), die beschaffen ist, während des ersten Zeitraums (T1) und während des zweiten Zeitraums (T2) abwechselnd eine erste Spannung bzw. eine Datenspannung (Vdata) zu erzeugen, den Datenänderungsbetrag (ΔVdata), der in einem Speicher gespeichert ist, basierend auf einem Abweichungsbetrag einer Beweglichkeit des Ansteuerelements (DR) in Abhängigkeit von einem Ansteuerungszeitraum zu extrahieren und den Datenänderungsbetrag (ΔVdata) von der ersten Spannung abzuziehen, um die Datenspannung (Vdata) zu erzeugen, und einen ersten Puffer (1202a), der beschaffen ist, die erste Spannung und die durch die Datenerzeugungseinheit (1201a) erzeugte Datenspannung (Vdata) zu stabilisieren, um während des ersten Zeitraums (T1) die stabilisierte erste Spannung und während des zweiten Zeitraums (T2) die stabilisierte Datenspannung (Vdata) an die Datenleitung (DLj) auszugeben, enthält.

2. Anzeige mit organischen Leuchtdioden nach Anspruch 1, wobei die erste Spannung eine Bezugsspannung (Vref) ist.

3. Anzeige mit organischen Leuchtdioden nach Anspruch 1, wobei die Ansteuerungsstrom-Stabilisierungsschaltung beschaffen ist, während des ersten Zeitraums (T1) die Quellenspannung des Ansteuerelements (DR) auf eine Abtastspannung (Vsens) festzulegen und dann während des zweiten Zeitraums (T2) die Spannung zwischen der Gate- und der Source-Elektrode (G, S) des Ansteuerelements (DR) zu modifizieren, so dass das Lichtemissionselement (OLED) während des ersten und des zweiten Zeitraums (T1, T2) ausgeschaltet ist und während eines dritten Zeitraums (T3) im Anschluss an den zweiten Zeitraum (T2) eingeschaltet ist.

4. Anzeige mit organischen Leuchtdioden nach Anspruch 3, wobei der erste Zeitraum (T1) eine erste Halbperiode des Abtastimpulses ist, der auf einem hohen Logikspannungszustand aufrechterhalten wird, der zweite Zeitraum (T2) eine zweite Halbperiode des Abtastimpulses ist, der auf einem hohen Logikspannungszustand aufrechterhalten wird, und der dritte Zeitraum (T3) ein Zeitraum ist, während dessen der Abtastimpuls in einem tiefen Logikspannungszustand aufrechterhalten wird.

5. Anzeige mit organischen Leuchtdioden nach Anspruch 1, wobei die Zellenansteuerschaltung (122a) enthält
einen Speicherkondensator (Cst), der eine erste Elektrode, die durch einen ersten Knoten (n1) mit der Gate-Elektrode (G) des Ansteuerelements (DR) verbunden ist, und eine zweite Elektrode, die durch einen zweiten Knoten (n2) mit der Source-Elektrode (S) des Ansteuerelements (DR) verbunden ist, enthält,
einen ersten Dünnschicht-Schalttransistor (Schalt-TFT) (SW1), der beschaffen ist, in Reaktion auf den Abtastimpuls einen Strompfad zwischen der Datenleitung (DLj) und dem ersten Knoten (n1) ein- und auszuschalten, und
einen zweiten Schalt-TFT (SW2), der beschaffen ist, in Reaktion auf den Abtastimpuls einen Strompfad zwischen der Abtastleitung (Slj) und dem zweiten Knoten (n2) ein- und auszuschalten.

6. Anzeige mit organischen Leuchtdioden nach Anspruch 1, wobei der zweite Datentreiber (120b) enthält
eine Bezugsstromquelle (IREF), die beschaffen ist, den Bezugsstrom (Iref) zu ziehen,
einen zweiten Puffer, der beschaffen ist, die Abtastspannung (Vsen) konstant zu halten,
einen ersten Schalter (S1), der beschaffen ist, während des ersten Zeitraums (T1) einen Strompfad zwischen der Bezugsstromquelle (IREF) und einem Eingangsanschluss (IN) des zweiten Puffers (1202b) zu bilden und während des zweiten Zeitraums (T2) den Strompfad zwischen der Bezugsstromquelle (IREF) und dem Eingangsanschluss (IN) des zweiten Puffers (1202b) zu unterbrechen, und
einen zweiten Schalter (S2), der beschaffen ist, während des ersten Zeitraums (T1) einen Strompfad zwischen der Abtastleitung (SLj) und der Bezugsstromquelle (IREF) zu bilden und während des zweiten Zeitraums (T2) einen

Strompfad zwischen der Abtastleitung (SLj) und einem Ausgangsanschluss (OUT) des zweiten Puffers (1202b) zu bilden.

7. Verfahren zum Ansteuern einer Anzeige mit organischen Leuchtdioden nach einem der vorhergehenden Ansprüche, wobei das Verfahren umfasst:

während des ersten Zeitraums (T1) Anlegen der ersten Spannung an die Gate-Elektrode (G) des Ansteuerelements (DR), um das Ansteuerelement (DR) einzuschalten; und
Ziehen des Bezugsstroms (Iref) durch das Ansteuerelement (DR), um die Quellenspannung des Ansteuerelements (DR) auf die Abtastspannung (Vsen) festzulegen; und
während des zweiten Zeitraums (T2) Modifizieren der Spannung zwischen der Gate- und der Source-Elektrode (G, S), um den in das Lichtemissionselement (OLED) eingespeisten Strom von dem Bezugsstrom (Iref) zu skalieren,
gekennzeichnet durch
Halten der festgelegten Abtastspannung (Vsen) konstant während des zweiten Zeitraums (T2) **durch** den zweiten Datentreiber (120b) und
abwechselndes Erzeugen während des ersten Zeitraums (T1) und während des zweiten Zeitraums (T2) der ersten Spannung bzw. der Datenspannung (Vdata), Extrahieren des Datenänderungsbetrags (ΔVdata), der im Speicher gespeichert ist, basierend auf einem Abweichungsbetrag der Beweglichkeit des Ansteuerelements (DR) in Abhängigkeit vom Ansteuerungszeitraum, Abziehen des Datenänderungsbetrags (ΔVdata) von der ersten Spannung, um die Datenspannung (Vdata) zu erzeugen, **durch** die Datenerzeugungseinheit (1201a) und Stabilisieren der ersten Spannung und der Datenspannung, um während des ersten Zeitraums (T1) die stabilisierte erste Spannung und während des zweiten Zeitraums (T2) die stabilisierte Datenspannung (Vdata) an die Datenleitung (DLj) auszugeben, **durch** den ersten Puffer (1202a).

Revendications

1. Affichage à diodes électroluminescentes organiques, comprenant :

une ligne de données (DLj) ;
une ligne de grille (GLj) qui croise la ligne de données (DLj) pour recevoir une impulsion de balayage ;
une ligne de détection (SLj) positionnée parallèlement à la ligne de données (DLj) ;
une source de tension d'attaque à haut potentiel apte à générer une tension d'attaque à haut potentiel (VDD) ;
une source de tension d'attaque à bas potentiel apte à générer une tension d'attaque à bas potentiel (VSS) ;
une élément électroluminescent (OLED) apte à émettre une lumière en raison d'un courant s'écoulant entre la source de tension d'attaque à haut potentiel et la source de tension d'attaque à bas potentiel ;
un élément d'attaque (DR) relié entre la source de tension d'attaque à haut potentiel et l'élément électroluminescent (OLED) apte à commander un courant s'écoulant dans l'élément électroluminescent (OLED) en fonction d'une tension entre une électrode de grille (G) et une électrode de source (S) de l'élément d'attaque (DR) ; et
un circuit de stabilisation de courant d'attaque apte, dans une première période (T1), à appliquer une première tension stabilisée (Vref) à l'électrode de grille (G) de l'élément d'attaque (DR) pour mettre l'élément d'attaque (DR) sous tension et dissiper un courant de référence (Iref) par l'intermédiaire de l'élément d'attaque (DR) pour régler une tension de source de l'élément d'attaque (DR) à une tension de détection (Vsen) et, dans une deuxième période (T2) suivant la première période, réduire la tension entre les électrodes de grille et de source (G, S) de l'élément d'attaque (DR) pour mettre à l'échelle un courant à appliquer à l'élément électroluminescent (OLED) à partir du courant de référence (Iref) en maintenant un potentiel de l'électrode de source (S) de l'élément d'attaque (DR) fixe à la tension de détection (Vsen) et en réduisant le potentiel de l'électrode de grille (G) de l'élément d'attaque (DR) à partir de la première tension stabilisée,
dans lequel le circuit de stabilisation de courant d'attaque comprend un circuit d'attaque de cellule (122a) relié à l'élément d'attaque (DR) et à l'élément électroluminescent (OLED) à un croisement de la ligne de données (DLj), la ligne de détection (SLj) et la ligne de grille (GLj), et un circuit d'attaque de données (120) relié au circuit d'attaque de cellule (122a) par l'intermédiaire de la ligne de données (DLj) et la ligne de détection (SLj),
dans lequel le circuit d'attaque de données (120) comprend comprend un premier circuit d'attaque de données (120a) apte à fournir la première tension stabilisée à la ligne de données (DLj) au cours de la première période (T1) et à fournir une tension de données stabilisée (Vdata) qui est réduite par rapport à la première tension stabilisée d'une quantité de changement de données (ΔVdata) à la ligne de données (DLj) au cours de la deuxième période (T2), et un deuxième circuit d'attaque de données (120b) apte à dissiper le courant de

référence (Iref) par l'intermédiaire de la ligne de détection (SLj) pour régler la tension de détection (Vsen) au cours de la première période (T1) ;
caractérisé en ce que :

le deuxième circuit d'attaque de données (120b) est en outre apte à maintenir la tension de détection réglée (Vsen) constante au cours de la deuxième période (T2), et
le premier circuit d'attaque de données (120a) comprend une unité de génération de données (1201a) apte à générer en alternance une première tension et une tension de données (Vdata) respectivement dans la première période (T1) et dans la deuxième période (T2), extraire la quantité de changement de données (ΔVdata) mémorisée dans une mémoire sur la base d'une quantité de déviation d'une mobilité de l'élément d'attaque (DR) en fonction du temps d'attaque, et soustraire la quantité de changement de données (ΔVdata) à la première tension pour générer la tension de données (Vdata), et une première mémoire tampon (1202a) apte à stabiliser la première tension et la tension de données (Vdata) générée par l'unité de génération de données (1201a) afin de délivrer la première tension stabilisée dans la première période (T1) et la tension de données stabilisée (Vdata) dans la deuxième période (T2) à la ligne de données (DLj).

2. Affichage à diodes électroluminescentes organiques selon la revendication 1, dans lequel la première tension est une tension de référence (Vref).

3. Affichage à diodes électroluminescentes organiques selon la revendication 1, dans lequel le circuit de stabilisation de courant d'attaque est apte à régler la tension de source de l'élément d'attaque (DR) à une tension de détection (Vsens) au cours de la première période (T1) puis modifier la tension entre les électrodes de grille et de source (G, S) de l'élément d'attaque (DR) au cours de la deuxième période (T2), de sorte que l'élément électroluminescent (OLED) soit mis hors tension au cours des première et deuxième périodes (T1, T2) et soit mis sous tension au cours d'une troisième période (T3) suivant la deuxième période (T2).

4. Affichage à diodes électroluminescentes organiques selon la revendication 3, dans lequel la première période (T1) est une première demi-période de l'impulsion de balayage maintenue dans un état de haute tension logique, la deuxième période (T2) est une deuxième demi-période de l'impulsion de balayage maintenue dans un état de haute tension logique, et la troisième période (T3) est une période au cours de laquelle l'impulsion de balayage est maintenue dans un état de basse tension logique.

5. Affichage à diodes électroluminescentes organiques selon la revendication 1, dans lequel le circuit d'attaque de cellule (122a) comprend :

un condensateur de stockage (Cst) comprenant une première électrode reliée à l'électrode de grille (G) de l'élément d'attaque (DR) par l'intermédiaire d'un premier noeud (n1) et une deuxième électrode reliée à l'électrode de source (S) de l'élément d'attaque (DR) par l'intermédiaire d'un deuxième noeud (n2),
un premier transistor à film mince (TFT) de commutation (SW1) apte à mettre une voie de courant sous tension et hors tension entre la ligne de données (DLj) et le premier noeud (n1) en réponse à l'impulsion de balayage, et
un deuxième TFT de commutation (SW2) apte à mettre une voie de courant sous tension et hors tension entre la ligne de détection (SLj) et le deuxième noeud (n2) en réponse à l'impulsion de balayage.

6. Affichage à diodes électroluminescentes organiques selon la revendication 1, dans lequel le deuxième circuit d'attaque de données (120b) comprend :

une source de courant de référence (IREF) apte à dissiper le courant de référence (Iref),
une deuxième mémoire tampon (1202b) apte à maintenir la tension de détection (Vsen) constante,
un premier commutateur (S1) apte à former une voie de courant entre la source de courant de référence (IREF) et une borne d'entrée (IN) de la deuxième mémoire tampon (1202b) au cours de la première période (T1) et à couper la voie de courant entre la source de courant de référence (IREF) et la borne d'entrée (IN) de la deuxième mémoire tampon (1202b) au cours de la deuxième période (T2), et
un deuxième commutateur (S2) apte à former une voie de courant entre la ligne de détection (SLj) et la source de courant de référence (IREF) au cours de la première période (T1) et former une voie de courant entre la ligne de détection (SLj) et une borne de sortie (OUT) de la deuxième mémoire tampon (1202b) au cours de la deuxième période (T2).

7. Procédé d'attaque d'un affichage à diodes électroluminescentes organiques selon l'une des revendications précé-

dentes, le procédé comprenant :

dans la première période (T1), l'application de la première tension à l'électrode de grille (G) de l'élément d'attaque (DR) pour mettre l'élément d'attaque (DR) sous tension ; et
la dissipation du courant de référence (Iref) par l'intermédiaire de l'élément d'attaque (DR) pour régler la tension de source de l'élément d'attaque (DR) à la tension de détection (Vsen) ; et
dans la deuxième période (T2), la modification de la tension entre les électrodes de grille et de source (G, S) pour mettre à l'échelle le courant à appliquer à l'élément électroluminescent (OLED) à partir du courant de référence (Iref),
caractérisé en ce que :

le deuxième circuit d'attaque de données (120b) maintient la tension de détection réglée (Vsen) constante au cours de la deuxième période (T2), et
l'unité de génération de données (1201a) génère en alternance la première tension et la tension de données (Vdata) respectivement dans la première période (T1) et dans la deuxième période (T2), extrait la quantité de changement de données (ΔVdata) mémorisée dans la mémoire sur la base d'une quantité de déviation de la mobilité de l'élément d'attaque (DR) en fonction du temps d'attaque, et soustrait la quantité de changement de données (ΔVdata) à la première tension pour générer la tension de données (Vdata), et
la première mémoire tampon (1202a) stabilise la première tension et la tension de données pour délivrer la première tension stabilisée dans la première période (T1) et la tension de données stabilisée (Vdata) dans la deuxième période (T2) à la ligne de données (DLj).

FIG. 1

(Related Art)

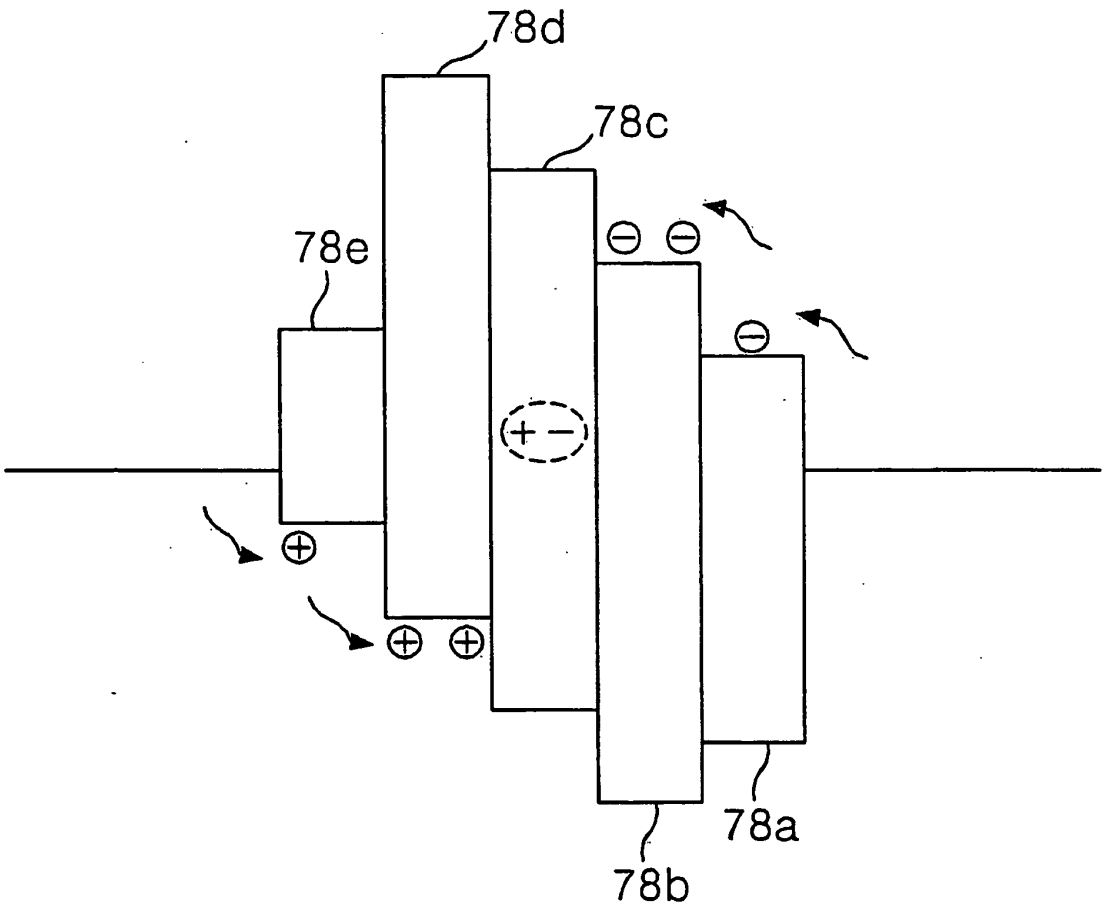


FIG. 2

(Related Art)

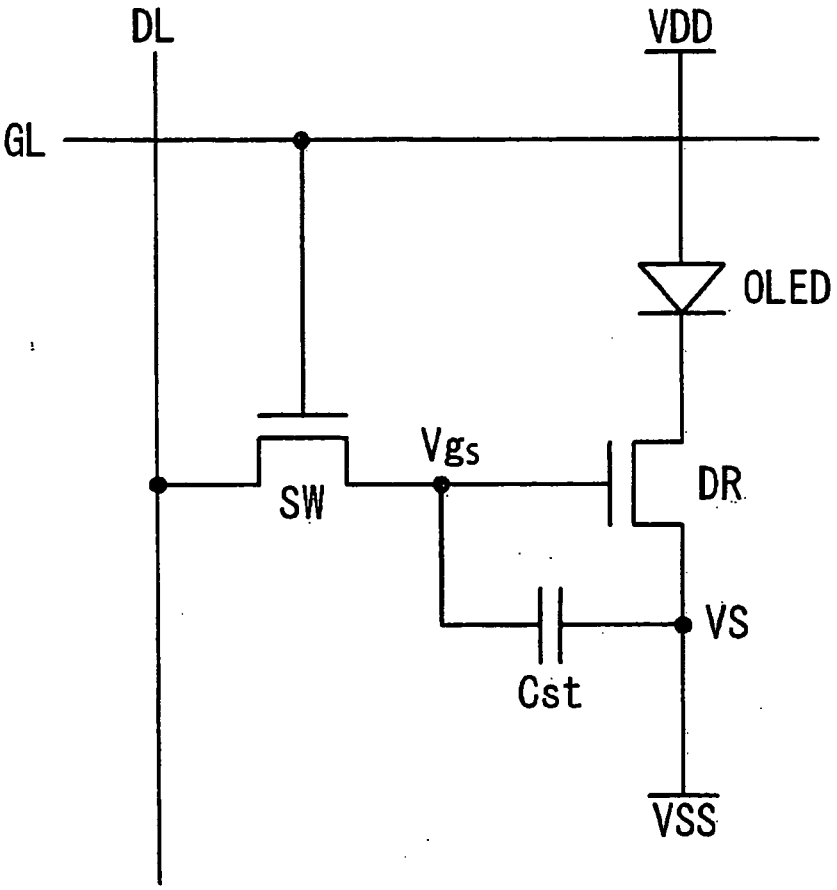


FIG. 3

(Related Art)

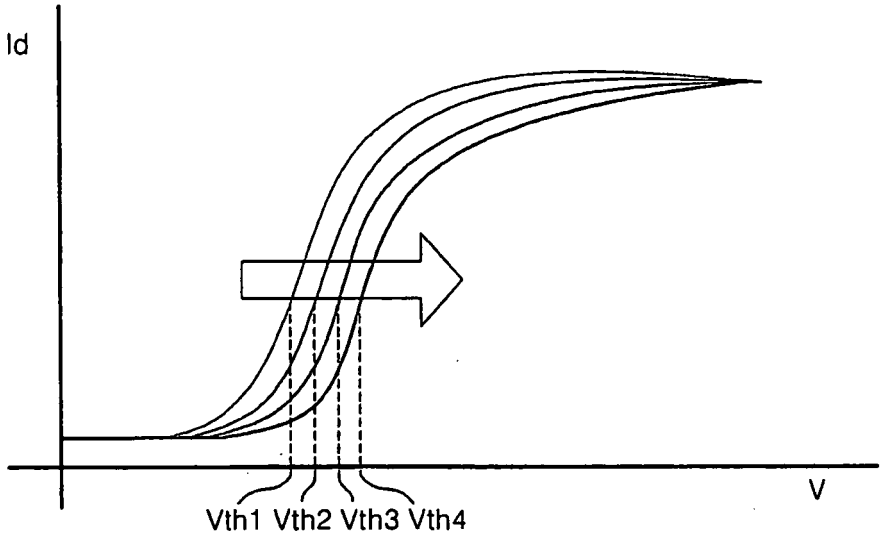


FIG. 4

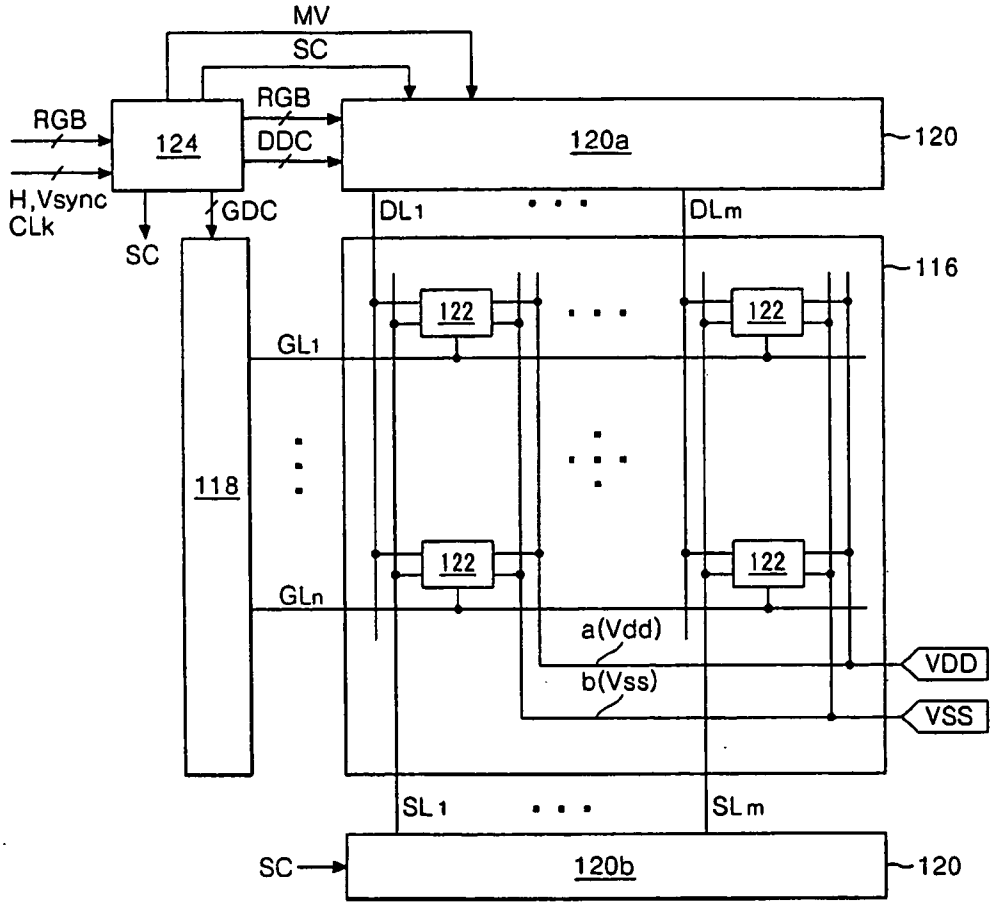

MV
SC
RGB
RGB
124
DDC
120a
120
H,Vsync
CLk
SC
GDC
DL1
DLm
116
122
GL1
118
GLn
a(Vdd)
b(Vss)
VDD
VSS
SL1
SLm
SC
120b
120

FIG. 5

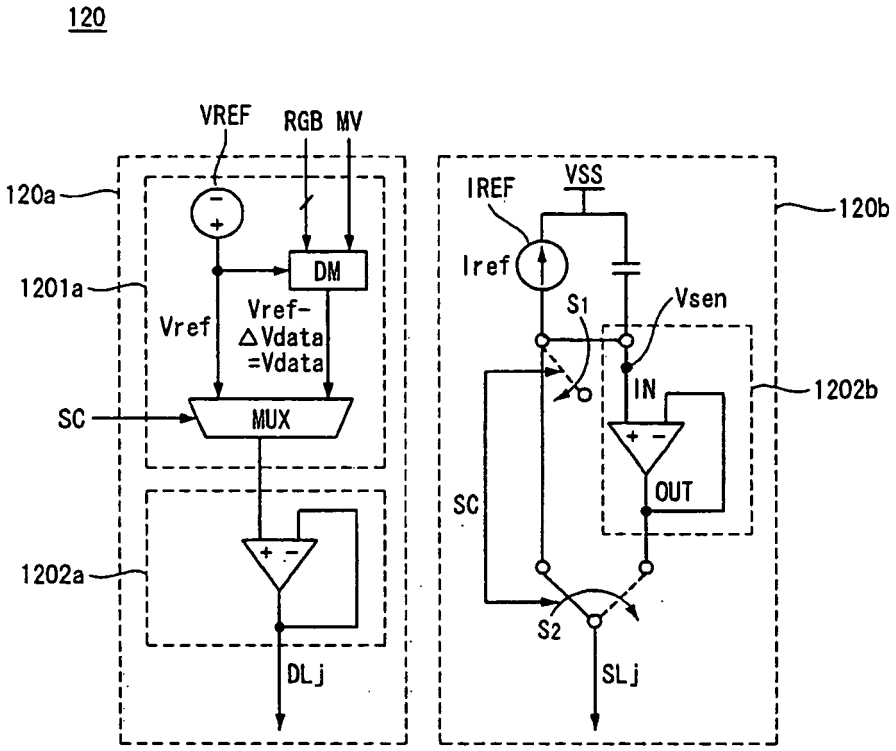

120
VREF
RGB MV
120a
1201a
DM
Vref
Vref-
ΔVdata
=Vdata
SC
MUX
1202a
DLj
IREF
VSS
120b
Iref
S1
Vsen
IN
1202b
OUT
SC
S2
SLj

FIG. 6

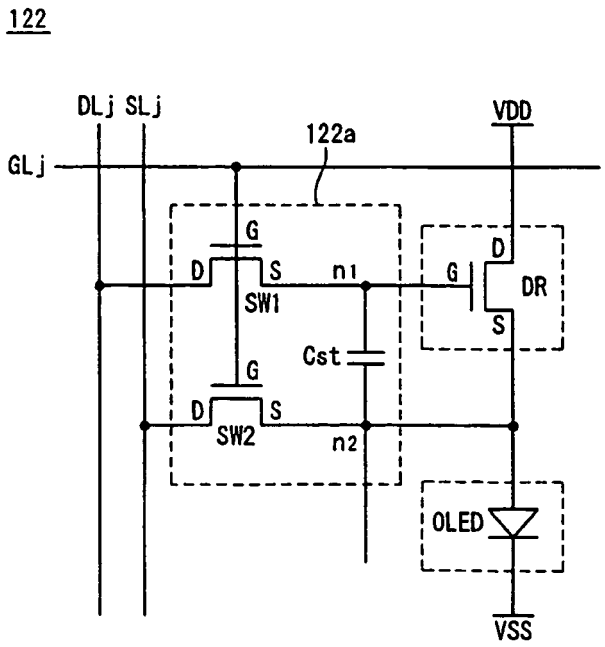

122
DLj SLj
VDD
122a
GLj
G
D
S
n1
SW1
G
DR
D
S
Cst
G
D
S
SW2
n2
OLED
VSS

FIG. 7

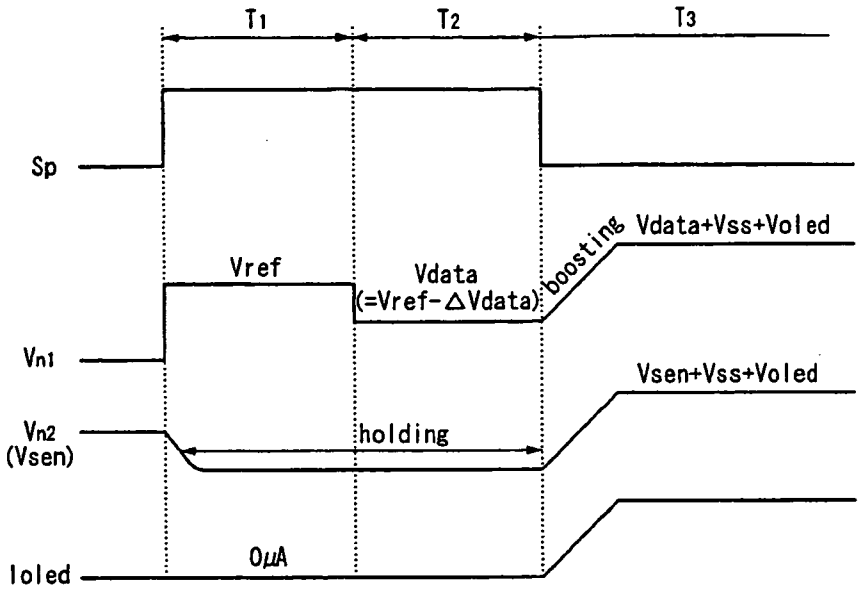

T1
T2
T3
Sp
Vref
Vdata
(=Vref-ΔVdata)
boosting
Vdata+Vss+Voled
Vn1
Vsen+Vss+Voled
Vn2
(Vsen)
holding
0μA
Ioled

FIG. 8A

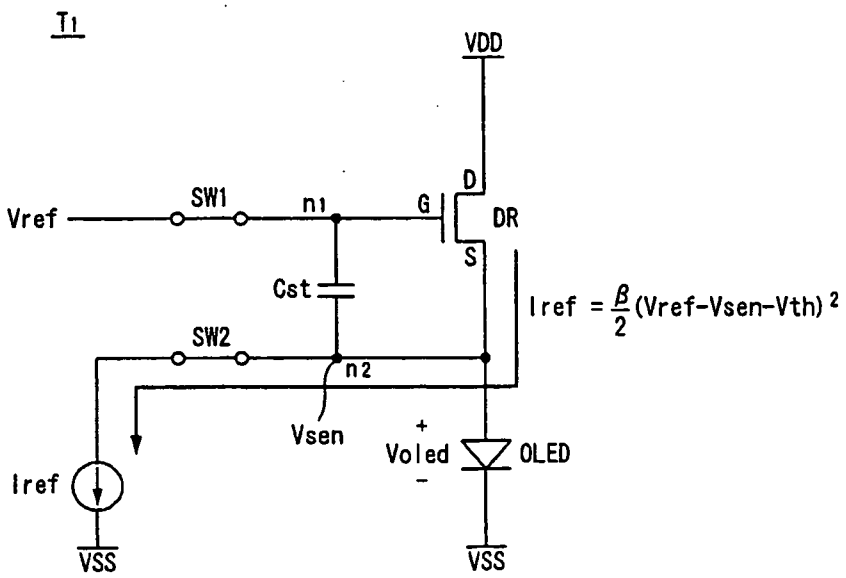

T1
VDD
D
Vref
SW1
n1
G
DR
S
Cst
Iref = β/2 (Vref-Vsen-Vth)²
SW2
n2
Vsen
+
Voled
-
OLED
Iref
VSS
VSS

FIG. 8B

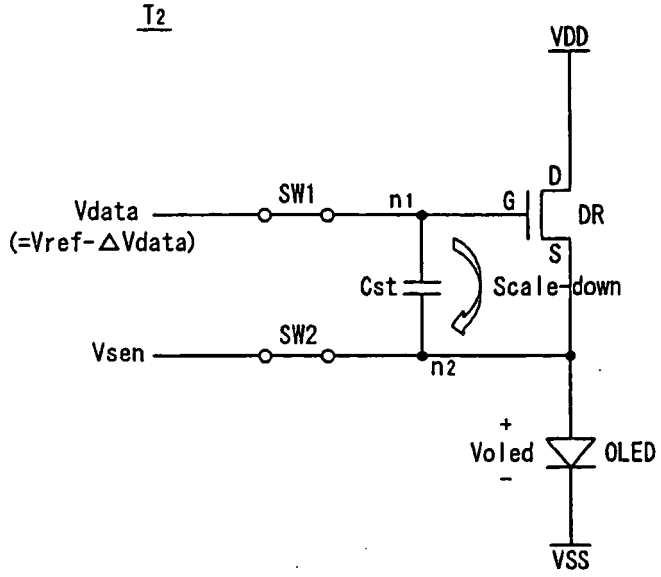

T2
VDD
D
Vdata
(=Vref-ΔVdata)
SW1
n1
G
DR
S
Cst
Scale-down
Vsen
SW2
n2
+
Voled
-
OLED
VSS

FIG. 8C

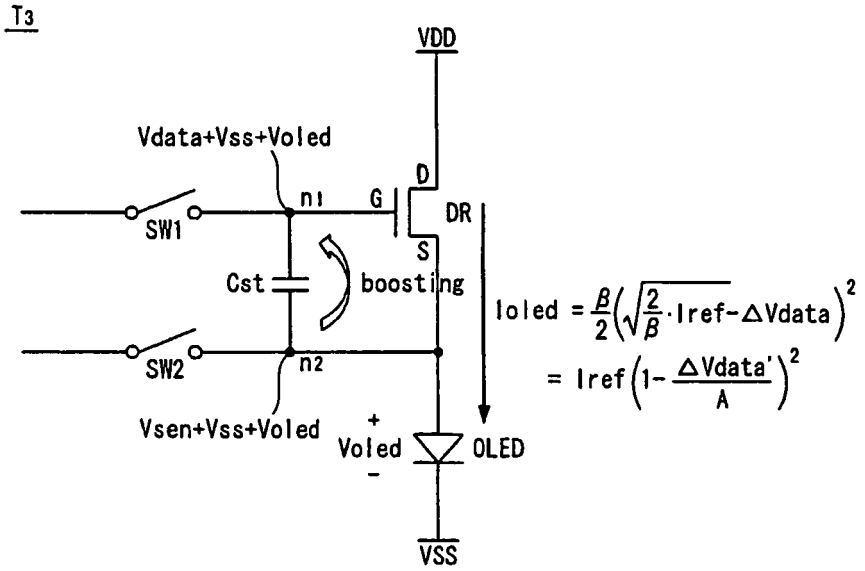
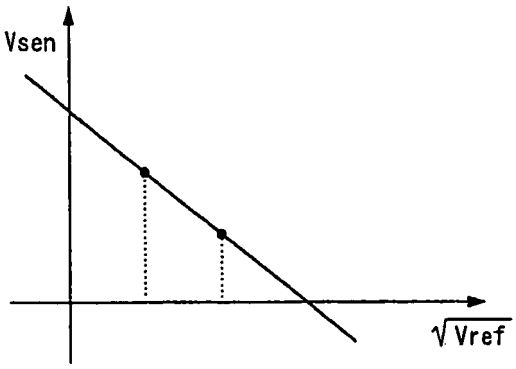

T3
VDD
Vdata+Vss+Voled
D
n1
G
DR
SW1
S
Cst
boosting
SW2
n2
Vsen+Vss+Voled
+
Voled
-
OLED
VSS
Ioled = β/2 (√(2/β)·Iref-ΔVdata)^2
= Iref (1- ΔVdata'/A)^2

FIG. 9



REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- WO 2006053424 A1 **[0014]**
- WO 2005015530 A1 **[0015]**

专利名称(译)	有机发光二极管显示器及其驱动方法		
公开(公告)号	EP2093749B1	公开(公告)日	2015-10-28
申请号	EP2008016568	申请日	2008-09-19
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	NAM WOOJIN		
发明人	NAM, WOOJIN		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G3/3291 G09G2300/0819 G09G2300/0842 G09G2310/0251 G09G2310/0262 G09G2320/0295		
优先权	1020080016503 2008-02-22 KR		
其他公开文献	EP2093749A3 EP2093749A2		
外部链接	Espacenet		

摘要(译)

有机发光二极管显示器包括数据线，与数据线交叉以接收扫描脉冲的栅极线，用于产生高电位驱动电压的高电位驱动电压源，用于产生低电位的低电位驱动电压源驱动电压，由于在高电位驱动电压源和低电位驱动电压源之间流动的电流而发光的发光元件，连接在高电位驱动电压源和发光元件之间的驱动元件以控制电流根据驱动元件的栅电极和源电极之间的电压在发光元件中流动，以及驱动电流稳定电路，以将第一电压施加到驱动元件的栅电极以接通驱动元件并且通过驱动元件吸收参考电流，以将驱动元件的源电压设置在感测电压并修改vo在驱动元件的栅极和源极之间的电流，以从参考电流缩放要施加到发光元件的电流。

$$Vgs = Vg - Vs$$

$$Vg = Vdata, \quad Vs = Vss$$

$$Ioled = \frac{\beta}{2}(Vgs - Vth)^2 = \frac{\beta}{2}(Vdata - Vss - Vth)^2$$