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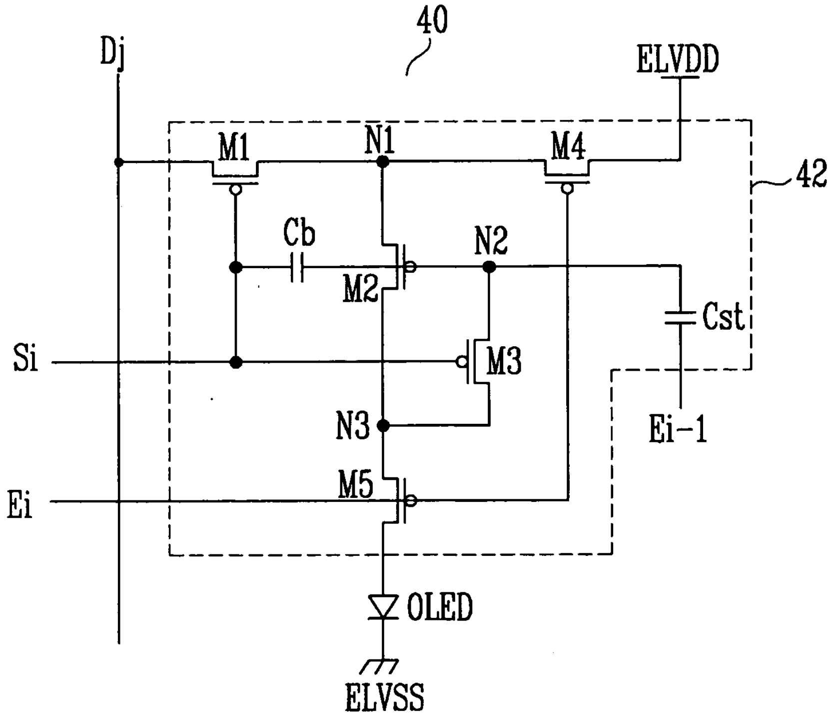
(54) **Pixel, organic light emitting display using the same, and associated methods**

(57) A display includes a pixel having an organic light emitting diode, a first transistor controlling a connection between a data line and a first node, a second transistor controlling a connection between the first node and a third node, a third transistor controlling a connection between the second node and the third node, a fourth transistor controlling a connection between a first power source and the first node, a fifth transistor controlling a connection between the third node and the organic light emitting diode, a storage capacitor coupled between an i-1[th] light emitting control line and the second node, and a boosting capacitor coupled between the i[th] scan line and the second node.

FIG. 3



EP 1 981 019 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] Embodiments relate to a pixel, an organic light emitting display using the same, and associated methods, which compensate for deterioration of a drive transistor.

2. Description of the Related Art

[0002] In the manufacture and operation of a display, e.g., a display used to reproduce text, images, video, etc., uniform operation of pixel elements of the display is highly desirable. However, providing such uniform operation may be difficult. For example, in some display technologies, e.g., those utilizing electroluminescent structures such as organic light emitting diodes (OLEDs), operational characteristics of the pixel elements may change over time. Accordingly, there is a need for a display adapted to compensate for changes in the operational characteristics of pixel elements.

SUMMARY OF THE INVENTION

[0003] Accordingly, the present invention aims to solve such drawbacks of the prior art, and therefore an object of the present invention is to provide an organic light emitting display capable of improving deterioration characteristics of a drive transistor and simultaneously displaying an image having a desired grey level, and a driving method of an organic light emitting display.

[0004] One embodiment of the present invention is achieved by providing an organic light emitting display including a scan driver for sequentially supplying a scan signal to scan lines and sequentially supplying a light emitting control signal to light emitting control lines; a data driver for supplying a data signal to data lines; and pixels arranged in crossing points of the scan lines, the data lines and the light emitting control lines, wherein each of the pixels includes an organic light emitting diode; a second transistor for controlling an electric current capacity supplied to the organic light emitting diode; a storage capacitor coupled between an i-1th (i is an integer) light emitting control line and a gate electrode of the second transistor; a first transistor coupled between an ith scan line, a data line and a first electrode of the second transistor and turned on when a scan signal is supplied to the ith scan line; and a third transistor coupled between a gate electrode and a second electrode of the second transistor and turned on when a scan signal is supplied to the ith scan line.

[0005] Preferably, each of the pixels further comprises a boosting capacitor coupled between the gate electrode of the second transistor and the ith scan line. Each of the pixels further includes a fourth transistor coupled between the second transistor and the first power source and turned on when the supply of a light emitting control signal to an ith light emitting control line is suspended; and a fifth transistor coupled between the second electrode of the second transistor and the organic light emitting diode and turned on when the supply of a light emitting control signal to the ith light emitting control line is suspended. The scan driver supplies a light emitting control signal supplied to the ith light emitting control line and a scan signal supplied to the i-1th scan line and the ith scan line so that the light emitting control signal can be overlapped with the scan signal. When a light emitting control signal is supplied to the i-1th light emitting control line, the i-1th light emitting control line is set to a higher voltage value than a voltage value supplied to the ith scan line when the supply of a scan signal to the ith scan line is suspended. The storage capacitor ha a higher capacity than the boosting capacitor.

[0006] Another embodiment of the present invention is achieved by providing a method for driving an organic light emitting display including pixels having a storage capacitor and coupled between a gate electrode of a drive transistor and an i-1th (i is an integer) light emitting control line, the method including: supplying a light emitting control signal to the i-1th light emitting control line to increase a voltage of a gate electrode of the drive transistor; suspending the supply of the light emitting control signal to the i-1th light emitting control line and simultaneously supplying a scan signal to an ith scan line to charge a voltage corresponding to a data signal and a threshold voltage of the drive transistor in the storage capacitor; and supplying to an organic light emitting diode an electric current corresponding to the voltage charged in the storage capacitor.

Preferably, the method for driving an organic light emitting display further includes: employing a boosting capacitor arranged between the ith scan line and a gate electrode of the drive transistor to increase a voltage of the gate electrode of the drive transistor when the supply of the scan signal to the ith scan line is suspended. When a light emitting control signal is supplied to the i-1th light emitting control line, the i-1th light emitting control line is set to a higher voltage value than a voltage value supplied to the ith scan line when the supply of a scan signal to the ith scan line is suspended. The storage capacitor is set to a higher capacity than the boosting capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The above and other features and advantages will become more apparent to those of ordinary skill in the art by describing in detail example embodiments with reference to the attached drawings, in which:

[0008] FIG. 1 illustrates a schematic diagram of an organic light emitting display according to an embodiment;

[0009] FIG. 2 illustrates signal waveforms for scan and light emitting control signals supplied from a scan driver shown in FIG. 1; and

[0010] FIG. 3 illustrates a schematic circuit diagram of a pixel according to an embodiment.

DETAILED DESCRIPTION OF THE INVENTION

[0011] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0012] In the drawing figures, the dimensions of layers and regions may be exaggerated, or elements may be omitted, for clarity of illustration. It will also be understood that when a layer or element is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being "under" another layer, it can be directly under, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present.

[0013] Similarly, where an element is described as being coupled to a second element, the element may be directly coupled to the second element, or may be indirectly coupled to the second element via one or more other elements. Further, where an element is described as being coupled to a second element, it will be understood that the elements may be electrically coupled, e.g., in the case of transistors, capacitors, power sources, nodes, etc. Where two or more elements are described as being coupled to a node, the elements may be directly coupled to the node, or may be coupled via conductive features to which the node is common. Thus, where embodiments are described or illustrated as having two or more elements that are coupled at a common point, it will be appreciated that the elements may be coupled at respective points on a conductive feature that extends between the respective points. Like reference numerals refer to like elements throughout.

[0014] As used herein, in the context of PMOS transistors, when a scan signal is described as being supplied, the scan signal has a LOW polarity, and when the scan signal is described as being stopped, the scan signal has a HIGH polarity. Further, when a light emitting control signal is described as being supplied, the light emitting control signal has a HIGH polarity, and when the light emitting control signal is described as being stopped, the light emitting control signal has a LOW polarity. When signals are described as overlapping at least a portion of the signals are concurrently supplied.

[0015] An organic light emitting display according to embodiments may generate light using an organic light emitting diode, which emits light corresponding to an amount of electric current supplied from a drive transistor. The drive transistor may deteriorate over time, however. Accordingly, an organic light emitting display according to embodiments may compensate for deterioration of a drive transistor by increasing a voltage of the gate electrode of the drive transistor during a portion of one frame. In particular, the organic light emitting display may compensate for deteriorated characteristics of the drive transistor by applying a high voltage to the gate electrode of the drive transistor during a portion of one frame.

[0016] An organic light emitting display according to embodiments may also display an image having a desired grey level by increasing a voltage of a node that is coupled to a gate electrode of the drive transistor using a boosting capacitor. In contrast, a conventional display may not display an image with a desired grey level, e.g., a black grey level, when the data signal is charged in a parasitic capacitor present in the data line, and is then supplied to a storage capacitor. Thus, in the conventional organic light emitting display, a voltage that is lower than a desired voltage may be stored in the storage capacitor due to charge sharing between the parasitic capacitor in the data line and the storage capacitor. This may prevent the conventional organic light emitting display from displaying an image having a desired grey level.

[0017] FIG. 1 illustrates a schematic diagram of an organic light emitting display 100 according to an embodiment. Referring to FIG. 1, the organic light emitting display 100 includes a pixel unit 30 including pixels 40 formed at crossing points of scan lines S1 to Sn, data lines D 1 to Dm, and light emitting control lines E 1 to En. The display 100 further includes a scan driver 10 for driving the scan lines S 1 to Sn and the light emitting control lines E 1 to En, a data driver 20 for driving the data lines D 1 to Dm, and a timing controller 50 for controlling the scan driver 10 and the data driver 20.

[0018] The scan driver 10 generates a scan signal in response to a scan drive control signal SCS supplied from the timing controller 50, and sequentially supplies the generated scan signal to the scan lines S1 to Sn. The scan driver 10 generates a HIGH light emitting control signal in response to the scan drive control signals SCS, and sequentially supplies the generated HIGH light emitting control signal to the light emitting control lines E1 to En.

[0019] The scan driver 10 sequentially supplies a HIGH light emitting control signal to an i-1th light emitting control line Ei-1 (i is a natural number from 1 to n, inclusive) and an ith light emitting control line Ei, and sequentially supplies a LOW scan signal to an i-1th scan line Si-1 and an ith scan line Si. The light emitting control signal may overlap the scan signal, such that the light emitting control signal is HIGH while the scan signal is LOW, as shown in FIG. 2.

[0020] The data driver 20 generates data signals in response to a data drive control signal DCS supplied from the timing controller 50, and supplies the generated data signals to the data lines D1 to Dm. During each horizontal period 1H, the data driver 20 supplies a data signal of one line to the data lines D1 to Dm.

[0021] The timing controller 50 generates the data drive control signal DCS and the scan drive control signal SCS in correspondence with externally-supplied synchronizing signals. The data drive control signal DCS generated in the timing controller 50 is supplied to the data driver 20, and the scan drive control signal SCS is supplied to the scan driver 10. The timing controller 50 rearranges data DATA supplied from an external source, and supplies the rearranged data DATA to the data driver 20.

[0022] The pixel unit 30 receives power from a first power source ELVDD and a second power source ELVSS. The first and second power sources ELVDD and ELVSS may be external to the pixel unit 30. The pixel unit 30 supplies the power from the first and second power sources ELVDD and ELVSS to each of the pixels 40.

[0023] The pixels 40 receives power from the first and second power sources ELVDD and ELVSS, and controls an amount of electric current flowing therebetween in correspondence with the data signal. The electric current controlled by the pixels 40 flows from the first power source ELVDD to the second power source ELVSS via respective organic light emitting diodes OLEDs in the pixels 40. A light emission time of the pixels 40 may be controlled by the light emitting control signal.

[0024] For an i^{th} horizontal line, pixels 40 arranged in the i^{th} horizontal line are coupled to the i^{th} scan line Si, the $i\text{-}1^{th}$ light emitting control line Ei-1, and the i^{th} light emitting control line Ei. In an implementation (not shown), pixels 40 arranged in the first horizontal line may be coupled to a 0^{th} light emitting control line E0.

[0025] FIG. 3 illustrates a schematic circuit diagram of a pixel 40 according to an embodiment. In FIG. 3, an example pixel 40 is coupled to the i^{th} scan line Si, a j^{th} data line Dj (j is a natural number from 1 to m, inclusive), the $i\text{-}1^{th}$ light emitting control line Ei-1, and the i^{th} light emitting control line Ei.

[0026] Referring to FIG. 3, the pixel 40 includes an organic light emitting diode OLED and a pixel circuit 42 for controlling an amount of electric current supplied to the organic light emitting diode OLED. The pixel circuit 42 controls the amount of electric current supplied to the organic light emitting diode OLED in correspondence with the data signal supplied to the data line Dj when a scan signal is supplied to the scan line Si. The organic light emitting diode OLED generates light having a predetermined luminance in correspondence with the electric current supplied from the pixel circuit 42. The organic light emitting diode OLED generates a color, e.g., one of red, green, or blue.

[0027] An anode electrode of the organic light emitting diode OLED is coupled to the pixel circuit 42, and a cathode electrode of the organic light emitting diode OLED is coupled to the second power source ELVSS. The second power source ELVSS is set to a lower voltage than that of the first power source ELVDD.

[0028] The pixel circuit 42 includes first to fifth transistors M1 to M5, a storage capacitor Cst, and a boosting capacitor Cb. A first electrode of the first transistor M1 is coupled to the data line Dj, and a second electrode of the first transistor M1 is coupled to a first electrode of the second transistor M2 via a first node N1. A gate electrode of the first transistor M1 is coupled to the scan line Si. The first transistor M1 may be turned on when a LOW scan signal is supplied to the scan line Si. The first transistor M1 may provide the data signal from the data line Dj to the first electrode of the second transistor M2 via the first node N1.

[0029] The first electrode of the second transistor M2 is coupled to the second electrode of the first transistor M1 via the first node N1, and a second electrode of the second transistor M2 is coupled to a first electrode of the fifth transistor M5 via a third node N3. A gate electrode of the second transistor M2 is coupled to a second node N2. The second transistor M2 may supply an electric current to the organic light emitting diode OLED, the electric current corresponding to a voltage applied to the second node N2.

[0030] A first electrode of the third transistor M3 is coupled to the second electrode of the second transistor M2 via the third node N3, and a second electrode of the third transistor M3 is coupled to the second node N2. Thus, the third transistor M3 may be configured to diode-connect the second transistor M2. A gate electrode of the third transistor M3 is coupled to the scan line Si. The third transistor M3 is turned on when a LOW scan signal is supplied to the scan line Si.

[0031] A first electrode of the fourth transistor M4 is coupled to the first power source ELVDD. A second electrode of the fourth transistor M4 is coupled to the first node N1, such that the second electrode of the fourth transistor M4 is coupled to the first electrode of the second transistor M2 as well as the second electrode of the first transistor M1. A gate electrode of the fourth transistor M4 is coupled to the i^{th} light emitting control line Ei. The fourth transistor M4 may be turned on when a HIGH light emitting control signal is not supplied, i.e., it may be turned on by a LOW signal. The fourth transistor M4 couples the first electrode of the second transistor M2 to the first power source ELVDD via the first node N1.

[0032] The first electrode of the fifth transistor M5 is coupled to the second electrode of the second transistor M2 via the third node N3, and a second electrode of the fifth transistor M5 may be coupled to the anode electrode of the organic light emitting diode OLED. A gate electrode of fifth transistor M5 may be coupled to the i^{th} light emitting control line Ei. The fifth transistor M5 may be turned on when a HIGH light emitting control signal is not supplied, i.e., it may be turned on by a LOW signal. The fifth transistor M5 couples the organic light emitting diode OLED to the second electrode of the second transistor M2 via the third node N3.

[0033] The storage capacitor Cst is coupled between the second node N2 and the $i\text{-}1^{th}$ light emitting control line Ei-1. The storage capacitor Cst may charge a voltage corresponding to the data signal. The storage capacitor Cst may transmit an amount of changed voltage of the i-1^{th} light emitting control line Ei-1 to the second node N2, as described in more detail below.

[0034] The boosting capacitor Cb is coupled between the scan line Si and the second node N2. The boosting capacitor Cb may increase a voltage of the second node N2 when the supply of the scan signal to the scan line Si stops, i.e., when the scan signal goes HIGH.

[0035] Operation of the organic light emitting display will now be described in more detail with reference to FIGS. 2 and 3. Referring to FIGS. 2 and 3, a HIGH light emitting control signal may be supplied to the i-1^{th} light emitting control line Ei-1 at the start of a first period T1, such that a voltage of the second node N2 set to a floating state is increased.

[0036] As the voltage of the second node N2 is increased, a voltage of the gate electrode of the second transistor M2 increases. Therefore, deteriorated characteristics of the second transistor M2 may be improved. For example, deterioration of the second transistor M2 may be compensated if a reverse bias voltage is applied to the second transistor M2 during a period of one frame, e.g., a period when the light emitting control signal is supplied to the i-1^{th} light emitting control line Ei-1.

[0037] Referring to FIG. 2, the scan signal may have a fourth voltage V4, and the light emitting control signal may have a third voltage V3. The third voltage V3 may be set to a higher voltage than the fourth voltage V4. For example, the third voltage V3 may have a value that is higher than the sum of the fourth voltage V4 and the threshold voltage of the third transistor M3. Thus, the third transistor M3 may be turned on when a HIGH light emitting control signal is supplied to the i-1^{th} light emitting control line En-1.

[0038] During the first period T1, a reverse bias voltage of the second transistor M2 is applied, and the third transistor M3 is turned on simultaneously. When the third transistor M3 is turned on, a voltage applied to the second node N2 during a prior period is reset via the third transistor M3, the fifth transistor M5, and the organic light emitting diode OLED.

[0039] At the start of a second period T2, a HIGH light emitting control signal is supplied to the i^{th} light emitting control line Ei, such that the fourth transistor M4 and the fifth transistor M5 are turned off.

[0040] At the start of a third period T3, the supply of the HIGH light emitting control signal to the i-1^{th} light emitting control line Ei-1 stops. During the third period T3, the scan signal is supplied to the scan line Si. When the scan signal is supplied to the scan line Si, the first transistor M1 and the third transistor M3 are turned on. When the first transistor M1 is turned on, a data signal is supplied from the data line Dj to the first electrode of the second transistor M2 via the first transistor M1. At this time, the second transistor M2 is turned on, since the voltage of the second node N2 may be reset during the first period T1. When the second transistor M2 is turned on, the data signal is supplied to the second node N2 via the second transistor M2 and the third transistor M3. At this time, the storage capacitor Cst charges a voltage corresponding to the data signal and the threshold voltage of the second transistor M2. The voltage value of the data signal may be determined experimentally and set to stably control a channel width of the second transistor M2.

[0041] At the end of the third period T3, the supply of a LOW scan signal to the scan line Si may stop. When the supply of the light emitting control signal to the i-1^{th} light emitting control line Ei-1 stops, a voltage of the second node N2 may decrease.

[0042] During a fourth period T4, the LOW scan signal is not supplied to the scan line Si, and the supply of the HIGH light emitting control signal to the i^{th} light emitting control line Ei may stop. When the supply of the LOW scan signal to the scan line Si stops, a voltage of the scan line Si increases from the LOW voltage to the fourth voltage V4. The voltage of the second node N2 may also be increased to a predetermined voltage by the boosting capacitor Cb, in correspondence with an amount of increased voltage of the scan line Si, as described in detail below. When the voltage of the second node N2 is increased, an image may be displayed with a desired grey level. In particular, an image having a desired grey level may be displayed by increasing a voltage of the second node N2 by as much as a voltage lost from charge sharing of a parasitic capacitor and a storage capacitor Cst of the data line Dj.

[0043] The amount of increased voltage of the second node N2 may be determined according to the amount of the increased voltage of the scan line Si, and according to the capacities of the boosting capacitor Cb and the storage capacitor Cst. The capacity of the storage capacitor Cst may be set to be higher than that of the boosting capacitor Cb. Accordingly, the voltage of the second node N2 may be increased as much as the voltage of the data signal that is lost to charge sharing.

[0044] When the supply of the HIGH light emitting control signal to the i^{th} light emitting control line Ei stops during the fourth period T4, the fourth transistor M4 and the fifth transistor M5 are turned on. At this time, the second transistor M2 supplies an electric current from the first power source ELVDD to the organic light emitting diode OLED via the fourth transistor M4 and the fifth transistor M5, where the amount of the electric current corresponds to the voltage applied to the second node N2. Thus, light having a predetermined luminance may be generated by the organic light emitting diode OLED.

[0045] Exemplary embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. For example, the first to fifth transistors M1 to M5 are shown as PMOS type transistors in FIG. 3, but it will be understood that the first to fifth transistors M1 to M5 may be implemented as NMOS type transistors, in which this case they may be driven with waveforms having a reversed polarity. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. An organic light emitting display, comprising:

a scan driver for sequentially supplying a scan signal to scan lines and for sequentially supplying a light emitting control signal to light emitting control lines;
a data driver for supplying a data signal to data lines; and
pixels arranged in crossing points of the scan lines, the data lines and the light emitting control lines,
wherein each of the pixels comprises:

an organic light emitting diode;
a second transistor for controlling an amount of electric current supplied to the organic light emitting diode;
a storage capacitor coupled between an i-1th light emitting control line and a gate electrode of the second transistor, where i is an integer;
a first transistor coupled between a data line and a first electrode of the second transistor and connected to an ith scan line and arranged to be turned on when a scan signal is supplied to the ith scan line; and
a third transistor coupled between a gate electrode and a second electrode of the second transistor and arranged to be turned on when a scan signal is supplied to the ith scan line.

2. An organic light emitting display according to claim 1, wherein each of the pixels further comprises a boosting capacitor coupled between the gate electrode of the second transistor and the ith scan line.

3. An organic light emitting display according to claim 2, wherein each of the pixels further comprises;

a fourth transistor coupled between the second transistor and the first power source and arranged to be turned on when the supply of a light emitting control signal to an ith light emitting control line is suspended; and
a fifth transistor coupled between the second electrode of the second transistor and the organic light emitting diode and arranged to be turned on when the supply of a light emitting control signal to the ith light emitting control line is suspended.

4. An organic light emitting display according to any one of claims 1 to 3, wherein the scan driver is arranged to supply a light emitting control signal to the ith light emitting control line and to supply a scan signal to the i-1th scan line and the ith scan line so that the light emitting control signal is overlapped with the scan signal.

5. An organic light emitting display according to any one of claims 1 to 4, wherein, when a light emitting control signal is supplied to the i-1th light emitting control line, the i-1th light emitting control line is set to a higher voltage value than a voltage value supplied to the ith scan line when the supply of a scan signal to the ith scan line is suspended.

6. An organic light emitting display according to claim 2 or any claim dependent on claim 2, wherein the storage capacitor is set to a higher capacity than the boosting capacitor.

7. A method for driving an organic light emitting display including pixels having a storage capacitor and coupled between a gate electrode of a drive transistor and an i-1th light emitting control line, where i is an integer, the method comprising:

supplying a light emitting control signal to the i-1th light emitting control line to increase a voltage of a gate electrode of the drive transistor;
suspending the supply of the light emitting control signal to the i-1th light emitting control line and simultaneously supplying a scan signal to an ith scan line to charge a voltage corresponding to a data signal and a threshold voltage of the drive transistor in the storage capacitor; and
supplying to an organic light emitting diode an electric current corresponding to the voltage charged in the storage capacitor.

8. A method for driving an organic light emitting display according to claim 7, further comprising: employing a boosting capacitor arranged between the ith scan line and a gate electrode of the drive transistor to increase a voltage of the gate electrode of the drive transistor when the supply of the scan signal to the ith scan line is suspended.

9. A method for driving an organic light emitting display according to claim 7 or 8, wherein, when a light emitting control signal is supplied to the i-1th light emitting control line, the i-1th light emitting control line is set to a higher voltage value than a voltage value supplied to the i^{th} scan line when the supply of a scan signal to the i^{th} scan line is suspended.

10. A method for driving an organic light emitting display according to claim 8 or claim 9 when dependent on claim 8, wherein the storage capacitor is set to a higher capacity than the boosting capacitor.

FIG. 1

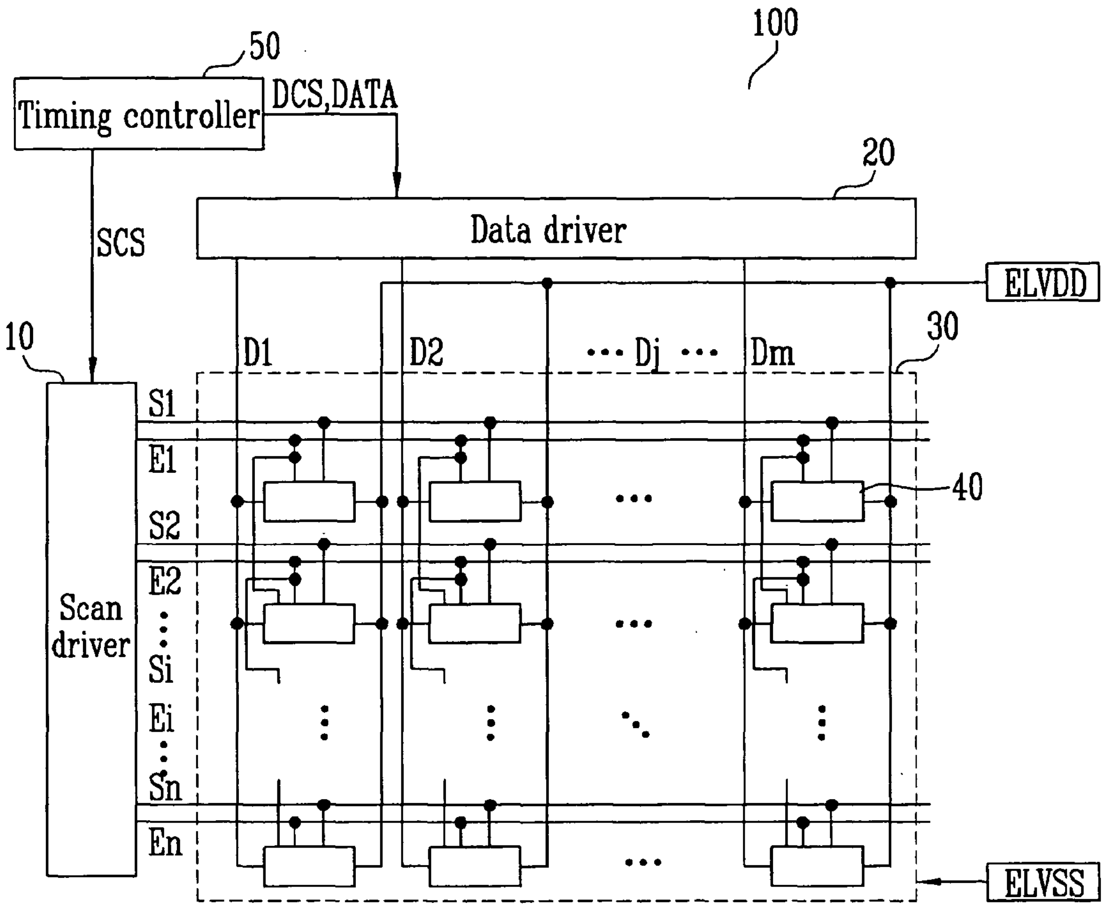

50
Timing controller
DCS,DATA
100
20
Data driver
SCS
ELVDD
10
30
D1
D2
··· Dj ···
Dm
S1
E1
40
S2
E2
Scan driver
Si
Ei
Sn
En
ELVSS

FIG. 2

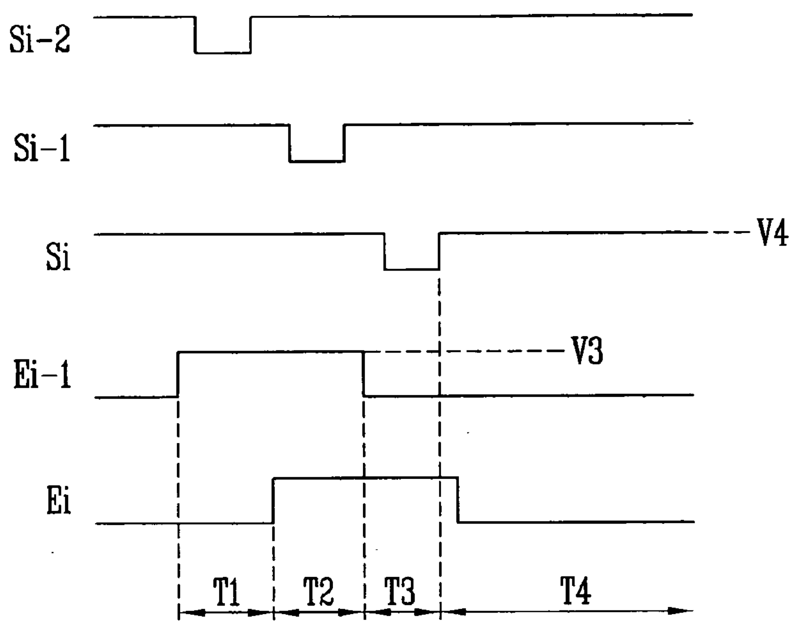
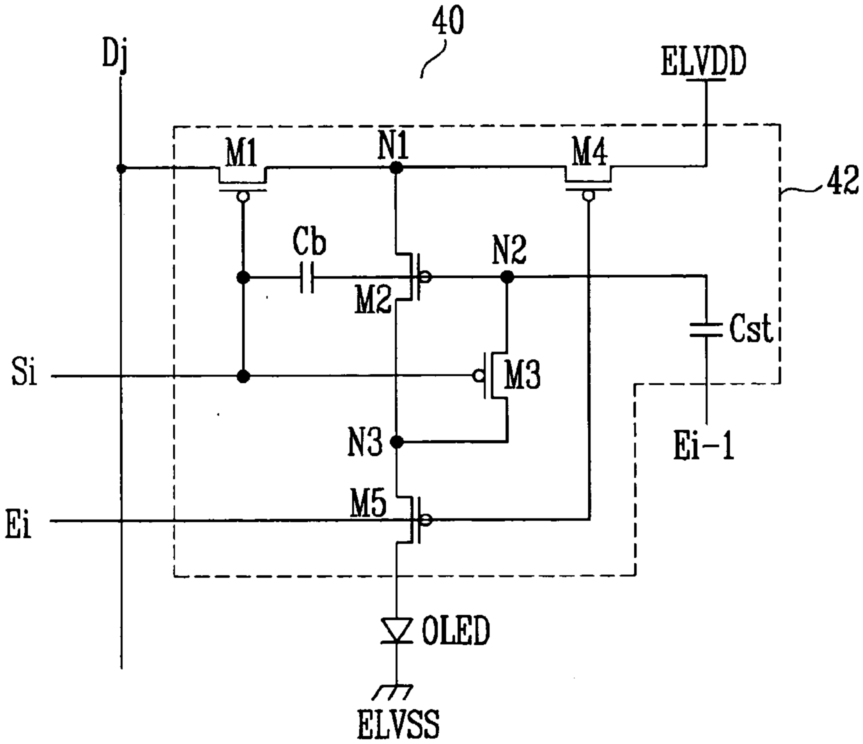

Si-2
Si-1
Si
V4
Ei-1
V3
Ei
T1
T2
T3
T4

FIG. 3


40
Dj
ELVDD
M1
N1
M4
42
Cb
N2
M2
Cst
Si
M3
N3
Ei-1
M5
Ei
OLED
ELVSS

专利名称(译)	像素，使用其的有机发光显示器以及相关方法		
公开(公告)号	EP1981019A2	公开(公告)日	2008-10-15
申请号	EP2008251393	申请日	2008-04-10
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摘要(译)

显示器包括具有有机发光二极管的像素，控制数据线和第一节点之间的连接的第一晶体管，控制第一节点和第三节点之间的连接的第二晶体管，控制第一节点和第三节点之间的连接的第三晶体管。第二节点和第三节点，控制第一电源和第一节点之间的连接的第四晶体管，控制第三节点和有机发光二极管之间的连接的第五晶体管，耦合在第i-1个灯之间的存储电容器发射控制线和第二节点，以及耦合在第i扫描线和第二节点之间的升压电容器。

FIG. 3