(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 944 816 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
16.07.2008 Bulletin 2008/29

(51) Int Cl.:
H01L 51/00 *(2006.01)*

(21) Application number: **07253273.2**

(22) Date of filing: **20.08.2007**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC MT NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR MK RS

(30) Priority: **18.08.2006 KR 20060078063**

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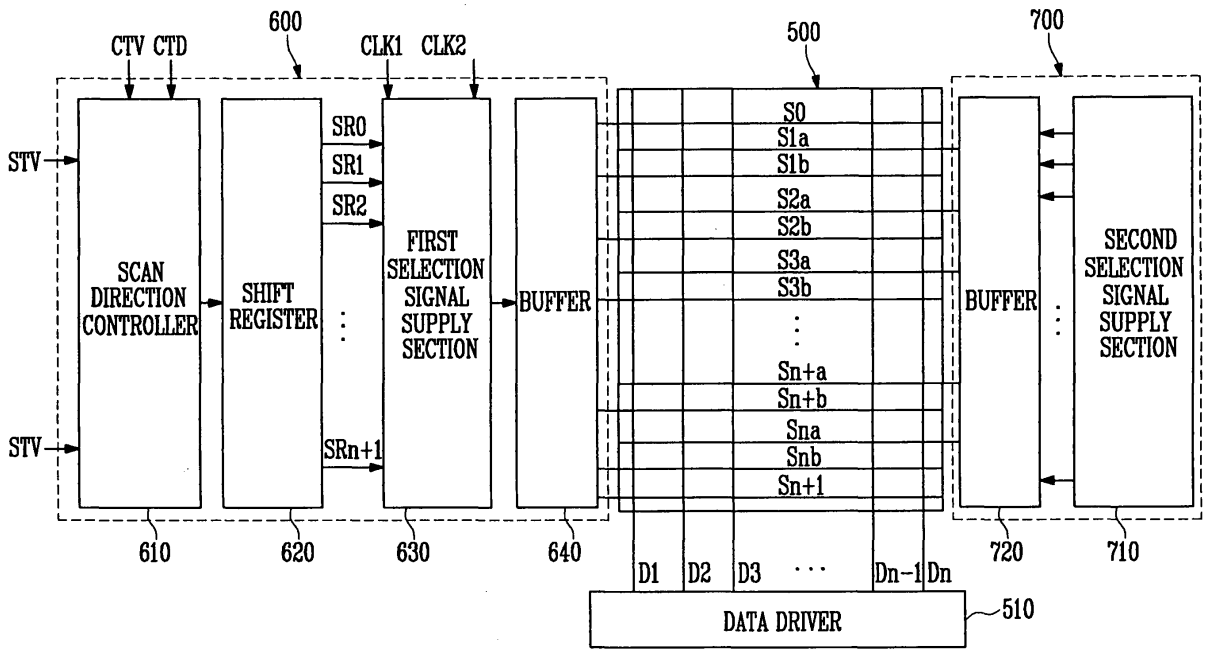
(54) Organic light emitting display

(57) An organic light emitting display operates on at least two different selection signals, which may perform a bi-directional scan that allows a double-sided screen to be displayed. The organic light emitting display includes a data line, first and second scan lines, a bi-directional data driver for applying a data signal in both directions, a first scan driver adapted to receive a forward or reverse signal and to selectively output a first selection signal having a forward or reverse direction to the first scan line in accordance with the forward or reverse signal, and a second scan driver adapted to receive the first selection signal and to selectively output a second selection signal of a forward or reverse direction to the second scan line in accordance with the forward or reverse signal.

FIG. 5



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to an organic light emitting display. More particularly, the present invention relates to an organic light emitting display capable of changing a display direction so as to permit a double-sided display.

2. Description of the Related Art

[0002] In general, an organic light emitting display electrically excites an organic phosphor to emit light by using voltage or current to drive M×M organic emitting cells arranged in an array to display images.

[0003] Since such an organic emitting cell has diode characteristics, it may be referred to as an organic light emitting diode (OLED). As shown in FIG. 1, an organic emitting cell includes an anode of indium tin oxide (ITO), an organic thin film, and a cathode layer. The organic thin film may have a multi-layer structure including an emitting layer (EML), an electron transport layer (ETL), and a hole transport layer (HTL) for maintaining balance between electrons and holes and for improving emitting efficiencies. The organic thin film may further include an electron injection layer (EIL) and a hole injecting layer (HIL). Additionally a metal cathode may be present.

[0004] FIG. 2 illustrates a partial perspective view schematically depicting an OLED capable of providing a double-sided display. The OLED includes a first transparent electrode 24, an emission layer 38, and a second transparent electrode 36, which are arranged between an upper transparent substrate 40 and a lower transparent substrate 22.

[0005] The first transparent electrode 24 includes an anode electrode formed on a lower glass substrate 22 by, e.g., vacuum-depositing or sputtering one of Indium-Tin-Oxide (ITO), Indium-Zinc-Oxide (IZO), or Indium-Tin-Zinc-Oxide (ITZO). The first transparent electrode 24 may used as a data electrode.

[0006] The emission layer 38 includes a hole injection layer 26, a hole transport layer 28, an organic emission layer 30, an electron transport layer 32, and an electron injection layer 34, which may be sequentially laminated on the first transparent electrode 24.

[0007] The second transparent electrode 36 is a cathode electrode formed on the emission layer 38 by, e.g., vacuum-deposition or sputtering one of ITO, IZO, or ITZO.

[0008] The first transparent electrode 24 and the second transparent electrode 36 may have differently set work functions according to a composition ratio of an oxide and O_2 plasma process. Accordingly, one of the work functions of the first transparent electrode 24 and the second transparent electrode 36 may be set lower than the other so that electrons and holes move. Owing to a difference between the work function of the first transparent electrode 24 and the work function of the second transparent electrode 36, the organic emission layer 38 may emit light using holes and electrons supplied from the first transparent electrode 24 and the second transparent electrode 36.

[0009] Visible light generated from the organic emission layer 30 may be discharged in both directions through the first and second transparent electrodes 24 and 36, and the upper and lower glass substrates 40 and 22. Accordingly, an electroluminescent (EL) device having a double-sided display function including the OLED may display an image in both front and rear directions.

[0010] FIG. 3 illustrates a schematic view of an organic light emitting display including the OLED shown in FIG. 2.

[0011] As shown in FIG. 3, the organic light emitting display includes an organic EL display panel 100, a scan driver 200, and a data driver 300.

[0012] The organic EL display panel 100 includes multiple data lines D1 to Dm, multiple scan lines S1 to Sn, and multiple pixel circuits 110. The data lines D1 to Dm are arranged in a row direction, and the of scan lines S1 to Sn are arranged in a column direction. The data lines D1 to Dm may transfer a data signal indicating an image signal to the pixel circuits 110. The scan lines S 1 to Sn may transfer a selection signal to the pixel circuits 110. Each of the pixel circuits 100 are formed at a pixel region, which is defined by two adjacent data lines D1 to Dm and two adjacent scan lines S1 to Sn. Hereinafter, a pixel coupled to a first scan line S1 is referred to as "P1", and a pixel coupled to an n-th scan line Sn is referred to as "Pn."

[0013] The scan driver 200 may sequentially apply the selection signal to the scan lines S1 to Sn, respectively. The data driver 300 may apply a data voltage corresponding to the image signal to the data lines D 1 to Dm.

[0014] The scan driver 200 and/or the data driver 300 may be electrically coupled to the organic EL display panel 100. Further, the scan driver 200 and/or the data driver 300 may be coupled to the organic EL display panel 100 and may be mounted on a tape carrier package (TCP) in a form of a chip, which may be electrically coupled thereto. Otherwise, the scan driver 200 and/or the data driver 300 may be coupled to the organic EL display panel 100 by mounting on a flexible printed circuit (FPC) or a film in a form of a chip, which may be electrically coupled thereto. In contrast to this, the scan driver 200 and/or the data driver 300 may be directly mounted on a glass substrate. Also, the scan driver 200

and/or the data driver 300 may be substituted by a driving circuit or may be directly mounted on the driving circuit, which may be formed on the same layer as that of the scan lines S1 to Sn, the data lines D1 to Dm, and a thin film transistor.

[0015] On the other hand, in an organic EL display having a double-sided display function, the left and right of the front screen and the rear screen are reversed. Thus, in order to match a screen displayed on a rear surface of a display device with a front surface thereof, a first data signal is applied to the first data line D1 in the front display and to the m-th data line Dm in the rear display. Further, an m-th data signal is applied to the m-th data line in the front display and to the first data line D1 in the rear display.

[0016] Similar to a rotation of 180 degrees, besides the left and the right of a screen in the display panel, when the top and the bottom of the display panel reverse, as in the data driver, a scan driver should include a bi-directional shift register, which applies a data signal in a bi-directional manner. In other words, an emission display device in which a display screen rotates at 180 degrees can use a bi-directional scan driver to display the screens before and after rotation to thus be equally displayed. In this case, the bi-directional scan driver applies a first selection signal to the first scan line S1 when the selection signal is sequentially applied from an upper side to a lower side (referred to as "forward scan" hereinafter), and to the n-th scan line Sn when the selection signal is sequentially applied from a lower side to an upper side (referred to as "reverse scan" hereinafter). Further, the bi-directional scan driver may apply an n-th selection signal to the n-th scan line Sn during the forward scan, and to the first scan line S1 during the reverse scan.

[0017] However, the pixel circuit may operate based on at least two different selection signals, e.g., an n-th selection signal applied to the current scan line Sn and an n-1-th selection signal applied to the previous scan line Sn-1. The aforementioned pixel circuit may have an arrangement structure, which may normally operate by applying the n-th selection signal to the n-th scan line Sn after an n-1-th selection signal was applied to an n-1-th scan line Sn-1 during the forward scan. In contrast, during the reverse scan, an applying direction of a scan line may be reversed. Accordingly, after the first selection signal has been applied to the n-th scan line Sn, a second selection signal may be applied to the n-1-th scan line Sn-1, so that the pixel circuit may fail to normally operate.

SUMMARY OF THE INVENTION

[0018] The present invention is therefore directed to an organic light emitting display including a pixel circuit operating based on at least two different selection signals, which substantially overcomes one or more of the problems due to the limitations and disadvantages of the related art.

[0019] It is therefore a feature of an embodiment of the present invention to provide a display, which may perform a bi-directional scan that allows a double-sided screen to be displayed.

[0020] According to an aspect of the invention, there is provided a driver for a display as set out in claim 1. Preferred features of this aspect are set out in claims 2 to 9.

[0021] According to a second aspect of the invention, there is provided a a display as set out in claim 10. Preferred features of this aspect are set out in claims 11 to 16.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The above and other features and advantages of the present invention will become more apparent to those of ordinary skill in the art as a result of the following description of exemplary embodiments thereof with reference to the attached drawings, in which:

[0023] FIG. 1 is a view of an OLED;

[0024] FIG. 2 is a partial perspective schematic view of an OLED capable of providing a double-sided display;

[0025] FIG. 3 is a schematic view of an organic light emitting display panel including the OLED in FIG. 2;

[0026] FIG. 4 is an equivalent circuit diagram showing a pixel circuit according to an embodiment of the present invention;

[0027] FIG. 5 is a block diagram of an organic light emitting display according to an embodiment of the present invention;

[0028] FIG. 6 is a detailed view of a construction of first and second scan drivers shown in FIG. 5;

[0029] FIG. 7 is a view of a forward driving operation of the first and second scan drivers shown in FIG. 6;

[0030] FIG. 8 is a timing chart of the forward driving operation of the first and second scan drivers shown in FIG. 6;

[0031] FIG. 9 is a view of a reverse driving operation of the first and second scan drivers shown in FIG. 6; and

[0032] FIG. 10 is a timing chart of the reverse driving operation of the first and second scan drivers shown in FIG. 6.

DETAILED DESCRIPTION OF THE INVENTION

[0033] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are illustrated. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are

provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0034] In the drawing figures, the dimensions of layers and regions may be exaggerated for clarity of illustration. It will also be understood that when a layer or element is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being "under" another layer, it can be directly under, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present. Like reference numerals refer to like elements throughout.

[0035] Hereinafter, exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when one element is coupled to another element, one element may be not only directly coupled to another element but also indirectly coupled to another element via another element. Further, some elements are omitted for clarity.

[0036] In accordance with embodiments of the present invention, an organic light emitting display, including a pixel circuit operating by employing at least two different selection signals, may be driven in both directions. In particular, in accordance with an embodiment of the present invention, a forward signal for controlling a forward scan sequentially applying a selection signal in a forward direction and a reverse signal for controlling a reverse scan sequentially applying a selection signal in a reverse direction, may be used as the selection signals.

[0037] FIG. 4 illustrates an equivalent circuit diagram of a pixel circuit according to an embodiment of the present invention. For convenience of description, FIG. 4 illustrates only a pixel circuit, which may be coupled to an m-th data line Dm and an n-th scan line Sn. As used herein, the term "current scan line" means a scan line to transfer a current selection signal, and the term "previous scan line" means a scan line to transfer a selection signal prior to transferring the current selection signal.

[0038] As shown in FIG. 4, the pixel circuit includes transistors M1 to M5, capacitors Cvth and Cst, and an OLED. A first transistor M1 may drive the OLED. The first transistor M1 is coupled between a power supply for supplying a voltage VDD to the OLED. The first transistor M1 controls an electric current flowing from the fifth transistor M5 to the OLED by a voltage applied to a gate thereto. The second transistor M2 connects the first transistor M1 in response to a selection signal from a previous scan line Sn-1.

[0039] An electrode A of the first capacitor Cvth is coupled to the gate of the first transistor M1. The second capacitor Cst is coupled in parallel between another electrode B of the first capacitor Cst and the power supply supplying the voltage VDD. The fourth transistor M4 supplies the voltage VDD from the power supply to the electrode B of the first capacitor Cvth in response to the selection signal from the previous scan line Sn-1.

[0040] The third transistor M3 transfers data from the data line Dm to the electrode B of the first capacitor Cvth in response to a selection signal from the scan line Sn. The fifth transistor M5 is coupled between a drain of the first transistor M1 and an anode of the OLED. The fifth transistor M5 can cut off a drain of the first transistor M1 and the OLED in response to the selection signal from the previous scan line Sn-1.

[0041] The OLED can emit light corresponding to an input electric current. A voltage VSS coupled to a cathode of the OLED has a level lower than that of the voltage VDD of the power supply. A ground voltage may be used as the voltage VSS.

[0042] Operation of the pixel circuit described above will now be explained.

[0043] First, when a low level scan voltage is applied to the previous scan line Sn-1, the third transistor M3 is turned on, so that the first transistor M1 may be diode-coupled. Accordingly, a voltage between a gate and a source of the first transistor M1 varies to reach to a threshold voltage VTH of the first transistor M1. At this time, because a source of the first transistor M1 is coupled to the power supply voltage VDD, a voltage is applied to a gate of the first transistor M1. Namely, the voltage at the first electrode A of the first capacitor Cvth becomes a sum of the power supply voltage VDD and the threshold voltage VTH. Further, the fourth transistor M4 is turned-on to apply the power supply voltage VDD to the second electrode B of the first capacitor Cvth, so that the first capacitor Cvth is charged with a voltage VCvth expressed by equation 1:

[0044]

$$VCvth = VCvthA - VCvthB = (VDD+VTH) - VDD = VTH \quad (1)$$

[0045] where VCvth represents a voltage charged in the first capacitor Cvth, VCvthA represents a voltage applied to the electrode A of the first capacitor Cvth, and VCvthB represents a voltage applied to the electrode B of the first capacitor Cvth.

[0046] Moreover, the second transistor M2 has an N-type channel in this embodiment. The second transistor M2 is cut off in response to a low level signal from the previous scan line Sn-1 to prevent an electric current flowing through the first transistor M1 to the OLED.

[0047] Next, when a low level scan voltage is applied to the current scan line Sn, the fifth transistor M5 is turned-on to apply a data voltage VDATA to the electrode B of the first capacitor Cvth. Further, since the first capacitor Cvth has been charged with a voltage corresponding to the threshold voltage VTH of the first transistor M1, a voltage corresponding to a sum of the data voltage VDATA and the threshold voltage VTH of the first transistor M1 isapplied to the gate of the first transistor M1. That is, a voltage VGS between the gate and the source of the first transistor M1 may be expressed by equation 2:

[0048]

$$VGS = (VDATA + VTH) - VDD \qquad (2)$$

[0049] Furthermore, the second transistor M2 is turned-on according to a high level of the current scan line Sn to supply an electric current to the OLED corresponding to a gate-source voltage of the first transistor M1 to the OLED, with the result that the OLED emits light. Here, an electric current I_{OLED} may be expressed by equation 3:

$$I_{OLED} = \frac{\beta}{2}(VGS - VTH)^2 = \frac{\beta}{2}\{(VDATA + VTH - VDD) - VTH\}^2 = \frac{\beta}{2}(VDD - VDATA)^2 \quad (3)$$

[0050] where, I_{OLED} is the electric current flowing through the OLED, V_{GS} is the voltage between the source and the gate of the first transistor M1, VTH is the threshold voltage of the first transistor M1, VDATA is the data voltage, and β is a constant.

[0051] While a scan signal is being applied to the previous scan line Sn-1, the second transistor M2 can be turned-off to prevent a leakage current from flowing and to express a substantially exact black gradation.

[0052] Up to now, an embodiment of the present invention has been described where five transistors and two capacitors are included in the pixel circuit. However, embodiments of the present invention are not limited to this configuration. Embodiments of the present invention are applicable to all pixel circuits, which operate by at least two selection signals.

[0053] FIG. 5 is a block diagram of an organic light emitting display according to an embodiment of the present invention. Here, multiple pixel circuits included in a display panel of FIG. 5 operate by at least two selection signals, as was described earlier with reference to FIG. 4.

[0054] With reference to FIG. 5, the organic light emitting display includes a display panel 500, a first scan driver 600, a second scan driver 700, and a data driver 510. The display panel 500 can display a normal screen or a screen rotated by about 180 degrees. NxM pixels (not shown) are arranged on the display panel 500 in an array. Hereinafter, an unspecified pixel is referred to as "Pk," where, k is a natural number from 1 to n. The pixel circuit is provided at an intersection of a pair of scan lines Ska and Skb and the data line Dm. One pixel Pk is electrically coupled to two scan lines Ska and Skb to which different selection signals are applied. In this case, in one pixel Pk, passive elements operating by the same selection signal are coupled to the same scan line. For example, for k=1, pixel P1 is provided at an intersection of scan lines S1a and S1b.

[0055] In the pixel circuit Pk, the scan line Ska is electrically coupled to the second transistor M2, the fourth transistor M4, and the fifth transistor M5, and can function as a previous scan line. The scan line Skb is electrically coupled to the third transistor M3, and can function as a current scan line. Accordingly, the number of scan lines S1a, S1b, S2a... Sna, and Snb present at the display panel 500 are twice the total number of pixels.

[0056] As illustrated earlier, the data driver 510 includes a bi-directional shift register, which results in a bi-directional data driver capable of applying a data signal in both directions. Furthermore, the first and second scan drivers 600 and 700 are provided at both sides of the display panel 500. The first scan driver 600 includes a scan direction controller 610, a shift register 620, a first selection signal supply section 630, and a buffer section 640. The second scan driver 700 includes a second selection signal supply section 710 and a buffer section 720.

[0057] The first scan driver 600 functions to provide a selection signal to the first scan line, namely, the current scan line Skb in the pixel circuit included in the display panel 500. The second scan driver 700 functions to provide a selection signal to the second scan line, namely, the previous scan line Ska in the pixel circuit included in the display panel 500.

[0058] Moreover, the first and second scan drivers 600 and 700 form a bi-directional scan drive. During a forward scan drive, the first and second scan drivers 600 and 700 sequentially apply a selection signal to scan lines S1a, S1b,

S2a... Sna, and Snb in a lower direction. In contrast, during a reverse scan drive, the first and second scan drivers 600 and 700 sequentially apply the selection signal to scan lines Sna, Snb, S2a ... Sn-1a ... Sn-1b, S1a, S1b in an upper direction. In other words, the terms "forward" and "reverse" in this context refer to opposite scanning directions.

[0059] The scan direction controller 610 controls the first scan driver 600 to perform a forward or reverse scan drive. When the scan direction controller 610 receives a forward signal CTV or a reverse signal CTD, it causes the shift register 620 coupled to a next stage to generate sequential signals in a forward or a reverse direction.

[0060] That is, when the scan direction controller 610 receives the forward signal CTV, an initial start signal STV is transferred to a zero-th unit SRU#0 of the shift register 620, where it may cause the shift register 620 to generate sequential signals SR0, SR1, SR2...SRn+1 in the forward direction. In contrast, when the scan direction controller 610 receives the reverse signal CTD, the initial start signal STV is transferred to an n+1-th unit SRU#n+1 of the shift register 620, where it causes the shift register 620 to generate sequential signals SRn+1, SRn, SRn-1...SR0 in the reverse direction. The units of the shift register 620 are illustrated in FIG. 6.

[0061] Furthermore, the shift register 620 is a bi-directional shift register, which may perform a bi-directional scan. The shift register 620 includes units 622, which comprise n+2 units SRU#0, SRU#1...SRU#n+1, in the embodiment shown in FIG. 6. Under control of the scan direction controller 610, the shift register 620 shifts the initial start signal STV in the forward or reverse direction to generate sequential signals.

[0062] The first selection signal supply section 630 is composed of multiple three terminal NAND gates 632, which receive one of two adjacent signals from the shift register 620, and first and second clock signals CLK1 and CLK2. The first selection signal supply section 630 provides selection signals to the current scan lines Skb of the pixel circuits in the display panel 500 through the NAND gates 632. In order to stabilize the selection signals output to the display panel 500, a buffer section 640 can be further provided between the first selection signal supply section 630 and the display panel 500.

[0063] That is, during a forward scan drive, the first selection signal supply section 630 sequentially applies a selection signal to current scan lines S1b, S2b...Snb of the scan lines in the lower direction. In contrast, during a reverse scan drive, the first selection signal supply section 630 sequentially applies the selection signal to current scan lines Snb, Sn-1b...S1b of the scan lines in the upper direction.

[0064] As described above, when one of the forward signal CTV and the reverse signal CTD is applied to the second selection signal supply section 710, it provides the selection signal to the previous scan line Skb of the pixel circuit included in the display panel 500 in the forward or reverse direction.

[0065] Here, the selection signal provided by the second selection signal supply section 710 is a selectively output signal among signals received from the first scan driver 600 according to the forward or reverse signal. For stabilization of the selection signal output to the display panel 500, the buffer section 720 can be further provided between the second selection signal supply section 710 and the display panel 500.

[0066] During the forward scan drive, the second selection signal supply section 710 sequentially applies the selection signal to previous scan lines S1a, S2a...Sna of scan lines in the lower direction. In contrast, during the reverse scan drive, the second selection signal supply section 710 sequentially applies the selection signal to previous scan lines Snb, Sn-1b...S1b of the scan lines in the upper direction.

[0067] Here, the selection signal provided by the second selection signal supply section 710 is a selectively output signal among signals received from the first selection signal supply section 610 according to the forward or reverse signal. For example, during the forward scan drive, the selection signal output to the previous scan line S1a from the second scan driver 700 is identical to the selection signal output to a scan line S0 from the first scan driver 600. Further, the selection signal output to the previous scan line S2a from the second scan driver 700 is substantially identical to the selection signal output to the previous scan line S1b from the first scan driver 600.

[0068] In the same manner, during the reverse scan drive, the selection signal output to the previous scan line Sna from the second scan driver 700 may be substantially identical to the selection signal output to a scan line Sn+1 from the first scan driver 600. Further, the selection signal output to the previous scan line Sn-1a from the second scan driver 700 is substantially identical to the selection signal output to the previous scan line Snb from the first scan driver 600.

[0069] As explained previously, the first and second scan drivers 600 and 700 apply respective selection signals to corresponding scan lines S1a, S1b, S2a, S2b... Sna, Snb in response to the forward signal CTV and the reverse signal CTD.

[0070] Namely, when the forward signal CTV is applied, the selection signals from the second scan driver 700 are sequentially applied to previous scan lines ("a" scan lines) S1a, S2a, S3a, S4a...Sna in the lower direction, whereas the selection signals from the first scan driver 700 are sequentially applied to current scan lines ("b" scan line) S1b, S2b, S3b, S4b...Snb in the upper direction.

[0071] Here, the selection signals output to previous scan lines S1a, S2a, S3a, S4a... Sna from the second scan driver 700 are substantially identical with the selection signals output to the current scan lines S1b, S2b, S3b, S4b...Snb from the first scan driver 600, respectively.

[0072] According to an embodiment of the present invention, in a panel including passive elements M2, M4, and M5

in one pixel operating by the previous selection signal coupled to the "a" scan lines, and the passive element M3 operating by a current selection signal coupled to the "b" scan lines, the previous selection signal is applied to the "a" scan lines in the case of the forward or reverse scan, and the current selection signal is applied to the "b" scan lines, so that a normal image may be displayed.

[0073] FIG. 6 illustrates a detailed view of the first and second scan drivers illustrated in FIG. 5.

[0074] Referring to FIG. 6, the scan direction controller 610 includes n+2 control units 612. Each of the control units 612 include a first transistor T1 and a second transistor T2. The first transistors T1 are turned-on according to the forward signal CTV, and may provide a start signal STV or an output signal of a shift register unit in a previous stage to a shift register unit. The second transistors T2 are turned-on according to the reverse signal CTD, and may provide a start signal STV or an output signal of a shift register unit in a previous stage.

[0075] Namely, as shown in FIG. 6, when the forward signal CTV is applied to a gate of the first transistor T1 of a zero-th control unit of the control units 612, the first transistor T1 is turned-on to transfer the start signal STV applied to a source thereof to the zero-th shift register unit SRU#0. When the reverse signal CTD is applied to a gate of the second transistor T2 of the zero-th control unit, the second transistor T2 is turned-on to transfer an output signal of a shift register unit of a next stage, e.g., a first shift register unit SRU#1 applied to a source thereof to the zero-th shift register unit SRU#0.

[0076] Furthermore, when the forward signal CTV is applied to gates of first transistors T1 of first to n-th control units, the first transistors T1 are turned-on to transfer output signals of shift register units SRU#0...SRU#n-1 of the previous stage applied to a source thereto to first to n-th shift registers SRU#1... SRU#n. When the reverse signal CTD is applied to gates of second transistors T2 of the first to n-th control units, the second transistors are turned-on to transfer output signals of shift register units SRU#2...SRU#n+1 of the next stage applied to a source thereto to first to n-th shift registers SRU#1...SRU#n.

[0077] Moreover, when the forward signal CTV is applied to a gate of the first transistor T1 of an n-1-th control unit, the first transistor T1 are turned-on to transfer an output signal of the shift register unit in the previous stage, namely a n-th shift register SRU#n applied to a source of an n+1-th shift register SRU#n+1. When the reverse signal CTD is applied to a gate of the second transistor T2 of an n+1-th control unit, the second transistor T2 are turned-on to transfer the start signal STV applied to the source of the n+1-th shift register SRU#n+1.

[0078] Here, the respective control units 612 constituting the scan direction controller 610 are not limited to the arrangement shown in FIG. 6. For example, the respective control units 612 are formed by transmission gates.

[0079] The shift register 620 may be a bi-directional shift register having a bi-directional scan function. The shift register 620 includes n+2 units 622, which may include units SRU0, SRU1...SRUn+1. Under control of the scan direction controller 610, the shift register 620 shifts the start signal STV in the forward or reverse direction to generate sequential signals SR0, SR1...SRn+1 or SRn+1, SRn, SRn-1...SR0.

[0080] In addition, the first selection signal supply section 630 includes n+1 three terminal NAND gates 632, which receive one of two adjacent signals from the shift register 620, and first and second clock signals CLK1 and CLK2. The first selection signal supply section 630 provides a selection signal to a current scan line Skb of the pixel circuit in the display panel 500 through the NAND gates. In order to stabilize the selection signal output to the display panel 500, the buffer section 640 is further provided between the first selection signal supply section 630 and the display panel 500.

[0081] That is, a zero-th NAND gate of the first selection signal supply section 630 receives and performs a NAND operation on the output signal SR0 of the zero-th shift register unit SRU#0, an output signal of a first shift register unit, and the first clock signal CLK1, and outputs the selection signal to the S0 scan line.

[0082] Moreover, first to n-1 NAND gates of the first selection signal supply section 630 receives NAND output signals SR1, SR2...SRn-1, SRn of the shift register 620 and the first clock signal CLK1 or second clock signal CLK2, and may output the selection signal to scan lines S1b, S2b...Snb.

[0083] Furthermore, a n-th NAND gate of the first selection signal supply section 630 receives and performs a NAND operation on the output signal SRn of a n-th shift register unit, the output signal SRn+1 of the n+1-th shift register, and the first clock signal CLK1, and outputs the selection signal to the Sn+1 scan line. Here, the S0 and Sn+1 scan lines may be dummy scan lines, and a pixel coupled thereto may not emit light.

[0084] In addition, during the forward scan drive, the first selection signal supply section 630 sequentially applies the selection signal to previous scan lines S1b, S2b...Snb in the lower direction, which is coupled to respective pixel circuits of the display panel 500. In contrast, during the reverse scan drive, the first selection signal supply section 610 sequentially applies the selection signal to previous scan lines Snb, Sn-1b...S1b of the scan lines in the upper direction, which are coupled to respective pixel circuits of the display panel 500.

[0085] A waveform of a final output signal through the NAND operations of output signals SR0, SR1...SRn+l, and the first and second clock signals will be now explained with reference to the timing charts of FIG. 8 and FIG. 10, which illustrate the forward or reverse drive.

[0086] The second selection signal supply section 710 of the second scan driver 700 is composed of n selection units 712. Each of the n selection units 712 includes a first transistor TR1 and a second transistor TR2. The first transistor TR1 is turned-on according to the forward signal CTV and provides an output signal of a NAND gate of a previous stage

of the first selection signal supply section 630 as the selection signal of the display panel. The second transistor TR2 is turned-on according to the reverse signal CTD and provides an output signal of a NAND gate of a next stage of the first selection signal supply section 630 as the selection signal of the display panel 500.

[0087] As shown in FIG. 6, when the forward signal CTV is applied to gates of the first transistors TR1 of first to n selection units 712, the first transistors TR1 are turned-on to provide output signals S0, S1b...Sn-1b of NAND gates of the previous stage, namely, zero to n-1 NAND gates, applied to a source thereto as the selection signal of the display panel 500. When the reverse signal CTD is applied to gates of the second transistors TR2 of first to n-th selection units 712, the second transistors TR2 are turned-on to provide output signals S2b, S3b...Sn+1b of NAND gates of the next stage, namely, second to n+1 NAND gates applied to a source thereto, as the selection signal of the display panel 500.

[0088] Here, the respective selection units 712 constituting the second selection signal supply section 710 are not limited to an arrangement shown in FIG. 6. For example, the respective selection units 712 may be embodied by transmission gates.

[0089] As any one of the forward signal CTV and the reverse signal CTD may be applied to the second selection signal supply section 710, it may provide the selection signal to a previous scan line Skb of a pixel circuit in the display panel 500 in the forward or reverse direction.

[0090] Here, the selection signal provided by the second selection signal supply section 710 can be a selectively output signal among signals received from the first scan driver 600 (or the first selection signal supply section 630) according to the forward or reverse signal. In order to stabilize the selection signal output to the display panel 500, the buffer section 720 can be further provided between the second selection signal supply section 710 and the display panel 500.

[0091] That is, during the forward scan drive, the second selection signal supply section 710 sequentially applies the selection signal to previous scan lines S 1 a, S2a... Sna in the lower direction, which may be coupled to the respective pixel circuits of the display panel 500. In contrast, during the reverse scan drive, the second selection signal supply section 710 sequentially applies the selection signal to previous scan lines Snb, Sn-1b...S1b in the upper direction, which is coupled to the respective pixel circuits of the display panel 500.

[0092] Here, as described earlier, the selection signal provided by the second selection signal supply section 710 can be a selectively output signal among signals received from the first selection signal supply section 630 according to the forward or reverse signal. For example, during the forward drive, the selection signal output to the S1a scan line from the second scan driver 700 is substantially identical to the selection signal output to the S0 scan line from the first scan driver 600. Further, the selection signal output to the S2a scan line from the second scan driver 700 is substantially identical to the selection signal output to the S1b scan line from the first scan driver 600.

[0093] In a similar manner, during the reverse drive, the selection signal output to the Sna scan line from the second scan driver 700 is substantially identical to the selection signal output to the Sn+1 scan line from the first scan driver 600. Further, the selection signal output to the Sn-1a scan line from the second scan driver 700 is substantially identical to the selection signal output to the Snb scan line from the first scan driver 600.

[0094] FIG. 7 illustrates a view of the forward driving operation of the first and second scan drivers shown in FIG. 6. FIG. 8 illustrates a timing chart of the forward driving operation of the first and second scan drivers shown in FIG. 6.

[0095] With reference to FIG. 7 and FIG. 8, when the low level forward signal CTV is applied to scan direction controller 610 of the first scan driver 600, first transistors T1 of control unit 612 in the scan direction controller 610 are turned-on. The first transistors T1 are P-channel transistors in the embodiment.

[0096] On the other hand, the low level reverse signal CTD may be applied to the scan direction controller 610 of the first scan driver 600. In this case, second transistors T2 of the control units 612 can turned-off. The second transistors T2 may be N-channel transistors. In other words, although the forward signal CTV and the reverse signal CTD can separately applied, they can alternately be applied as the same signal.

[0097] Accordingly, when the first transistors T1 of the control units 612 are turned-on, the initial start signal STV is provided to the zero-th shift register unit SRU#0 through the zero-th control unit, and the shifted signal SR0 thereof is output. The shifted signal SR0 is provided to the first shift register SRU#1 through the first control unit, so that it outputs the signal SR1 shifted by about one horizontal period 1H.is be applied to the scan direction controller 610 of the first scan driver 600, a start signal is applied to the zero-th shift register SRU#0 through the zero-th control unit to output the SR0 signal. The SR0 signal is applied to the shift register unit of the next stage, namely, the first shift register unit SRU#1 through the control unit of the next stage, namely, a first control unit to output the SR1 signal.

[0098] As a result, as shown in FIG. 8, SR0, SR1, SR2, SR3... signals are sequentially generated in the lower direction of the display panel 500 through the scan direction controller 610 and the shift register 620.

[0099] Accordingly, one of two adjacent signals and first and second clock signals CLK1 and CLK2 from the shift register 620 are input to n+1 three terminal NAND gates 632 included in the first selection signal supply section 630.

[0100] Here, the first and second clock signals CLK1 and CLK2 have a time period of about 1H, and the phases thereof are inverted and input.

[0101] That is, a zero-th NAND gate receives and performs a NAND operation on the output signal SR0 of the zero-

th shift register unit SRU#0, the output signal SR1 of the first shift register unit SRU#1, and the first clock signal CLK1, and outputs the selection signal to the S0 scan line.

[0102] With reference to FIG. 8, the selection signal output from the S0 scan line become a low level signal by a NAND operation of the first high level clock signal CLK1, the high level SR0 signal, and the high level S1 signal.

[0103] Moreover, first to n-1 NAND gates receive one of SR1, SR2 to SRn-1, SRn, along with the first clock signal CLK1 or the second clock signal CLK2, and output the selection signal to S1b to Snb scan lines.

[0104] Namely, as shown in FIG. 8, the selection signal output to the S1b scan line may have a low level by a NAND operation of the second high level clock signal CLK2, and SR1 and SR2 of a high level. The selection signal output to the S2b scan line has a low level signal resulting from a NAND operation of the high level first clock CLK1, and SR2 and SR3 of a high level.

[0105] The generated selection signals is finally provided to the current scan line Skb of the pixel circuit included in the display panel 500 as the selection signal. Here, the S0 and Sn+1 scan lines can be dummy scan lines, and any pixel coupled thereto do not emit light.

[0106] That is, during the forward scan drive, the first selection signal supply section 630 sequentially applies the selection signal to previous scan lines S1b, S2b... Snb in the lower direction, which is coupled to the respective pixel circuits of the display panel 500.

[0107] When the low level forward signal CTV is applied to the first transistor TR1 of the selection units 712, it is turned-on. The first transistors TR1 are P-channel transistors in this embodiment.

[0108] On the other hand, the low level reverse signal CTD can be applied. In this case, the second transistors TR2 of the selection units 712 are N-channel transistors, and are all turned-off. In other words, although the forward signal CTV and the reverse signal CTD have been illustrated as being separately applied, they may also be applied as the same signal.

[0109] Accordingly, in the selection units 712, each first transistor TR1 is turned-on to provide an output signal of the NAND gate in a previous stage as the selection signal of the display panel 500. The NAND gates may be included in the first selection signal supply section 612 of the first scan driver 600.

[0110] Namely, as shown in FIG. 7, when the forward signal CTV is applied to the gates of first transistors TR1 of first to n selection units 712, the first transistors TR1 may be turned-on according to the forward signal CTV to provide output signals S0, S1b, ..., Sn-1b of NAND gates of the previous stage, namely, zero to n-1 NAND gates applied as a source of the selection signal of the display panel 500.

[0111] Accordingly, during the forward drive, the second selection signal supply section 710 sequentially applies a selection signal to previous scan lines S1a, S2a... Sna of the scan lines in the lower direction, which are coupled to the respective pixel circuits of the display panel 500.

[0112] Here, the selection signal provided by the second selection signal supply section 710 is a selectively output signal among signals received from the first selection signal supply section 630 according to the forward or reverse signal. As shown in FIG. 8, in the case of the forward drive, the selection signal output to the S1a scan line from the second scan driver 700 is substantially identical to the selection signal output to the S0 scan line from the first scan driver 600. Further, the selection signal output to the S2a scan line from the second scan driver 700 is substantially identical to the selection signal output to the S1b scan line from the first scan driver 600.

[0113] As a result, in the display panel 500 including passive elements M2, M4, and M5 in one pixel operating by the previous selection signal coupled to the "a" scan lines, and the passive element M3 operating by the current selection signal coupled to the "b" scan lines, the previous selection signal are applied to the "a" scan lines, and the current selection signal are applied to the "b" scan lines during the forward scan, so that a normal image may be displayed.

[0114] FIG. 9 illustrates a view of a reverse driving operation of the first and second scan drivers shown in FIG. 6. FIG. 10 illustrates a timing chart of the reverse driving operation of the first and second scan drivers shown in FIG. 6.

[0115] With reference to FIG. 9 and FIG. 10, when the high level reverse signal CTD is applied to the scan direction controller 610 of the first scan driver 600, the second transistor T2 of each of the control units 612 included in the scan direction controller 610 may be turned-on. Here, the second transistors T2 are N-channel transistors in this embodiment.

[0116] On the other hand, the low level reverse signal CTD can be applied. In this case, the first transistors T1 are P-channel transistors, and are all turned-off.

[0117] Accordingly, as the first transistors T1 of the control unit 612 are turned-on, the initial start signal STV is provided to the n+1 th shift register unit SRU#n+1 through the n+1 th control unit and the shifted signal SRn+1 thereof is output. The shifted signal SRn+1 is provided to the n-th shift register SRU#n through the n-th control unit, so that it may output the signal SRn shifted by about 1 horizontal period 1H.

[0118] That is, when applying the high level reverse signal CTD, the initial start signal STV is provided to the n+1 th shift register unit SRU#n+1 through the n+1-th control unit to output the SRn+1 signal. The SRn+1 signal is applied to the shift register unit, namely, the n-th shift register unit SRU#n through the control unit of the previous stage, namely, the n-th control unit to output the SRn signal.

[0119] As a result, as illustrated in FIG. 10, SRn+1, SRn, SRn-1, SRn-2... signals are sequentially generated through

the scan direction controller 610 and the shift register 620. Accordingly, one of two adjacent signals and first and second clock signals CLK1 and CLK2 from the shift register 620 is input to the n+1 three terminal NAND gates 632 included in the first selection signal supply section 630. Here, the first and second clock signals CLK1 and CLK2 have a time period of 1H, and the phases thereof are inverted and input. That is, the n+1-th NAND gate receives and performs a NAND operation on the output signal SRn+1 of the n+1-th shift register unit, the output signal SRn of the n-th shift register, and the first clock signal CLK1, and outputs the selection signal to the Sn+1 scan line.

[0120] With reference to FIG. 10, the selection signal output from the Sn+1 scan line has a low level signal resulting from a NAND operation of the first high level clock signal CLK1, the high level SRn+1 signal, and the high level SRn signal. Moreover, the first to n NAND gates receives one of SRn, SRn-1 to SR1, SR0, and the first clock signal CLK1 or the second clock signal CLK2, and may output a selection signal to the Snb to S1b scan lines.

[0121] Namely, as shown in FIG. 10, the selection signal output to the Snb scan line has a low level signal resulting from a NAND operation of the second high level clock signal CLK2, and high level SRn and SRn-1. The selection signal output to the Sn-1b scan line has a low level signal resulting from a NAND operation of the high level first clock signal CLK1, and high level SR2 and SR3.

[0122] The generated selection signals are finally provided to the current scan line Skb of the pixel circuits included in the display panel 500. Here, the Sn+1 and S0 scan lines may be dummy scan lines, and any pixel coupled thereto may not emit light.

[0123] That is, during the reverse scan drive, the first selection signal supply section 630 sequentially applies the selection signal to current scan lines Snb, Sn-1b... S1b of scan lines in the lower direction, which is coupled to the respective pixel circuits of the display panel 500.

[0124] When the high level reverse signal CTD is applied to the second transistor TR2 of the selection unit 712, it is turned-on. The second transistors TR2 are N-channel transistors. On the other hand, the high level forward signal CTV are applied. In this case, the second transistors TR2 of the selection unit 712 are formed of P-channel transistors, and are all turned-off.

[0125] In other words, although the forward signal CTV and the reverse signal CTD have been described as being separately applied, they may also be applied as the same signal.

[0126] Accordingly, in the selection units 712, each second transistor TR2 are turned-on according to the reverse signal CTD to provide the output signal of the NAND gate in the previous stage as the selection signal of the display panel 500. Here, the NAND gates are included in the first selection signal supply section 630 of the first scan driver 600.

[0127] Namely, as shown in FIG. 9, when the reverse signal CTD is applied to the gates of second transistors TR2 of the first to n selection units 712, the second transistors TR2 are turned-on to provide output signals S2b, S3b... Sn+1 of the NAND gates of the previous stage, namely, second to n+1 NAND gates applied as a source of the selection signal of the display panel 500.

[0128] Accordingly, during reverse driving, the second selection signal supply section 710 sequentially applies the selection signal to previous scan lines Sna, Sn-1a... S1a in the upper direction, which may be coupled to respective pixel circuits of the display panel 500.

[0129] Here, the selection signal provided by the second selection signal supply section 710 is a selectively output signal among signals received from the first selection signal supply section 630 according to the forward or reverse signal. As shown in FIG. 10, when in forward drive, the selection signal output to the Sna scan line from the second scan driver 700 is substantially identical to the selection signal output to the Sn+1 scan line from the first scan driver 600. Further, the selection signal output to the Sn-1a scan line from the second scan driver 700 is substantially identical to the selection signal output to the Snb scan line from the first scan driver 600.

[0130] As a result, in the panel 500 including passive elements M2, M4, and M5 in one pixel operating by the previous selection signal coupled to the "a" scan lines, and the passive element M3 operating by the current selection signal coupled to the "b" scan lines, the previous selection signal is applied to the "a" scan lines, and the current selection signal may be applied to the "b" scan lines during the forward scan, so that a normal image may be displayed.

[0131] The driving technology of the present invention has been described as being applied to OLEDS. However, embodiments of the present invention are not restricted to OLEDS, and the driving technology may be applied to any appropriate display.

[0132] Exemplary embodiments of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A driver for a display, comprising:

a bi-directional data driver adapted to apply a data signal in a forward direction and a reverse direction;
a first scan driver adapted to receive a forward or reverse signal and to selectively output a first selection signal in the forward or reverse direction to a first scan line of a display panel in accordance with the forward or reverse signal; and
a second scan driver adapted to receive the first selection signal and to selectively output a second selection signal in the forward or reverse direction to the second scan line of the display panel in accordance with the forward or reverse signal.

2. A driver according to claim 1, wherein the first scan driver includes:

a scan direction controller adapted to receive the forward or reverse signal, and to cause a shift register of a next stage to generate a sequential signal in the forward or reverse direction;
a shift register adapted to shift a start signal received by the scan direction controller to generate the sequential signal; and
a first selection signal supply section adapted to receive one of two adjacent signals, and first and second clock signals from the shift register and to provide the first selection signal to the first scan line.

3. A driver according to claim 2, wherein the scan direction controller includes a plurality of control units, each control unit having a first transistor adapted to be turned-on according to the forward signal to provide the start signal or an output signal of a shift register in a previous stage to a shift register unit, and a second transistor adapted to be turned-on according to the reverse signal to provide the start signal or an output signal of a shift register unit in a next stage to the shift register unit.

4. A driver according to claim 3, wherein the first and second transistors are different types from each other.

5. A driver according to any one of claims 2 to 4, wherein the first selection signal supply section includes a plurality of three terminal NAND gates, which are adapted to receive one of two adjacent signals, and first and second clock signals from the shift register.

6. A driver according to any one of claims 1 to 5, wherein the first and second clock signals have a time period of 1H, and the phases thereof are inverted and input.

7. A driver according to any one of claims 1 to 6, wherein the second scan driver includes a second signal selection supply section, which outputs a first previous selection signal of the first scan driver as a second selection signal in response to the forward signal, and outputs a first next selection signal of the first scan driver as the second selection signal in response to the reverse signal.

8. A driver according to claim 7, wherein the second signal selection supply section includes a plurality of selection units, each having a first transistor adapted to be turned-on according to the forward signal for providing a first previous selection signal of the first scan driver as a second selection signal, and a second transistor adapted to be turned-on according to the reverse signal for providing a first next selection signal of the first scan driver as the second selection signal.

9. A driver according to claim 8, wherein the first and second transistors are different types from each other.

10. An organic light emitting display, comprising:

a display panel including a plurality of pixel circuits, a data line, and first and second scan lines; and
a driver according to any one of claims 1 to 9.

11. A display according to claim 10, wherein the first and second scan drivers are respectively positioned at either side of the display panel.

12. A display according to claim 10 or 11 when dependent on Claim 2, further comprising:

a buffer section between the first selection signal supply section and the display panel.

13. A display according to any one of claims 10 to 12 when dependent on Claim 7, further comprising:

a buffer section between the second signal selection supply section and the display panel.

14. A display according to any one of claims 10 to 13, wherein the first scan line includes current scan lines S0, S1b, S2b...Snb, Sn+1, which are coupled to respective pixel circuits of the display panel, and the first scan line includes previous scan lines, which are coupled to the respective pixel circuits of the display panel.

15. A display according to claim 14, wherein the S0 and Sn+1 scan lines of the first scan line are dummy scan lines, and any pixel coupled to the dummy scan lines emits substantially no light.

16. A display according to any one of claims 10 to 13, wherein the first scan line includes current scan lines S0, S1b, S2b...Snb, Sn+1, which are coupled to respective pixel circuits of the display panel, and the first scan line includes previous scan lines, which are coupled to the respective pixel circuits of the display panel.

FIG. 1
(RELATED ART)

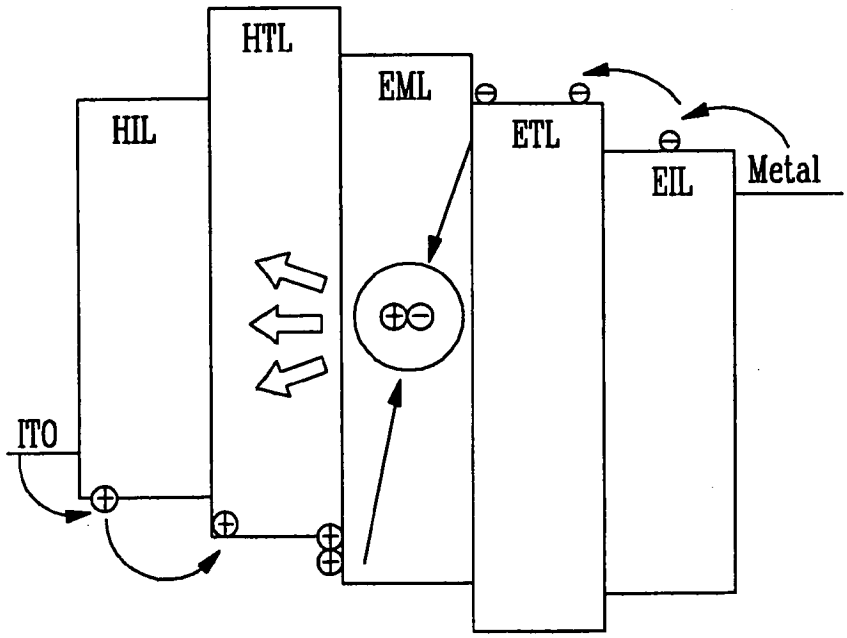


FIG. 2
(RELATED ART)

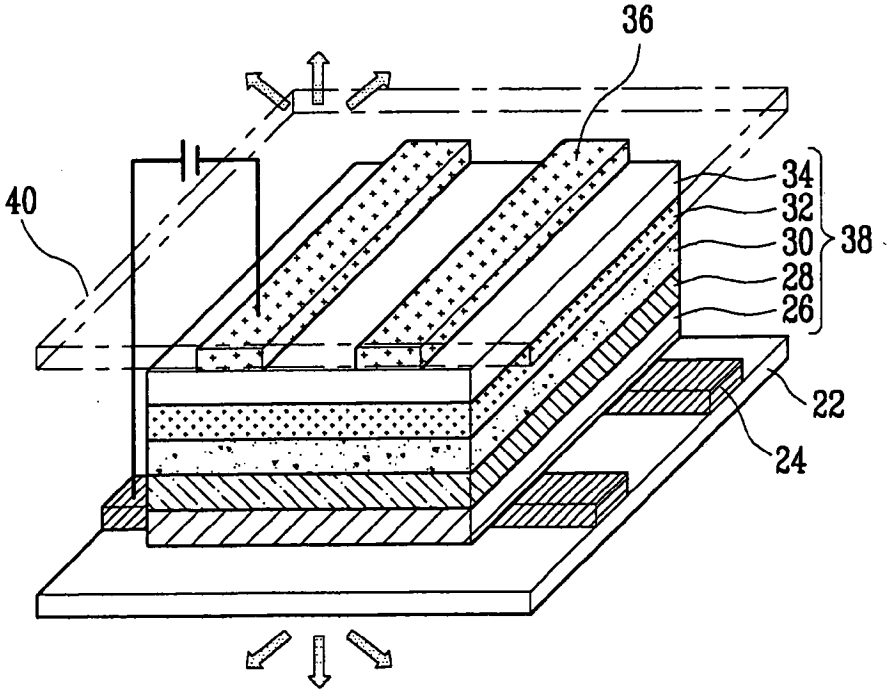


FIG. 3
(RELATED ART)

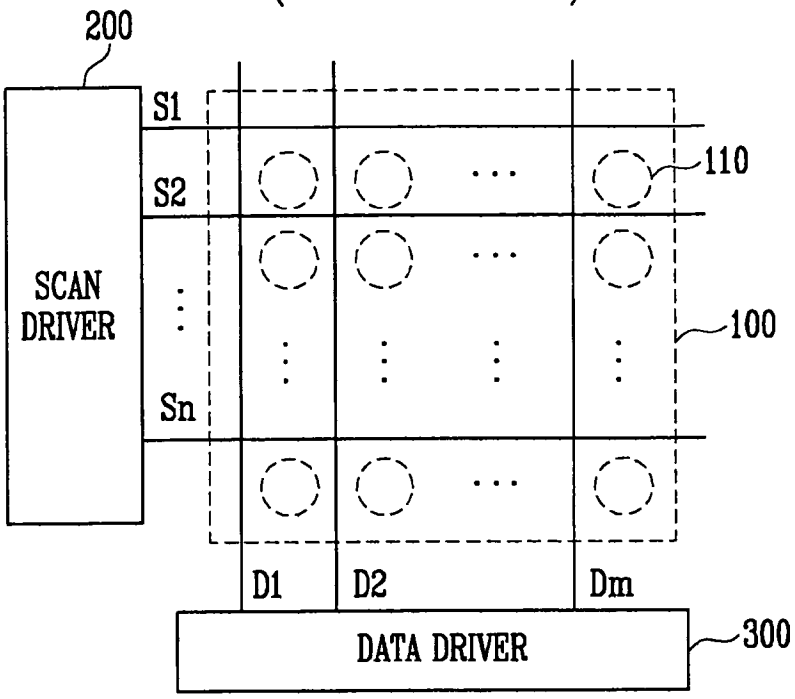


FIG. 4

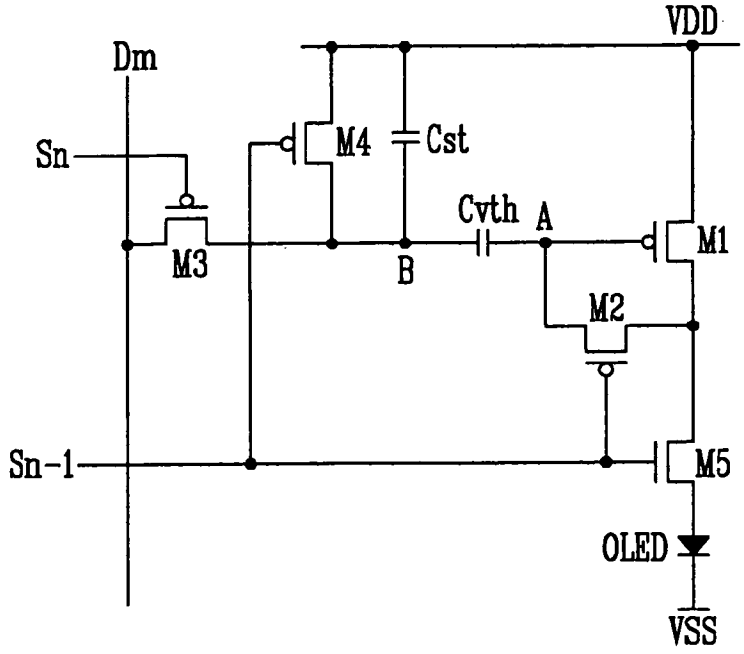


FIG. 5

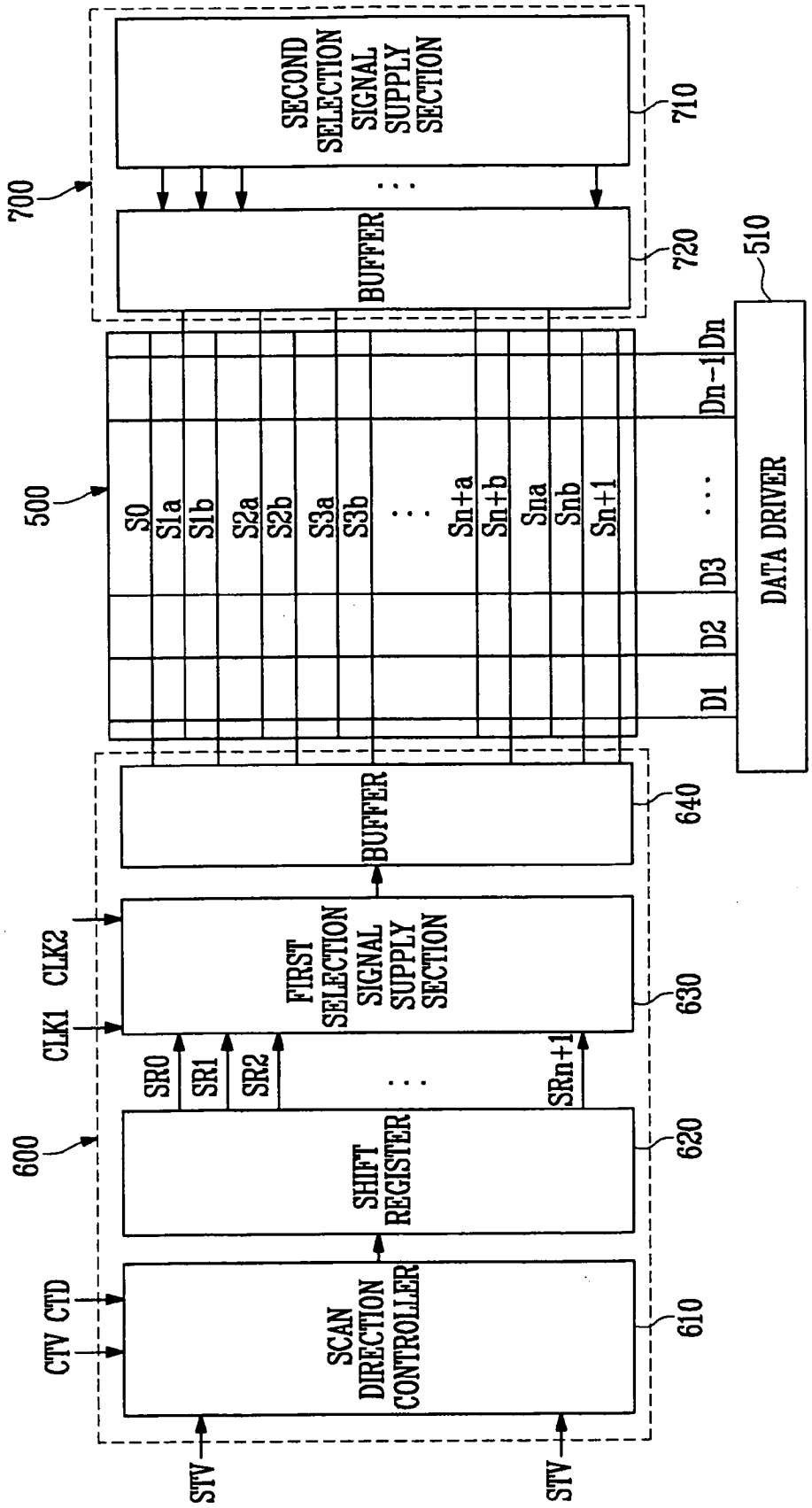

700
SECOND SELECTION SIGNAL SUPPLY SECTION
710
BUFFER
720
510
500
S0
S1a
S1b
S2a
S2b
S3a
S3b
Sn+a
Sn+b
Sna
Snb
Sn+1
Dn
Dn-1
D3
D2
D1
DATA DRIVER
BUFFER
640
CLK1
CLK2
FIRST SELECTION SIGNAL SUPPLY SECTION
630
SR0
SR1
SR2
SRn+1
600
SHIFT REGISTER
620
CTV
CTD
SCAN DIRECTION CONTROLLER
610
STV
STV

FIG. 6

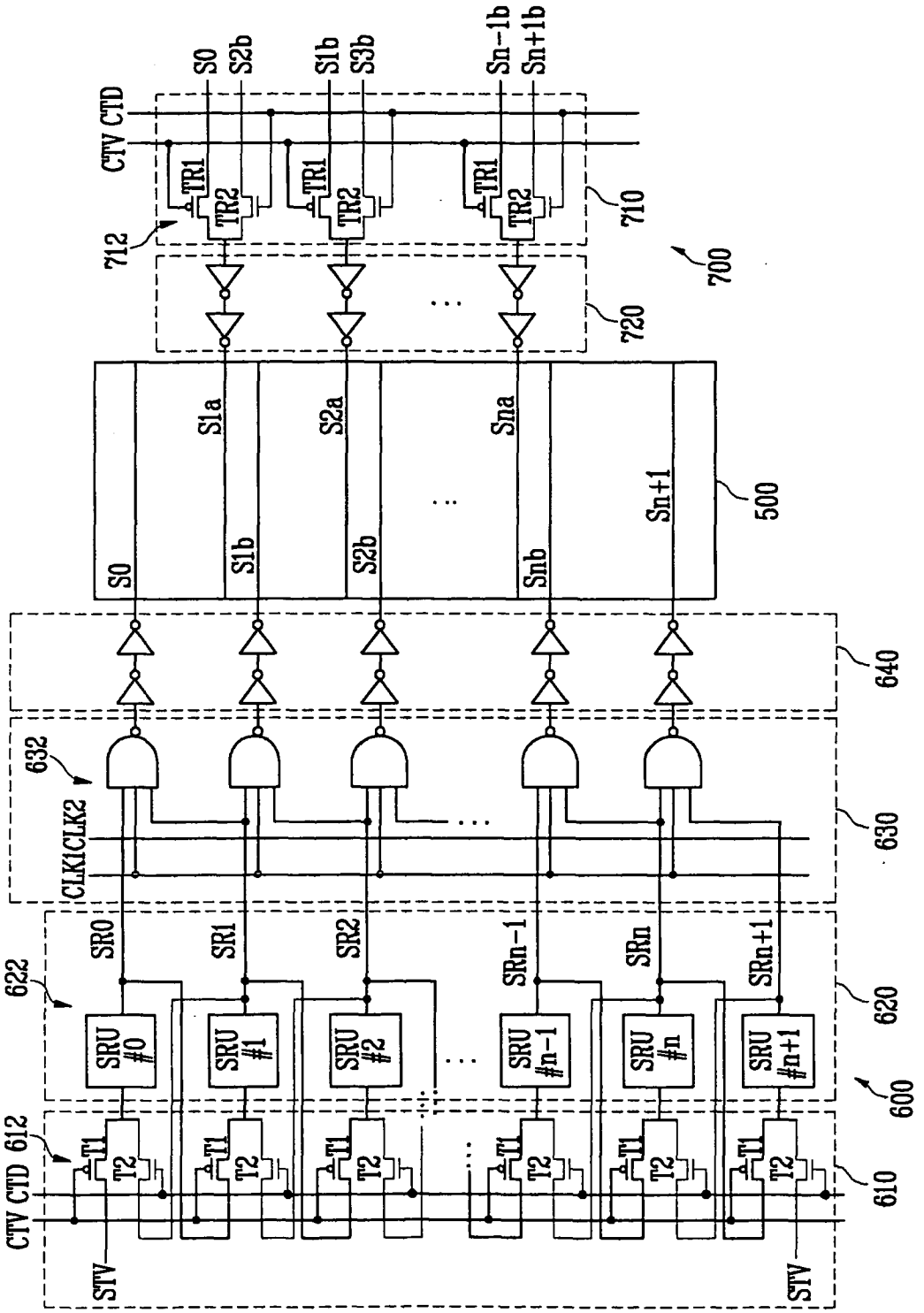

CTV CTD
S0
S2b
S1b
S3b
Sn-1b
Sn+1b
TR1
TR2
710
712
720
700
S1a
S2a
Sna
Sn+1
S0
S1b
S2b
Snb
500
640
632
CLK1CLK2
630
SR0
SR1
SR2
SRn-1
SRn
SRn+1
622
SRU #0
SRU #1
SRU #2
SRU #n-1
SRU #n
SRU #n+1
620
600
CTV CTD 612
T1
T2
610
STV
STV

FIG. 7

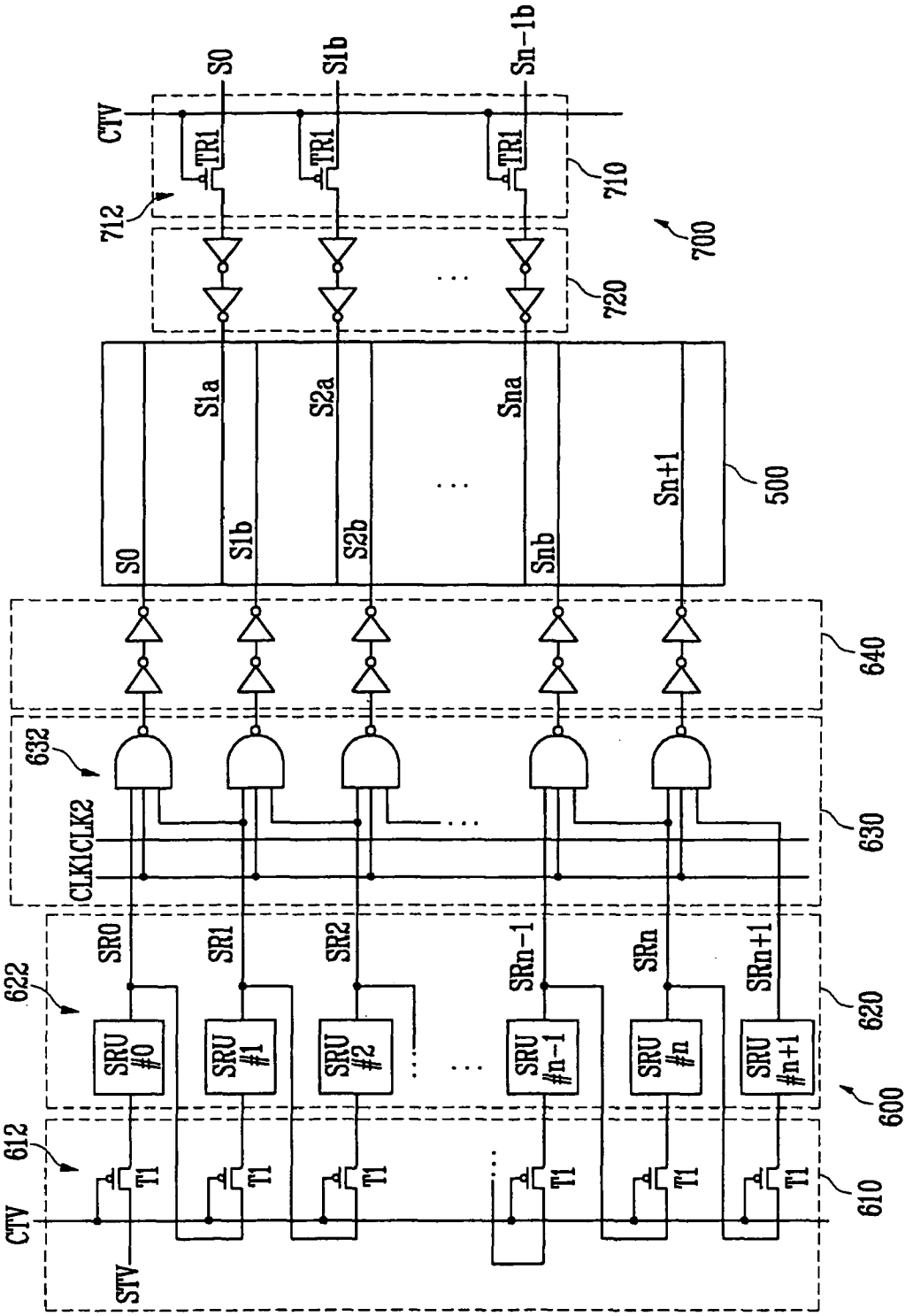

CTV
S0
S1b
Sn-1b
TR1
710
712
720
700
S1a
S2a
Sna
Sn+1
500
S0
S1b
S2b
Snb
640
632
CLK1CLK2
630
SR0
SR1
SR2
SRn-1
SRn
SRn+1
622
SRU #0
SRU #1
SRU #2
SRU #n-1
SRU #n
SRU #n+1
620
600
612
T1
CTV
610
STV

FIG. 8

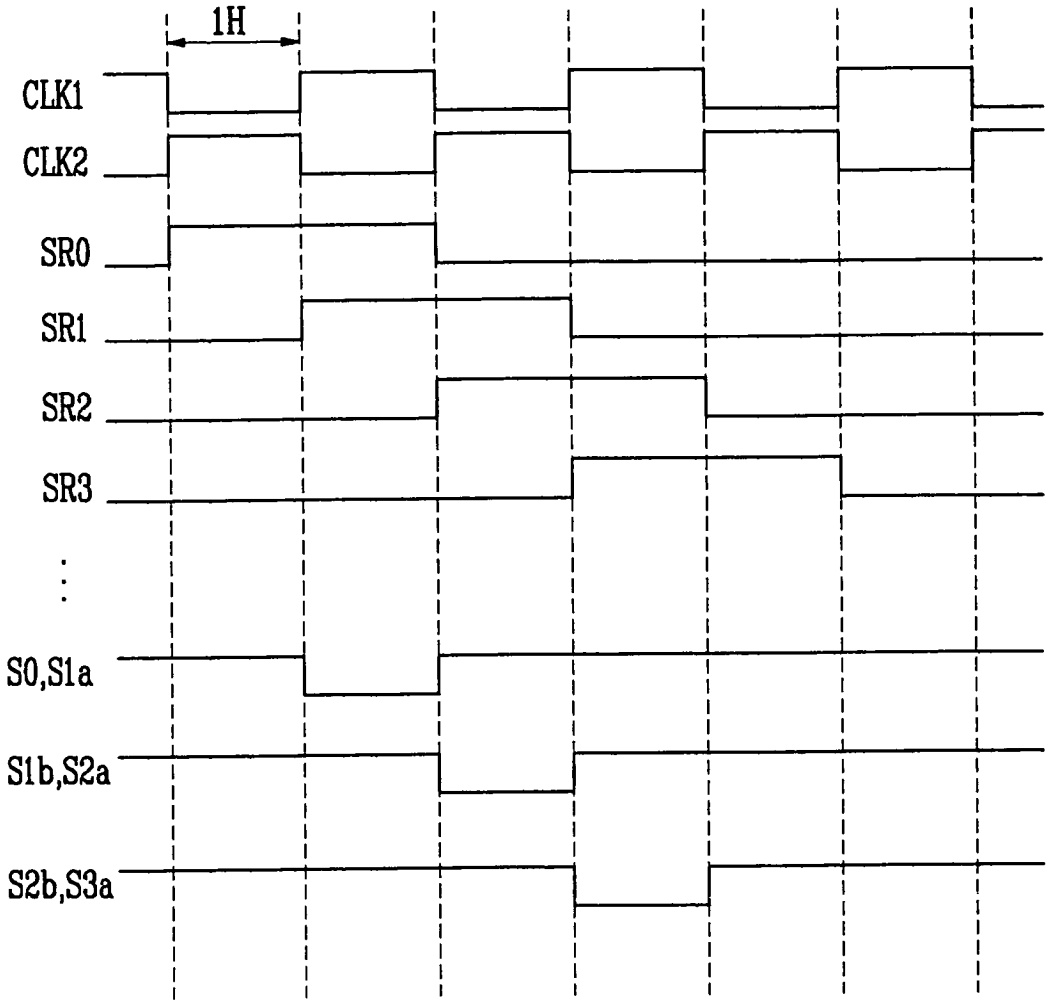
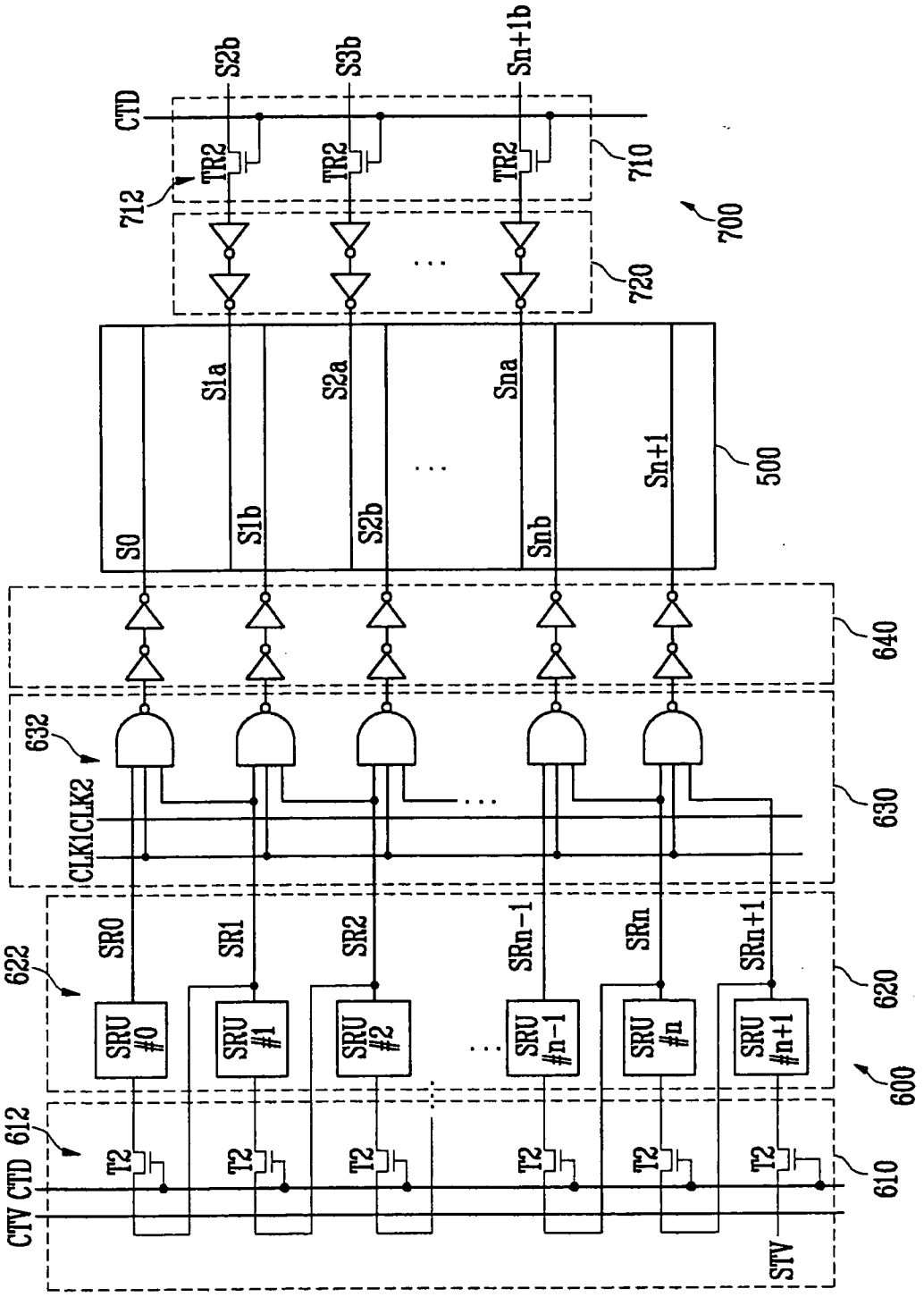


FIG. 9


CTD
S2b
S3b
Sn+1b
TR2
712
710
700
720
S1a
S2a
Sna
Sn+1
S0
S1b
S2b
Snb
500
640
632
630
CLK1CLK2
622
SR0
SR1
SR2
SRn-1
SRn
SRn+1
620
SRU #0
SRU #1
SRU #2
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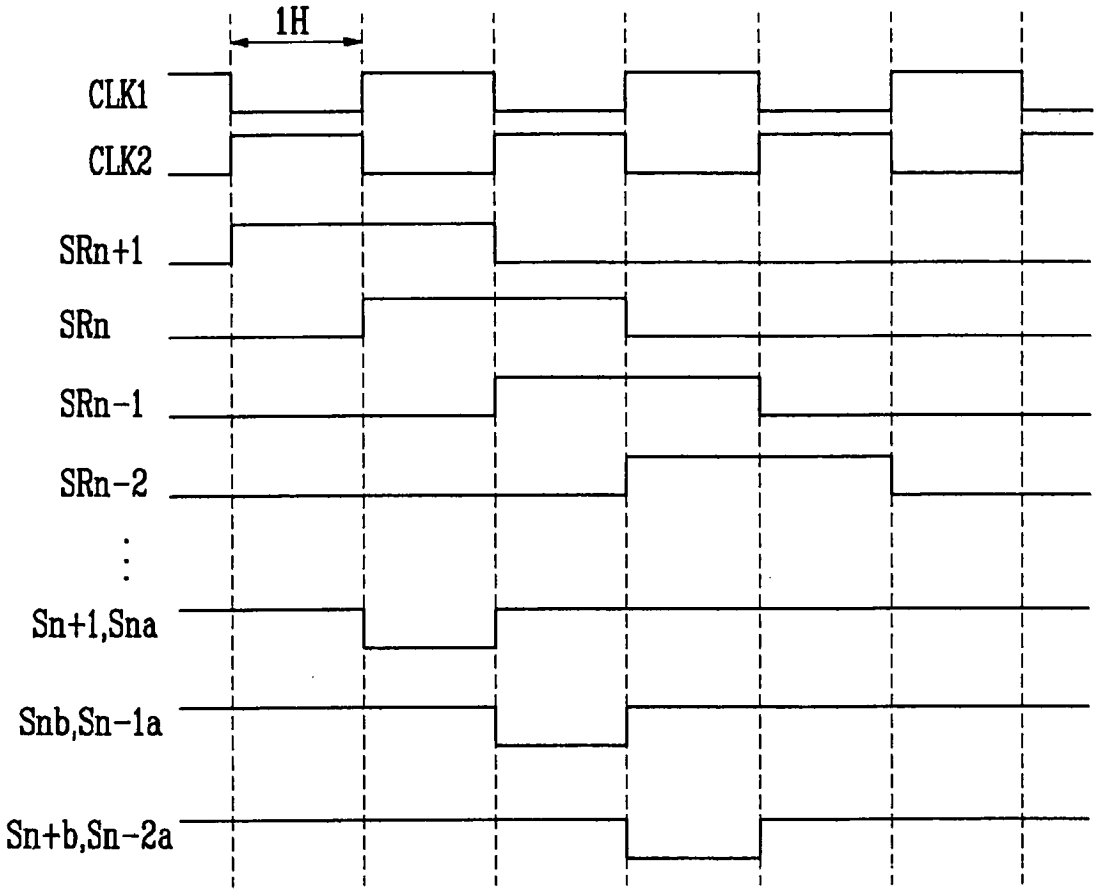
SRU #n
SRU #n+1
600
612
T2
CTV
CTD
610
STV

FIG. 10



专利名称(译)	有机发光显示器		
公开(公告)号	EP1944816A2	公开(公告)日	2008-07-16
申请号	EP2007253273	申请日	2007-08-20
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
发明人	EOM, KI MYEONG, LEGAL & IP TEAM		
IPC分类号	H01L51/00 G09G3/32		
CPC分类号	G09G3/3266 G09G3/20 G09G3/3275 G09G2300/0861 G09G2310/0283 G09G2340/0492		
优先权	1020060078063 2006-08-18 KR		
其他公开文献	EP1944816B1 EP1944816A3		
外部链接	Espacenet		

摘要(译)

有机发光显示器对至少两个不同的选择信号进行操作，这些选择信号可以执行允许显示双面屏幕的双向扫描。有机发光显示器包括数据线，第一和第二扫描线，用于在两个方向上施加数据信号的双向数据驱动器，适于接收前向或反向信号的第一扫描驱动器以及选择性地输出第一选择根据正向或反向信号向第一扫描线具有正向或反向的信号，以及用于接收第一选择信号并向第二选择信号选择性地输出正向或反向的第二选择信号的第二扫描驱动器扫描线按照正向或反向信号。

FIG. 5