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(57) An organic light emitting display including a scan signal line forwarding a scan signal, a data line sending a data signal and a pixel coupled to the scan signal line and the data line, the organic light emitting diode display, wherein the pixel includes a first switching transistor transmitting a data signal from the data line in response to the scan signal of the scan signal line, a driving transistor, coupled to the first switching transistor, controlling driving current from a first power source line, a storage capacitor coupled between the driving transistor and the

first power source line, an organic light emitting diode, coupled between the driving transistor and a second power source line, displaying an image with the driving current controlled by the driving transistor, an initial switching transistor, coupled between the storage capacitor and an initial power source line, initializing the storage capacitor, and a switching transistor for applying a reverse bias, coupled between the second power source line and the initial power source line, applying a reverse bias voltage to the organic light emitting diode.

[illegible]

Description

CROSS-REFERENCE TO RELATED APPLICATIONS

5 **[0001]** This application claims the benefit of Korean Patent Application No. 10-2006-0131962 filed on December 21, 2006, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND

10 1. Field of the Invention

[0002] The present invention relates to an organic light emitting display and a driving method thereof and, more particularly, to an organic light emitting display and a driving method thereof that ensure an operation margin of a driving circuit when driving a large-size panel by applying an interlaced scanning method, prevent a voltage drop (IR-drop) of a first power source line VDD and, simultaneously, minimize degradation of the organic light emitting diode OLED in a pixel circuit of the organic light emitting display by dividing a data write period from a light emission period in driving the panel.

20 2. Discussion of Related Art

[0003] Recently, the organic light emitting display has attracted attention as the next generation flat panel display due to its advantages such as a thin thickness, a wide viewing angle, a high response rate, etc. Such an organic light emitting display controls the amount of current flowing in the organic light emitting diodes of the respective pixels to control the brightness of the respective pixels, thus displaying an image. That is, a current corresponding to a data voltage is supplied to the organic light emitting diode and thereby the organic light emitting diode emits light correspondingly to the supplied current. Here, the data voltage applied has multilevel values in a predetermined range so as to express gradation.

[0004] If a thin film transistor TFT using amorphous silicon (a-si) is used as a driving transistor, the current driving capability is relatively low; however, it has advantages in that the uniformity of the display device is excellent and it is more favorable to a large-size process.

30 **[0005]** As driving methods for driving such an organic light emitting diode display, there are a progressive scanning method and an interlaced scanning method. The progressive scanning method drives scan lines in sequence from top left to bottom right of a screen, in which an image is displayed on all horizontal lines in one frame at one time.

[0006] The interlaced scanning method displays only the half of the horizontal lines in one image frame and this method may scan an image by dividing one image frame into two fields (odd and even) or may scan an image by dividing two frames into a first frame (odd) and a second frame (even).

35 **[0007]** If using the progressive scanning method, it has an advantage in that it provides an excellent image quality in a static screen; however, it also has drawbacks in that it is difficult to ensure an operation margin of a driving circuit when driving a large-size panel, since its scanning rate is no more than half that of the interlaced scanning method. Moreover, the progressive scanning method has drawbacks in that it may cause a voltage drop (IR-drop) as a first power source line VDD passes through the respective pixel circuits, thus decreasing the brightness of the pixels gradually. Furthermore, in the general organic light emitting diode display, as current flows in one direction from an anode to a cathode of the organic light emitting diode OLED, space charges are stored between a hole transport layer HTL and an emitting layer EML or between an electron transport layer ETL and an emitting layer EML. Due to the accumulation of the space charges, the current IOLED flowing in the organic light emitting diode OLED may be dropped. Accordingly, as the brightness of the respective pixels may be decreased, the brightness of the organic light emitting display applying the pixel circuits is lowered gradually with time. Furthermore, the lifespan of the organic light emitting display may be shortened. In addition, due to the difference of the degradation degrees of the organic light emitting diodes in the respective pixel circuits, the brightness of the whole organic light emitting display becomes non-uniform as a result.

50 SUMMARY OF THE INVENTION

[0008] A first aspect of the invention therefore provide a pixel circuit for an organic light emitting display comprising first through seventh transistors, a capacitor, and an organic light emitting diode (OLED). The first transistor has a first electrode connected to a data signal input and a control electrode connected to a first scan signal input. The second transistor has a first electrode connected to a second electrode of the first transistor, a second electrode connected to a first power supply input, and a control electrode connected to a first emission control signal input. The capacitor has a first terminal connected to the first power supply input. The third transistor (driving transistor) has a first electrode connected to the second electrode of the first transistor, and a control electrode connected to a second terminal of the

capacitor. The fourth transistor has a first electrode connected to a second electrode of the third transistor and a control electrode connected to the first emission control signal input. The fifth transistor has a first electrode connected to the control electrode of the third transistor, a second electrode connected to the second electrode of the third transistor, and a control electrode connected to the first scan signal input. The sixth transistor has a first electrode connected to the second terminal of the capacitor and a control electrode connected to a second scan signal input. The seventh transistor has a first electrode connected to a second electrode of the fourth transistor, a second electrode connected to an initialisation power supply input, and a control electrode connected to a second emission control signal input. The organic light emitting diode has a first electrode connected to the second electrode of the fourth transistor and a second electrode connected to a second power supply input.

[0009] A second aspect of the invention provides an organic light emitting diode display device comprising a scan driver, an emission control driver, a data driver, a first power supply, a second power supply, an initialisation power supply, and a plurality of pixels according to the first aspect of the invention. The scan driver is connected to a plurality of scan lines extending in a first direction. The emission control driver is connected to a plurality of emission control lines extending in the first direction and comprising at least a first emission control line and a second emission control line. The data driver is connected to a plurality of data lines extending in a second direction crossing the first direction. The first power supply is adapted to provide a first power supply voltage. The second power supply is adapted to provide a second power supply voltage. The initialisation power supply is adapted to provide an initialisation power supply voltage. The pixels are arranged in a plurality of rows, each of the pixels being connected to a corresponding first one and a corresponding second one of the scan lines, to the at least one first emission control line, to the at least one second emission control line, and a corresponding one of the data lines. The first power supply inputs of the pixels are connected to the first power supply, the second power supply inputs of the pixels are connected to the second power supply, and the initialisation power supply input of the pixels are connected to the initialisation power supply.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1 is a schematic diagram depicting a basic structure of a general organic light emitting diode;

[0011] Fig. 2 is a schematic diagram depicting a basic pixel circuit of a voltage driving method;

[0012] Fig. 3 is a driving timing diagram of the pixel circuit depicted in Fig. 2;

[0013] Fig. 4 is a block diagram depicting a basic structure of an organic light emitting display in accordance with the present invention driven in a progressive scanning method;

[0014] Fig. 5 is a circuit diagram depicting a pixel circuit of an organic light emitting display in accordance with an exemplary embodiment of the present invention;

[0015] Fig. 6 is a driving timing diagram, in which the pixel circuit depicted in Fig. 5 is driven in a progressive scanning method;

[0016] Fig. 7 depicts a current flow during an initialization period T11, in which the pixel circuit depicted in Fig. 5 is driven in a progressive scanning method;

[0017] Fig. 8 depicts a current flow during a storage period T12 for storing a data voltage and a threshold voltage of a driving transistor, in which the pixel circuit depicted in Fig. 5 is driven in a progressive scanning method;

[0018] Fig. 9 depicts a current flow during a light emission period T13, in which the pixel circuit depicted in Fig. 5 is driven in a progressive scanning method;

[0019] Fig. 10 is a circuit diagram depicting a pixel circuit of an organic light emitting display in accordance with another embodiment of the present invention;

[0020] Fig. 11 is a circuit diagram depicting a pixel circuit of an organic light emitting display in accordance with still another embodiment of the present invention;

[0021] Fig. 12 is a driving timing diagram, in which the pixel circuit depicted in Fig. 11 is driven in a progressive scanning method;

[0022] Fig. 13 is a block diagram depicting a basic structure of an organic light emitting display in accordance with the present invention driven in an interlaced scanning method;

[0023] Fig. 14 is a driving timing diagram, in which the pixel circuit depicted in Fig. 5 is driven in an interlaced scanning method;

[0024] Fig. 15 depicts a current flow during an initialization period T21 in a pixel circuit on an odd line, in which the pixel circuit depicted in Fig. 5 is driven in an interlaced scanning method;

[0025] Fig. 16 depicts a current flow during a storage period T22 of a data voltage and a threshold voltage of a driving transistor in a pixel circuit on an odd line, in which the pixel circuit depicted in Fig. 5 is driven in an interlaced scanning method;

[0026] Fig. 17 depicts a current flow during a light emission period T23 in a pixel circuit on an odd line, in which the pixel circuit depicted in Fig. 5 is driven in an interlaced scanning method;

[0027] Fig. 18 depicts a current flow during an initialization period in a pixel circuit on an even line, in which the pixel

circuit depicted in Fig. 5 is driven in an interlaced scanning method;

[0028] Fig. 19 depicts a current flow during a storage period of a data voltage and a threshold voltage of a driving transistor in a pixel circuit on an even line, in which the pixel circuit depicted in Fig. 5 is driven in an interlaced scanning method;

[0029] Fig. 20 depicts a current flow during a light emission period in a pixel circuit on an even line, in which the pixel circuit depicted in Fig. 5 is driven in an interlaced scanning method; and

[0030] Fig. 21 depicts an electrical connection between a first power source line including an odd line and an even line and the respective pixels of the organic light emitting display depicted in Fig. 13.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0031] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those having skill in the art.

[0032] For the purpose of explaining the present invention explicitly, the portions unrelated to the present invention are omitted in the drawings. Throughout the specification of the present invention, the elements having the same configuration and operation are denoted by the same reference numerals. Supposed that a certain portion is coupled to another portion, it includes the case where it is connected to the same via a different element as well as the case where it is directly connected to the same.

[0033] In general, the organic light emitting display panel expresses an image by voltage-driving or by current-driving the organic light emitting cells of $N \times M$ arranged in the form of a matrix.

[0034] The organic light emitting diode having diode characteristics (generally called the OLED) includes an anode (ITO), an organic thin film (organic layer) and a cathode (metal) as depicted in Fig. 1. The organic thin film may include a multilayered structure including an emitting layer EML, an electron transport layer ETL transporting electrons and a hole transport layer HTL transporting holes to ensure the balance of holes, thus improving the luminescent efficiency. Moreover, an electron injecting layer EIL injecting electrons may be further established on one side of the electron transport layer and a hole injecting layer injecting holes may be also further established on one side of the hole transport layer. Furthermore, in case of a phosphorescent organic light emitting diode, a hole blocking layer HBL may be selectively formed between the emitting layer EML and the electron transport layer ETL and an electron blocking layer EBL may be selectively arranged between the emitting layer EML and the hole transport layer HTL. In addition, the organic thin film (organic layer) may be formed in a slim organic light emitting diode structure in which two kinds of layers are mixed with each other, thus reducing the thickness. For example, a hole injection transport layer HITL structure, in which the hole injecting layer HIL, and the hole transport layer HTL are simultaneously established, and an electron injection transport layer EITL, in which the electron injecting layer EIL and the electron transport layer ETL are simultaneously formed, may be selectively provided. The slim organic light emitting diode aims at improving the luminescent efficiency. A buffer layer may be selectively formed between the anode and the emitting layer EML. The buffer layer may be classified into an electron buffer layer buffering electrons and a hole buffer layer buffering holes. The electron buffer layer may be selectively formed between the cathode and the electron injecting layer EIL and established on behalf of the function of the electron injecting layer EIL. Here, a stack structure of the organic thin film may be emitting layer EML/electron transport layer ETL/electron buffer layer/cathode. The hole buffer layer may be selectively established between the anode and the hole injecting layer EIL and provided on behalf of the function of the hole injecting layer HIL. Here, a stack structure of the organic thin film may be anode/hole buffer layer/hole transport layer HTL/emitting layer EML.

[0035] As driving methods for driving the above-described organic light emitting diode, a passive matrix method and an active matrix method are widely known. The passive matrix method has advantages in that the manufacturing process is simple and the investment cost is low by arranging the anode and the cathode orthogonally and selectively driving the lines; however it has a drawback in that the current consumption is increased when applied to a large-size display. The active matrix driving method has advantages in that the current consumption is low, it provides an excellent image quality and a long lifespan and it is possible to readily fabricate medium and large-size display by establishing an active element and a storage capacitor like a thin film transistor in the respective pixels. As described above, a pixel circuit configuration based on the organic light emitting diode and the thin film transistor is necessary in the active matrix method. Here, as the thin film transistor, an amorphous silicon thin film transistor or a polycrystalline silicon thin film transistor is applied thereto. Referring to Fig. 2, a pixel circuit of an organic light emitting display is depicted. Fig. 3 shows a driving timing diagram of the pixel circuit depicted in Fig. 2. Such a pixel circuit is directed to an exemplary one of the pixel circuits of an $N \times M$ number. As depicted in Fig. 2, the pixel circuit of the organic light emitting display includes a scan signal line $S[N]$ supplying a scan signal, a data signal line $D[M]$ supplying a data signal, a first power source line VDD supplying a first power voltage, a second power source line VSS supplying a second power voltage, a driving

transistor DR_TR, a switching transistor SW_TR, a storage capacitor C and an organic light emitting diode OLED. Here, the first power voltage may have a level higher than that of the second power voltage.

[0036] The operation of the above-described pixel circuit for one frame will be described with reference to Fig. 3.

[0037] As shown in Fig. 3, a scan signal is supplied and then a data signal is supplied for a slight time difference. The reason of the slight time difference is to ensure a margin from the time that the switching transistor is turned on by the supplied scan signal to the time that the data signal is supplied. Describing the pixel circuit of Fig. 2 based on the timing diagram of Fig. 3, if a scan signal is supplied from the scan signal line S[N], the switching transistor SW_TR is turned on. Accordingly, a data signal (voltage) from the data line D[M] is supplied to a control electrode of the driving transistor DR_TR and a first electrode A of the storage capacitor C.

[0038] Accordingly, as a first power voltage from the first power source line VDD is supplied to the organic light emitting diode OLED through the driving transistor DR_TR, the organic light emitting diode OLED emits light at a predetermined brightness for one frame. Since the data voltage supplied from the data line D[M] is stored in the storage capacitor C, the driving transistor DR_TR is kept in a turned-on state for one frame, even though the scan signal from the scan signal line S[N] is cut off.

[0039] Moreover, current in a forward direction from the anode to the cathode is continuously applied to the organic light emitting diode as the frames proceed. That is, if current flows in the organic light emitting diode in one direction from the anode to cathode, space charges are stored between a hole transport layer HTL and an emitting layer EML or between an electron transport layer ETL and an emitting layer EML of the organic thin film. Due to the accumulation of the space charges, the current IOLED flowing in the organic light emitting diode OLED may be dropped. Accordingly, as the brightness of the respective pixels may be decreased, the brightness of the organic light emitting display applying the pixel circuits is lowered gradually with time. Furthermore, the lifespan of the organic light emitting display may be shortened, and due to the difference of the degradation degrees of the organic light emitting diodes in the respective pixel circuits, the brightness of the whole organic light emitting display becomes non-uniform as a result.

[0040] Moreover, if driving the organic light emitting display in the progressive scanning method, it may cause a problem in ensuring an operation margin of the driving circuit when driving a large-size panel. Furthermore, if driving the organic light emitting display using one first power source line VDD in the progressive scanning method, the first power source line VDD is coupled to the organic light emitting display through the respective pixel circuits and thereby it causes a problem in that the brightness is decreased as it goes far from the first power source line VDD.

[0041] Referring to Fig. 4, a basic structure diagram of an organic light emitting display in accordance with the present invention driven in a progressive scanning method is depicted.

[0042] As depicted in Fig. 4, an organic light emitting display 100 may include a scan signal driver 110, a data signal driver 120, an emission control signal driver 130, an organic light emitting display panel 140 (hereinafter referred to as the panel 140), a first power supply unit 150, a second power supply unit 160, and an initial power supply unit 170.

[0043] The scan signal driver 110 may supply scan signals to the panel 140 in sequence through a plurality of scan signal lines S[1] to S[N].

[0044] The data signal driver 120 may supply data signals to the panel 140 through a plurality of data signal lines D[1] to D[M].

[0045] The emission control signal driver 130 may in sequence supply an emission control signal and an emission reverse control signal to the panel 140 through a plurality of emission control signal lines EM[1] to EM[N] and a plurality of emission reverse control signal lines EMB[1] to EMB[N]. Moreover, the panel 140 may include a plurality of scan signal lines S[1] to S[N], a plurality of emission control signal lines EM[1] to EM[N] and a plurality of emission reverse control signals EMB[1] to EMB[N], arranged in the vertical direction, a plurality of data signal lines D[1] to D[M] arranged in the horizontal direction, and a plurality of pixel circuits 142 defined by the scan signal lines S[1] to S[N], the emission control signal lines EM[1] to EM[N], the emission reverse control signal lines EMB[1] to EMB[N] and the data signal lines D[1] to D[M].

[0046] Here, the pixel circuit 142 may be formed in a pixel area defined by the scan line and the data line. Of course, as described above in detail, the scan signals may be supplied from the scan signal driver 110 to the scan signal lines S[1] to S[N], the data voltages may be supplied from the data signal driver 120 to the data signal lines D[1] to D[M], and the emission control signals and the emission reverse control signals may be supplied from the emission control signal driver 130 to the emission control signal lines EM[1] to EM[N] and the emission reverse control signal lines EMB[1] to EMB[N].

[0047] Moreover, the first power supply unit 150, the second power supply unit 160 and the initial power supply unit 170 supply a first power voltage, a second power voltage and an initial power voltage to the pixel circuits 142, respectively.

[0048] As depicted in Fig. 4, the scan signal driver 110, the data signal driver 120, the emission control signal driver 130, the panel 140, the first power supply unit 150, the second power supply unit 160 and the initial power supply unit 170 may be arranged all on a single substrate 102.

[0049] Especially, the drivers 110, 120 and 130 and the power supply units 150, 160 and 170 may be established on the identical layer where the scan signal lines S[1] to S[N], the data signal lines D[1] to D[M], the emission control signal

lines EM[1] to EM[N], the emission reverse control signal lines EMB[1] to EMB[N] and the pixel circuits 142 are established.

[0050] It is possible to form the drivers 110, 120 and 130 and the power supply units 150, 160 and 170 on a separate substrate, not depicted, different from the substrate 102, and electrically connect the substrate with the substrate 102. Furthermore, the drivers 110, 120 and 130 and the power supply units 150, 160 and 170 may be arranged in a form selected from the group consisting of a tape carrier package TCP, a flexible printed circuit FPC, a tape automatic bonding TAB, a chip on glass COG and an equivalent thereof coupled to the substrate 102; however, the form and the position of the drivers 110, 120 and 130 and the power supply units 150, 160 and 170 are not limited thereto in the present invention.

[0051] Referring to Fig. 5, a circuit diagram depicting a pixel circuit of an organic light emitting display in accordance with an exemplary embodiment of the present invention is depicted. The pixel circuit described below denotes one of the pixel circuits in the organic light emitting display 100 depicted in Fig. 4. As depicted in Fig. 5, the pixel circuit of the organic light emitting display in accordance with the present invention may include a scan signal line S[N], a previous scan signal line S[N-1], a data signal line D[M], an emission control signal line EM[N], an emission reverse control signal line EMB[N], a first power source line VDD, a second power source line VSS, a first switching transistor SW_TR1, a second switching transistor SW_TR2, a third switching transistor SW_TR3, a fourth switching transistor SW_TR4, a driving transistor DR_TR, an initial switching transistor SW_TR5, a switching transistor SW_TR6 for applying a reverse bias and a storage capacitor C.

[0052] The scan signal line S[N] supplies a scan signal for selecting an organic light emitting diode OLED to be turned on to a control electrode of the first switching transistor SW_TR1.

[0053] Moreover, the scan signal line S[N] supplies a scan signal to a control electrode of the fourth switching transistor SW_TR4 so that the fourth switching transistor SW_TR4 may be coupled to a gate and a drain of the driving transistor DR_TR to be diode-like connected thereto. The scan signal line S[N] may be coupled to the scan signal driver 110 generating scan signals (See Fig. 4).

[0054] The previous scan signal line S[N-1] supplies a previous scan signal to a control electrode of the initial switching transistor SW_TR5. The initial switching transistor SW_TR5 is configured to be coupled to the initial power source line Vinit, the storage capacitor C and a control electrode of the driving transistor DR_TR, thus initializing the storage capacitor C and the control electrode of the driving transistor DR_TR. The previous scan signal line S[N-1] may be coupled to the scan signal driver 110 generating scan signals (See Fig. 4).

[0055] The data signal line D[M] supplies a data signal (voltage) in proportion to a luminescent brightness to a first electrode A of the storage capacitor C and the driving transistor DR_TR. The data signal line D[M] may be coupled to the data signal driver 120 generating data signals (See Fig. 4).

[0056] The emission control signal line EM[N], coupled to the second switching transistor SW_TR2 and the third switching transistor SW_TR3, supplies an emission control signal. If the second switching transistor SW_TR2 and the third switching transistor SW_TR3 are turned on by the emission control signal, a current corresponding to the data signal stored in the storage capacitor C may be applied from the first power source line VDD to the organic light emitting diode OLED through the driving transistor DR_TR. Accordingly, the organic light emitting diode OLED can emit light. The emission control signal line EM[N] may be coupled to the emission control signal driver 130 generating emission control signals (See Fig. 4).

[0057] The emission reverse control signal line EMB[N] supplies a signal of low level to a control electrode the switching transistor SW_TR6 for applying a reverse bias when the emission control signal is high level. If the switching transistor SW_TR6 for applying a reverse bias is turned on by the emission reverse control signal, a reverse bias voltage may be applied to the organic light emitting diode OLED. The emission reverse control signal line EMB[N] may be coupled to the emission control signal driver 130 generating emission control signals (See Fig. 4). Substantially, the emission reverse control signal may be readily obtained by coupling an inverter to a previous end of an output end of the emission control signal driver outputting the emission control signal.

[0058] The first power source line VDD serves to supply a first power voltage to the organic light emitting diode OLED. The first power source line VDD may be coupled to the first power supply unit 150 supplying the first power voltage (See Fig. 4).

[0059] The second power source line VSS serves to supply a second power voltage to the organic light emitting diode OLED. The second power source line VSS may be coupled to the second power supply unit 160 supplying the second power voltage (See Fig. 4). Here, the first power voltage may be high level compared with the second power voltage.

[0060] Moreover, as the second power voltage, a ground voltage may be used.

[0061] The initial power source line Vinit initializes the storage capacitor C and the control electrode of the driving transistor DR_TR. The initial power source line Vinit may be coupled to the initial power supply unit 170 supplying the initial power voltage (See Fig. 4).

[0062] A first electrode (source electrode or drain electrode) of the first switching transistor SW_TR1 is coupled to the data signal line D[M], a second electrode thereof (drain electrode or source electrode) may be coupled to a first electrode (source electrode or drain electrode) of the driving transistor DR_TR and a control electrode thereof (gate electrode) may be coupled to the scan signal line S[N]. Such a first switching transistor SW_TR1 may be a P-channel transistor.

The first switching transistor SW_TR1 is turned on, if a scan signal of low level is applied to the control electrode thereof through the scan signal line S[N], to supply a value subtracting a threshold voltage V_{th} of the driving transistor from the data voltage to the first electrode A of the storage capacitor C.

[0063] A first electrode of the driving transistor DR_TR is coupled to the second electrode of the first switching transistor SW_TR1, a second electrode thereof is coupled to a first electrode of the third switching transistor SW_TR3, and a control electrode thereof may be coupled to a second electrode of the fourth switching transistor SW_TR4 and a first electrode A of the storage capacitor C. Such a driving transistor DR_TR may be a P-channel transistor. The driving transistor DR_TR is turned on, if a signal of low level is applied to the control electrode thereof, and supplies current of a predetermined amount from the first power source line VDD to the organic light emitting diode OLED. Since the data signal is supplied to the first electrode A of the storage capacitor C to charge the same, the signal of low level is applied to the control electrode of the driving transistor DR_TR continuously by the charged voltage of the storage capacitor C for a predetermined time, even if the first switching transistor SW_TR1 is turned off. Here, the driving transistor DR_TR may be one selected from the group consisting of an amorphous silicon thin film transistor, a polysilicon thin film transistor, an organic thin film transistor, a nano thin film transistor and an equivalent thereof; however, the material or the kind thereof are not limited thereto.

[0064] Moreover, if the driving transistor DR_TR is the polysilicon thin film transistor, it may be fabricated through a process selected from the group consisting of a laser crystallization, a metal-induced crystallization, a high-pressure crystallization and an equivalent thereof; however, the process of fabricating the polysilicon thin film transistor is not limited thereto in the present invention. The laser crystallization is directed to a process in which an excimer laser, for example, is irradiated to an amorphous silicon to be crystallized, the metal-induced crystallization is a process in which a metal is positioned on the amorphous silicon and a predetermined heat, for example, is applied thereto to cause the crystallization of the metal, and the high-pressure crystallization is a process in which a predetermined pressure, for example, is applied to the amorphous silicon to be crystallized. Moreover, if the driving transistor DR_TR is fabricated through the metal-induced crystallization, the driving transistor DR_TR may further include any one selected from the group consisting of nickel Ni, cadmium Cd, cobalt Co, titanium Ti, palladium Pd, tungsten W, aluminum Al and an equivalent thereof.

[0065] An anode of the organic light emitting diode OLED may be coupled to a first electrode of a switching transistor SW_TR6 for applying a reverse bias and a second electrode of the third switching transistor SW_TR3 and a cathode thereof may be coupled to the second power source line VSS. Such an organic light emitting diode OLED emits light at a predetermined brightness by current controlled through the driving transistor DR_TR while the third switching transistor SW_TR3 is being turned on.

[0066] Subsequently, the organic light emitting diode OLED includes an emitting layer, not depicted, and the emitting layer may be any one selected from the group consisting of a fluorescent material, a phosphorescent material, a mixture thereof and an equivalent thereof; however, the material or the kind thereof are not limited thereto. Moreover, the emitting layer may be any one selected from the group consisting of a red light emitting material, a green light emitting material, a blue light emitting material, a mixture thereof and an equivalent thereof; however, the material or the kind thereof are not limited thereto.

[0067] A first electrode of the second switching material SW_TR2 may be coupled to the first power source line VDD and a second electrode B of the storage capacitor C, a second electrode thereof may be coupled to the second electrode of the first switching transistor SW_TR1 and a first electrode of the driving transistor DR_TR, and a control electrode thereof may be coupled to the emission control signal line EM[N].

[0068] Such a second switching transistor SW_TR2 may be a P-channel transistor and is turned on, if a signal of low level is applied to the control electrode thereof through the emission control signal line EM[N], to make the current from the first power source line VDD to flow in the organic light emitting diode OLED.

[0069] A first electrode A of the storage capacitor C may be connected to the control electrode of the driving transistor DR_TR, the second electrode of the fourth switching transistor SW_TR4 and a first electrode of the initial switching transistor SW_TR5, a second electrode thereof may be coupled to a first electrode of the second switching transistor SW_TR2 and the first power source line VDD.

[0070] Such a storage capacitor C maintains the data signal voltage and the threshold voltage V_{th} of the driving transistor at the first electrode thereof for a predetermined time and, if the second switching transistor SW_TR2 and the third switching transistor SW_TR3 are turned on as a signal of low level is applied thereto by the emission control signal line EM[N], makes the current in proportion to the magnitude of the data signal to flow from the first power source line VDD to the organic light emitting diode OLED so that the organic light emitting diode OLED emits light.

[0071] A first electrode of the fourth switching transistor SW_TR4 may be coupled to a second electrode of the driving transistor DR_TR, a second electrode thereof may be coupled to the control electrode of the driving transistor DR_TR and the first electrode A of the storage capacitor C, and a control electrode thereof may be coupled to the scan signal line S[N]. Such a fourth switching transistor SW_TR4 may be a P-channel transistor and is turned on, if a signal of low level is applied from the scan signal line S[N], to electrically connect the control electrode (gate electrode) with second

electrode (drain electrode) of the driving transistor DR_TR, to be diode-like connected thereto as a result.

[0072] A first electrode of the initial switching transistor SW_TR5 may be coupled between the initial power source line Vinit and a second electrode of the switching transistor SW_TR6 for applying a reverse bias, a second electrode thereof may be coupled to the first electrode A of the storage capacitor C, a control electrode thereof may be coupled to the previous scan signal line S[N-1]. Such an initial switching transistor SW_TR5 may be a P-channel transistor and is turned on, if a signal of low level is applied from the previous scan signal line S[N-1], to electrically connect the initial power source line Vinit, the first electrode A of the storage capacitor C and the control electrode of the driving transistor DR_TR. Accordingly, the storage capacitor C and the control electrode of the driving transistor DR_TR are initialized.

[0073] A first electrode of the third switching transistor SW_TR3 may be coupled to the second electrode of the driving transistor DR_TR, a second electrode thereof may be coupled to the anode of the organic light emitting diode OLED, and a control electrode may be coupled to the emission control signal line EM[N]. Such a third switching transistor SW_TR3 may be a P-channel transistor and is turned on, if a signal of low level is applied from the emission control signal line EM[N], to electrically connect the driving transistor DR_TR with the organic light emitting diode OLED so that the current is applied from the driving transistor DR_TR to the organic light emitting diode OLED.

[0074] A first electrode of the switching transistor SW_TR6 for applying a reverse bias may be coupled to the anode of the organic light emitting diode OLED, a second electrode thereof may be coupled to the initial power source line Vinit, and a control electrode thereof may be coupled to the light emitting reverse control line EMB[N]. Such a switching transistor SW_TR6 for applying a reverse bias may be a P-channel transistor and is turned on, if a signal of low level is applied from the emission reverse control signal line EMB[N], to apply a reverse bias voltage to the organic light emitting diode OLED in the direction from the second power source line VSS to the initial power source line Vinit. To apply such a reverse bias voltage, it is desirable that the voltage of the second power source line VSS be higher than that of the initial power source line Vinit. If using a ground voltage as the voltage of the second power source line VSS, i.e., the cathode voltage of the organic light emitting diode OLED, the voltage of the initial power source line Vinit may have a negative value desirably.

[0075] Here, the first switching transistor SW_TR1, the driving transistor DR_TR, the second switching transistor SW_TR2, the third switching transistor SW_TR3, the fourth switching transistor SW_TR4, the initial switching transistor SW_TR5 and the switching transistor SW_TR6 for applying a reverse bias may be any one of the P-channel transistor and an equivalent thereof; however, the kind of the transistor is not limited hereto.

[0076] Referring to Fig. 6, a driving timing diagram, in which the pixel circuit depicted in Fig. 5 is driven in the progressive scanning method, is depicted. As depicted in the figure, if the pixel circuit of the organic light emitting display in accordance with the present invention is driven in the progressive scanning method, a frame may be classified into a first period, a second period and a third period. More specifically, a frame may include an initialization period T11, a storage period T12 for storing a data voltage and a threshold voltage of the driving transistor and a light emission period T13. During the initialization period T11 and the storage period T12 for storing a data voltage and a threshold voltage of the driving transistor, a reverse bias voltage is applied to the organic light emitting diode OLED. The ratio of the initialization period T11, the storage period T12 for storing a data voltage and a threshold voltage of the driving transistor and the light emission period T13 may be made variously and, it is desirable that the times of the initialization period T11 and the storage period T12 for storing a data voltage and a threshold voltage of the driving transistor be set shorter than that of the light emission period T13.

[0077] Referring to Fig 7, a current flow in the initialization period T11, in which the pixel circuit depicted in Fig. 5 is driven in the progressive scanning method, is depicted. Here, the operation of the pixel circuit will be described with reference to the timing diagram of Fig. 6.

[0078] First, the initial switching transistor SW_TR 5 is turned on as a scan signal of low level is applied from the previous scan signal line S[N-1] to the control electrode of the initial switching transistor SW_TR5, and the switching transistor SW_TR6 for applying a reverse bias is turned on as a signal of low level of the emission reverse control signal line EMB[N] is applied to the control electrode of the switching transistor SW_TR6 for applying a reverse bias. As the initial switching transistor SW_TR5 is turned on, the initial power voltage of the initial power source line Vinit is applied to a node, in which the first electrode A of the storage capacitor C is coupled to the control electrode of the driving transistor DR_TR, thus initializing the stored voltage of the storage capacitor C and the control electrode of the driving transistor DR_TR. Here, since the third switching transistor SW_TR3 is turned off as a signal of high level of the emission control signal line EM[N] is applied to the control electrode of the third switching transistor SW_TR3, the organic light emitting diode OLED does not emit light. If the voltage of the second power source line VSS is set higher than that of the initial power source line Vinit during such a non-light emission period, a reverse bias voltage is applied to the organic light emitting diode OLED, thus preventing degradation of the organic light emitting diode OLED. Moreover, a ground voltage may be used as the voltage of the second power source line VSS. In this case, a reverse bias voltage can be applied to the organic light emitting diode OLED if the voltage of the initial power source line Vinit applied thereto is a negative voltage. During such a period, the first switching transistor SW_TR1, the fourth switching transistor SW_TR4, the second switching transistor SW_TR2 and the third switching transistor SW_TR3 are turned off as a signal of high

level is applied to the respective control electrodes. In other words, during the initialization period T11, the storage capacitor C and the control electrode of the driving transistor DR_TR are initialized and, simultaneously, a reverse bias voltage is applied thereto during the non-light emission period of the organic light emitting diode OLED.

[0079] Referring to Fig. 8, a current flow during the storage period T12 for storing a data voltage and a threshold voltage of the driving transistor, in which the pixel circuit depicted in Fig. 5 is driven in the progressive scanning method, is depicted. Here, the operation of the pixel circuit will be described with reference to the timing diagram of Fig. 6.

[0080] First, the scan signal line S[N] is coupled to the control electrode of the first switching transistor SW_TR1. The first switching transistor SW_TR1 is turned on, if a scan signal of low level is applied from the scan signal line S[N], and then a data signal is applied from the data signal line D[M]. Moreover, the scan signal of low level of the scan signal line S[N] is applied to the control electrode of the fourth switching transistor SW_TR4 to be turned on. The fourth switching transistor SW_TR4 is coupled between the control electrode (gate electrode) and the second electrode (drain electrode) of the driving transistor DR_TR, thus making a diode-like connection.

[0081] The present invention including such a diode-like connection has a function of compensating the threshold voltage of the driving transistor. The principle of compensating the threshold voltage of the driving transistor will be described with reference to the following formula 1.

[0082] Under the diode-like connection, the first power voltage VDD is applied to the second electrode B of the storage capacitor C and a voltage VDATA-|Vth| corresponding to a difference between the data voltage VDATA and the threshold voltage Vth of the driving transistor is applied to the first electrode A of the storage capacitor C. Referring to Fig. 9, a current flow during the light emission period T13, in which the pixel circuit depicted in Fig. 5 is driven in the progressive scanning method, is depicted, and the description will be given with reference to the timing diagram of Fig. 6.

[0083] Here, the current IOLED flowing in the organic light emitting diode OLED is the same as the following formula 1;

[Formula 1]

$$I_{OLED} = \frac{\beta}{2} (V_{GS} - V_{th})^2 = \frac{\beta}{2} (V_{SG} - |V_{th}|)^2 = \frac{\beta}{2} (V_{DD} - (V_{DATA} - |V_{th}|) - |V_{th}|)^2$$

$$I_{OLED} = \frac{\beta}{2} (V_{DD} - V_{DATA})^2$$

wherein VDD denotes a first power voltage of the first power source line, VDATA denotes a data voltage applied through the data signal line, Vth denotes a threshold voltage of the driving transistor DR_TR, and β denotes a constant.

[0084] As can be seen from the above formula 1, the current IOLED flowing in the organic light emitting diode OLED during the light emission period T13 flows correspondingly to the data voltage VDATA regardless of the threshold voltage of the driving transistor DR_TR. That is, the threshold voltage Vth of the driving transistor DR_TR is compensated.

[0085] Moreover, as the emission reverse control signal line EMB[N] is coupled to the control electrode of the switching transistor SW_TR6 for applying a reverse bias, the switching transistor SW_TR6 for applying a reverse bias is being kept in a turned-on state by a signal of low level of the emission reverse control signal line EMB[N]. During such a period T12, since the third switching transistor SW_TR3 is being in a turned-off state as a signal of high level of the emission control signal line EM[N] is applied to the control electrode of the third switching transistor SW_TR3, like the initialization period T11, the organic light emitting diode OLED does not emit light. If the voltage of the second power source line VSS is set higher than that of the initial power source line Vinit during such a non-light emission period, a reverse bias voltage is applied to the organic light emitting diode OLED, thus preventing degradation of the organic light emitting diode OLED. Furthermore, a ground voltage may be used as the voltage of the second power source line VSS. In this case, a reverse bias voltage can be applied to the organic light emitting diode OLED if the voltage of the initial power source line Vinit applied thereto is a negative voltage. During such a period, the initial switching transistor SW_TR5, the second switching transistor SW_TR2 and the third switching transistor SW_TR3 are turned off as a signal of high level is applied to the respective control electrodes. In other words, during the storage period T12 for storing a data voltage and a threshold voltage of the driving transistor, the data voltage is stored in the storage capacitor C and, simultaneously, a reverse bias voltage is applied thereto during the non-light emitting period of the organic light emitting diode OLED.

[0086] Referring to Fig. 9, a current flow during the light emission period T13, in which the pixel circuit depicted in Fig. 5 is driven in the progressive scanning method, is depicted, and the description will be given with reference to the timing diagram of Fig. 6. First, if an emission control signal of low level is applied to the control electrode of the second switching transistor SW_TR2 coupled to the emission control signal line EM[N], the second switching transistor SW_TR2 is turned

on, and the first power voltage is supplied from the first power source line VDD to the driving transistor DR_TR. Moreover, if an emission control signal of low level is applied to the control electrode of the third switching transistor SW_TR3 coupled to the emission control signal line EM[N], the third switching transistor SW_TR3 is turned on, and a driving voltage is supplied to the organic light emitting diode OLED through the driving transistor DR_TR. Accordingly, the organic light emitting diode emits light correspondingly to the respective data signals.

[0087] During this period, the first switching transistor SW_TR1, the fourth switching transistor SW_TR4, the initial switching transistor SW_TR5 and the switching transistor SW_TR6 for applying a reverse bias are turned off as a signal of high level is applied to the respective control electrodes.

[0088] In other words, during the light emission period T13, the data voltage stored in the storage capacitor C and the threshold voltage of the driving transistor are applied through the driving transistor DR_TR so that the organic light emitting diode OLED emits light. At this time, the switching transistor SW_TR6 for applying a reverse bias is turned off and thereby it does not perform an operation of applying a reverse bias voltage to the organic light emitting diode OLED. It is desirable that the initialization period T11 and the storage period T12 for storing a data voltage and a threshold voltage of the driving transistor be set shorter than the light emission period T13 so as to prolong the time that the organic light emitting diode OLED emits light.

[0089] Referring to Fig. 10, a pixel circuit of an organic light emitting display in accordance with another embodiment of the present invention is depicted. The pixel circuit depicted in Fig. 10 is identical with that of Fig. 5. However, the first electrode of the switching transistor SW_TR6 for applying a reverse bias in the pixel circuit depicted in Fig. 10 is coupled to the first electrode of the initial switching transistor SW_TR5. That is, the configuration in which the switching transistor SW_TR6 for applying a reverse bias is positioned between the second power source line VSS and the initial power source line Vinit is identical with that of Fig. 5; however, in another embodiment of Fig. 10, the first electrode of the switching transistor SW_TR6 for applying a reverse bias may be coupled to the first electrode of the initial switching transistor SW_TR5, differently from the configuration of Fig. 5, in which the first electrode of the switching transistor SW_TR5 is coupled to a common node between the anode of the organic light emitting diode OLED and the third switching transistor SW_TR3.

[0090] Referring to Fig. 11, a pixel circuit of an organic light emitting display in accordance with still another embodiment of the present invention is depicted. The pixel circuit depicted in Fig. 11 is also identical with that of Fig. 5. However, all transistors depicted in Fig. 11 are N-channel transistors, while all those transistors in the pixel circuit depicted in Fig. 5 are P-channel transistors. Accordingly, the electrical connections between the respective elements are slightly different from those depicted in Fig. 5.

[0091] For example, if the top and bottom of the pixel circuit using P-channel transistors of Fig. 5 are turned over, if the direction of the organic light emitting diode OLED is left the same as Fig. 5, and if the P-channel transistors are replaced with the N-channel transistors, the pixel circuit using N-channel transistors of Fig. 11 can be achieved. Here, the positions of the first electrodes (source electrodes or drain electrodes) and the second electrodes (drain electrodes or source electrodes) of the P-channel transistor and the N-channel transistor are changed reversely.

[0092] Fig. 12 is a driving timing diagram, in which the pixel circuit using the N-channel transistors depicted in Fig. 11 is driven in a progressive scanning method. The N-channel transistor is turned on if a signal of high level is applied to the control electrode thereof. When comparing the driving timing diagram depicted in Fig. 12 with that of Fig. 6, a signal of high level is changed into a signal of low level and a signal of low level is changed into a signal of high level.

[0093] Referring to Fig. 13, a block diagram depicting a basic structure of an organic light emitting display in accordance with the present invention driven in an interlaced scanning method is shown.

[0094] As depicted in Fig. 13, an organic light emitting display 100 may include a scan signal driver 110, a data signal driver 120, an emission control signal driver 130, an organic light emitting display panel 140 (hereinafter referred to as the panel 140), a first power supply unit 150, a second power supply unit 160, and an initial power supply unit 170.

[0095] The scan signal driver 110 may supply scan signals to the panel 140 through a plurality of scan signal lines S[1] to S[N]. As depicted in Fig. 13, the scan signal lines may be configured in such a manner that a first scan signal line and a third scan signal line are coupled to pixels in a first line, and a second scan signal line and a fourth scan signal line are coupled to pixels in a second line. That is, the scan signal lines may be coupled to pixels on odd and even lines in sequence.

[0096] The data signal driver 120 may supply data signals to the panel 140 through a plurality of data signal lines D[1] to D[M].

[0097] The emission control signal driver 130 may supply in sequence emission control signals and emission reverse control signals to the panel 140 through a plurality of emission control signal lines EM[1] to EM[N] and a plurality of emission reverse control signal lines EMB[1] to EMB[N].

[0098] Moreover, the panel 140 may include a plurality of scan signal lines S[1] to S[N], a plurality of emission control signal lines EM[1] to EM[N] and a plurality of emission reverse control signals EMB[1] to EMB[N], arranged in the vertical direction, a plurality of data signal lines D[1] to D[M] arranged in the horizontal direction, and a plurality of pixel circuits 142 defined by the scan signal lines S[1] to S[N], the emission control signal lines EM[1] to EM[N], the emission reverse

control signal lines EMB[1] to EMB[N] and the data signal lines D[1] to D[M].

[0099] Here, the pixel circuit 142 may be formed in a pixel area defined by the scan line and the data line. As described above in detail, the scan signals may be supplied from the scan signal driver 110 to the scan signal lines S[1] to S[N], the data voltages may be supplied from the data signal driver 120 to the data signal lines D[1] to D[M], and the emission control signals and the emission reverse control signals may be supplied from the emission control signal driver 130 to the emission control signal lines EM[1] to EM[N] and the emission reverse control signal lines EMB[1] to EMB[N]. Moreover, the first power supply unit 150, the second power supply unit 160 and the initial power supply unit 170 supply a first power voltage, a second power voltage and an initial power voltage to the pixel circuits 142, respectively.

[0100] As depicted in Fig. 13, the scan signal driver 110, the data signal driver 120, the emission control signal driver 130, the panel 140, the first power supply unit 150, the second power supply unit 160 and the initial power supply unit 170 may be arranged all on a single substrate 102.

[0101] Especially, the drivers 110, 120 and 130 and the power supply units 150, 160 and 170 may be established on the same layer where the scan signal lines S[1] to S[N], the data signal lines D[1] to D[M], the emission control signal lines EM[1] to EM[N], the emission reverse control signal lines EMB[1] to EMB[N] and the pixel circuits 142 are established.

[0102] It is possible to form the drivers 110, 120 and 130 and the power supply units 150, 160 and 170 on a separate substrate, not depicted, different from the substrate 102, and electrically connect the substrate with the substrate 102. Furthermore, the drivers 110, 120 and 130 and the power supply units 150, 160 and 170 may be arranged in a form selected from the group consisting of a tape carrier package TCP, a flexible printed circuit FPC, a tape automatic bonding TAB, a chip on glass COG and an equivalent thereof coupled to the substrate 102; however, the form and the position of the drivers 110, 120 and 130 and the power supply units 150, 160 and 170 are not limited thereto in the present invention.

[0103] Referring to Fig. 14, a driving timing diagram, in which the pixel circuit depicted in Fig. 5 is driven in the interlaced scanning method, is depicted. As depicted in Fig. 14, the pixel circuit of the organic light emitting display in accordance with the present invention proceeds with a first frame, a second frame, a third frame and a fourth frame in sequence, in which the driving timing diagram of the odd frames such as the first frame, the third frame and the fifth frame may be the same and the driving timing diagram of the even frames such as the second frame, the fourth frame and the sixth frame may be the same.

[0104] In more detail, during the odd frame period, each of the pixels on the odd line writes a data voltage and a threshold voltage of the driving transistor to the storage capacitor C in the pixel circuit and, simultaneously, applies a reverse bias voltage to the organic light emitting diode OLED. During such an odd frame period, the pixels on the even line emit light.

[0105] Meanwhile, during the even frame period, each of the pixels on the odd line emits light and each of the pixels on the even line writes a data voltage and a threshold voltage of the driving transistor to the storage capacitor C in the pixel circuit and, simultaneously, applies a reverse bias voltage to the organic light emitting diode OLED.

[0106] Like this, while the pixels on the odd line in the panel emit light as the odd frame and the even frame are performed in sequence, each of the pixels on the even line performs the data write and applies a reverse bias voltage to the organic light emitting diode OLED. While the pixels on the even line in the panel emit light as the odd frame and the even frame are performed in sequence, each of the pixels on the odd line performs the data write and applies a reverse bias voltage to the organic light emitting diode OLED. That is, by driving the pixel circuits in such an interlaced scanning method, it is possible to ensure an operation margin of a driving circuit when driving a large-size panel.

[0107] In order to drive the pixel circuit of Fig. 5 in an interlaced scanning method, the terminal of a pixel in an odd scan line N which according to Fig. 5 would be connected to the previous scan line S[N-1] has to be connected to the previous odd scan line S[N-2] instead. The same applies for a pixel in an even scan line N whose terminal for the previous scan line has to be connected to the previous even scan line S[N-2]. Furthermore, according to the driving scheme illustrated in Fig. 14, the EM and EMB emission control signals will be provided independently to pixels of odd and even scan lines and therefore the terminals of the pixel circuit of Fig. 5 connected to the EM[N] and EMB[N] signals will be connected to either the EM_Odd[N] and EMB_Odd[N] signals or the EM_Even[N] and EMB_Even[N] signals depending on whether the pixel forms part of an odd or even scan line.

[0108] Referring to Fig. 15, a current flow during the initialization period T21 in a pixel circuit on an odd line, in which the pixel circuit depicted in Fig. 5 is driven in the interlaced scanning method, is shown. Here, the operation of the pixel circuit will be described with reference to the driving timing diagram of Fig. 14.

[0109] First, the initial switching transistor SW-TR5 is turned on as a scan signal of low level is applied from the previous scan signal line S[N-2] to the control electrode of the initial switching transistor SW_TR5, and the switching transistor SW_TR6 for applying a reverse bias is turned on as a signal of low level of the emission reverse control signal line EMB_Odd[N] is applied to the control electrode of the switching transistor SW_TR6 for applying a reverse bias.

[0110] As the initial switching transistor SW_TR5 is turned on, an initial power voltage of the initial power source line Vinit is applied to a node, in which the first electrode A of the storage capacitor C is coupled to the control electrode of the driving transistor DR_TR, thus initializing the stored voltage of the storage capacitor C and the control electrode of the driving transistor DR_TR. Here, since the third switching transistor SW_TR3 is turned on as a signal of high level of

the emission control signal line EM_Odd[N] is applied to the control electrode of the third switching transistor SW_TR3, the organic light emitting diode OLED does not emit light. If the voltage of the second power source line VSS is set higher than that of the initial power source line Vinit during such a non-light emission period, a reverse bias voltage is applied to the organic light emitting diode OLED, thus preventing degradation of the organic light emitting diode OLED. Moreover, a ground voltage may be used as the voltage of the second power source line VSS. In this case, a reverse bias voltage can be applied to the organic light emitting diode OLED if the voltage of the initial power source line Vinit applied thereto is a negative voltage.

[0111] During such a period, the first switching transistor SW_TR1, the fourth switching transistor SW_TR4, the second switching transistor SW_TR2 and the third switching transistor SW_TR3 are turned off as a signal of high level is applied to the respective control electrodes.

[0112] In other words, during the initialization period T21 of the pixel circuit on the odd line, the storage capacitor C and the control electrode of the driving transistor DR_TR are initialized and, simultaneously, a reverse bias voltage is applied thereto during the non-light emission period of the organic light emitting diode OLED.

[0113] Referring to Fig. 16, a current flow during the storage period T22 of a data voltage and a threshold voltage of the driving transistor in a pixel circuit on an odd line, in which the pixel circuit depicted in Fig. 5 is driven in the interlaced scanning method, is depicted. Here, the operation of the pixel circuit will be described with reference to the driving timing diagram of Fig. 14.

[0114] First, the scan signal line S[N] is coupled to the control electrode of the first switching transistor SW_TR1. The first switching transistor SW_TR1 is turned on, if a scan signal of low level is applied from the scan signal line S[N], and then a data signal is applied from the data signal line D[M]. Moreover, the scan signal of low level of the scan signal line S[N] is applied to the control electrode of the fourth switching transistor SW_TR4 to be turned on. The fourth switching transistor SW_TR4 is coupled between the control electrode (gate electrode) and the second electrode (drain electrode) of the driving transistor DR_TR, thus making a diode-like connection. The present invention including such a diode-like connection has a function of compensating the threshold voltage of the driving transistor. The principle of compensating the threshold voltage of the driving transistor will be described with reference to the following formula 1.

[0115] Under the diode-like connection, the first power voltage VDD is applied to the second electrode B of the storage capacitor C and a voltage VDATA-|Vth| corresponding to a difference between the data voltage VDATA and the threshold voltage Vth of the driving transistor is applied to the first electrode A of the storage capacitor C.

[0116] Referring to Fig. 17, a current flow during the light emission period T23 in a pixel circuit on an odd line, in which the pixel circuit depicted in Fig. 5 is driven in the interlaced scanning method, is depicted, and the description will be given with reference to the timing diagram of Fig. 14.

[0117] Here, the current IOLED flowing in the organic light emitting diode OLED is the same as the following formula 1:

[Formula 1]

$$I_{OLED} = \frac{\beta}{2} (V_{GS} - V_{th})^2 = \frac{\beta}{2} (V_{SG} - |V_{th}|)^2 = \frac{\beta}{2} (V_{DD} - (V_{DATA} - |V_{th}|) - |V_{th}|)^2$$

$$I_{OLED} = \frac{\beta}{2} (V_{DD} - V_{DATA})^2$$

wherein VDD denotes a first power voltage of the first power source line, VDATA denotes a data voltage applied through the data signal line, Vth denotes a threshold voltage of the driving transistor DR_TR, and β denotes a constant.

[0118] As can be seen from the above formula 1, the current IOLED flowing in the organic light emitting diode OLED during the light emission period T23 flows correspondingly to the data voltage VDATA regardless of the threshold voltage of the driving transistor DR_TR. That is, the threshold voltage Vth of the driving transistor DR_TR is compensated.

[0119] Moreover, as The emission reverse control signal line EMB_Odd[N] is coupled to the control electrode of the switching transistor SW_TR6 for applying a reverse bias, the switching transistor SW_TR6 for applying a reverse bias is being kept in a turned-on state by a signal of low level of The emission reverse control signal line EMB_Odd[N].

[0120] During such a period T22, since the third switching transistor SW_TR3 is being in a turned-off state as a signal of high level of the emission control signal line EM_Odd[N] is applied to the control electrode of the third switching transistor SW_TR3, like the initialization period T21, the organic light emitting diode OLED does not emit light. If the voltage of the second power source line VSS is set higher than that of the initial power source line Vinit during such a non-light emission period, a reverse bias voltage is applied to the organic light emitting diode OLED, thus preventing

degradation of the organic light emitting diode OLED. Furthermore, a ground voltage may be used as the voltage of the second power source line VSS. In this case, a reverse bias voltage can be applied to the organic light emitting diode OLED if the voltage of the initial power source line Vinit applied thereto is a negative voltage.

[0121] During such a period, the initial switching transistor SW_TR5, the second switching transistor SW_TR2 and the third switching transistor SW_TR3 are turned off as a signal of high level is applied to the respective control electrodes.

[0122] In other words, during the storage period T22 for storing a data voltage and a threshold voltage of the driving transistor, the data voltage is stored in the storage capacitor C and, simultaneously, a reverse bias voltage is applied thereto during the non-light emission period of the organic light emitting diode OLED.

[0123] Referring to Fig. 17, a current flow during the light emission period T23 in a pixel circuit on an odd line, in which the pixel circuit depicted in Fig. 5 is driven in the interlaced scanning method, is depicted, and the description will be given with reference to the timing diagram of Fig. 14. First, if an emission control signal of low level is applied to the control electrode of the second switching transistor SW_TR2 coupled to the emission control signal line EM_Odd[N], the second switching transistor SW_TR2 is turned on, and the first power voltage is supplied from the first power source line VDD to the driving transistor DR_TR.

[0124] Moreover, if an emission control signal of low level is applied to the control electrode of the third switching transistor SW_TR3 coupled to the emission control signal line EM_Odd[N], the third switching transistor SW_TR3 is turned on, and a driving voltage is supplied to the organic light emitting diode OLED through the driving transistor DR_TR. Accordingly, the organic light emitting diode emits light correspondingly to the respective data signals.

[0125] During this period, the first switching transistor SW_TR1, the fourth switching transistor SW_TR4, the initial switching transistor SW_TR5 and the switching transistor SW_TR6 for applying a reverse bias are turned off as a signal of high level is applied to the respective control electrodes.

[0126] In other words, during the light emission period T23, the data voltage stored in the storage capacitor C and the threshold voltage of the driving transistor are applied through the driving transistor DR_TR so that the organic light emitting diode OLED emits light. At this time, the switching transistor SW_TR6 for applying a reverse bias is turned off and thereby it does not perform an operation of applying a reverse bias voltage to the organic light emitting diode OLED.

[0127] Referring to Fig. 18, a current flow during the initialization period in a pixel circuit on an even line, in which the pixel circuit depicted in Fig. 5 is driven in the interlaced scanning method, is depicted. Referring to Fig. 19, a current flow during the storage period of a data voltage and a threshold voltage of the driving transistor in a pixel circuit on an even line, in which the pixel circuit depicted in Fig. 5 is driven in the interlaced scanning method, is shown. Referring to Fig. 20, a current flow during the light emission period in a pixel circuit on an even line, in which the pixel circuit depicted in Fig. 5 is driven in the interlaced scanning method, is drawn. Here, the operation of the pixel circuit will be described with reference to the driving timing diagram of Fig. 14.

[0128] During the first frame period, the pixel circuits on the odd line proceed with the initialization period T21 and the storage period T22 of a data voltage and a threshold voltage of the driving transistor in sequence, and the pixel circuits on the even line perform the light emission operation of the organic light emitting diodes OLEDs as can be seen from the current flow depicted in Fig. 20. During the second frame period, the pixel circuits on the even line execute the initialization period and the storage period of a data voltage and a threshold voltage of the driving transistor in sequence, and the pixel circuits on the odd line emit light.

[0129] The current flow diagrams of the pixel circuits on the even line depicted in Figs. 18, 19 and 20 are the same as the pixel circuits on the odd line shown in Figs. 15, 16 and 17; however, those have differences in that the pixel circuits on the odd line execute the initial and data write operations during the odd frame period, whereas, the pixel circuits on the even line perform the initial and data write operations during the even frame period.

[0130] Referring to Fig. 21, an electrical connection between the first power source line including (odd line and even line) and the respective pixels of the organic light emitting display depicted in Fig. 13 is shown. The first power source line may include two lines of an odd first power source line VDD/Odd and an even first power source line VDD/Even; however, the second power source line VSS is composed of one line.

[0131] If driving the first power source line VDD with such two lines, and if dividing the data write period from the light emission period in driving the panel by applying an interlaced scanning method, it is possible to prevent a voltage drop (IR-drop) of the first power source line VDD, which will be described in more detail with reference to the driving timing diagram depicted in Fig. 14 below.

[0132] During the first frame period, the pixel circuit on the odd line initializes the storage capacitor C and the control electrode of the driving transistor, writes data in the storage capacitor C and applies a reverse bias voltage to the organic light emitting diode OLED. During such a first frame period, the third switching transistor SW_TR3 in the pixel circuit is turned off and thereby the electrical connection from the odd first power source line VDD/Odd to the second power source line VSS are cut off in the pixel circuits on the odd line. Accordingly, during the first frame period, the pixel circuits on the odd line perform the data write operation without any voltage drop (IR-drop),

[0133] Such pixel circuits on the odd line emit light during the second frame period, in which the current flow of the pixel circuit on the odd line is the same as depicted in Fig. 17.

[0134] At this time, the current flowing in the organic light emitting diode is the same as formula 1:

[Formula 1]

$$I_{OLED} = \frac{\beta}{2} (V_{GS} - V_{th})^2 = \frac{\beta}{2} (V_{SG} - |V_{th}|)^2 = \frac{\beta}{2} (V_{DD} - (V_{DATA} - |V_{th}|) - |V_{th}|)^2$$

$$I_{OLED} = \frac{\beta}{2} (V_{DD} - V_{DATA})^2$$

[0135] That is, when the data has been written in the storage capacitor C and then it becomes the light emission period, in the case where there is no voltage drop (IR-drop), the current IOLED flowing in the respective pixel circuit on the odd line has no voltage drop (IR-drop) as can be seen from the above formula 1. Accordingly, the pixels on the odd line have no voltage drop (IR-drop) during the light emission period due to the VDD having no voltage drop (IR-drop), thus preventing the brightness of the pixels from being decreased.

[0136] Likewise, since the data are written in the pixels on the even line in the state where there is no voltage drop (IR-drop) during the second frame period, it is possible to drive the panel without any voltage drop (IR-drop) during the light emission period.

[0137] As described in detail above, if driving the organic light emitting display and the pixel circuits thereof in accordance with the present invention in the progressive scanning method, the image display period of one frame is classified into the first period, the second period and the third period. During the first period, the storage capacitor and the control electrode of the driving transistor are initialized and, simultaneously, a reverse bias voltage is applied to the organic light emitting diode, thus preventing degradation of the organic light emitting diode. Moreover, during the second period, the data voltage and the threshold voltage of the driving transistor are stored in the storage capacitor and, simultaneously, a reverse bias voltage is applied to the organic light emitting diode, thus preventing degradation of the organic light emitting diode. Furthermore, during the third period, the operation of applying a reverse bias voltage to the organic light emitting diode is stopped and, simultaneously, the current corresponding to the data voltage stored in the storage capacitor and the threshold voltage of the driving transistor are supplied to the organic light emitting diode through the driving transistor, thus making the organic light emitting diode emit light.

[0138] The progressive scanning method is to prevent the degradation of the organic light emitting diode by applying a reverse bias voltage to the organic light emitting diode in the non-light emission period, thus improving the lifespan of the organic light emitting diode and the non-uniformity of the brightness of the respective pixels caused by the difference of the degradation degrees of the organic light emitting diodes in the respective pixel circuits.

[0139] Moreover, if driving the organic light emitting display and the pixel circuits thereof in accordance with the present invention in the interlaced scanning method, the image display period is classified into the first frame (odd frame) and the second frame (even frame). During the first frame, each of the pixels on the odd line in sequence stores the data voltage and the threshold voltage of the driving transistor in the storage capacitor and, simultaneously, applies a reverse bias voltage to the organic light emitting diode so that the pixels on the even line emit light.

[0140] During the second frame, each of the pixels on the odd line emits light and each of the pixels on the even line in sequence stores the data voltage and the threshold voltage of the driving transistor and, simultaneously, applies a reverse bias voltage to the organic light emitting diode. As the above frames are performed in sequence, the image display unit (panel) of the organic light emitting display is driven in the interlaced scanning method.

[0141] With the driving method using such an interlaced scanning method, it is possible to ensure an operation margin of a driving circuit when driving a large-size panel and prevent a voltage drop (IR-drop) of the first power source line by dividing the light emission period from the data write period.

[0142] Moreover, it is possible to prevent the degradation of the organic light emitting diode by applying a reverse bias voltage to the organic light emitting diode during the non-light emission period.

Claims

1. A pixel circuit for an organic light emitting display comprising:

a first transistor (SW_TR1) having a first electrode connected to a data signal input and a control electrode connected to a first scan signal input;
 a second transistor (SW_TR2) having a first electrode connected to a second electrode of the first transistor (SW_TR1), a second electrode connected to a first power supply input (VDD), and a control electrode connected to a first emission control signal input;
 a capacitor (C) having a first terminal connected to the first power supply input (VDD);
 a third transistor (DR-TR) having a first electrode connected to the second electrode of the first transistor (SW_TR1), and a control electrode connected to a second terminal of the capacitor (C);
 a fourth transistor (SW_TR3) having a first electrode connected to a second electrode of the third transistor (DR-TR) and a control electrode connected to the first emission control signal input;
 a fifth transistor (SW_TR4) having a first electrode connected to the control electrode of the third transistor (DR-TR), a second electrode connected to the second electrode of the third transistor (DR-TR), and a control electrode connected to the first scan signal input;
 a sixth transistor (SW_TR5) having a first electrode connected to the second terminal of the capacitor (C) and a control electrode connected to a second scan signal input (S[N-1], S[N-2]);
 a seventh transistor (SW_TR6) having a first electrode connected to a second electrode of the fourth transistor (SW_TR3), a second electrode connected to an initialisation power supply input (Vinit), and a control electrode connected to a second emission control signal input (EMB[N], EMB_Odd[N]); and
 an organic light emitting diode having a first electrode connected to the second electrode of the fourth transistor (SW_TR3) and a second electrode connected to a second power supply input (VSS).

2. The pixel circuit of claim 1, wherein a second electrode of the sixth transistor (SW_TR5) is connected to the initialisation power supply input (Vinit).

3. The pixel circuit of claim 1, wherein a second electrode of the sixth transistor (SW_TR5) is connected to the first electrode of the seventh transistor (SW_TR6).

4. The pixel circuit of one of the preceding claims, wherein the first, second, third, fourth, fifth, sixth, and seventh transistors (SW_TR1, SW_TR2, DR-TR, SW_TR3, SW_TR4, SW_TR5, SW_TR6) are PMOS transistors and wherein the first electrode of the organic light emitting diode (OLED) is an anode and the second electrode of the organic light emitting diode (OLED) is a cathode.

5. The pixel circuit of one of the claim 1 through 3, wherein the first, second, third, fourth, fifth, sixth, and seventh transistors (SW_TR1, SW_TR2, DR-TR, SW_TR3, SW_TR4, SW_TR5, SW_TR6) are NMOS transistors and wherein the first electrode of the organic light emitting diode (OLED) is a cathode and the second electrode of the organic light emitting diode (OLED) is an anode.

6. An organic light emitting diode display device comprising:

a scan driver connected to a plurality of scan lines extending in a first direction;
 an emission control driver connected to a plurality of emission control lines extending in the first direction and comprising at least a first emission control line and a second emission control line;
 a data driver connected to a plurality of data lines extending in a second direction crossing the first direction;
 a first power supply adapted to provide a first power supply voltage;
 a second power supply adapted to provide a second power supply voltage;
 an initialisation power supply adapted to provide an initialisation power supply voltage; and
 a plurality of pixels arranged in a plurality of rows, each of the pixels being connected to a corresponding first one and a corresponding second one of the scan lines, to the at least one first emission control line, to the at least one second emission control line, and a corresponding one of the data lines,

characterised in that each of the pixels is a pixel according to one of the preceding claims, wherein the first power supply inputs of the pixels are connected to the first power supply, wherein the second power supply inputs of the pixels are connected to the second power supply, and wherein the initialisation power supply input of the pixels are connected to the initialisation power supply.

7. The organic light emitting diode display device of claim 6, wherein the second scan line is a first scan line of an adjacent previous row of pixels.

8. The organic light emitting diode display device of claim 6, wherein the second scan line of an odd row of pixels is a first scan line of a previous odd row of pixels and wherein the second line of an even row of pixels is a first scan line of a previous even row of pixels.

5 9. The organic light emitting diode display device of claim 8, wherein the first emission control signal inputs of the pixels of the odd row of pixels are connected to the at least one first emission control line, the second emission control signal inputs of the pixels of the odd row of pixels are connected to the at least one second emission control line, the first emission control signal inputs of the pixels of the even row of pixels are connected to the at least one second emission control line, and the second emission control signal inputs of the pixels of the even row of pixels are connected to the at least one first emission control line.

10 10. The organic light emitting diode display device of one of the claims 8 or 9, wherein the first power supply inputs of the pixels of the odd row are connected to a first power supply line and wherein the first power supply inputs of the pixels of the even row are connected to a second power supply line.

15 11. The organic light emitting diode display device of one of the claims 6 through 10, wherein the second power supply voltage has a voltage value between a voltage value of the first power supply voltage and a voltage value of the initialisation power supply voltage.

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FIG. 1

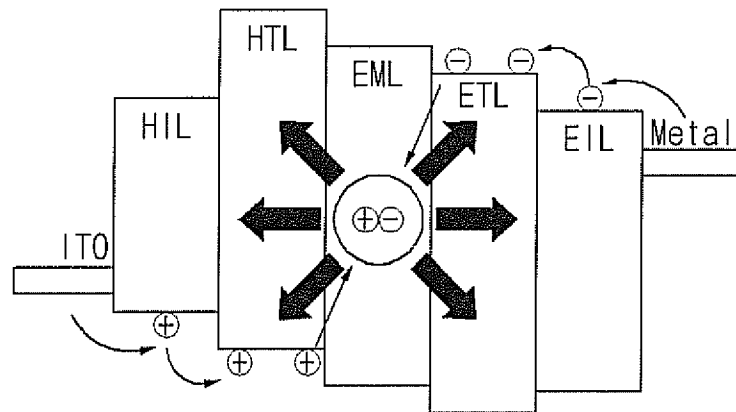


FIG. 2

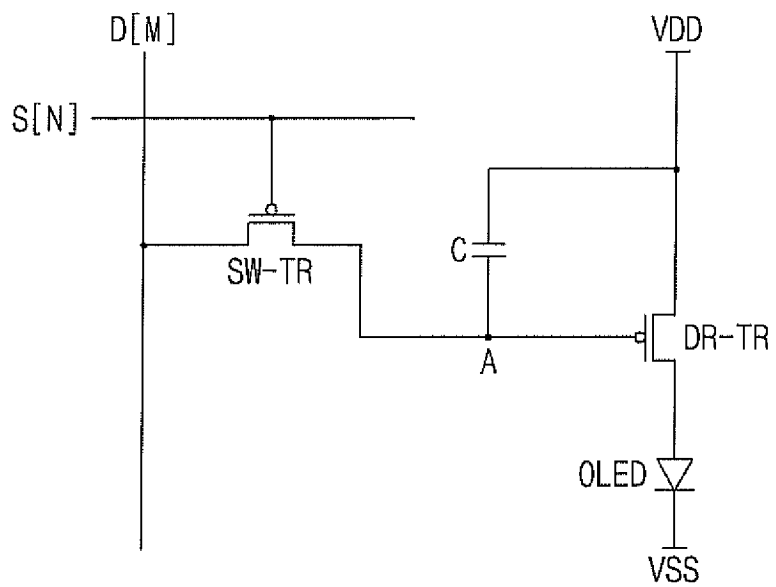


FIG. 3

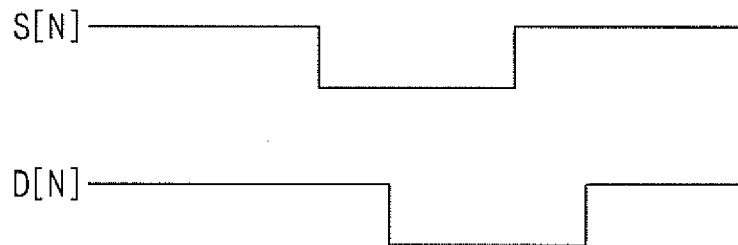


FIG. 4

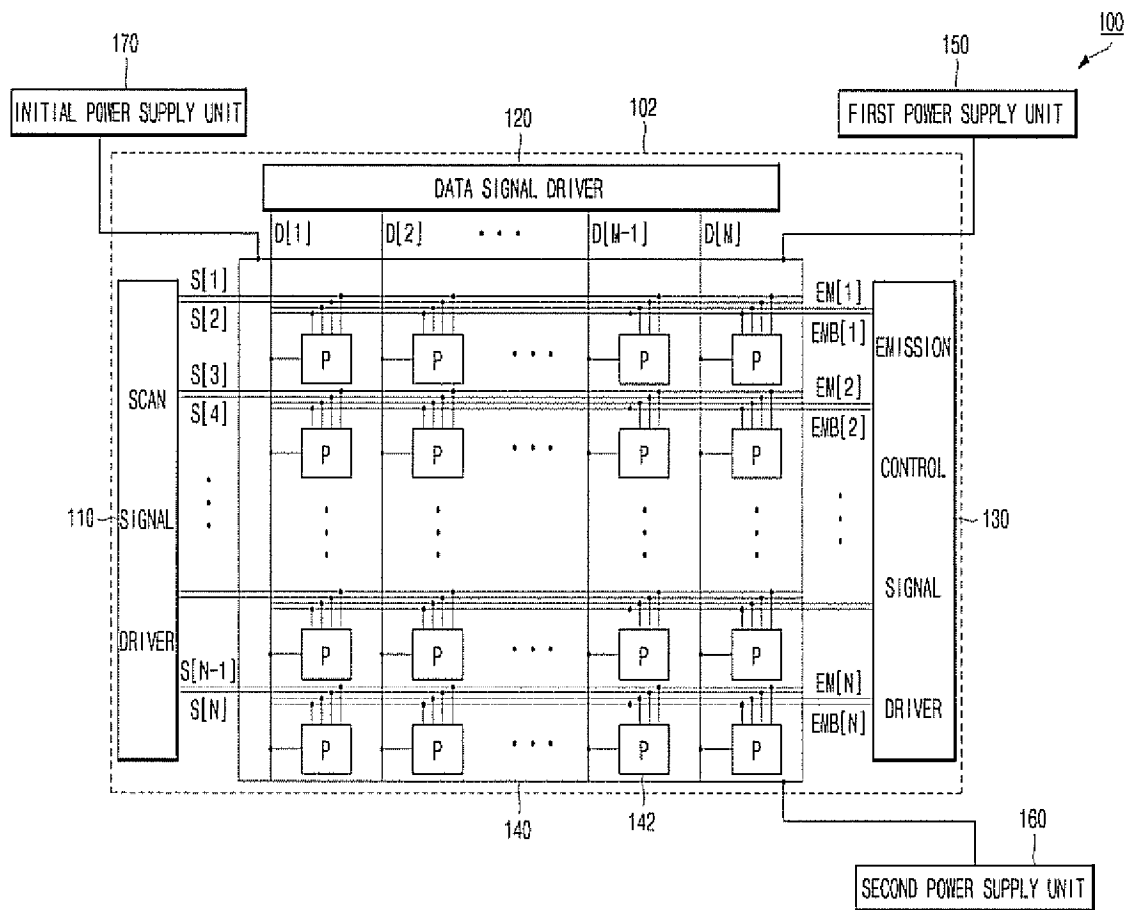


FIG. 5

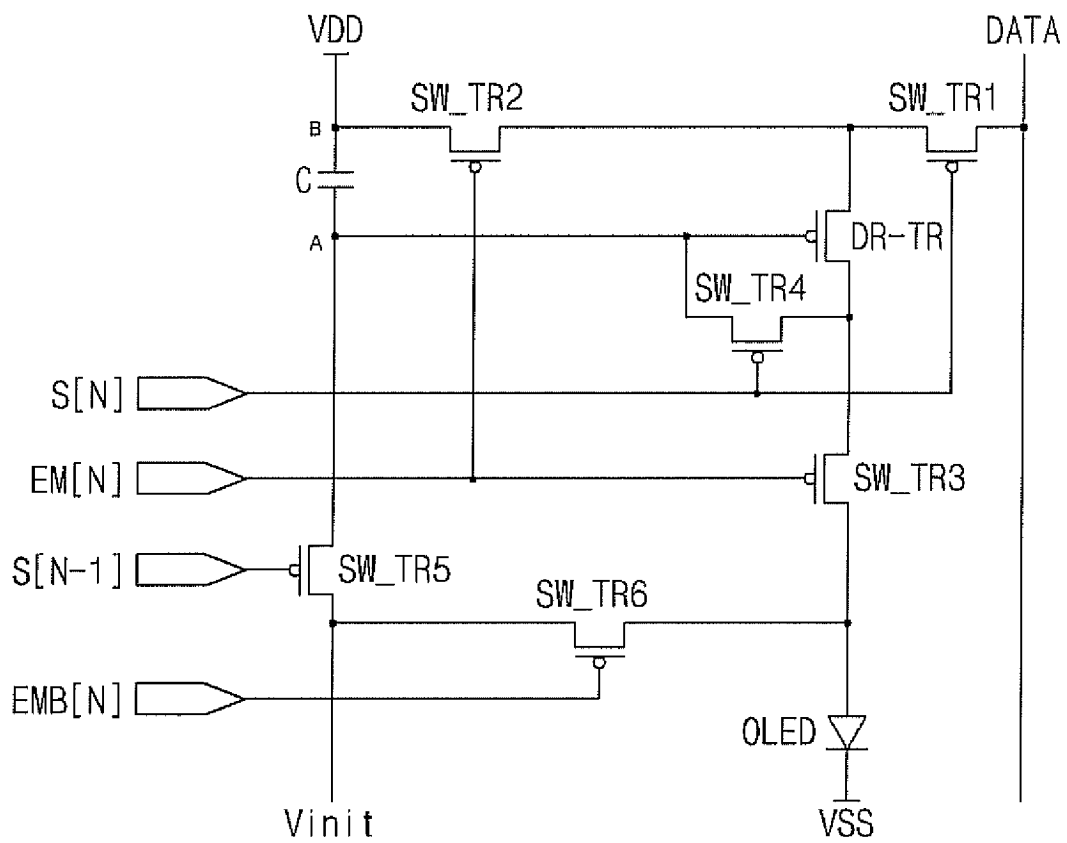


FIG. 6

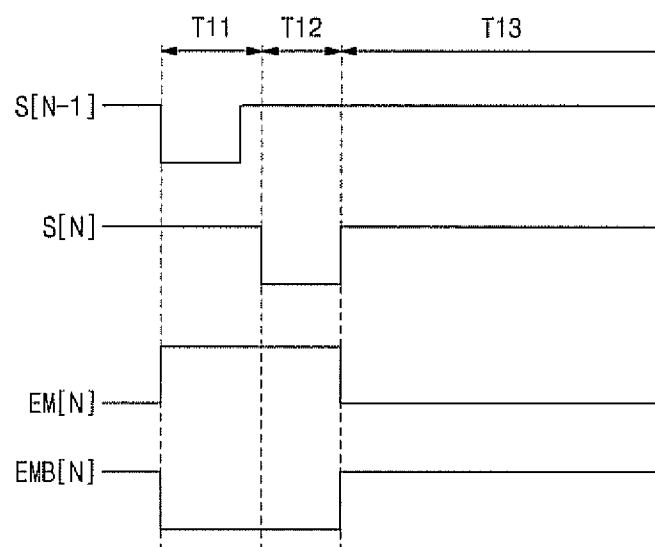


FIG. 7

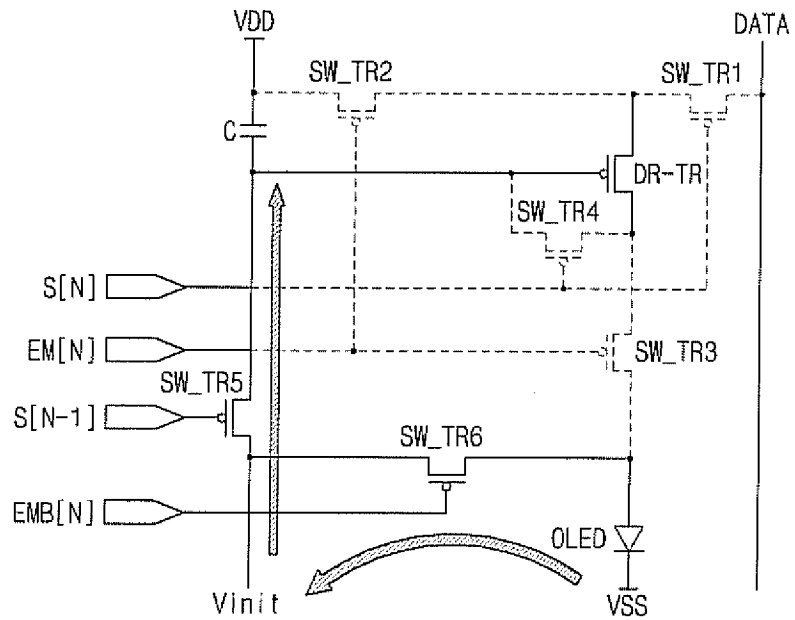


FIG. 8

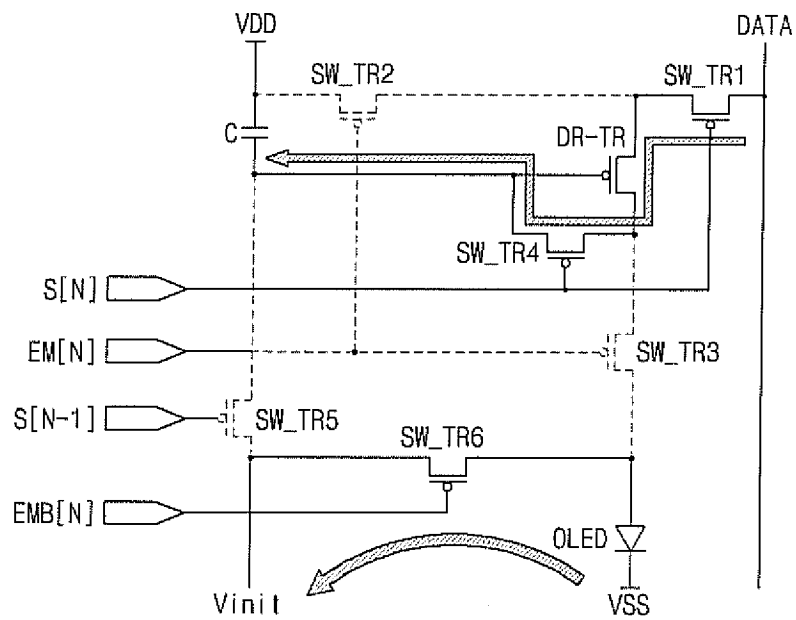


FIG. 9

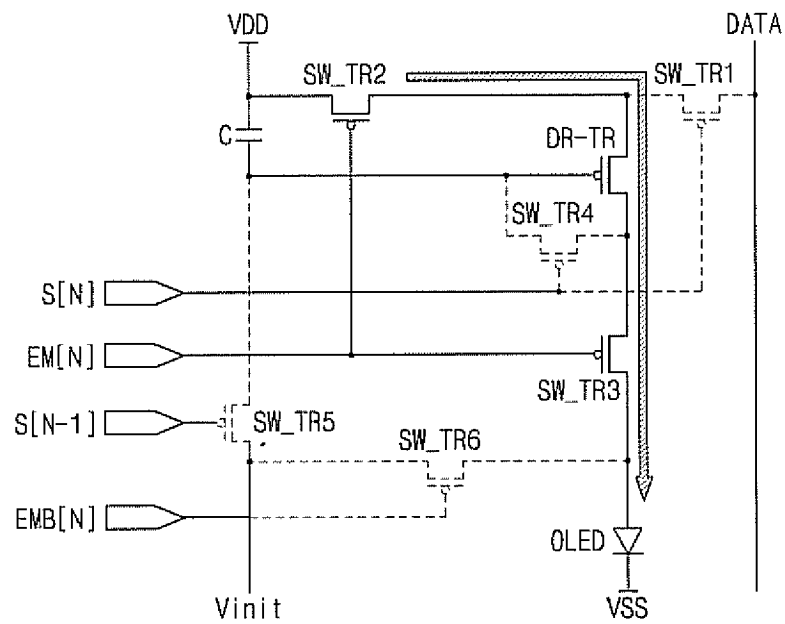


FIG. 10

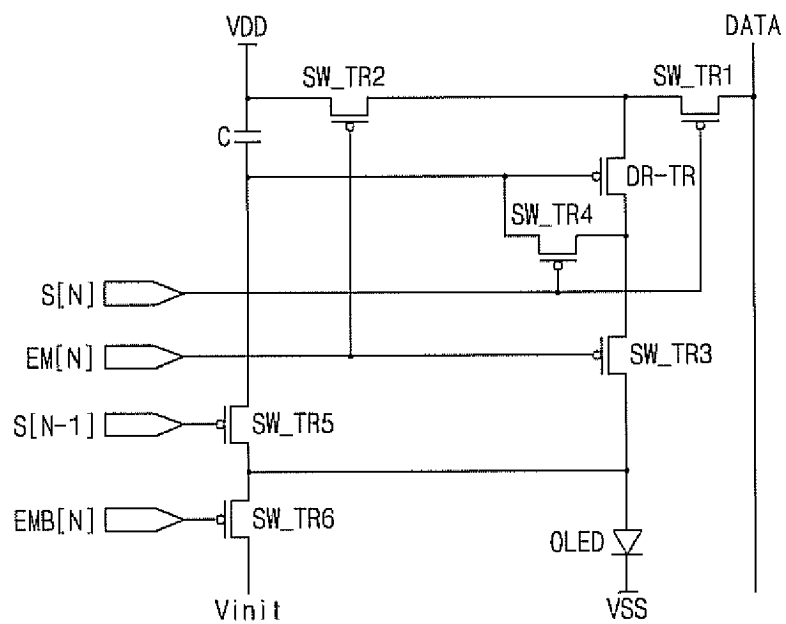


FIG. 11

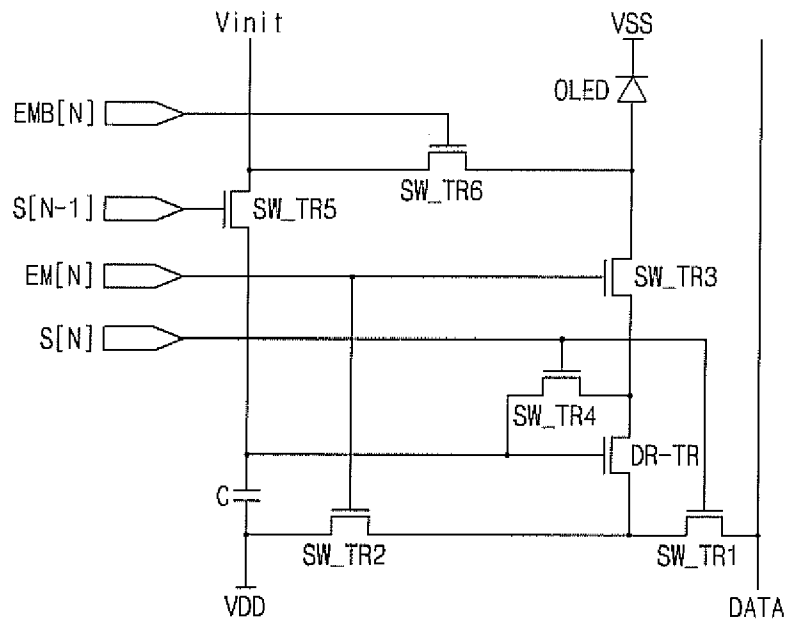


FIG. 12

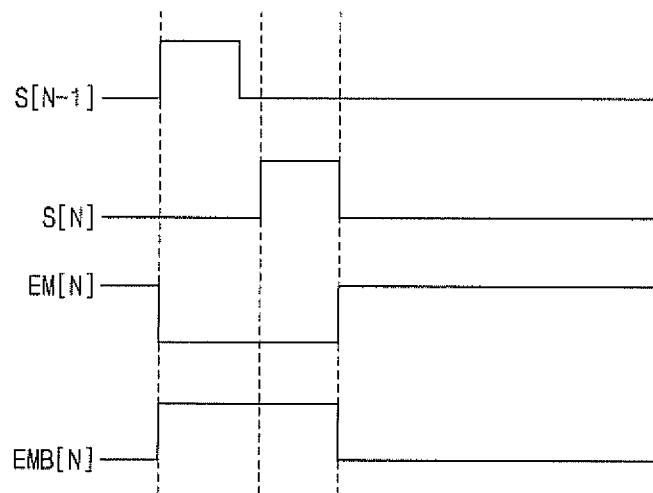


FIG. 13

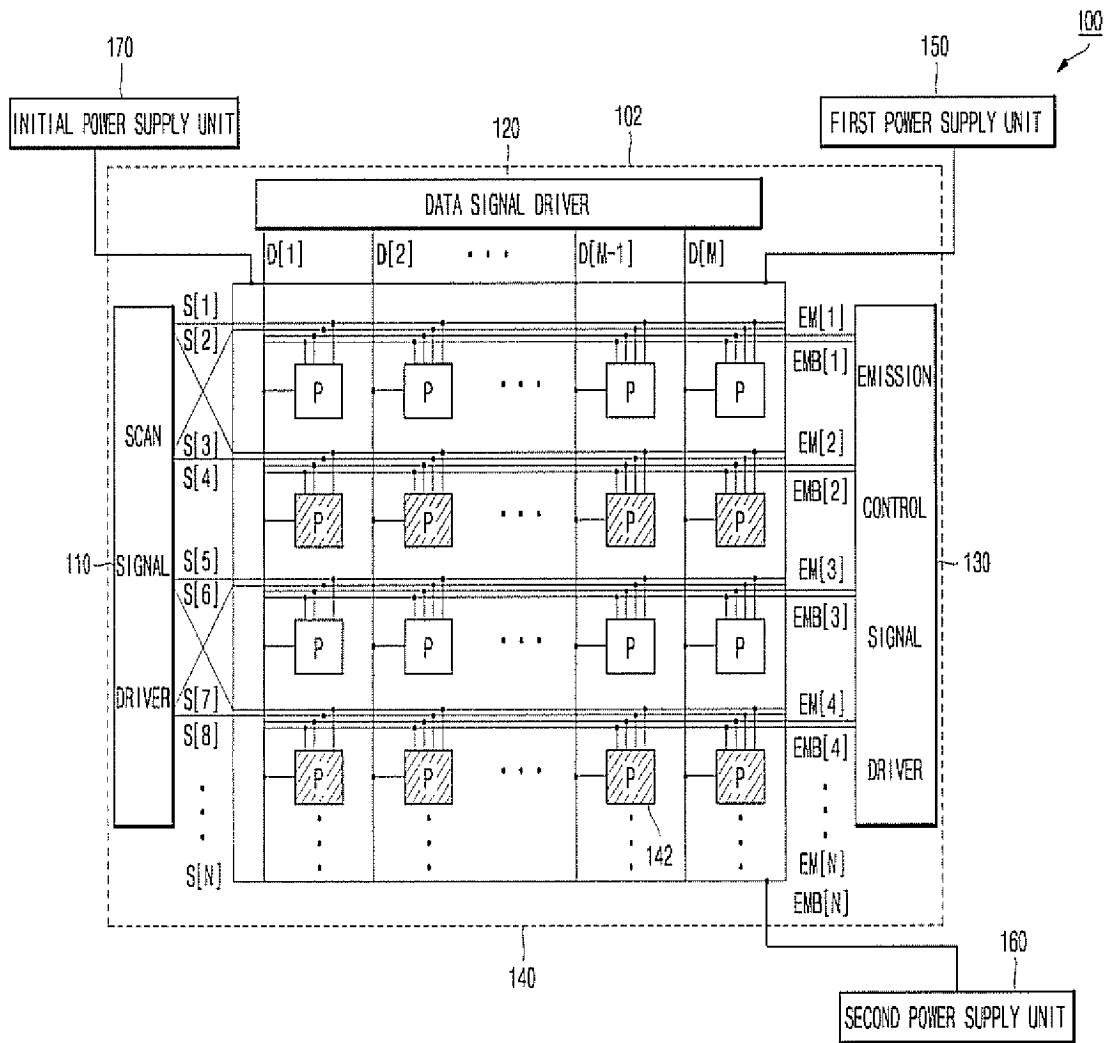


FIG. 14

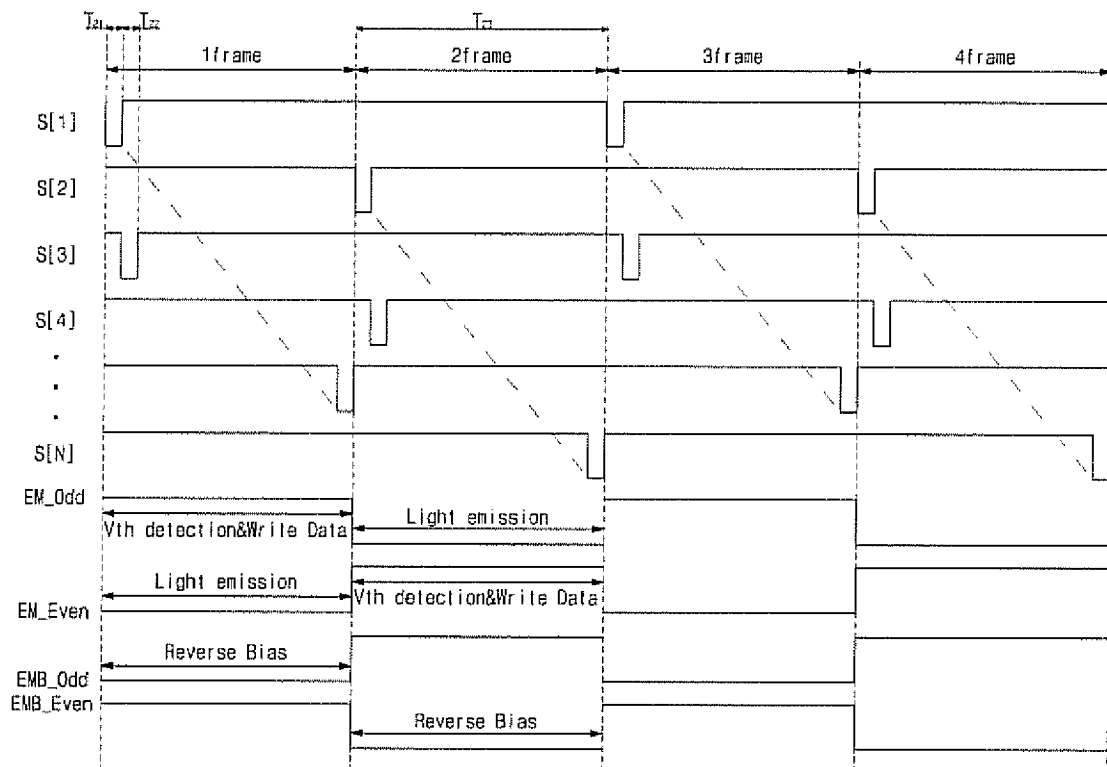


FIG. 15

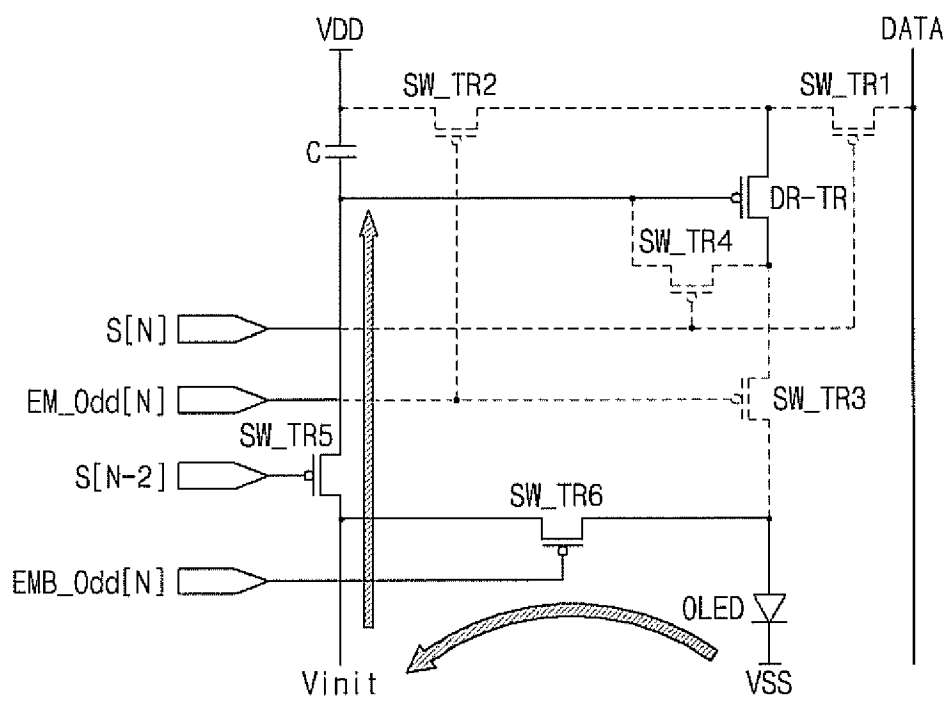


FIG. 16

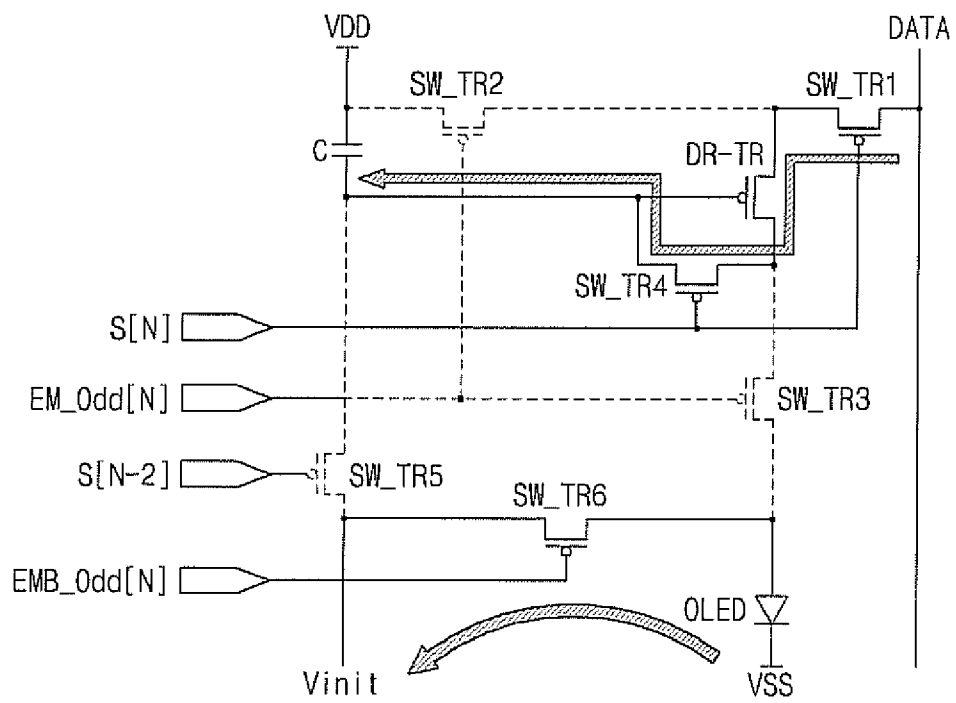


FIG. 17

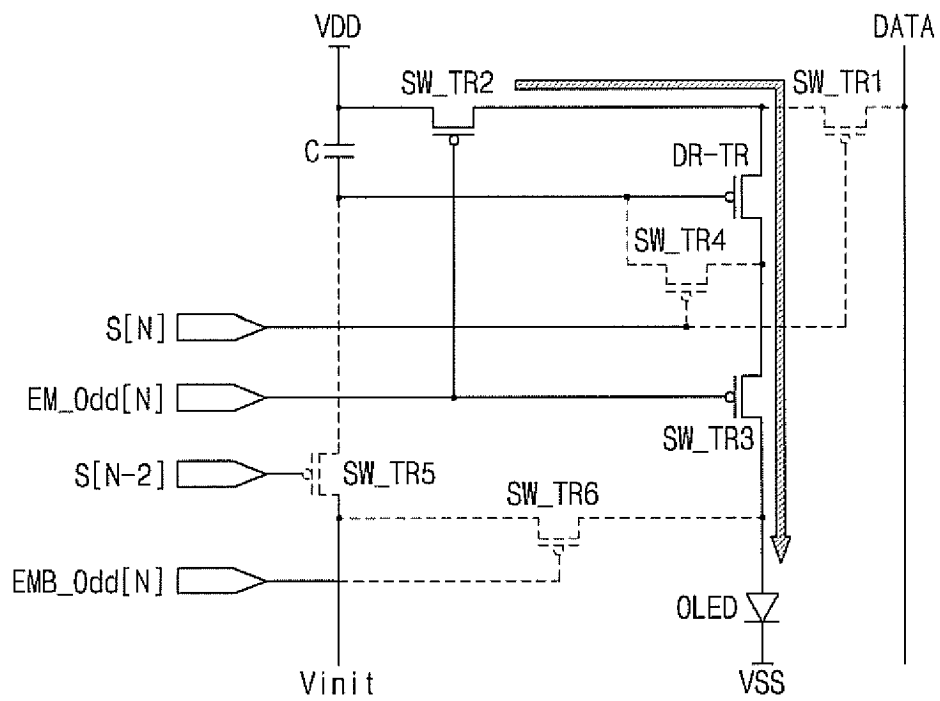


FIG. 18

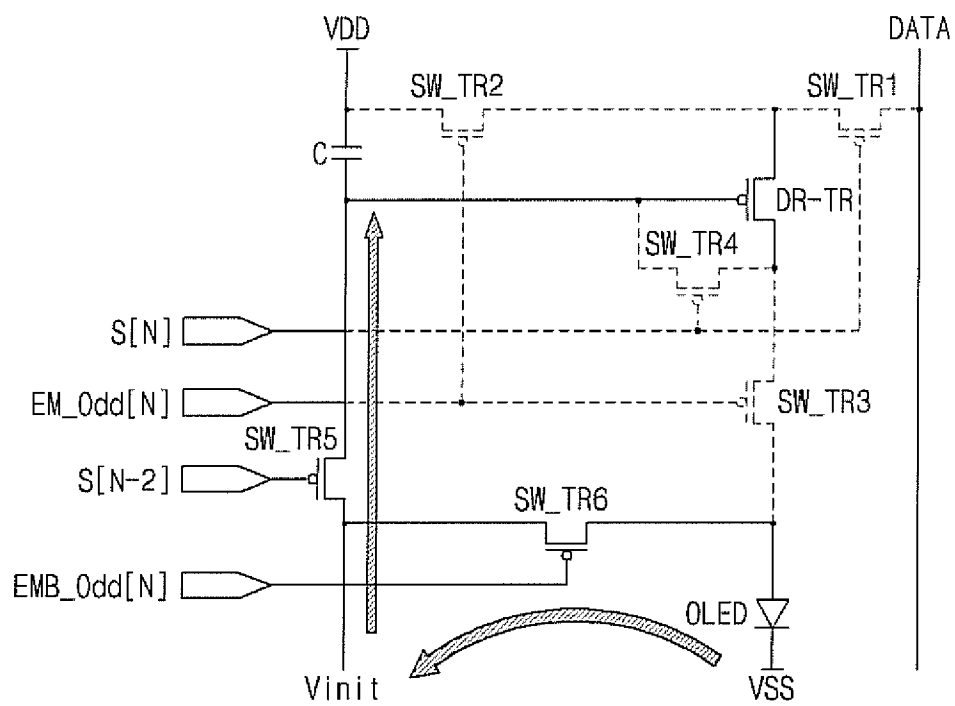


FIG. 19

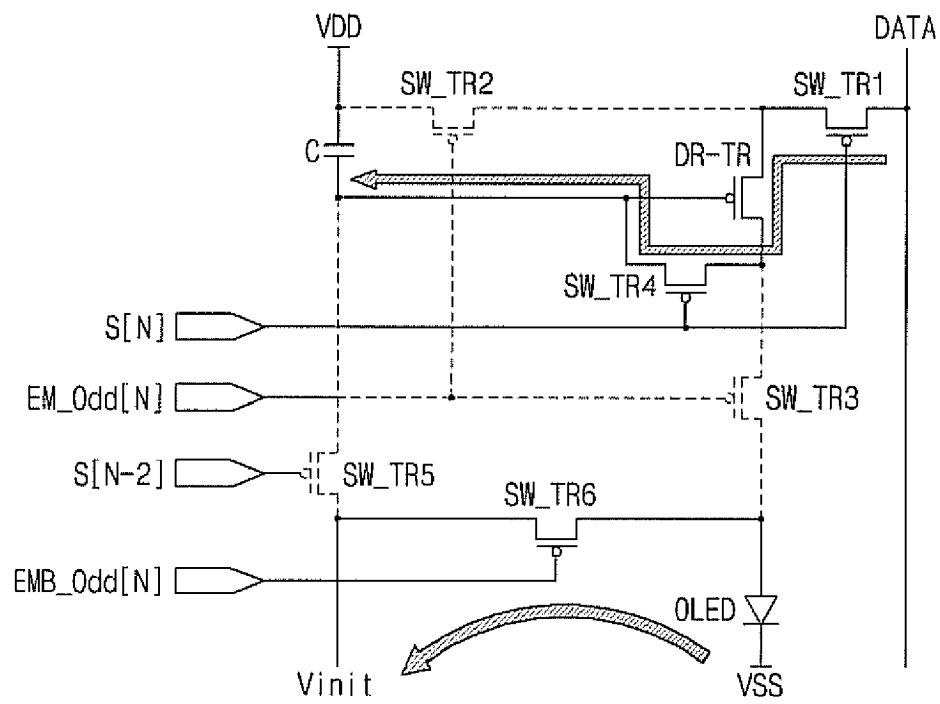


FIG. 20

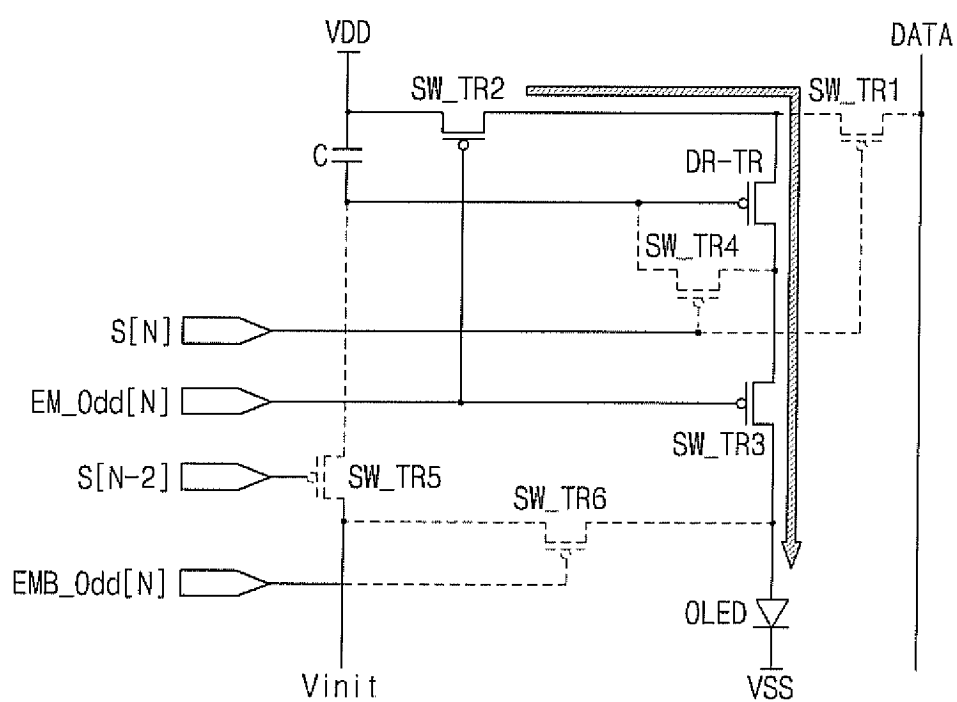
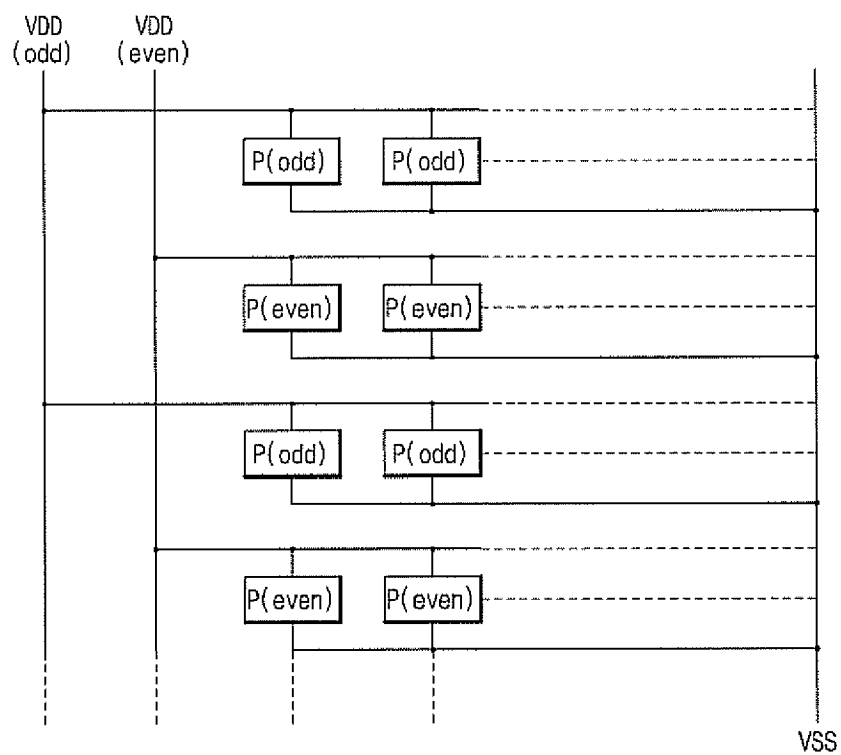


FIG. 21





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 07 12 3804

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2006/244695 A1 (KOMIYA NAOAKI [KR]) 2 November 2006 (2006-11-02) * figure 8B *	1-7	INV. G09G3/32
Y	* paragraph [0121] - paragraph [0136] * * paragraph [0005] - paragraph [0010] * * figure 8B * * paragraph [0121] - paragraph [0136] *	8-11	
X	US 2006/125737 A1 (KWAK WON K [KR] ET AL) 15 June 2006 (2006-06-15) * figure 4 * * figure 5 *	1-7	
Y	* paragraph [0040] - paragraph [0074] * * figure 4 * * paragraph [0040] - paragraph [0074] *	8-11	
Y	US 2006/103611 A1 (CHOI SANG M [KR]) 18 May 2006 (2006-05-18) * paragraph [0012] * * paragraph [0031] - paragraph [0049] *	8-11	
Y	* paragraph [0012] * * paragraph [0031] - paragraph [0049] *	8-11	TECHNICAL FIELDS SEARCHED (IPC)
			G09G
The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 28 February 2008	Examiner Lochhead, Steven
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

2
EPO FORM 1503 03.82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 07 12 3804

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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28-02-2008

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专利名称(译)	有机发光显示器及其驱动方法		
公开(公告)号	EP1936596A1	公开(公告)日	2008-06-25
申请号	EP2007123804	申请日	2007-12-20
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO. , LTD.		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
[标]发明人	CHUNG BOYONG		
发明人	CHUNG, BOYONG		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2310/0224 G09G2310/0256 G09G2320/043		
代理机构(译)	hengelhaupt, Jürgen		
优先权	1020060131962 2006-12-21 KR		
其他公开文献	EP1936596B1		
外部链接	Espacenet		

摘要(译)

一种有机发光显示器，包括转发扫描信号的扫描信号线，发送数据信号的数据线以及耦合到扫描信号线和数据线的像素，有机发光二极管显示器，其中像素包括第一切换晶体管响应于扫描信号线的扫描信号从数据线传输数据信号，驱动晶体管，耦合到第一开关晶体管，控制来自第一电源线的驱动电流，耦合在驱动晶体管之间的存储电容器第一电源线，有机发光二极管，耦合在驱动晶体管和第二电源线之间，显示具有由驱动晶体管控制的驱动电流的图像，初始开关晶体管，耦合在存储电容器和初始电源线上，初始化存储电容器和用于施加反向偏置的开关晶体管，耦合在一起在第二电源线和初始电源线上，向有机发光二极管施加反向偏压。

FIG. 5

