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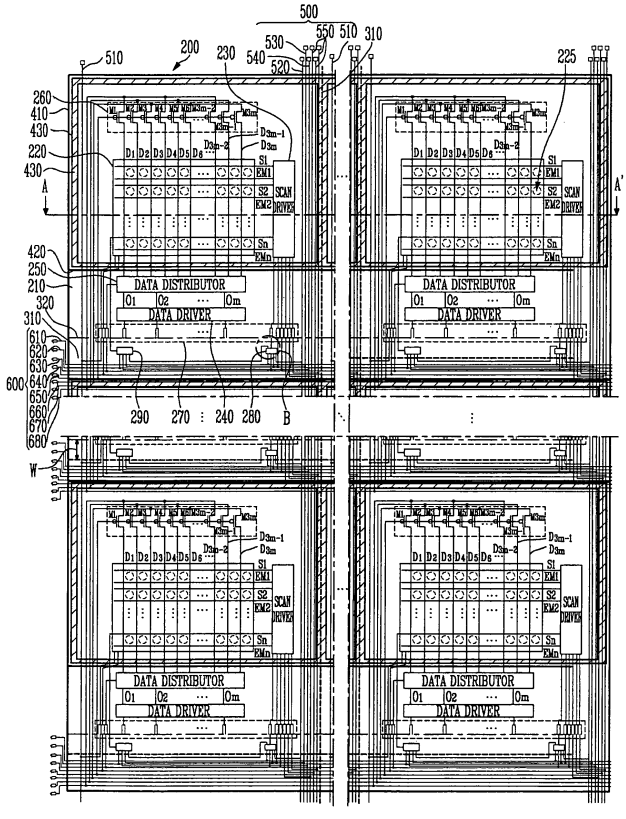
(54) **Organic light emitting display device and mother substrate of the same**

(57) A light emitting display device may include a plurality of pixels, a plurality of scan lines for selectively applying a scan signal to the pixels, a plurality of data lines crossing the scan lines for applying a data signal to the respective pixels, a scan driver for applying a scan signal to the scan lines, and at least one first testing unit electrically connected to the scan driver, wherein at least one output line of the first testing unit is electrically connected to the scan driver, and at least one other output line of the first testing unit is electrically disconnected and in an electrically open state.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a light emitting display device and a mother substrate of the same. More particularly, the present invention relates to a light emitting display device, e.g., an organic light emitting display device, capable of performing a sheet unit test on light emitting display devices on a mother substrate before scribing, independently controlling predetermined signals supplied to the respective light emitting display devices during the sheet test, and preventing or reducing damage to circuits for controlling the signals, and a mother substrate of the same.

2. Description of Related Art

[0002] Generally, a plurality of light emitting display devices, e.g., organic light emitting display devices, are formed on one mother substrate, and then scribed and separated into individual light emitting display devices. Tests on the light emitting display devices may be carried out on each of the scribed light emitting display devices.

[0003] A test on the individual light emitting display devices may be carried out using an apparatus for testing each of the light emitting display devices. However, a test apparatus, or a jig required for testing needs to be changed if a circuit wire constituting the light emitting display device is changed, or if a size of the light emitting display device is varied. Also, the test time is extended and the cost is increased as the tests need to be separately carried out on each of the light emitting display devices, which results in a reduced testing efficiency. Accordingly, it is desirable to carry out a test on a plurality of the light emitting display devices on a mother substrate prior to scribing the light emitting display devices.

[0004] Tests on normal light emitting display devices may not be suitably carried out if inferior or defective light emitting display device(s) are included on a mother substrate being subjected to a sheet unit test. Accordingly, in order to increase reliability and efficiency of the sheet unit test, predetermined signals supplied to selected ones of the light emitting display devices should be independently controlled by, e.g., turning off the inferior light emitting display device(s), so that the effect of the inferior light emitting display device(s) on tests of other light emitting display devices may be reduced or eliminated.

[0005] Also, the predetermined signals supplied to the selected ones of the organic light emitting display devices should be effectively controlled to reduce or prevent damage to circuits for controlling the signals.

SUMMARY OF THE INVENTION

[0006] The present invention is therefore directed to a light emitting display device and mother substrate thereof, which substantially overcome one or more of the problems due to the limitations and disadvantages of the related art.

[0007] It is therefore a feature of an embodiment of the present invention to provide a light emitting display device, e.g., an organic light emitting display device, capable of performing a sheet unit test on a plurality of light emitting display devices formed on a mother substrate, and a mother substrate of the same.

[0008] It is therefore a separate feature of an embodiment of the present invention to provide a light emitting display device, e.g., an organic light emitting display device, which may independently controlling the predetermined signals supplied to the respective light emitting display device for testing.

[0009] It is therefore a separate feature of an embodiment of the present invention to provide a light emitting display device, e.g., an organic light emitting display device that may prevent and/or reduce damage to circuits for controlling the signals in the test on at least one light emitting display device formed on a mother substrate, and a mother substrate of the same.

[0010] According to a first aspect of the invention, there is provided a light emitting display as set out in claim 1. Preferred features of this aspect are set out in claims 2 to 24.

[0011] According to a second aspect of the invention, there is provided a mother substrate as set out in claim 25. Preferred features of this aspect are set out in claims 26 to 35.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The above and other features and advantages of the present invention will become more apparent to those of ordinary skill in the art upon making reference to the following description, which describes in detail embodiments thereof with reference to the attached drawings, in which :

[0013] FIG. 1 is a schematic diagram of an exemplary mother substrate of an organic light emitting display device according to one embodiment of the present invention;

[0014] FIG. 2 is a schematic diagram of one of the organic light emitting display devices shown in FIG. 1;

[0015] FIG. 3 is a cross-sectional view, taken along a line A-A', of the mother substrate shown in FIG. 1;

[0016] FIG. 4 is a circuit diagram of a first embodiment of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2;

[0017] FIG. 5 is a circuit diagram of a second embodiment of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2;

[0018] FIG. 6 is a circuit diagram of a third embodiment

of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2;

[0019] FIG. 7 is a circuit diagram of a fourth embodiment of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2;

[0020] FIG. 8 is a layout diagram of the fourth embodiment of the logic gate shown in FIG. 7, as formed in region B of FIG. 1;

[0021] FIG. 9 is a circuit diagram of a fifth embodiment of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2;

[0022] FIG. 10 is a circuit diagram of a sixth embodiment of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2;

[0023] FIG. 11 is a circuit diagram of a seventh embodiment of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2;

[0024] FIG. 12 is a circuit diagram of an embodiment of the pixel shown in FIG. 1 and FIG. 2; and

[0025] FIG. 13 is an exemplary waveform diagram of driving signals for driving the pixel circuit shown in FIG. 12.

DETAILED DESCRIPTION OF THE INVENTION

[0026] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are illustrated. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout the specification.

[0027] Hereinafter, embodiments of the present invention will be described with reference to the accompanying drawings, as apparent to those skilled in the art. In the following description, when one element is connected to another element, one element may be not only directly connected to another element but also indirectly connected to another element via another element.

[0028] In the following description of embodiments, organic light emitting display devices may be employed as exemplary light emitting display devices. However, embodiments of the invention are not limited to organic light emitting display devices and one or more aspects of the invention may be applied to other light emitting display devices.

[0029] FIG. 1 is a schematic diagram of an mother substrate of an organic light emitting display device according to one exemplary embodiment of the present invention.

[0030] Referring to FIG. 1, a mother substrate 200 of the organic light emitting display device according to the exemplary embodiment of the present invention includes a plurality of organic light emitting display devices 210 arranged in a matrix-like manner, first and second wire groups 500, 600 disposed in a border region of the organic light emitting display devices 210, and first and second circuit units 280, 290 disposed in a region between a scribing line (a first line) 310 and a grinding line (a second line) 320 of the organic light emitting display devices 210.

[0031] Each of the organic light emitting display devices 210 includes a pixel unit 220, a scan driver 230, a data driver 240, a data distributor 250, a transistor group 260 including a plurality of transistors (M1 to M3m), and a pad unit 270 for receiving a driving signal from the outside.

[0032] The pixel unit 220 includes a plurality of pixels 225, a plurality of scan lines (S1 to Sn) for selectively applying a scan signal to the pixels 225, a plurality of emission control lines (EM1 to EMn) for selectively applying an emission control signal to the pixels 225, and a plurality of data lines (D1 to D3m) arranged so as to be crossing the scan lines (S1 to Sn) and the emission control lines (EM1 to EMn) and applying a test signal or a data signal to the respective pixels 225. Each of the pixels 225 include an organic light emitting diode.

[0033] The pixel unit 220 displays a predetermined image corresponding to voltages from first and second power sources ELVDD, ELVSS (not shown), scan signal(s) and emission control signal(s) from the scan driver 230, and test signal(s) from the transistor group 260. The voltages from first and second power source ELVDD, ELVSS are supplied from a first wire 510 of the first wire group 500 and a fourteenth wire 640 of the second wire group 600, respectively, when the test(s) on the organic light emitting display device(s) on the mother substrate 200 is carried out. In some embodiments of the invention, depending on a configuration of the pixels 225 in the pixel unit 220, the pixel unit 220 may further receive additional voltages, e.g., a reset power source voltage Vinit.

[0034] After testing of the organic light emitting display devices 210 on the mother substrate 200 has been performed and/or the organic light emitting display devices 210 have been scribed, the pixel unit 220 can display a predetermined image corresponding to the data signal(s) supplied from the data distributor 250. That is, after testing of the organic light emitting display devices 230 on the mother substrate 200 has been performed and/or the organic light emitting display devices 210 have been scribed, the image(s) that may be displayed on the organic light emitting display devices 210 may not to correspond to the test signal(s) supplied from the transistor group 260, i.e., after scribing, the transistor group 260 may not supply signals for generating an image to the pixel unit 220.

[0035] The scan driver 230 receives a voltage from a third power source VDD, a voltage fourth power source VSS and a scan control signal from a third wire 530, a fourth wire 540 and fifth wires 550 of the first wire group 500, and receives a control signal from the first circuit unit 280 when the test(s) are carried out on the organic

light emitting display device on the mother substrate 200.

[0036] The scan driver 230 generates a scan signal and an emission control signal having a high level or a low level voltage corresponding to power source voltages and signals supplied to the scan driver 230 itself. The scan signal(s) and the emission control signal(s) generated by the scan driver 230 are applied to the scan lines (S1 to Sn) and the emission control lines (EM1 to EMn), and then supplied to the pixel unit 220.

[0037] The scan driver 230 generates a scan signal and an emission control signal corresponding to voltages of the third and fourth power sources VDD, VSS and a scan control signal (SCS) supplied through the pad unit 270 from an external printed circuit board after the organic light emitting display devices 210 on the mother substrate 200 are scribed.

[0038] In the embodiment illustrated in FIGS. 2 and 3, one scan driver 230 arranged on one side of the pixel unit 220 is shown. However, embodiments of the present invention are not limited thereto. For example, two scan drivers 230 can be arranged on both sides of the pixel unit 220, or an emission control driver for generating an emission control signal can be formed in a separate region.

[0039] After the light emitting display device 210 is scribed from the mother substrate 200, the data driver 240 of the respective light emitting display device 210 can generate a data signal corresponding to data supplied from the outside through the pad unit 270. The data signal generated in the data driver 240 is supplied to the data lines (D1 to D3m) through the data distributor 250.

[0040] The data distributor 250 is connected between the data driver 240 and the data lines (D1 to D3m), and more particularly, between the output lines (O1 to Om) of the data driver 240 and first ends of the data lines (D1 to D3m). The data distributor 250 respectively supplies data signal(s), which are received via the output lines (O1 to Om) of the data driver 240, to the plurality of the data lines (D1 to D3m).

[0041] The data distributor 250 receives selection signals, e.g., CLR, CLG, CLB, etc., from the pad unit 270 after the organic light emitting display devices 210 are scribed from the mother substrate 200.

[0042] The data distributor 250 may be set to be turned off by a bias signal (Vbias) supplied from a thirteenth wire 630 of the second wire group 600 when the test on the organic light emitting display device 210 is carried out on the mother substrate 200. If a test signal is to be supplied via the data distributor 250, a suitable image may not be displayed or it may be difficult to synchronize the selection signals because the selection signals may in such cases be delayed if supplied via the data distributor 250 through the first or second wire group 500, 600. Therefore, in such cases, a sufficient amount of time for charging a data voltage in the pixel(s) may not be ensured.

[0043] Embodiments of the invention overcome such problems by, e.g., providing a separate transistor group 260 for supplying a test signal to each of the organic light emitting display devices 210. That is, in embodiments of the invention, when the organic light emitting display device(s) 210 on the mother substrate 200 are being tested, the respective test signals are supplied via the separate transistor group 260 instead of the data distributor 250. In some embodiments of the invention, the transistor group 260 is connected to second ends of the data lines (D1 to D3m). That is, in some embodiments of the invention, the data distributor 250 and the transistor group 260 are arranged so as to be connected to different ends of the data lines (D1 to D3m), and the ends of the data lines (D1 to D3m) extend beyond the pixel unit 220 of the respective organic light emitting display 210.

[0044] The transistor group 260 includes a plurality of transistors (M1 to M3m) whose gate electrodes are commonly connected to a fifteenth wire 650 of the second wire group 600.

[0045] A source electrode of each of the transistors (M1 to M3m) is connected to one of a sixteenth wire to an eighteenth wire 660 to 680 of the second wire group 600, and a drain electrode of each of the transistors (M1 to M3m) is connected to one of the data lines (D1 to D3m). In some embodiments of the invention, transistors (M1, M4, ..., M3m-2) connected to the eighteenth wire 680 are connected to data lines (D1, D4, ..., D3m-2) of a red subpixel, transistors (M2, M5, ..., M3m-1) connected to a seventeenth wire 670 may be connected to data line (D2, D5, D3m-1) of a green subpixel, and transistors (M3, M6, ..., M3m) connected to the sixteenth wire 660 are connected to data line (D3, D6, ..., D3m) of a blue subpixel.

[0046] When the organic light emitting display device 210 on the mother substrate 200 is being tested, transistors (M1 to M3m) of the transistor group 260 are simultaneously turned on by a test control signal, supplied through the fifteenth wire 650. As discussed above, the fifteenth wire 650 is connected to gate electrodes of the transistors (M1 to M3m). Thus, the transistors (M1 to M3m) themselves supply the test signal, supplied from a wire connected to the source electrodes of the transistors (M1 to M3m) of the transistor group 260, to the data line (D).

[0047] The transistor group 260 maintains a turned-off state based on a control signal, which can be externally supplied after the organic light emitting display devices 210 are scribed from the mother substrate 200.

[0048] The pad unit 270 transfers power source voltages and signals, which can be externally supplied, to each of the organic light emitting display devices 210. For example, the pad unit 270 can transfer the power source voltages and the driving signals supplied, e.g., from a printed circuit board, etc., to at least one of the pixel unit 220, the scan driver 230, the data driver 240 and the data distributor 250. The pad unit 270 may include a plurality of pads.

[0049] The first circuit unit 280 is a circuit employable for testing the organic light emitting display 210, and independently controls a predetermined signal supplied to

the organic light emitting display device 210 when the test on at least one organic light emitting display device 210 is carried out in the mother substrate 200. The first circuit unit 280 can independently control at least one of the scan control signals SCS supplied to the scan driver 230.

[0050] For example, when one or some organic light emitting display devices 210 are erroneously operated due to a signal delay, etc., that occurs while testing at least one organic light emitting display device 210 arranged on the mother substrate 200, the first circuit unit 280 has a function of independently turning off the erroneously operated organic light emitting display device.

[0051] Thus, the first circuit unit 280 is connected between the scan driver 230 and a predetermined wire included in the first or second wire group 500, 600. For example, the first circuit unit 280 may be connected to the scan driver 230, and a second wire 520, the third wire 530 and the fourth wire 540 of the first wire group 500 and an eleventh wire 610 of the second wire group 600.

[0052] Such a first circuit unit 280 controls the scan driver 230 by generating a predetermined control signal corresponding to the power source voltages and signals supplied from the second wire 520, the third wire 530, the fourth wire 540 and the eleventh wire 610, and outputs the predetermined control signal to the scan driver 230. The first circuit unit 280 includes at least one logic gate for generating a control signal, e.g., the predetermined control signal. The logic gate included in the first circuit unit 280 will be described below in detail.

[0053] In some embodiments of the invention, the first circuit unit 280 does not affect an operation of the organic light emitting display devices 210 after the testing of the at least one organic light emitting display device 210 on the mother substrate 200 is completed and/or the organic light emitting display devices 210 have been scribed.

[0054] Thus, in some embodiments of the invention, the first circuit unit 280 is arranged between the scribing line (a first line) 310 and the grinding line (a second line) 320, and electrical connection points between the first circuit unit 280 and the first and second wire groups 500, 600 are positioned outside of the scribing line 310. In the following description, the scribing line 310 corresponds to a line for separating each of the organic light emitting display devices 210 from the mother substrate 200, and the grinding line 320 corresponds to a line for additionally grinding along a model of the organic light emitting display device 210 after the scribing process has been completed. A position of the grinding line 320 generally corresponds to a lower end of the pad unit 270. A region between the scribing line 310 and the grinding line 320 may be called an edge region. That is, the first circuit unit 280 may be arranged in the edge region, namely between the pad unit 270 and the scribing line 310.

[0055] A width (W) of the edge region may be varied according to the model of the organic light emitting display device 210. In some embodiments of the invention, the edge region may be less than or equal to about $\pm$300 μm from the scribing line 310. That is, e.g., in some embodiments of the invention, the first circuit unit 280 may be arranged at or within a distance of about 300 μm from the scribing line 310.

[0056] The second circuit unit 290 is a measuring circuit in this embodiment. More particularly, the second circuit unit 290 measures a scan signal generated in the scan driver 230 of each of the organic light emitting display devices 210 and supplied to the pixel unit 220.

[0057] The second circuit unit 290 may be connected between any one of a plurality of the scan lines and the predetermined wire included in the first or second wire group 500, 600, and may include at least one logic gate. For example, the second circuit unit 290 may be connected between an nth scan line (Sn), and each of the third wire 530 and the fourth wire 540 of the first wire group 500 and a twelfth wire 620 of the second wire group 600. In embodiments in which a shift control signal is generated in the first circuit unit 280, then the second circuit unit 290 may be connected to the first circuit unit 280 so that it may receive the shift control signal from the first circuit unit 280.

[0058] Such a second circuit unit 290 outputs a scan measuring signal to the twelfth wire 620. The scan measuring signal corresponds to the scan signal output to the nth scan line (Sn), the voltages from the third and fourth power sources VDD, VSS respectively supplied from the third wire 530 and the fourth wire 540, and the shift control signal supplied from the first circuit unit 280. Then, it may be determined whether or not the scan signal is normally generated by measuring a signal output from the twelfth wire 620 when the test on the organic light emitting display device 210 on the mother substrate 200 is carried out.

[0059] In some embodiments of the invention, similar to the first circuit unit 280, the second circuit unit 290 does not affect operation of the organic light emitting display devices 210 after the organic light emitting display device(s) are scribed. Thus, the second circuit unit 290 can be arranged between the scribing line 310 and the grinding line 320, and electrical connection points between the second circuit unit 290 and the first and second wire groups 500, 600 may be formed outside of the scribing line 310. In some embodiments of the invention, the second circuit unit 290 is arranged at or within a distance of about 300 μm from the scribing line 310.

[0060] The second circuit unit 290 may measure an emission control signal that is generated in the scan driver 230 of the respective organic light emitting display devices 210 and supplied to the pixel unit 220. In such embodiments, the second circuit unit 290 may be connected between any one out of a plurality of emission control lines (EM1 to EMn) and a predetermined wire included in the first or second wire groups 500, 600. In some embodiments of the invention, a plurality of second circuit units 290 may be provided to measure a plurality of signals, e.g., two second circuits 290 may be provided to measure both the scan signal and the emission control

signal.

[0061] The first wire group 500 extends in a first direction at a border region of the organic light emitting display devices 210. More particularly, the first wire group 500 is commonly connected to the organic light emitting display devices 210 arranged in a same column on the mother substrate 200.

[0062] Such a first wire group 500 includes, e.g., the first through fifth wires 510 to 550. The first wire 510 may receive the voltage of the first power source ELVDD. The second wire 520 may receive a vertical control signal (VC). The third wire 530 may receive the voltage of the third power source VDD. The fourth wire 540 may receive the fourth power source voltage VSS. The fifth wires 550 may receive the scan control signal(s) SCS.

[0063] The first wire 510 supplies the voltage of the first power source ELVDD, which may be supplied to the first wire 510 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the pixel unit 220 of the organic light emitting display devices 210 connected to the first wire 510 itself.

[0064] The second wire 520 supplies the vertical control signal (VC), which may be supplied to the second wire 520 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the first circuit unit 280 connected to the second wire 520 itself.

[0065] The third wire 530 supplies the voltage of the third power source voltage, which may be supplied to the third wire 530 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the scan driver 230, the first circuit unit 280 and the second circuit unit 290 of the organic light emitting display device(s) 210 connected to the third wire 530 itself.

[0066] The fourth wire 540 supplies the voltage of the fourth power source VSS, which may be supplied in the fourth wire 540 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the scan driver 230, the first circuit unit 280 and the second circuit unit 290 of the organic light emitting display device(s) 210 connected to the fourth wire 540 itself.

[0067] The fifth wires 550 supplies the scan control signals SCS, which may be supplied to the fifth wires 550 during the testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the scan driver 230 of the organic light emitting display devices 210 connected to the fifth wire 550 itself. The scan control signals (SCS) supplied to the scan driver 230 may include a clock signal, an output enable signal, and a start pulse, etc. A number of the scan control signals (SCS) that may be supplied to the scan driver 230 may be varied according to circuit configurations of the scan driver 230. Accordingly, the number of the wires included in the fifth wires 550 may vary widely. Although three wires are described in the exemplary embodiment described below, embodiments of the invention are not limited to such characteristics and may include less than or more than three wires.

[0068] In some embodiments of the invention, at least one of the fifth wires 550 may supply a clock signal to the first circuit unit 280.

[0069] The second wire group 600 extends in a second direction at a border region of the organic light emitting display devices 210. More particularly, the second wire group 600 may be commonly connected to the organic light emitting display devices 210 arranged in a same row on the mother substrate 200.

[0070] The second wire group 600 may include the eleventh through eighteenth wires 610 through 680. The eleventh wire 610 may receive a horizontal control signal (HC). The twelfth wire 620 may output a scan measuring signal. The thirteenth wire 630 may receive the bias voltage (Vbias). The fourteenth wire 640 may receive the voltage of second power source ELVSS. The fifteenth wire 650 may receive a test control signal. The sixteenth wire 660 may receive a blue test signal; a seventeenth wire 670 may receive a green test signal; and an eighteenth wire 680 may receive a red test signal.

[0071] The eleventh wire 610 supplies the horizontal control signal (HC), which may be supplied to the eleventh wire 610 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the first circuit unit 280 of the organic light emitting display devices 210 connected to the eleventh wire 610 itself.

[0072] The twelfth wire 620 outputs the scan measuring signal, which may be supplied to the twelfth wire 620 from the second circuit unit 290 during testing of the at least one organic light emitting display device 210 on the mother substrate 200.

[0073] The thirteenth wire 630 supplies the bias voltage (Vbias), which may be supplied to the thirteenth wire 630 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the data distributor 250 of the organic light emitting display devices 210 connected to the thirteenth wire 630 itself.

[0074] The fourteenth wire 640 supplies the voltage of the second power source ELVSS, which may be supplied during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the pixel unit 220 of the organic light emitting display devices 210 connected to the fourteenth wire 640 itself.

[0075] The fifteenth wire 650 supplies the test control signal, which may be supplied to the fifteenth wire 650 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the transistors (M1 to M3m) of the transistor group 260 of the organic light emitting display devices 210 connected to the fifteenth wire 650 itself.

[0076] The sixteenth wire 660 supplies a blue test signal, which may be supplied to the sixteenth wire 660 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the transistors (M1 to M3m) of the transistor group 260 of the organic

light emitting display devices 210 connected to the sixteenth wire 660 itself.

[0077] The seventeenth wire 670 supplies a green test signal, which may be supplied to the seventeenth wire 670 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the transistor group 260 of the organic light emitting display devices 210 connected to the seventeenth wire 670 itself.

[0078] The eighteenth wire 680 supplies a red test signal, which may be supplied to the eighteenth wire 680 during testing of the at least one organic light emitting display device 210 on the mother substrate 200, to the transistor group 260 of the organic light emitting display devices 210 connected to the eighteenth wire 680 itself.

[0079] Each of the organic light emitting display devices 210 on the mother substrate 200 may be scribed from the mother substrate 200, e.g., after a sheet unit test is completed. In some embodiments of the invention, the scribing line 310 is arranged such that, after scribing, the first wire group 500 and the second wire group 600 can be electrically isolated from the pixel unit 220, the scan driver 230, the data driver 240, the data distributor 250 and the transistor group 260. That is, in some embodiments of the invention, an electrical connection point between the first wire group 500 and the second wire group 600, and the pixel unit 220, the scan driver 230, the data driver 240, the data distributor 250 and the transistor group 260 is arranged outside the scribing line 310 of the organic light emitting display device 210. Accordingly, embodiments of the invention may prevent and/or reduce noise such as electrostatics flowing in the first wire group 500 and the second wire group 600 from the outside from being supplied to the pixel unit 220, the scan driver 230, the data driver 240, the data distributor 250 and the transistor group 260.

[0080] In cases employing the mother substrate 200 describe above, a test on one, some or all of the organic light emitting display devices 210 may be carried out without scribing a plurality of organic light emitting display devices 210 formed on the mother substrate 200 because the mother substrate 200 includes the first and second wire groups 500, 600.

[0081] Wires supplying the voltages of the first and second power source ELVDD, ELVSS extend in different directions and are employed to carry out a test on respective ones of the organic light emitting display device 210 during testing of the organic light emitting display devices on the mother substrate 200.

[0082] The predetermined signal supplied to the respective organic light emitting display device 210 can be independently controlled using, e.g., the first and second circuit units 280, 290 on the mother substrate 200. Accordingly, each of the organic light emitting display devices 210 can be independently controlled, by, e.g., turning off the respective organic light emitting display devices when testing of another or other ones of the organic light emitting display devices 210 are carried out.

[0083] In some embodiments of the invention, each of the organic light emitting display devices 210 can be independently driven, e.g., completely independently driven, and can substantially or completely avoid erroneous operation that may result from, e.g., wire interference between the first and second wire groups 500, 600 after scribing, by arranging the first and second circuit units 280, 290 between the scribing line 310 and the grinding line 320 and separating the electrical connection point between the first and second circuit units 280, 290 and the first and second wire groups 500, 600.

[0084] FIG. 2 illustrates a schematic diagram of one of the exemplary organic light emitting display devices shown in FIG. 1.

[0085] Referring to FIG. 2, in this embodiment each of the organic light emitting display devices 210 can be independently driven, e.g., completely independently driven, and can avoid erroneous operation that may result from interference of wires by electrically disconnecting the organic light emitting display devices 210 from the first and second wire group 500, 600 after scribing. That is, in some embodiments of the invention, an end of the first and second wire groups 500, 600 is electrically disconnected and maintained in an electrically open state, and the power sources and signals for driving the organic light emitting display device 210 are supplied by an external circuit (not shown), such as a printed circuit board, connected to the pad unit 270.

[0086] The first circuit unit 280 and the second circuit unit 290 may be arranged between the pad unit 270 and a side edge of the organic light emitting display device 210. For example, as shown in FIG. 2, the first circuit unit 280 and the second circuit unit 290 are disposed below the pad portion and above the side edge, which may correspond to the scribing line 310. More particularly, e.g., in some embodiments of the invention, if a width between the pad unit 270 and the edge region of the organic light emitting display device 210 is 300 μm, then the first and second circuit units 280, 290 are arranged within a distance of 300 μm from the side edge of the organic light emitting display device 210.

[0087] In some embodiments of the invention, the first circuit unit 280 is arranged between the scan driver 230 and the side edge of the organic light emitting display device 210. That is, as shown in FIG. 2, one or more signal lines, e.g., signal lines extending from one side, of the first circuit unit 280 are connected to the pad portion 270 and/or the scan driver 230, and other signal lines, e.g., signal lines extending from another side, of the first circuit unit 280 are electrically disconnected and maintained in an open state.

[0088] Similarly, one or more signal lines, e.g., signal lines extending from one side, of the second circuit unit 290 are connected, e.g., to one or more of the plurality of scan lines, e.g., nth scan line Sn, and other signal lines, e.g., signal lines extending from another side, of the second circuit unit 290 are electrically disconnected and maintained in an open state.

[0089] FIG. 2 illustrates an organic light emitting dis-

play device 210 in a state in which the organic light emitting display device 210 has not been subjected to a grinding process. That is, the organic light emitting display device 210 illustrated in FIG. 2 has only undergone a scribing process along the scribing line 310 in order to separate the organic light emitting display device 210 from the mother substrate 200 and/or to electrically disconnect the first and/or second wire groups 500, 600 from the pixel portion 220, the scan driver 230, the data distributor 25, the data driver 240, etc. Thus, in some embodiments of the invention, the organic light emitting display device 210 may only undergo a scribing process.

[0090] However, embodiments of the invention need not be limited thereto. For example, in some embodiments of the invention, the organic light emitting display device may be subjected to a scribing process and a grinding process. In such cases, e.g., the grinding process may be carried out along the grinding line 320. In cases in which the first and second circuit units 280, 290 are arranged outside the grinding line 320, the first and second circuit units 280, 290 may be separated from the organic light emitting display device 210 as a result of the grinding process.

[0091] As discussed above, the first and second circuit units 280, 290 can independently control and measure predetermined signals supplied to the respective organic light emitting display device 210. In some embodiments of the invention, the first and second circuit units 280, 290 are arranged between the scribing line 310 and the grinding line 320, but embodiments of the present invention are not limited thereto. For example, some of the first and/or second circuit units 280, 290 can be arranged outside of the scribing line 310. In such cases, the first and/or second circuits 280, 290 arranged outside of the scribing line 310 are removed as a result of the scribing process. In some embodiments of the invention, at least some of the first and second circuit units 280, 290 are arranged between the scribing line 310 and the grinding line 320, and some of the first and second circuit units 280, 290 are arranged outside the scribing line 310.

[0092] In some embodiments of the invention, the above-mentioned organic light emitting display devices 210 on the mother substrate 200 are protected from oxygen and moisture by a sealer 430, which can be provided between a supporting substrate 410 and a sealing substrate 420. The sealing substrate 420 is arranged so as to overlap at least one region of the supporting substrate 410 in some embodiments of the invention.

[0093] FIG. 3 illustrates a cross-sectional view taken along a line A-A' of the mother substrate 200 shown in FIG. 1.

[0094] Referring to FIG. 3 in combination with FIG. 1, each of the organic light emitting display devices 210 formed on the mother substrate 200 in this embodiment includes the supporting substrate 410, the sealing substrate 420 and the sealer 430.

[0095] The supporting substrate 410 is arranged below the pixel unit 220 and the scan driver 230, i.e., the pixel unit 220 and the scan driver 230 are disposed on the supporting substrate 410. The sealing substrate 420 is arranged above the supporting substrate 410, and is arranged above the pixel portion 220 and the scan driver 230 in this embodiment of the invention. The sealer 430 is disposed between the supporting substrate 410 and the sealing substrate 420.

[0096] More particularly, to prevent the organic light emitting diode from infiltration of oxygen and moisture, the sealing substrate 420 is first be arranged above the pixel unit 220 and/or the scan driver 230, and then is attached to the supporting substrate 410 using the sealer 430. That is, a region between the sealing substrate 420 and the supporting substrate 410 that is sealed by the sealer 430 may includes at least one pixel unit 220. For example, the sealing substrate 420 can be arranged above the pixel unit 220 and the scan driver 230, and the sealer 430 can be coated along an edge of the sealing substrate 420 in order to attach the supporting substrate 410 and the sealing substrate 420 to each other. That is, the sealer 430 may be formed in a region outside the pixel unit 220, which may include the organic light emitting diode.

[0097] In some embodiments of the invention, the sealing substrate 420 is formed so as not to overlap the data driver 240 and the data distributor 250. More particularly, the data driver 240 and the like may be installed as chips after the sealing process has been completed, e.g., after the sealing substrate 420 and the supporting substrate 410 have been sealed together.

[0098] In some embodiments of the invention, as discussed above, an additional grinding process may be carried out along the grinding line(s) 320 and the first and second circuit units 280, 290 may be removed from the organic light emitting display device 210 as a result of such grinding. However, in cases in which a laser is employed to seal the supporting substrate 410 and the sealing substrate 420, components of the organic light emitting display device 210 can be arranged a predetermined distance away from the region to be irradiated. For example, in cases in which the data driver 240 and the data distributor 250 are provided as chips installed after the sealing process, care may need to be taken in order to prevent damage to the first and second circuit units 280, 290. In some embodiments, to prevent damage to the first and second circuit units 280, 290 as a result of a laser that may be irradiated during the sealing process, the sealing substrate 420 may be arranged so as not to overlap the first and second circuit units 280, 290, and the sealer 430 may be spaced a predetermined distance away from the first and second circuit unit 280, 290.

[0099] In some cases, a frit is used as the sealer 430. In such cases , e.g., even without employing an absorber, the frit can completely seal a region between the supporting substrate 410 and the sealing substrate 420 such that oxygen and moisture may be effectively prevented from infiltrating into a sealing region (especially, the pixel unit 220). More particularly, in some cases, two sub-

strates may be completely sealed by hardening a melted frit.

[0100] In some cases, the frit may be provided in the form of a powder-type glass material including additives, or a glass in which the frit is generally melted and formed in the related art of glass. Therefore, it may be considered that the frit includes both of the glass material and the glass in such an application. Such a frit may include transition metals. Oxygen and moisture may be prevented from infiltrating between two substrates as a result of the frit completely sealing a region between the supporting substrate 410 and the sealing substrate 420. The frit may be melted by a laser or an infrared ray and hardened.

[0101] More particularly, in some embodiments of the invention, the frit can be coated on the sealing substrate 420 in the form of a frit paste state, and may include an absorber for absorbing a laser or infrared rays and a filler for reducing a thermal expansion coefficient, and may be calcined to remove moisture or an organic binder included in the paste, and then hardened. The frit paste may be a gel-state paste obtained by adding oxide powders and organic materials to the glass powder.

[0102] The frit disposed between the supporting substrate 410 and the sealing substrate 420 may be irradiated by a laser (or the like). However, the laser may damage circuit elements in the vicinity of the frit, e.g., circuit elements that are overlapped with the frit.

[0103] Accordingly, in some embodiments of the present invention, the first and the second circuit units 280, 290 do not overlap the frit 430 in order to prevent heat damage to the first and the second circuit units 280, 290. Thus, in some embodiments of the invention, the first and the second circuit units 280, 290 are disposed in an edge region that is spaced a predetermined distance away from the frit. In some cases, the sealing substrate 420 of the organic light emitting display device 210, arranged in an nth+1 (n is an integer) row on the mother substrate 200, may be spaced apart from the scribing line 310 of the organic light emitting display device 210 arranged in an nth row by a predetermined distance.

[0104] Accordingly, by arranging the first and second circuit units 280, 290 at least a predetermined distance away from the frit, embodiments of the invention enable electrical shorts that may result, e.g., from defects in spacers in a sealing region, and/or thermal damage by laser to be prevented.

[0105] Accordingly, embodiments of the invention enable the first and second circuit units 280, 290 to be protected from damage or deformation from, e.g., the laser, such that the first and second circuit units 280, 290 can independently control and measure predetermined signals to be supplied to the respective organic light emitting display device when the test on the organic light emitting display device 210 on the mother substrate 200 is carried.

[0106] FIG. 4 illustrates a circuit diagram of a first embodiment of a logic gate 380 that may be employed by the first circuit unit 280 shown in FIGS. 1 2. FIG. 5 illustrates a circuit diagram of a second embodiment of a logic gate 380' that may be employed by the first circuit unit 280 shown in FIGS. 1 and 2. More particularly, the second exemplary logic gate 380' illustrated in FIG. 5 includes the first exemplary logic gate 380 shown in FIG. 4.

[0107] Referring to FIGS. 4 and 5, the first logic gate 380 includes an NOR gate.

[0108] The NOR gate includes first to fourth transistors (T1 to T4) connected between the third power source voltage VDD and the fourth power source VSS having a lower voltage value than that of the voltage of the third power source VDD.

[0109] More particularly, the first and second transistors (T1, T2) are connected in series between the third power source VDD and the fourth power source VSS, and may be P-type transistors. The third and fourth transistors (T3, T4) are connected in parallel between the second transistor (T2) and the fourth power source voltage VSS, and may be N-type transistors. Gate electrodes of the first and fourth transistors (T1, T4) are connected to the eleventh wire 610 to receive the horizontal control signal (HC), and gate electrodes of the second and third transistor (T2, T3) are connected to the second wire 520 to receive the vertical control signal (VC).

[0110] Such an NOR gate outputs a signal having a high level voltage value corresponding to the voltage of the third power source VDD only if both the horizontal control signal (HC) and the vertical control signal (VC) supplied to the NOR gate itself have a low level voltage value.

[0111] The above-mentioned NOR gate can be used for generating a shift control signal by outputting a signal having a predetermined voltage value corresponding to the horizontal control signal (HC) and the vertical control signal (VC).

[0112] Referring to FIGS. 4 and 5, the output signal of the NOR gate can be used as a first shift control signal (SCTL). Referring to FIG. 5, a second shift control signal (SCTLB) can be generated by connecting an inverter (IN) to an output terminal of the NOR gate for inverting the first shift control signal (SCTL). That is, the second exemplary logic gate 380' includes the inverter (IN) and the NOR gate of the first exemplary logic gate 380.

[0113] The inverter (IN) of the second exemplary logic gate 380' includes the fifth and sixth transistors (T5, T6) connected in series between the third power source VDD and the fourth power source VSS. A gate electrode of the fifth and sixth transistors (T5, T6is connected to the output terminal of the NOR gate. The fifth and sixth transistors (T5, T6) are formed of different transistor types, i.e., the fifth transistor (T5) may be an P-type transistor and the sixth transistor (T6) may be an N-type transistor.

[0114] As described above, the first shift control signal (SCTL) and the second shift control signal (SCTLB) output from the logic circuits shown in FIGS. 4 and 5 may be used to generate a shift clock signal for controlling the scan driver 230. Details about these features will be described below.

[0115] FIGS. 6 and 7 respectively illustrate third and fourth embodiments 480, 580 of a logic gate that may be included in the first circuit unit 280 shown in FIGS. 1 and 2. As shown in FIG. 7, the fourth exemplary logic gate 580 includes the third exemplary logic gate 480 shown in FIG. 6.

[0116] Referring to FIGS. 6 and 7, the first and second exemplary logic gates 480, 580 includes a generation circuit of the first shift clock signal (SFTCLK) having a tristate inverter (T_IN), a control transistor (Tc) and an inverter (IN 1).

[0117] The tristate inverter (T_IN) includes eleventh to fourteenth transistors (T11 to T14) connected in series between the third power source VDD and the fourth power source VSS. The eleventh and twelfth transistors (T11, T12) are P-type transistors, and the thirteenth and fourteenth transistors (T13, T14) are N-type transistors in this embodiment. A gate electrode of the eleventh transistor (T11) is connected to the output terminal of the NOR gate, as shown in FIG. 4 and FIG. 5, and may thereby receive the first shift control signal (SCTL). Gate electrodes of the twelfth and thirteenth transistors (T12, T13) are connected to one of the fifth wires 550 receiving the scan control signal, and may thereby receive the first clock signal (CLK1). A gate electrode of the fourteenth transistor (T 14) is connected to an output end of a combinational logic gate of the NOR gate and inverter (IN) shown in FIG. 5, and thereby receives the second shift control signal (SCTLB).

[0118] The control transistor (Tc) is connected between the fourth power source voltage VSS and a first node (N1), which is an output terminal of the tristate inverter (T_IN). The control transistor Tc may be an N-type transistor. A gate electrode of the control transistor (Tc) is connected to the output terminal of the NOR gate shown in FIGS. 4 and 5, and thereby receives the first shift control signal (SCTL).

[0119] The inverter (IN1) includes fifteenth and sixteenth transistors (T15, T16) connected in series between the third power source VDD and the fourth power source VSS. Gate electrodes of the fifteenth and sixteenth transistors (T15, T16) are commonly connected to the first node (N1).

[0120] Such a generation circuit of the first shift clock signal (SFTCLK) can generate the first shift clock signal (SFTCLK) having a high level voltage regardless of the first clock signal (CLK1) if the first shift control signal (SCTL) having a high level voltage and the second shift control signal (SCTLB) having a low level voltage are supplied thereto. In other cases, the generation circuit of the first shift clock signal (SFTCLK) generates the first shift clock signal (SFTCLK) having a same waveform as the first clock signal (CLK1). For example, if the generation circuit receives the first shift control signal (SCTL) having a low level voltage and the second shift control signal (SCTLB) having a high level voltage, the generation circuit generates the first clock signal (CLK1) having a same waveform as the first clock signal (CLK1).

[0121] In some embodiments of the invention, the first circuit unit 280 includes logic gates that further include a generation circuit of a second shift clock signal (SFTCLKB), as shown in FIG. 7.

[0122] The logic gates shown in FIG. 7 are identical to the logic gates shown in FIG. 6, except that the logic gates shown in FIG. 7 further include two inverters (IN2, IN3), namely buffers (BU), at an input terminal of the first clock signal (CLK1) in the generation circuit of the first shift clock signal (SFTCLK) shown in FIG. 6, and input terminals of the first and second shift control signals (SCTL, SCTLB) of the second shift clock signal (SFTCLKB) are reversed. Therefore, a detailed description of the logic gates shown in FIG. 7 is omitted.

[0123] Such a generation circuit of the first and second shift clock signals (SFTCLK, SFTCLKB) generates the first and second shift clock signals (SFTCLK, SFTCLKB) having a high level voltage regardless of the first clock signal (CLK1) if the first shift control signal (SCTL) having a high level voltage and the second shift control signal (SCTLB) having a low level voltage are supplied thereto. The generation circuit of the first and second shift clock signals (SFTCLK, SFTCLKB) generates the first shift clock signal (SFTCLK) having the same waveform as that of the first clock signal (CLK1), and the second shift clock signal (SFTCLKB) having a reversed waveform to that of the first clock signal (CLK1) in other cases, e.g., if the generation circuit of the first and second shift clock signals (SFTCLK, SFTCLKB) receives the first shift control signal (SCTL) having a low level voltage and the second shift control signal (SCTLB) having a high level voltage.

[0124] As described above, if the logic gates as shown in FIG. 4 to FIG. 7 are included in the first circuit unit 280, then the generation circuit of the first and second shift clock signals (SFTCLK, SFTCLKB) generates first and second shift clock signals (SFTCLK, SFTCLKB) corresponding to a predetermined horizontal control signal (HC) and a predetermined vertical control signal (VC), and may output the first and second shift clock signals (SFTCLK, SFTCLKB) to the scan driver 230 to independently control the scan driver 230.

[0125] For example, if only a certain one or ones of the organic light emitting display devices 210 have to be turned off for testing one or some others of the organic light emitting display devices 210 on the mother substrate 200, then the vertical control signal (VC) having a low level and the horizontal control signal (HC) having a low level is respectively supplied to the second wire 520 and the eleventh wire 610 connected to the certain organic light emitting display device(s) 210. Then, the first circuit unit 280 receiving the vertical control signal (VC) having the low level and the horizontal control signal (HC) having the low level generates a high level for the first and second shift clock signals (SFTCLK, SFTCLKB) regardless of the first clock signal (CLK1). The high levels of the first and second shift clock signals (SFTCLK, SFTCLKB) generated in the first circuit unit 280 are input into the scan

driver 230 to generate a scan signal and/or an emission control signal for controlling the pixel unit 220 to be turned off. However, this is only an embodiment of one or more aspects of the invention. In embodiments of the invention, signals to be input and their voltage levels may vary according to the circuit configuration of the scan driver 230.

[0126] As discussed above, in some embodiments of the invention, at least some of the first circuit unit 280 are arranged in the edge region between the scribing line 310 and the grinding line 320, and in such cases, the above-mentioned logic gates may be arranged in the edge region of the organic light emitting display devices 210.

[0127] FIG. 8 illustrates a layout diagram of the fourth exemplary embodiment of the logic gate shown in FIG. 7, as formed in region B of FIG. 1. For example, the logic gates such as the tristate inverters (T_IN), the buffers (BU) and the inverters (IN) are arranged between the scribing line 310 on the second wire group 600 and the grinding line 320 beneath the pad unit 270. As shown in FIG. 8, a width (W) of the region between the grinding line 320 and the scribing line 310 along the edge region of the organic light emitting display device 210 may be at or within a range of about 200 μm to 300 μm.

[0128] As shown in FIG. 6, in some embodiments of the invention, the control transistor (Tc) may be an N-type transistor. However, embodiments of the invention are not limited thereto.

[0129] FIG. 9 illustrates a circuit diagram of a fifth exemplary embodiment of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2. The exemplary logic gate 480' illustrated in FIG. 9 substantially corresponds to the exemplary logic gate 480 illustrated in FIG. 6, except for the control transistor (Tc') being a P-type transistor. In this case, the logic gate 480' shown in FIG. 9 is configured and driven in the same manner in the logic gate 480 as shown in FIG. 6, except that the control transistor (Tc') receives the second shift control signal (SCTLB). Therefore the other components of the logic gate 480' shown in FIG. 9 have the same reference numerals as those of the logic gate 480 shown in FIG. 6 and their detailed descriptions are omitted.

[0130] FIG. 10 illustrates a circuit diagram of a sixth embodiment of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2.

[0131] Referring to FIG. 10, the first circuit unit 280 includes a plurality of inverters (IN). Each of the inverters (IN) includes different types of transistors that are connected in series between the third power source VDD and the fourth power source VSS. The first circuit unit 280 receives a scan control signal (SCS) from one of the fifth wires 550 of the first wire group 500, and may repeatedly invert (three times in FIG. 10) and output the scan control signal (SCS) using each of the inverters (IN).

[0132] If the input signals are delayed, then such a first circuit unit 280 may be effective to prevent the organic light emitting display device 210 (especially, the scan driver 230) from being erroneously operated by compensating for a delay of the scan control signal (SCS), which may be supplied from the first or second wire group 500, 600 when testing of the organic light emitting display device on the mother substrate 200 is being out. That is, in some embodiments of the invention, the first circuit unit 280 can have a function of compensating for the delay.

[0133] If, as described above, the first circuit unit 280 includes a plurality of inverters (IN) to compensate for a delay of input signals, the first circuit unit 280 is arranged between the scan driver 230 and the fifth wires 550 to which the scan control signal (SCS) may be supplied from the outside.

[0134] In some embodiments of the invention, the first circuit unit 280 includes a transmission gate, an NAND gate or an exclusive XOR gate, in addition to the logic gates as described above. The transmission gate can be used for the purpose of selectively turning on the respective organic light emitting display device(s) 210 formed on the mother substrate 200, and the NAND gate or the exclusive XOR gate may be used for the purpose of generating a shift control signal (SCTL) and/or a shift clock signal (SFTCLK) and the like.

[0135] FIG. 11 illustrates a circuit diagram of a seventh embodiment of a logic gate employable by the first circuit unit shown in FIGS. 1 and 2.

[0136] Referring to FIG. 11, the second circuit unit 290 includes a tristate inverter 390 connected between the third power source VDD and the fourth power source VSS.

[0137] The tristate inverter includes twenty first to twenty fourth transistors (T21 to T24) connected in series between the third power source voltage VDD and the fourth power source voltage VSS. The twenty first and twenty second transistors (T21, T22) are P-type transistors, and the twenty third and twenty fourth transistors (T23, T24) are N-type transistors in this embodiment. A gate electrode of the twenty first transistor (T21) is connected to the first circuit unit 280 to receive the first shift control signal (SCTL). Gate electrodes of the twenty second and twenty third transistors (T22, T23) are connected to an nth scan line (Sn) to receive an nth scan signal (SSn). A gate electrode of the twenty fourth transistor (T24) are connected to the first circuit unit 280 to receive the second shift control signal (SCTLB).

[0138] Such a second circuit unit 290 outputs the scan measuring signal, corresponding to the nth scan signal (SSn), to a twelfth wire 620 if the organic light emitting display device 210 connected to the second circuit unit 290 is normally operated, e.g., in cases other than when the first shift control signal (SCTL) is at a high level and the second shift control signal (SCTLB) is at a low level, when the test on the organic light emitting display device 210 on the mother substrate 200 is carried out. Accordingly, it may be tested whether or not a scan signal is generated normally by measuring the signals output from the twelfth wire 620 when the test on the organic light emitting display device 210 on the mother substrate 200 is carried out.

[0139] The second circuit unit 290 receives the first and second shift control signals (SCTL, SCTLB) from the first or second wire group 500, 600 if the generation circuits of the first and second shift control signals (SCTL, SCTLB) are not included in the first circuit unit 280.

[0140] FIG. 12 illustrates a circuit diagram of an embodiment of the pixel shown in FIG. 1 and FIG. 2. Referring to FIG. 12, the pixel 225 includes an organic light emitting diode (OLED), and a pixel circuit 227 connected to the nth scan line (Sn), the nth emission control line (EMn), the mth data line (Dm), the first power source voltage ELVDD, the reset power source voltage Vinit and the organic light emitting diode (OLED) to allow the organic light emitting diode (OLED) to emit the light. The reset power source Vinit is supplied to each pixel 225 from predetermined wires (not shown), belonging to the first or second wire group 500, 600 when the test on the organic light emitting display device 210 on the mother substrate 200 is carried out.

[0141] An anode electrode of the organic light emitting diode (OLED) is connected to the pixel circuit 227, and a cathode electrode of the organic light emitting diode (OLED) is connected to the second power source voltage ELVSS. Such an organic light emitting diode (OLED) emits light with a predetermined luminance corresponding to an electric current supplied to the organic light emitting diode (OLED) itself.

[0142] The pixel circuit 227 includes first to sixth transistors (M1 to M6) and a storage capacitor (Cst). The first to sixth transistors (M1 to M6) are P-type transistors, as shown in FIG. 12. Embodiments of the present invention need not be limited thereto. A first electrode of the first transistor (M1) is connected to a second node (N2), and a second electrode of the first transistor (M1) is connected to a third node (N3). A gate electrode of the first transistor (M1) is connected to the first node (N1). The first transistor (M1) supplies an electric current to the third node (N3) corresponding to a voltage stored in the storage capacitor (Cst).

[0143] A first electrode of the second transistor (M2) is connected to the mth data line (Dm), and a second electrode of the second transistor (M2) is connected to the third node (N3). A gate electrode of the second transistor (M2) is connected to the nth scan line (Sn). The second transistor (M2) is turned on when a scan signal is supplied to the nth scan line (Sn), and thereby supplies a data signal, supplied to the mth data line (Dm), to the third node (N3).

[0144] A first electrode of the third transistor (M3) is connected to the second node (N2), and a second electrode of the third transistor (M3) is connected to the first node (N1). A gate electrode of the third transistor (M3) is connected to the nth scan line (Sn). The third transistor (M3) is turned on when a scan signal is supplied to the nth scan line (Sn), and thereby connects the first transistor (M1) in a diode-connected mode.

[0145] A first electrode of the fourth transistor (M4) is connected to the reset power source voltage Vinit, and a second electrode of the fourth transistor (M4) is connected to the first node (N1). A gate electrode of the fourth transistor (M4) is connected to the nth-1 scan line (Sn-1). The fourth transistor (M4) is turned on when a scan signal is supplied to the nth-1 scan line (Sn-1), and may thereby reset the storage capacitor (Cst) and a gate terminal of the first transistor (M1). Thus, a voltage level of the reset power source voltage Vinit is set to a lower range than that of the data signal.

[0146] A first electrode of the fifth transistor (M5) is connected to the first power source voltage ELVDD, and a second electrode of the fifth transistor (M5) is connected to the second node (N2). A gate electrode of the fifth transistor (M5) is connected to the nth emission control line (EMn). The fifth transistor (M5) is turned on when an emission control signal is supplied to the nth emission control line (EMn), and thereby transfers a voltage value of the first power source voltage ELVDD to the second node (N2).

[0147] A first electrode of the sixth transistor (M6) is connected to the third node (N3), and a second electrode of the sixth transistor (M6) is connected to the anode electrode of the organic light emitting diode (OLED). A gate electrode of the sixth transistor (M6) is connected to the nth emission control line (EMn). The sixth transistor (M6) is turned on when an emission control signal is supplied to the nth emission control line (EMn), and thereby electrically connects the organic light emitting diode (OLED) to the third node (N3).

[0148] One terminal of the storage capacitor (Cst) is connected to the first power source voltage ELVDD and the first electrode of the fifth transistor (M5), and another terminal of the storage capacitor (Cst) is connected to the first node (N1). The storage capacitor (Cst) charges a voltage corresponding to the data signal and a threshold voltage (Vth) of the first transistor (T1) when a scan signal is supplied to the nth scan line (Sn), and maintains the charged voltage during one frame.

[0149] FIG. 13 illustrates an exemplary waveform diagram of driving signals for driving the pixel circuit shown in FIG. 12. Exemplary operation system of the pixel 225 as shown in FIG. 12 will be described in detail, in combination with FIGS. 12 and 13.

[0150] Referring to FIG. 13, during a first time period t1, a scan signal (SS) may be supplied to an nth-1 scan line (Sn-1), and an emission control signal (EMI) is supplied to an nth emission control line (EMn). If the emission control signal (EMI) having a high level is supplied to the nth emission control line (EMn), then the fifth and sixth transistors (M5, M6) is turned off. If the scan signal (SS) is supplied to the nth-1 scan line (Sn-1), then the fourth transistor (M4) is turned on. If the fourth transistor (M4) is turned on, then the storage capacitor (Cst) and the gate terminal of the first transistor (M1) are connected to the reset power source (Vinit). If the storage capacitor (Cst) and the gate terminal of the first transistor (M1) are connected to the reset power source (Vinit), then the reset power source (Vinit) is supplied to the storage capac-

itor (Cst) and the gate terminal of the first transistor (M1), and then reset.

[0151] Subsequently, during a second period t2, a scan signal is supplied to the nth scan line (Sn). If the scan signal (SS) is supplied to the nth scan line (Sn), then the second and third transistor (M2, M3) is turned on. If the third transistor (M3) is turned on, then the first transistor (M1) is diode-connected. If the second transistor (M2) is turned on, then the data signal supplied to the mth data line (Dm) is transferred to the third node (N3). At this time, the voltage supplied to the third node (N3) is supplied to the first node (N1) via the first and third transistors (M1, M3) because the gate terminal of the first transistor (M1) is reset to a lower voltage value than that of the data signal by means of the reset power source (Vinit). Then, voltages corresponding to the threshold voltage (Vth) of the first transistor (M1) and the data signal are stored in the storage capacitor (Cst).

[0152] Subsequently, the fifth and sixth transistors (M5, M6) are turned on if the emission control signal (EMI) is not supplied to the nth emission control line (EMn), i.e., the emission control signal (EMI) has a low level. If the fifth and sixth transistors (M5, M6) are turned on, then an electric current corresponding to the data signal flows from the first power source voltage ELVDD to the organic light emitting diode (OLED), and therefore, the lights corresponding to the data signal is generated in the organic light emitting diode (OLED).

[0153] The above-mentioned pixel 225 receives the scan signal (SS) and the emission control signal (EMI), which control all of the switching transistors (M2 to M6) to be turned off, from the scan driver 230 receiving the predetermined first and second shift clock signals (SFTCLK, SFTCLKB) from the first circuit unit 280, if the organic light emitting display device 210 is set to be turned off by means of the predetermined vertical control signal (VC) and the predetermined horizontal control signal (HC) when the test on the organic light emitting display device on the mother substrate 200 is carried out.

[0154] As described above, the organic light emitting display device according to some embodiments of the present invention and the mother substrate of the same may carry out sheet unit tests on a plurality of organic light emitting display devices formed on the mother substrate prior to scribing the organic light emitting display devices, because the mother substrate includes the first and second wire groups. Accordingly, the test time may be shortened, and the expense may be lowered, which result in improved test efficiency.

[0155] Also, a predetermined signal supplied to the certain organic light emitting display device can be independently controlled because the mother substrate includes the first and second circuit units. Accordingly, it is possible to independently control and measure each of the organic light emitting display devices, e.g., by turning off the erroneously operated certain organic light emitting display devices when the tests on a plurality of organic light emitting display devices on the mother substrate are carried out.

[0156] Also, the first and second circuit units can effectively control the organic light emitting display devices by preventing deformation and damage to the first and second circuit units that may occur during the sealing process because the first and second circuit units can be arranged between the scribing lines and the grinding lines and spaced at a predetermined distance apart from the sealer (especially, the frit).

[0157] Exemplary embodiments of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A light emitting display device, comprising:

   a plurality of pixels;
   a plurality of scan lines for selectively applying a scan signal to the pixels;
   a plurality of data lines arranged to cross the scan lines for applying a data signal to the respective pixels;
   a scan driver for applying a scan signal to the scan lines; and
   at least one first testing unit electrically connected to the scan driver,

   wherein at least one output line of the first testing unit is electrically connected to the scan driver, and at least one other output line of the first testing unit is electrically disconnected and in an electrically open state.

2. A light emitting display device according to claim 1, wherein the light emitting display device is an organic light emitting display device and each of the pixels includes an organic light emitting diode.

3. A light emitting display device according to claim 1 or 2, further comprising a pad unit for receiving a driving signal from the outside.

4. A light emitting display device according to claim 3, wherein the first testing unit is electrically connected to the scan driver through the pad unit, and arranged in an edge region of the light emitting display device.

5. A light emitting display device according to any one of claims 1 to 4, wherein the first testing unit is arranged within a distance of about 300 μm from one

side edge of the light emitting display device.

6. A light emitting display device according to any one of claims 1 to 5, wherein the first testing unit includes at least one logic gate.

7. A light emitting display device according to claim 6, wherein the logic gate comprises at least one of a NOR gate, a buffer and an inverter.

8. A light emitting display device according to claim 7, wherein the inverter is a tristate inverter.

9. A light emitting display device according to any one of claims 1 to 8, further comprising a second testing/measuring unit arranged in an edge region of the light emitting display device.

10. A light emitting display device according to claim 9, wherein at least one output line of the second testing/measuring unit is electrically connected to any one of a plurality of the scan lines, and at least one other output line of the second testing/measuring unit is electrically disconnected and in an electrically open state.

11. A light emitting display device according to claim 10, wherein the second testing/measuring unit includes at least one logic gate.

12. A light emitting display device according to claim 11, wherein the logic gate includes at least one inverter.

13. A light emitting display device according to claim 12, wherein the inverter is a tristate inverter.

14. A light emitting display device according to any one of claims 1 to 13, further comprising a transistor group having a plurality of transistors connected to respective first ends of the data lines.

15. A light emitting display device as claimed in claim 14, wherein the data lines are directly connected to the pixels.

16. A light emitting display device according to claim 15, wherein the transistors provided in the transistor group are arranged to be in a turned-off state to corresponding to a control signal supplied from the outside.

17. A light emitting display device according to claim 15 or 16, further comprising:

a data driver for supplying a data signal to the data lines; and
a data distributor connected between the data driver and respective second ends of the data lines to supply the data signals, supplied via at least one of output line of the data driver, to the plurality of the data lines.

18. A light emitting display device according to any one of claims 1 to 17, further comprising a supporting substrate and a sealing substrate, wherein the pixels are sandwiched between the supporting substrate and the sealing substrate.

19. A light emitting display device according to claim 18, further comprising a sealer formed between the supporting substrate and the sealing substrate, and formed outside of the pixels.

20. A light emitting display device according to claim 19, wherein the sealer comprises at least one of a transition metal and a filler.

21. A light emitting display device according to claim 20, wherein the sealer is a frit.

22. A light emitting display device according to any one of claims 18 to 21, wherein the sealing substrate is arranged so as to keep the first testing unit exposed.

23. A light emitting display device according to according to any one of claims 1 to 22, further comprising at least one of a first wire group extending in a first direction on a border region of the light emitting display device, and a second wire group extending in a second direction on the border.

24. A light emitting display device according to claim 23, wherein ends of the first and second wire groups are electrically disconnected and maintained in an electrically open state.

25. A mother substrate including a plurality of light emitting display devices, the mother substrate comprising:

a first wire group extending in a first direction on a border region of the light emitting display devices; and
a second wire group extending in a second direction in the border region of the light emitting display devices,

wherein each of the light emitting display devices includes:

a plurality of pixels;
a plurality of scan lines for selectively applying a scan signal to the pixels;
a plurality of data lines crossing the scan line and applying a data signal to the pixel;
a scan driver for applying a scan signal to the

scan lines; and
at least one first testing unit connected between the scan driver and a predetermined wire included in the first or second wire group,

wherein the scan driver is arranged to generate a scan signal corresponding to a control signal supplied from the first testing unit, and power sources and signals supplied via the first or second wire group.

26. A mother substrate according to claim 25, wherein the first testing unit is arranged between a first scribing line for separating the light emitting display devices and a second grinding line of the light emitting display devices.

27. A mother substrate according to claim 26, wherein each of the light emitting display devices includes a pad unit for receiving a driving signal, and the first testing unit is arranged between the pad unit and the first scribing line.

28. A mother substrate as according to any one of claims 25 to 27, wherein the first testing unit controls the scan driver based on signals supplied from predetermined wires included in the first and second wire group.

29. A mother substrate according to any one of claims 25 to 28, further comprising a second testing/measuring unit connected between any one of a plurality of the scan lines and a predetermined wire included in the first or second wire group.

30. A mother substrate according to claim 29, wherein the second testing/measuring unit is arranged to output an output signal to a predetermined wire included in the first or second wire group, the output signal corresponding to the scan signal supplied from the scan line connected to the second circuit unit itself, and the power sources and signals supplied from the first or second wire group.

31. A mother substrate according to claim 29, wherein the second testing/measuring circuit unit is arranged within a distance about 300 μm from a first line for separating the light emitting display devices.

32. A mother substrate as claimed in claim 31, wherein the second testing/measuring unit is arranged between a first scribing line and a second grinding line of the light emitting display devices.

33. A mother substrate according to any one of claims 25 to 32, wherein the light emitting display devices further comprise a transistor group having a plurality of transistors connected between first respective ends of the data lines and a predetermined wire included in the first or second wire group.

34. A mother substrate according to claim 33, wherein the transistors provided in the transistor group are turned on at a same time to corresponding to a test control signal supplied from the first or second wire group.

35. A mother substrate according to claim 34, wherein the transistor group outputs a test signal, supplied from the first or second wire group, to the data lines corresponding to the test control signal.

FIG. 1

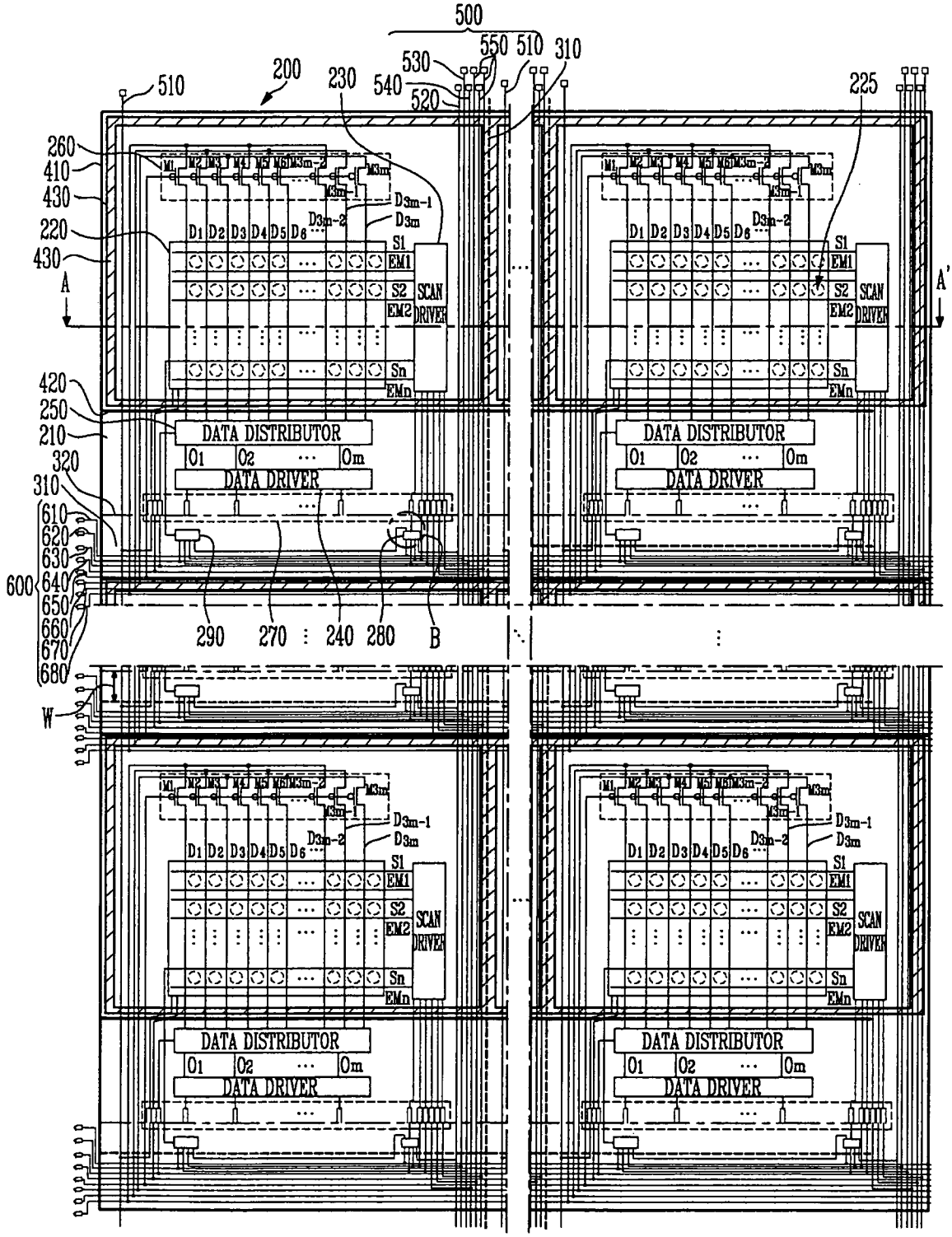

500
550
510
310
530
540
520
200
230
510
225
260
410
430
220
430
A
A'
420
250
210
320
310
610
620
630
600
640
650
660
670
680
W
290
270
240
280
B
DATA DISTRIBUTOR
DATA DRIVER
SCAN DRIVER
S1
S2
Sn
EM1
EM2
EMn
D1 D2 D3 D4 D5 D6
D3m-2
D3m-1
D3m
O1 O2 Om

FIG. 2

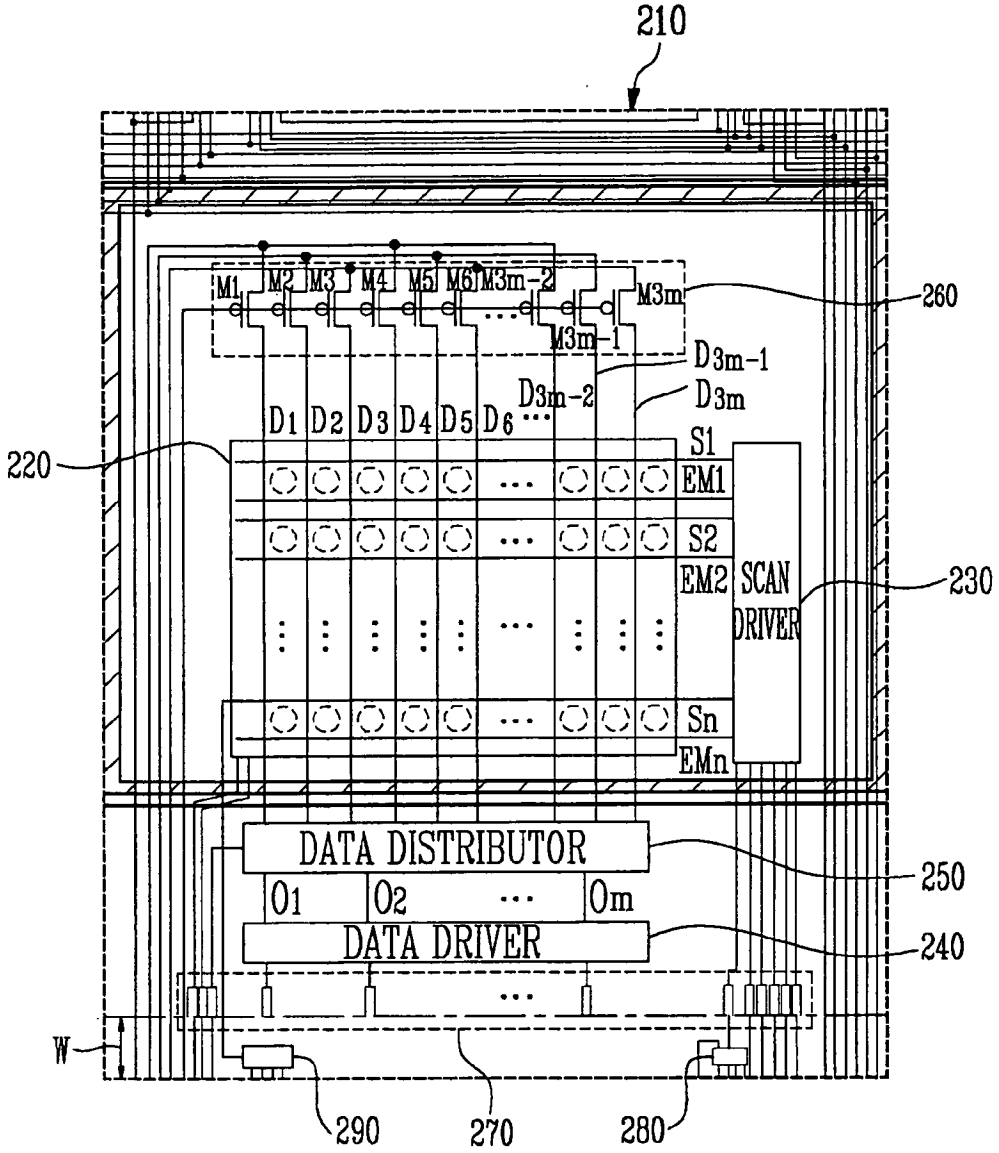

210
M1
M2
M3
M4
M5
M6
M3m-2
M3m-1
M3m
260
D3m-1
D3m-2
D3m
D1
D2
D3
D4
D5
D6
S1
EM1
S2
EM2
Sn
EMn
SCAN DRIVER
220
230
DATA DISTRIBUTOR
250
O1
O2
Om
DATA DRIVER
240
W
290
270
280

FIG. 3

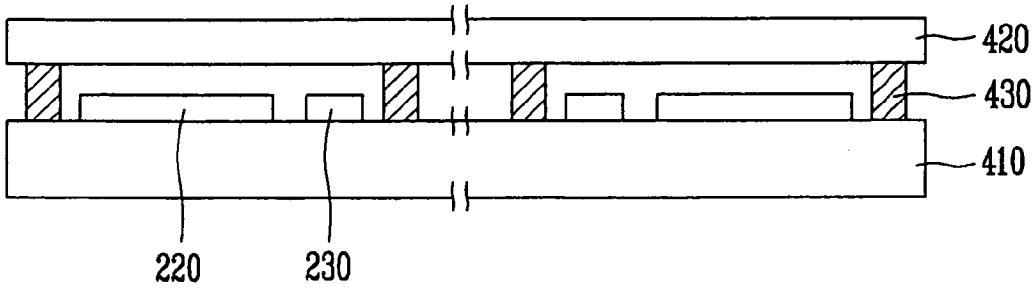

420
430
410
220
230

FIG. 4

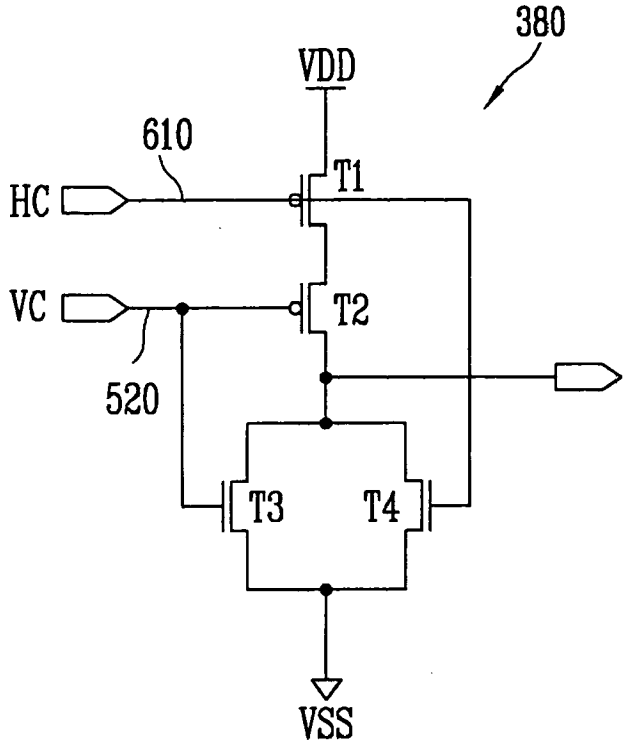

380
VDD
610
T1
HC
VC
T2
520
T3
T4
VSS

FIG. 5

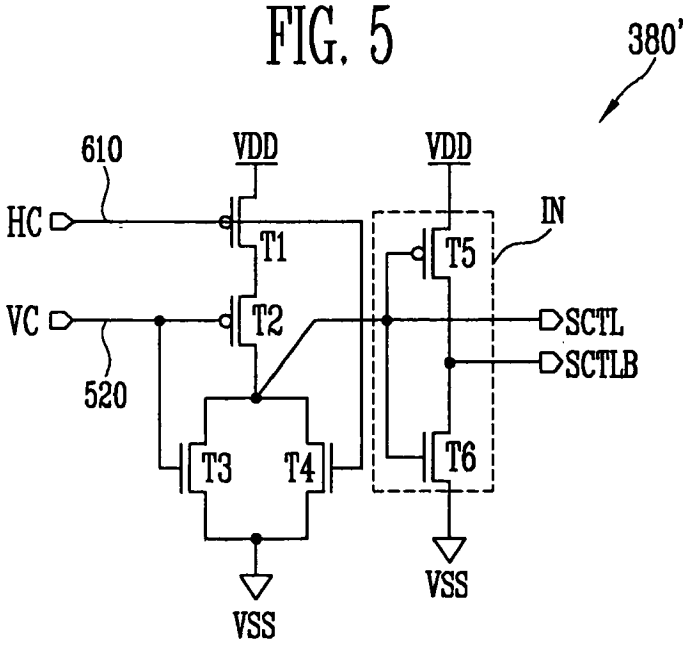

380'
610
VDD
VDD
HC
T1
IN
T5
VC
T2
SCTL
SCTLB
520
T3
T4
T6
VSS
VSS

FIG. 6

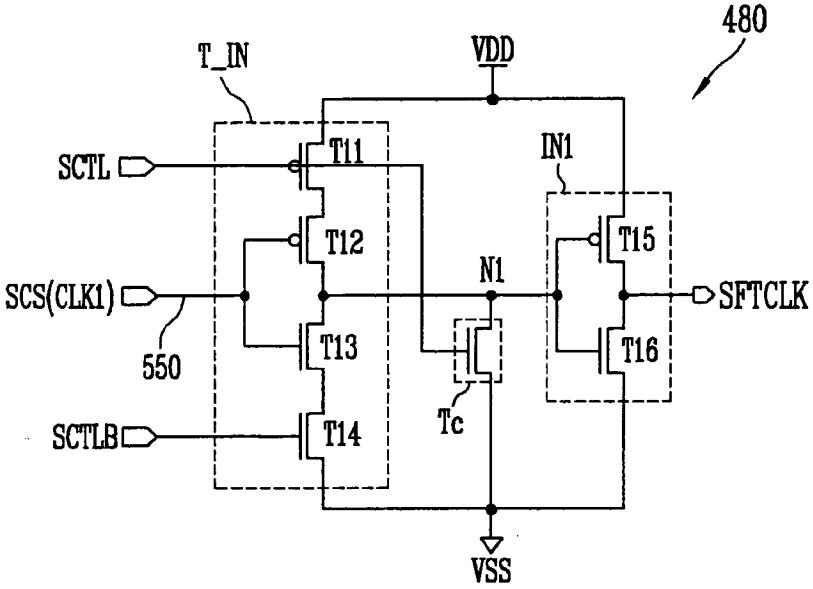

480
T_IN
VDD
SCTL
T11
IN1
T12
T15
N1
SCS(CLK1)
SFTCLK
550
T13
T16
Tc
SCTLB
T14
VSS

FIG. 7

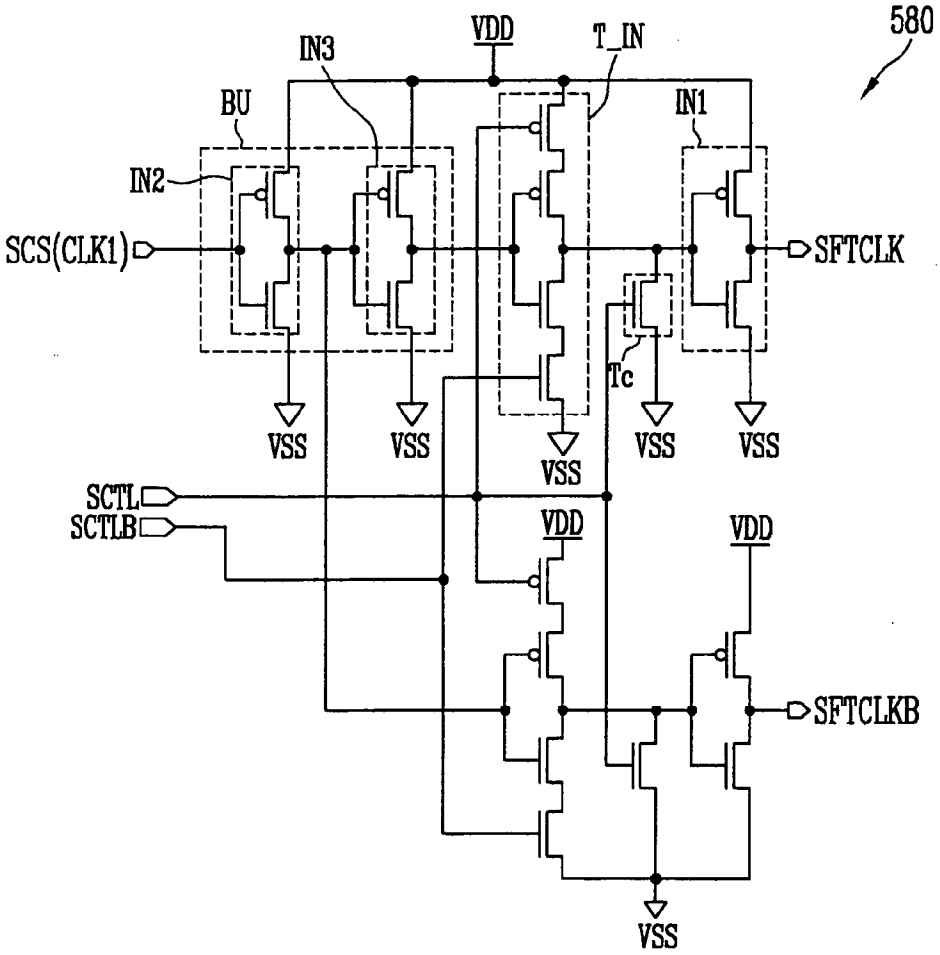

580
VDD
T_IN
IN3
BU
IN1
IN2
SCS(CLK1)
SFTCLK
Tc
VSS
VSS
VSS
VSS
VSS
SCTL
SCTLB
VDD
VDD
SFTCLKB
VSS

FIG. 8

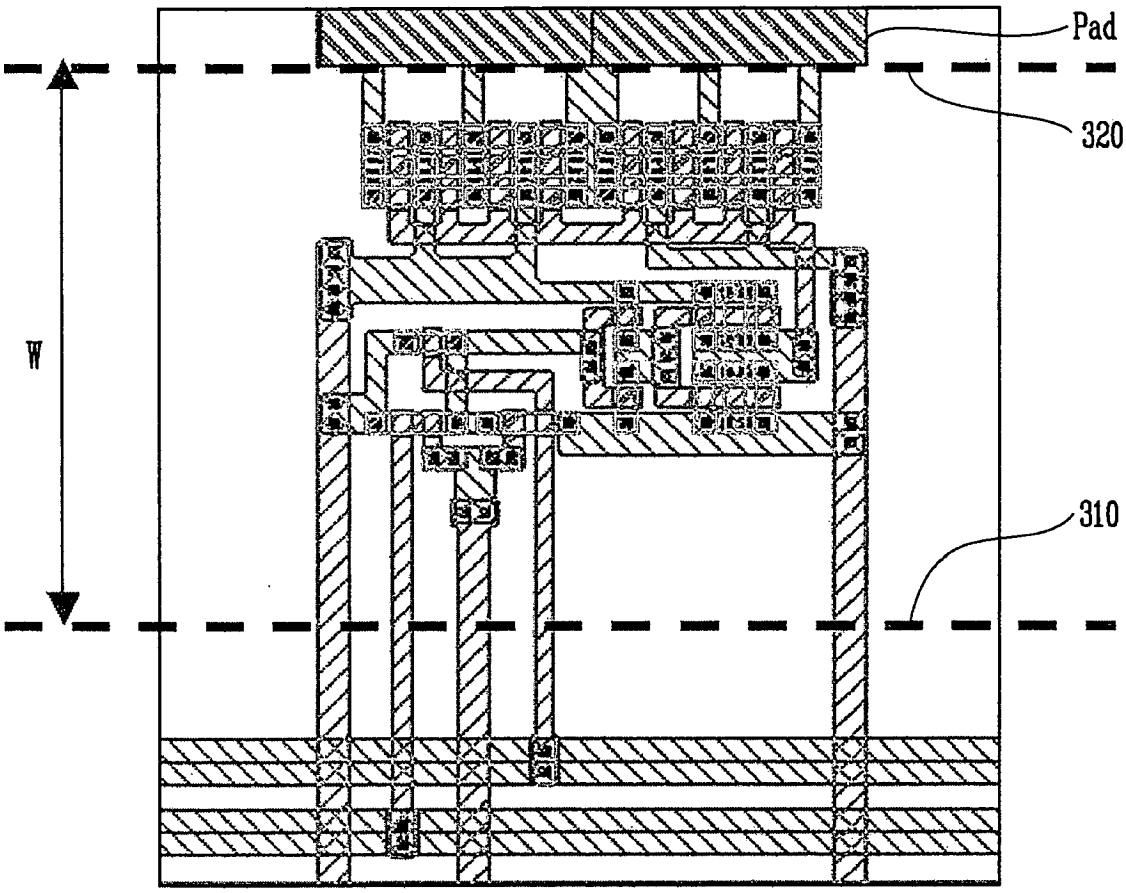


FIG. 9

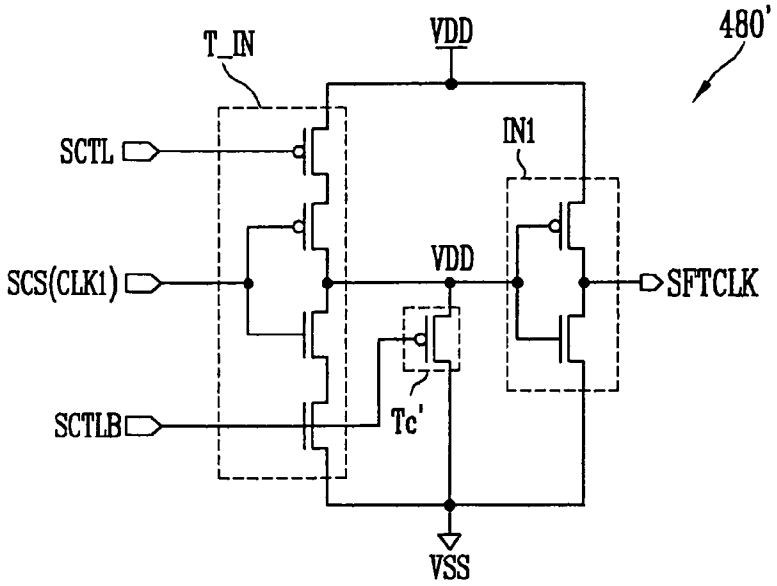


FIG. 10

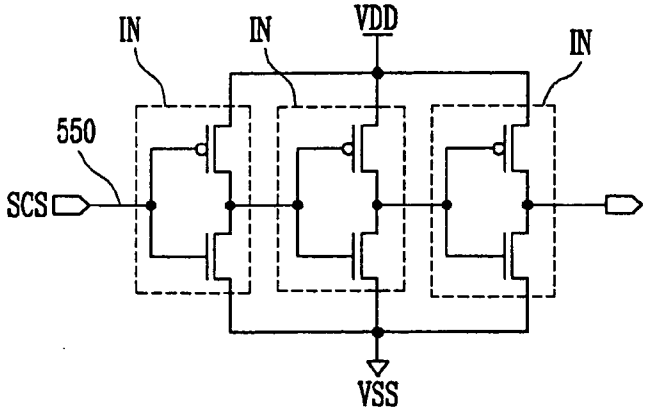


FIG. 11

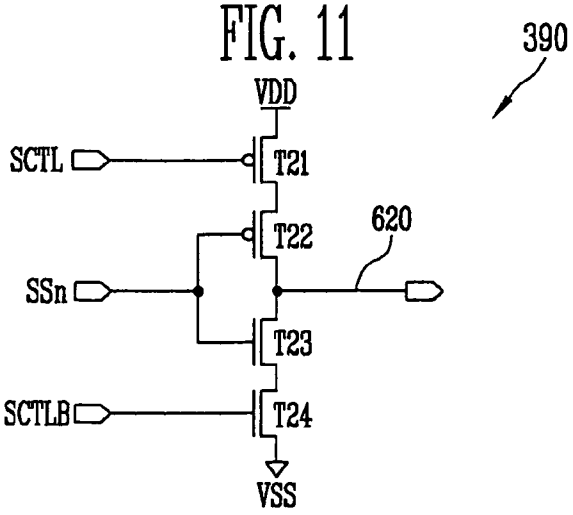


FIG. 12

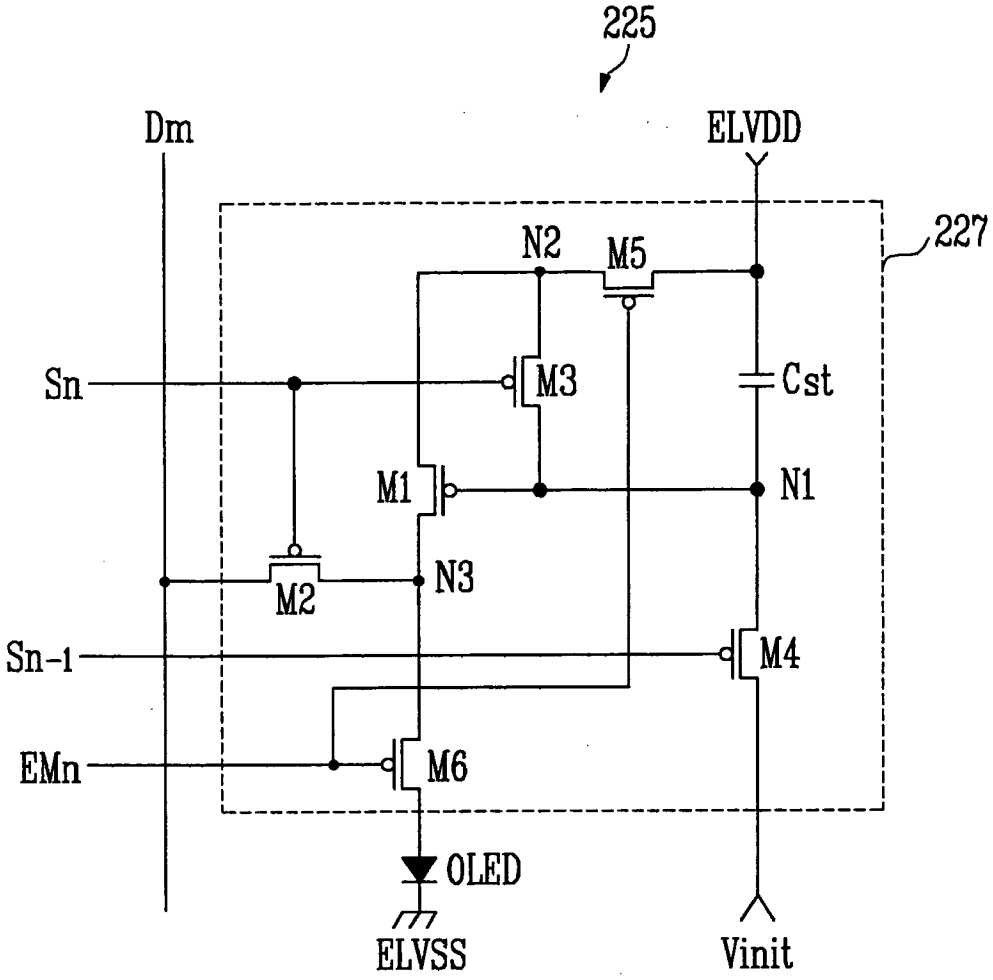
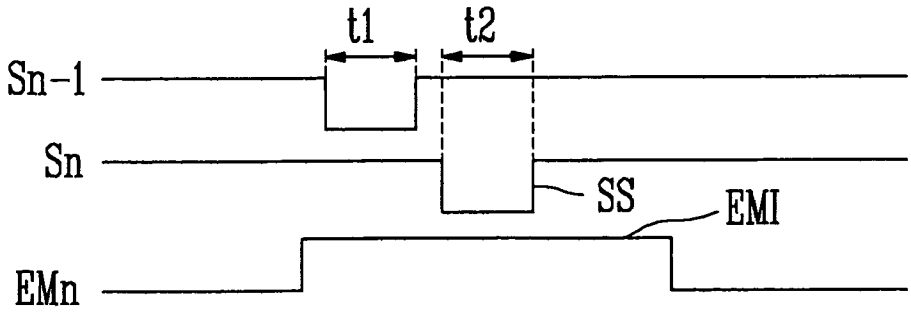

225
Dm
ELVDD
227
N2
M5
Sn
M3
Cst
M1
N1
M2
N3
Sn-1
M4
EMn
M6
OLED
ELVSS
Vinit

FIG. 13


t1
t2
Sn-1
Sn
SS
EMI
EMn

专利名称(译)	有机发光显示装置及其母基板		
公开(公告)号	EP1892695A2	公开(公告)日	2008-02-27
申请号	EP2007253326	申请日	2007-08-23
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	KWAK WON KYU		
发明人	KWAK, WON-KYU		
IPC分类号	G09G3/30 G09G3/32 G09G3/00		
CPC分类号	G09G3/3266 G09G3/006 G09G2300/0842 G09G2300/0861 G09G2310/0251 G09G2310/0262 G09G2310/0289 G09G2320/0693		
优先权	1020060079930 2006-08-23 KR		
其他公开文献	EP1892695A3 EP1892695B1		
外部链接	Espacenet		

摘要(译)

发光显示装置可包括多个像素，用于选择性地将扫描信号施加到像素的多条扫描线，与用于将数据信号施加到各个像素的扫描线交叉的多条数据线，用于扫描驱动器的扫描驱动器将扫描信号施加到扫描线，并且至少一个第一测试单元电连接到扫描驱动器，其中第一测试单元的至少一个输出线电连接到扫描驱动器，以及至少一个其他输出线。第一测试单元电断开并处于电开路状态。