(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 764 773 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
08.04.2015 Bulletin 2015/15

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **06254876.3**

(22) Date of filing: **20.09.2006**

(54) **Scan driving ciruit and organic light emitting display using the same**

Zeilentreiberschaltung und organische lichtemittierende Anzeige mit einer solchen Einheit

Circuit de commande de balayage et affichage électroluminescent organique l'utilisant

(84) Designated Contracting States:
DE FR GB

(30) Priority: **20.09.2005 KR 20050087426**

(43) Date of publication of application:
21.03.2007 Bulletin 2007/12

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The field of the present invention relates to an organic light emitting display, and more particular to a scan driving circuit used for a current programming type organic light emitting display.

2. Description of the Related Art

[0002] In general, an organic light emitting display electrically excites a phosphorous organic compound to emit light, and it voltage- or current-drives an array of organic light emitting cells to display images. Such an organic light emitting cell includes an anode of indium tin oxide (ITO), an organic thin film, and a cathode layer of metal.

[0003] The organic thin film has a multi-layer structure including an emitting layer (EML), an electron transport layer (ETL), and a hole transport layer (HTL) so as to maintain a balance between electrons and holes and to improve the light emitting efficiency, and further includes an electron injection layer (EIL) and a hole injecting layer (HIL).

[0004] Methods for driving the organic emitting cells include the passive matrix driving method, and the active matrix driving method using thin film transistors (TFTs) or metal oxide semiconductor field effect transistors (MOSFETs). The passive matrix display includes an array of cathode lines and anode lines which cross with each other. The active matrix display includes an array of pixels each having a TFT, a capacitor and an ITO pixel electrode to maintain a voltage across the capacitor.

[0005] Active matrix driving methods may be classified as voltage programming methods or a current programming methods, according to the type signal used to charge a voltage on a capacitor.

[0006] An active matrix type of organic light emitting display includes a display panel, a data driving circuit, a scan driving circuit, and a timing controller. The scan driving circuit receives a scan drive control signal from the timing controller, generates a scan signal, and sequentially provides the scan signal to scan lines of the display panel. That is, the scan driving circuit functions to sequentially generate the scan signal to be provided to the display panel in order to drive pixels included in the display panel.

[0007] FIG. 1 is a block diagram showing a conventional scan driving circuit. With reference to FIG. 1, the conventional scan driving circuit includes a plurality of stages ST 1 to STn, which are coupled with a start pulse SP input line. The plurality of stages ST1 to STn sequentially shifts a clock signal C in response to a start clock SP so as to generate output signals SO1 to Son. Each of the second to n-th stages ST2 to STn receives and shifts an output signal of a previous stage as a start pulse for the next stage. Accordingly, the stages generate output signals SO1 to SOn in such a way that the start pulse is sequentially shifted, and provide the output signals for a matrix pixel array.

[0008] FIG. 2 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 1. FIG. 3 is an input/output waveform diagram of the stage shown in FIG. 2. Referring to FIG. 2 and FIG. 3, conventionally, each stage constituting a scan driving circuit uses a master-slave flip-flop. When a clock clk is at a low level, such a flip-flop continues to receive an input while maintaining the previous output. In contrast to this, when the clock clk is at high level, the flip-flop maintains an input IN received when the clock clk is at the low level, and outputs the received input, but no longer receives input.

[0009] In the aforementioned circuit, an inverter included in the flip-flop has disadvantages which include that a static current flows when the input thereof is at a low level. Furthermore, in the flip-flop, the number of inverters having received a low-level input is the same number as that of inverters having received a high-level input. Accordingly, the static current flows through half of all the inverters in the flip-flop, thereby causing excessive power consumption.

[0010] In addition, FIG. 2 shows an embodiment of the inverter circuit. According to this embodiment the high level output of the inverter is determined according to the ratio of resistance values of first and second PMOS transistors M1 and M2. The low level output of the inverter is determined according to the threshold voltage of the first PMOS transistor M1.

[0011] Due to manufacturing variations, resistance and threshold parameters vary significantly from transistor to transistor. This is a significant problem because the transistors for organic light emitting displays often use transistors having high manufacturing variability. As a result, the performance of the circuit of FIG. 2 is uncertain. For example, threshold variation causes the low level output of each inverter to vary. As a result, when a low level output from a first inverter having an uncertain value is provided as the input to a second inverter, the second inverter may have a degraded high output level because the uncertain low value results in uncertain pull-up resistance in the first PMOS transistor of the second inverter.

[0012] Furthermore, in the inverter, when outputting a high level, a constant electric current flows through both the first and second PMOS transistors M1 and M2. This results in constant power consumption. Also, the constant electric current flowing in the second PMOS transistor M2 causes slower rise times for the inverter output signal.

[0013] US 2005/0093464 discloses a pixel circuit of an organic EL display. The pixel circuit includes a driving transistor for transmitting a driving current to an organic EL element. A first capacitor is provided that is connected between a gate and a source of the driving transistor, and a second capacitor is provided that is connected between a gate thereof and a boosting scan line.

[0014] US 6,339,631 discloses a shift register that uses a plurality of stages connected in series to a start pulse input line. In each stage, an output circuit current responds to a first control signal to apply any one of first and second clock signals to a row line of a liquid crystal cell array, and thus to charge the low line of the liquid crystal cell array, and responds to a second control signal to discharge a voltage at the row line.

[0015] US 2004/0227718 discloses a shift register and includes stages that shift an input signal with phase-delayed control signals and first and second supply voltages, and for applying shifted input signals as output signals and as input signals of succeeding stages.

[0016] US 5,517,543 discloses a circuit having a plurality of cascaded stages. Each stage includes several partial stages and has at most two capacitors and at most seven transistors. The second device includes a device for controlling the stages with four periodic clock signals phase shifted by about 90° relative to each other such that each of the cascaded stages is controlled by a respective assigned one of four predetermined sets of two of the four periodic clock signals and the same one of the four predetermined set repeats every fifth cascaded stage.

[0017] US 2005/0078076 discloses a scan driver comprising a first scanning section 530 comprising a plurality of stages configured to sequentially output selection signals and a clearing section 540 comprising a plurality of stages and configured to sequentially output clear signals. Each stage of the first scanning section 530 and the clearing section being configured to receive a first and a second clock signal as input. US 2005/0078076 further discloses the scan driver comprising a first section configured to output selection and clear signals to odd signal lines and a second section configured to output selection and clear signals to even signal lines.

SUMMARY OF CERTAIN INVENTIVE ASPECTS

[0018] Accordingly, some embodiments of the invention provide a scan driving circuit and an organic light emitting display using the same, which reduce power consumption by removing a current flow path of a static current from a stage of each unit, wherein the scan driving circuit includes a first scan driver for providing a selection signal and/or a boost signal, and a second scan driver for providing an emission signal, wherein the first scan driver includes a scan drive unit for outputting the selection signal, a first boost drive unit for outputting an odd-numbered boost signal, and a second boost drive unit for outputting an even-numbered boost signal.

[0019] According to a first aspect of the invention there is provided a scan driving circuit as set out in claim 1. Preferred features of this aspect are set out in claims 2 to 5.

[0020] According to a second aspect of the invention, there is provided an organic light emitting display as set out in claim 6.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] These and/or other aspects and advantages of the invention will become apparent and more readily appreciated from the following description of the preferred embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 is a block diagram showing a conventional scan driving circuit;
FIG. 2 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 1;
FIG. 3 is an input/output waveform diagram of the stage shown in FIG. 2;
FIG. 4 is a block diagram showing an organic light emitting display according to one embodiment;
FIG. 5 is a circuit diagram showing an example of a pixel circuit arranged at each pixel region of the organic light emitting display shown in FIG. 4;
FIG. 6 is a waveform diagram of selection, emission, and boost signals that are supplied to the pixel circuit shown in FIG. 5;
FIG. 7 is a block diagram showing a configuration of a first scan driver of a scan driving circuit according to an embodiment;
FIG. 8 is a circuit diagram of a stage in a first scan driver of the scan driving circuit according to a first embodiment;
FIG. 9 is an input/output waveform diagram of the stage shown in FIG. 8;
FIG. 10 is a block diagram showing a configuration of a first scan driver of a scan driving circuit according to an embodiment;
FIG. 11 is a circuit diagram of a stage in a first scan driver of the scan driving circuit according to another embodiment;
FIG. 12 is an input/output waveform diagram of the stage shown in FIG. 11;

FIG. 13 is a block diagram showing a configuration of a first scan driver of a scan driving circuits according to a first complementary example;

FIG. 14 is a circuit diagram of a stage in a first scan driver of the scan driving circuit according to the first complementary example;

FIG. 15 is an input/output waveform diagram of the stage shown in FIG. 14;

FIG. 16 is a block diagram showing a configuration of a first scan driver of a scan driving circuit according to a second complementary example;

FIG. 17 is a circuit diagram of a stage in a first scan driver of the scan driving circuit according to the second complementary example;

FIG. 18 is an input/output waveform diagram of the stage shown in FIG. 17.

DETAILED DESCRIPTION OF CERTAIN INVENTIVE ASPECTS

[0022] Hereinafter, certain inventive aspects will be described with reference to the accompanying drawings. Here, when a first element is connected to a second element, the first element may be directly connected to the second element or may be indirectly connected to the second element via a third element. Further, irrelative elements are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0023] FIG. 4 is a block view showing an organic light emitting display according to one embodiment;

[0024] As shown in FIG. 4, the organic light emitting display according to one embodiment includes an organic light emitting display panel (referred to as 'display panel' hereinafter) 100, a data driving circuit 200, and a scan driving circuit. The scan driving circuit includes a first scan driver 310 and a second scan driver 320. The first scan driver 310 provides a selection signal and/or a boost signal. The second scan driver 320 provides an emission signal.

[0025] The first scan driver 310 may be configured to be divided into a scan drive unit and a boost drive unit for outputting the selection signal and the boost signal, respectively. In this case, the boost drive unit can be further divided into odd- and even-numbered boost signals.

[0026] The display panel 100 includes a plurality of data lines D1 through Dn, a plurality of signal lines S1 to Sn, E1 to En, B1 to Bm, and a plurality of pixel circuits 11. The plurality of data lines D1 through Dm are arranged in a column direction. The plurality of signal lines S1 to Sm and E1 to Em are arranged in a row direction. The plurality of pixel circuits 11 are arranged in an array.

[0027] Here, the signal lines S1 to Sn and E1 to En include a plurality of selection signal lines S1 to Sm for transferring a selection signal to select a pixel row, a plurality of emission signal lines E1 to En for transferring an emission signal to control an emission period of a pixel row, and a plurality of boost signal lines B 1 to Bn for transferring a boost signal to set a gate voltage of the drive thin film transistors in a pixel row.

[0028] Further, pixel circuits 11 are formed at a pixel region defined by the data lines D1 through Dm, the selection signal lines S1 to Sn, the emission signal lines E1 to En, and boost signal lines B1 to Bn.

[0029] The data driving circuit 200 applies a data current I_{DATA} to the data lines D1 through Dm. The first scan driver 310 of the scan driving circuit 300 sequentially applies a selecting signal for selecting a pixel circuit 11 to the selection signal lines S1 to Sn. Further, the first scan driver 310 sequentially applies a boost signal to the boost signal lines B1 to Bn to set a gate voltage of the drive thin film transistors of each pixel row.

[0030] Further, the second scan driver 320 of the scan driving circuit 300 applies an emission signal for controlling a luminance of the pixel circuit 11 to the emission signal lines E1 to En.

[0031] FIG. 5 is a circuit diagram showing an example of a pixel circuit arranged shown in FIG. 4. However, in order to help understanding of the pixel circuit, only a pixel circuit connected to a j-th data line Dj and i-th signal lines Si and Ei is shown in FIG. 5.

[0032] As shown in FIG. 5, the pixel circuit according to one embodiment includes an organic light emitting diode OLED, transistors m1 to m4, and first and second capacitors C1 and C2. Here, although PMOS transistors are used for each of the transistors m1 to m4, NMOS and CMOS implementations are also possible.

[0033] A first transistor m1 is coupled between a power supply VDD and an organic light emitting diode OLED, and controls an electric current through the organic light emitting diode OLED. In detail, a source of the first transistor m1 is coupled with the power supply VDD, and a drain thereof is coupled with a cathode of the organic light emitting diode OLED through a third transistor m3.

[0034] Furthermore, in response to a selection signal from the selection signal line Si, the second transistor m2 passes a voltage from the data line Dj to a gate of the first transistor m1. A fourth transistor m4 diode-connects the first transistor m1 in response to the selection signal.

[0035] Moreover, the first capacitor C1 is coupled between a gate and a source of the first transistor m1, and is charged with a voltage corresponding to the gate voltage of the first transistor m1 when sourcing the data current I_{DATA} to the data line Dj. A third transistor m3 passes an electric current flowing through the first transistor m1 to the organic light emitting diode OLED in response to an emission signal from the emission signal line Ei.

[0036] Further, the second capacitor C2 is coupled between the gate of the first transistor m1 and the boost signal line Bj.

[0037] Here, a voltage of the second capacitor C2 is increased by a voltage increase magnitude ΔV_B of a boost signal on the boost signal line Bj, and thus an increase magnitude ΔV_G of a gate voltage V_G of the first transistor m1 is generated. V_G may be approximated by the following equation 1.

$$\Delta V_G = \frac{\Delta V_B C_2}{C_1 + C_2} \qquad (1)$$

[0038] As indicated by equation 1, by increasing the voltage of the boost signal by ΔV_B; the gate voltage V_G is increased by ΔV_G according to the capacitances of the first and second capacitors. Parasitic capacitances of the transistors m1, m2, and m4, and the interconnects will also affect ΔV_G. The parasitic capacitances decrease ΔV_G by an amount related to the amount of parasitic capacitance relative to the sum of the first and second capacitors. Accordingly, the current I_{OLED} supplied to an organic light emitting diode OLED can be set at the desired value.

[0039] FIG. 6 is a timing diagram of selection, emission, and boost signals that are supplied to the pixel circuit shown in FIG. 5.

[0040] Referring to FIG. 5 and FIG. 6, while the first, second, and fourth transistors m1, m2, and m4 are turned-on and the data current I_{DATA} is being sourced by the first transistor m1, the third transistor m3 is turned-off. While in this state, the first transistor is effectively diode connected by the second and fourth transistors m2 and m4. Accordingly, the gate voltage of the first transistor m1, goes to a value corresponding to the data current I_{DATA}, and is stored in the capacitor C1.

[0041] As shown in FIG. 6, by generating a pulse end of an emission signal of an emission signal line Ei so as to be generated after a pulse end of selection signal line Si, the third transistor m3 is not turned on while the second transistor m2 is on.

[0042] That is, in the embodiment of FIGs. 5 and 6, the selection signal is applied in such a manner that a pulse of a low level of the selection signal ends before horizontal period by approximately 2 μs. Also shown in FIG. 6, the emission signal is applied in such a way that the pulse width of a high level of the emission signal spans the pulse width of the low level of the selection signal.

[0043] Moreover, when the pulse end of a boost signal from the boost signal line Bi is generated after the pulse end of the selection signal, when a node voltage of the second capacitor C2 is increased, programming of the data current I_{DATA} is complete, and thus the effect of increasing a node voltage of the second capacitor C2 is removed. Therefore, in this embodiment, as shown in FIG. 6, by controlling a pulse end of a selection signal transferred to the selection signal line Sn to be generated before the pulse end of a boost signal transferred to the boost signal line Bn, a node voltage of the second capacitor C2 is increased after a programming of the data current I_{DATA}.

[0044] Furthermore, by controlling a pulse start of the boost signal so as to be generated before a pulse start of the selection signal, while a voltage is programming in the first capacitor C1, a voltage of the first capacitor C1 varies due to a drop of a node voltage of the second capacitor C2. As noted previously, when the voltage of the first capacitor C1 changes, a voltage programming operation of the first capacitor C1 should be again performed, and thus a time of programming a voltage in the first capacitor C1 is needed. Accordingly, as shown in FIG. 6, by controlling a start of the selection signal transferred to the selection signal line Sn to be generated after a start of the boost signal transferred to the boost signal line Bn, a programming operation of the data current I_{DATA} is performed after a node voltage of the second capacitor C2 drops.

[0045] Due to a difference between a load connected to the boost signal line Bn and a load connected to the emission signal line En, a pulse end of the emission signal is generated prior to a pulse end of the boost signal, during a time period between the pulse end of the emission signal and the pulse end of the boost signal, an electric current before an increase in a node voltage of the second capacitor C2 flows through an organic light emitting diode OLED, thereby occurring stress in the organic light emitting diode OLED. When such an operation repeats, the lifetime of the organic light emitting diode OLED may be shortened. Consequently, as shown in FIG. 6, by generating a pulse end of the boost signal transferred to the boost signal line Bn before a pulse end of the emission signal transferred to the emission signal line En, an electric current flows through the organic light emitting diode OLED after a node voltage of the second capacitor C2 has been increased.

[0046] Furthermore, if a pulse start of the emission signal is generated after a pulse start of the boost signal, during a time period between the pulse start of the emission signal and the pulse start of the boost signal, an electric current due to a drop in a node voltage of the second capacitor C2 flows through an organic light emitting diode OLED, thereby resulting in stress in the organic light emitting diode OLED. When such an operation repeats, the lifetime of the organic light emitting diode OLED may be shortened. Consequently, as shown in FIG. 6, by generating the pulse start of the emission signal ahead of the pulse start of the boost signal, a node voltage of the second capacitor C2 drops after the

third transistor m3 has been turned-off.

[0047] That is, in this embodiment, the boost signal is applied in such a manner that a pulse width of a low level of the boost signal spans a pulse width of a low level of the selection signal and is less than that of a high level of the emission signal.

[0048] As seen from FIG. 4, the selection signal, the boost signal, and the emission signal are output through a first scan driver 310 and a second scan driver 320, which are provided to a panel.

[0049] A construction and an operation of a scan driving circuit of one embodiment for outputting selection and boost signals having waveforms as shown in FIG. 6 will now be given.

[0050] That is, only the first scan driver of the scan driving circuit will be described. Since a description of the second scan driver can be easily obtained from the description of the first scan driver, no further detailed description will be provided.

[0051] FIG. 7 is a block diagram showing a configuration of a first scan driver of a scan driving circuit according to one embodiment.

[0052] Here, the first scan driver 310 according to one embodiment is divided into a scan drive unit 312 and boost drive units 314 and 316, so that the scan drive unit 312 and the boost drive units 314 and 316 output a selection signal and a boost signal, respectively. Further, the boost drive unit includes a first boost drive unit 314 and a second boost drive unit 316 for separately outputting odd- and even-numbered boost signals.

[0053] The scan drive unit 312, the first and second boost drive units 314 and 316 include n stages that are dependently coupled with input signal IN1, IN2, IN3 lines thereof, respectively.

[0054] First output lines of the first n stages of the scan drive unit 312 are coupled with first n row lines S1 to Sn included in the pixel array, and provide a selection signal to respective pixels defining the pixel array. Second output lines of the second n stages of the boost drive units 314 and 316 are coupled with second n row lines B1 to Bn included in the pixel array, and provide a boost signal to respective pixels defining the pixel array.

[0055] Here, a first input signal IN1 is supplied to a first stage included in the scan drive unit 312, a first input signal IN2 is supplied to a first stage included in the first boost drive unit 314, and a first input signal IN3 is supplied to a first stage included in the second boost drive unit 316. Output signals of first to (n-1) th stages are supplied to respective next stages as input signals.

[0056] Further, each stage of the scan drive unit 312 includes a first clock terminal CLKa and a second clock terminal CLKb. First and second phase inverted clock signals CLK1 and CLK2 in which parts of high levels overlap with each other, are supplied to the first clock terminal CLKa and the second clock terminal CLKb, respectively. A first clock signal CLK1 is supplied to the first clock terminal CLKa of odd-numbered stages in the first scan driver 310, and a second clock signal CLK2 is supplied to the second clock terminal CLKb. In contrast to this, the second clock signal CLK2 is supplied to a first clock terminal CLKa of even-numbered stages, and the first clock signal CLK1 is supplied to a second clock terminal CLKb of the even-numbered stages.

[0057] That is, when each stage receives the first input signal IN1 or an output voltage of a previous stage, and the first and second clock signals CLK1 and CLK2, it sequentially outputs a low-level signal through an output lines thereof at time intervals as the first and second clock signals overlap with each other at high level.

[0058] In the same manner as above, respective stages of the first boost drive unit 314 and the second boost drive unit 316 include first and second clock terminals CLKa and CLKb. Third and fourth clock signals CLK3 and CLK4 whose phases are inverted and in which parts of high level overlap with each other, and fifth and sixth clock signals CLK5 and CLK6, are provided to the first and second clock terminals CLKa and CLKb.

[0059] Here, as shown, a third clock signal CLK3 or a fifth clock signal CLK5 is supplied to the first clock terminal CLKa of odd-numbered stages, and a fourth clock signal CLK4 or a sixth clock signal CLK6 is supplied to the second clock terminal CLKb thereof.

[0060] In contrast to this, the fourth clock signal CLK4 or the sixth clock signal CLK6 is supplied to a first clock terminal CLKa of even-numbered stages, and the third clock signal CLK3 or the fifth clock signal CLK5 is supplied to a second clock terminal CLKb of the even-numbered stages.

[0061] That is, when each stage receives the first input signal IN2 or IN3, or an output voltage of a previous stage, and the third and fourth clock signals CLK3 and CLK4, or the fifth and sixth clock signals CLK4 and CLK6, it sequentially outputs a low-level signal to respective odd- and even-numbered boost signal lines through an output line thereof at time intervals in which the third and fourth clock signals CLK3 and CLK4, or the fifth and sixth clock signals CLK4 and CLK6 overlap with each other at high level.

[0062] As seen from FIG. 6, the boost signal is output in such a manner that a pulse width of a low level of the boost signal spans a pulse width of a low level of the selection signal and is less than that of a high level of the emission signal. Further, the selection having a pulse width of a low level less than that of a horizontal period is output.

[0063] Namely, in this embodiment, in order to set a pulse width of the boost signal greater than that of the horizontal period, the boost drive unit is configured to be divided into an odd-numbered output unit 314 and an even-numbered output unit 316.

[0064] FIG. 8 is a circuit diagram of an embodiment of a stage in the scan driving circuit shown in FIG. 7, which shows a detailed circuit arrangement of odd-numbered stages of the scan drive unit, first and second boost drive units. FIG. 9 is an input/output waveform diagram of the stage shown in FIG. 8.

[0065] With reference to FIG. 8 and FIG. 9, each odd-numbered stage of the scan drive unit, first and second boost drive units is precharged to first and second input clock signals CLK1 and CLK2, CLK3 and CLK4, or CLK5 and CLK6 during the first time period having phases inverted to each other. The odd-numbered stage performs an evaluation operation during a second period having a phase inverted to a phase of the first period to sequentially output a low-level pulse at overlapped time intervals of the clock signal at a high level.

[0066] Namely, the odd-numbered stage outputs a high-level signal during a precharge period, and outputs a signal corresponding to an input received during the precharge period during an evaluation period.

[0067] Moreover, the evaluation period of the odd-numbered stages is designated to coincide with the precharge period of even-numbered stages,

[0068] Hereinafter, operation of stages will be explained in detail by reference to a circuit arrangement of an odd-numbered stage shown in FIG. 8.

[0069] PMOS thin film transistors will be now described as an example of transistors included in the stages. However, other implementations are also possible, such as NMOS or CMOS embodiments.

[0070] Referring to FIG. 8, an odd-numbered stage 400 according to one embodiment includes a first PMOS transistor M1, a second PMOS transistor M2, a third PMOS transistor M3, a fourth PMOS transistor M4, and a fifth PMOS transistor M5. The first PMOS transistor M1 receives an output voltage of a previous stage or a first input signal N1 or N2. A gate terminal of the first PMOS transistor M1 is coupled with a first clock terminal. The second PMOS transistor M2 is coupled with a second clock terminal and an output line OUT, and a gate terminal thereof is coupled with an output terminal of the first PMOS transistor M1. The third PMOS transistor M3 is coupled between a second power supply VSS and a first node N1, a gate terminal thereof is coupled with the first clock terminal. The fourth PMOS transistor M4 is coupled between the first clock terminal and the first node, and a gate terminal thereof is coupled with an output terminal of the first PMOS transistor M1. The fifth PMOS transistor M5 is coupled between a first power supply VDD and the output line OUT, and a gate terminal thereof is coupled with the first node N1.

[0071] The scan driving circuit further includes a first capacitor C1 that is coupled between an output terminal of the first PMOS transistor M1 and the output line OUT.

[0072] As shown, when the stage is an odd-numbered stage of the scan drive unit, a first clock signal CLK1 is supplied to the first clock terminal, and a second clock signal CLK2 is supplied to the second clock terminal. On the contrary, when the stage is an even-numbered stage 322 of the scan drive unit, the second clock signal CLK2 is supplied to the first clock terminal, and the first clock signal CLK1 is supplied to the second clock terminal.

[0073] In contrast to this, as shown, when the stage is an odd-numbered stage of the first boost drive unit 314, a third clock signal CLK3 is supplied to the first clock terminal, and a fourth clock signal CLK4 is supplied to the second clock terminal. On the contrary, when the stage is an even-numbered stage of the first boost drive unit, the fourth clock signal CLK4 is supplied to the first clock terminal, and the third clock signal CLK3 is supplied to the second clock terminal.

[0074] Further, as shown, when the stage is an odd-numbered stage of the second boost drive unit 316, a fifth clock signal CLK5 is supplied to the first clock terminal, and a sixth clock signal CLK6 is supplied to the second clock terminal. On the contrary, when the stage is an even-numbered stage of the second boost drive unit 316, the sixth clock signal CLK6 is supplied to the first clock terminal, and the fifth clock signal CLK5 is supplied to the second clock terminal.

[0075] Furthermore, a negative supply voltage may be applied to the second power supply VSS, but the second power supply VSS may be grounded as shown in FIG. 8. In one embodiment, it is shown that the second power supply VSS is embodied to be grounded.

[0076] Each stage includes a transfer unit, an inversion unit, and a buffer unit. The transfer unit is composed of first PMOS transistor M1, second PMOS transistor M2, and first capacitor C1. The inversion unit is composed of first, third, and fourth PMOS transistors M1, M3, and M4. The buffer unit is composed of a fifth PMOS transistor M5.

[0077] Assuming that the stage is an odd-numbered stage 312 of the first scan driver, a time period when the first clock signal CLK1 has a low level but the second clock signal CLK2 has a high level becomes a precharge period. A time period when the first clock signal CLK1 has a high level but the second clock signal CLK2 has a low level becomes an evaluation period. The odd-numbered stage 312 of the first scan driver outputs a high-level signal during the precharge period, and outputs a signal corresponding to an input received during the precharge during the evaluation period.

[0078] In this embodiment, as shown, first and second clock signals, third and fourth clock signals, or fifth and sixth clock signals as input signals of each stage are each provided so as to overlap each other at a part of a high level.

[0079] Each stage outputs a pair of clock signals CLK1 and CLK2, CLK3 and CLK4, or CLK5 and CLK6 so as to have time intervals corresponding to an overlapped time of the first and second clock signals CLK1 and CLK2 at a high level. The reason to have predetermined time intervals between output signals of each stage is for guaranteeing a margin for a clock skew or delay.

[0080] An operation of the odd-numbered stage will be explained with reference to FIG. 8 and FIG. 9. First, during the

precharge period, namely, while the first clock signal CLK1 of a low level and a second clock signal CLK2 of a high level are inputting thereto, the first and third transistors M1 and M3 are turned-on, whereby an input signal IN1 is transferred to gate terminals of the second and fourth transistors M2 and M4.

[0081] Accordingly, since an output voltage of a previous stage or an input signal IN1 is stored in the first capacitor C1 as an input signal, and a first node N1 is charged with a second clock signal CLK2 or a low-level signal from the second power supply VSS, the fifth transistor M5 is turned-on, with the result that a first power supply VDD of a high level is output through an output terminal OUT.

[0082] That is, during the precharge period, an output of the buffer unit of the stage becomes a high level. Moreover, during the evaluation period, the first transistor M1 is turned-off, thereby blocking an input signal IN1 and the third and fourth transistors M3 and M4 are accordingly turned-off.

[0083] When a signal received during the precharge period, namely, an output voltage of a previous stage or an input signal IN1 is at a high level, the received signal maintains a level of a signal precharged during the precharge period, whereby the buffer unit outputs a high-level signal unchanged.

[0084] In contrast to this, when the signal received during the precharge period, namely, an output voltage of a previous stage or an input signal IN1 is at a low level, the second transistor M2 is turned-on according to the low-level signal stored in the first capacitor C1. Accordingly, in the transfer unit, as the second transistor M2 is turned-on, a second clock signal CLK2 of a low level is output through an output terminal OUT.

[0085] That is, during the evaluation period, when a signal received during the precharge period, namely, an output voltage of a previous stage or an input signal IN1 is at a low level, the stage outputs a low-level signal. When the received signal is at a high level, the stage outputs a high-level signal.

[0086] As noted previously, first and second clock signals as input signals of each stage are provided to overlap each other at a part of a high level as shown in FIG. 9.

[0087] In a case that the first and second clock signals CLK1 and CLK2 are at high level, when a previous period is a precharge period, first and third transistors M1 and M3 controlled by the first clock signal CLK1 are all turned-off, and a voltage of a capacitor C1 remains unchanged, thereby maintaining a previous output.

[0088] In contrast to this, when the previous period is an evaluation period, the first and third transistors M1 and M3 are turned-off, a second transistor M2 maintains a previous state. When the second transistor M2 is turned-off, the stage receives a high-level signal, with the result that a high-level output is remained by a fifth transistor M5.

[0089] On the contrary, when the evaluation transistor M3 is turned-on, since the stage receives a low-level signal, namely, a gate terminal of the second transistor M2 is in a floating state, a voltage of the capacitor C1 remains unchanged, and thus the second transistor M2 continues to be turned-on that causes a second clock signal of high level to be output as an output signal.

[0090] As is seen from the foregoing description, in a case that the first and second clock signals CLK1 and CLK2 are at high level, when a previous period is a precharge period, an output maintains a previous state. When the previous period is an evaluation period, an output has a high level. Consequently, a time interval may be reduced between output pulses of adjacent stages by an overlapped time in high levels of the first and second clock signals CLK1 and CLK2.

[0091] Although, described above were results on the odd-numbered state of the first scan driver, the same results were obtained on an odd-numbered stage of the first boost drive unit or the second boost drive unit

[0092] Accordingly, when the first boost drive unit 314 and the second boost drive unit 316 of FIG. 7 receive third and fourth clock signals CLK3 and CLK4, and an input signal IN2; and fifth and sixth clock signals CLK5 and CLK6, and an input signal IN3, respective, they sequentially output a low-level pulse at overlapped time intervals of a pair of clock signals CLK3 and CLK4 or CLK5 and CLK6 at a high level.

[0093] As shown in FIG. 9, third and fourth clock signals CLK3 and CLK4, or fifth and sixth clock signals CLK5 and CLK6 are input to have longer overlapped time, precharge period, and evaluation period as compared with first and second clock signals CLK1 and CLK2. Further, input signals IN1 and IN3 respectively input to the first and second boost drive units have low level of greater width in comparison with that of an input signal IN1 input to the scan drive unit.

[0094] In addition, the fifth and sixth clock signals CLK5 and CLK 6, and an input signal IN2 are input to a stage of the second boost drive unit 316 to be delayed by approximately one horizontal period in comparison with the third and fourth clock signals CLK3 and CLK4 and the input signal IN3 input to a stage of the first boost drive unit 314.

[0095] As seen from FIG. 6, this operation is performed to cause the boost signal to be greatly applied in such a way that a pulse width of a high level of the boost signal contains the pulse width of a low level of a corresponding selection signal.

[0096] That is, in one embodiment, in order to make the output boost signal to have a pulse width greater than that of a corresponding selection signal, the boost drive unit is configured to be divided into an odd-numbered output unit and an even-numbered output unit. Time periods of clock signals CLK3, CLK4, CLK5, and CLK6 applied to respective boost drive units and low-level widths of the input signals IN1 and IN2 are adjusted.

[0097] FIG. 10 is a block diagram showing a configuration of a first scan driver of a scan driving circuit according to another embodiment.

[0098] However, a description of the same construction and operation of the second embodiment as those of the first embodiment shown in FIG. 7 is omitted.

[0099] In the same manner as in the first embodiment shown in FIG. 7, a first scan drive of the first embodiment is configured to be divided into a scan drive unit and a boost drive unit for outputting a selection signal and a boost signal, respectively. In particular, the boost drive unit is composed of a first boost drive unit and a second boost drive unit for separating outputting an odd-numbered boost signal and an even-numbered boost signal.

[0100] However, besides clock signals CLK3, CLK4, CLK5, and CLK6, and input signals IN2 and IN3, control signals D1, D2, D3, and D4 are applied to the first and second boost drive units to adjust a swing of an output pulse.

[0101] The first and third control signals D1 and D3 are input to odd-numbered stages of the first and second boost drive units, whereas the second and fourth control signals D2 and D4 are input to even-numbered stage of the first and second boost drive units.

[0102] FIG. 11 is a circuit diagram of an embodiment of a stage in a first scan driver of the scan driving circuit, which shows a detailed circuit arrangement of odd-numbered stages of the scan drive unit, first and second boost drive units shown in FIG. 10. FIG. 12 is an input/output waveform diagram of the stage shown in FIG. 11.

[0103] A portion of a stage 400 of a scan drive unit shown in FIG. 11, and the timing chart of signals input thereto are identical with those of the first embodiment shown in FIG. 9, and thus a description thereof is omitted.

[0104] However, in a case of the first and second boost drive units, a sixth PMOS thin film transistor M6 and a seventh PMOS thin film transistor M7 are further provided in the construction of the first embodiment shown in FIG. 8. Further, the control signals B1, B2, B3, and B4 are input to an input terminal of a sixth transistor M6 in order to adjust a swing of an output boost signal.

[0105] Here, first and second control signals D1 and D2 are respectively input to odd- and even-numbered stages of the first boost drive unit, whereas third and fourth control signals D3 and D4 are respectively input to odd- and even-numbered stages of the second boost drive unit.

[0106] In a detailed description, as shown in FIG. 11, an odd-numbered stage 500 of a boost drive unit includes first to fifth transistors M1 to M5, a sixth PMOS transistor M6, and a seventh PMOS transistor M7. The sixth PMOS transistor M6 is coupled to a control signal D1 or D3 input line and a boost signal output line BST, and a gate terminal thereof is coupled to an output terminal of the first transistor M1. The seventh PMOS transistor M7 is coupled between a first power supply VDD and the boost signal output line BST.

[0107] As noted previously, the sixth and seventh PMOS transistors M6 and M7 are further included. As a control signal is applied through the sixth PMOS transistor M6, a difference between high and low levels in a boost signal output from each stage, namely, a swing of an output pulse is controlled by the control signal.

[0108] That is, similar to the first embodiment, the same signal is output through an output terminal of a stage to be input to a next stage. However, a corresponding boost signal is output through a boost signal output line BST of each stage depending on a swing level of the control signal.

[0109] As shown in FIG. 12, the first and second control signals D1 and D2 are applied to the first boost drive unit with a less difference of high and low levels as compared with that of the third and fourth clock signals CLK3 and CLK4 applied to the first boost drive unit. That is, the first and second control signals have a swing less than that of the third and fourth corresponding clock signals CLK3 and CLK4.

[0110] Similar to that described above, the boost signal is output through a stage of a boost drive unit shown in FIG. 11 as a pulse width greater than that of a corresponding selection signal, and as a pulse having a small difference of high and low levels by the control signal.

[0111] That is, this embodiment has an advantage in that it may adjust a pulse swing of an output boost signal.

[0112] FIG. 13 is a block diagram showing a configuration of a first scan driver of a scan driving circuit according to a first complementary example.

[0113] In the embodiments discussed above, the first scan driver is divided into a scan drive unit, and first and second boost drive units. In other embodiments the scan drive unit is configured to be divided into odd- and even-numbered scan drive units, and the odd- and even-numbered scan drive units are connected to the first and second boost drive units.

[0114] In other words, as shown in FIG. 13, the first scan driver 310 includes a first scan/boost drive unit 318 and a second scan/boost drive unit 319. The first scan/boost drive unit 318 outputs odd-numbered selection signal and boost signal. The second scan/boost drive unit 319 outputs even-numbered selection signal and boost signal.

[0115] In addition to clock signals CLK7, CLK8, CLK9, CLK10, input signals IN4, IN5, and control signals D1, D2, D3, D4 for adjusting a swing of an output pulse, which have similar function to corresponding signals discussed above, selection control signals A1, A2, A3, and A4 for sequentially outputting odd- and even-numbered selection signals are further applied to the first scan/boost drive unit 318 and the second scan/boost drive unit 319.

[0116] First and third selection control signals A1 and A3 are input to odd-numbered stage of the first and second scan/boost drive units 318 and 319, respectively. Second and fourth selection control signals A2 and A4 are input to even-numbered stage of the first and second scan/boost drive units 318 and 319, respectively.

[0117] FIG. 14 is a circuitry diagram of a stage in a first scan driver of the scan driving circuit, which shows a detailed

circuit arrangement of odd-numbered stages of first and second scan/boost drive units 318 and 319 shown in FIG. 13. Further, FIG. 15 is an input/output waveform diagram of the stage shown in FIG. 14.

[0118] As shown in FIG. 14 and FIG. 15, a scan/boost drive unit is configured by adding an eighth PMOS transistor M8 and a ninth PMOS transistor M9 to an arrangement of the second embodiment shown in FIG. 11. In order to sequentially output odd- and even-numbered selection signals, selection control signals A1, A2, A3, and A4 are input to an input terminal of the eighth PMOS transistor M8.

[0119] Herein, first and second selection control signals A1 and A2 are input to odd- and even-numbered stages of the first scan/boost drive unit, respectively. Further, third and fourth selection control signals A3 and A4 are input to odd- and even-numbered stages of the second scan/boost drive unit, respectively.

[0120] As shown in FIG. 14, an odd-numbered stage 600 of a scan/boost drive unit further includes first to seventh transistors M1 to M7, a first capacitor C1, an eighth PMOS transistor M8, and a ninth PMOS transistor M9. The eighth PMOS transistor M8 is coupled to a selection control signal A1 or A3 input line and a selection signal output line SEL, and a gate terminal thereof is coupled to an output terminal of the first transistor M1. The ninth PMOS transistor M9 is coupled between a first power supply VDD and the selection signal output line SEL, and a gate terminal thereof is coupled to the first node.

[0121] As noted previously, the eighth and ninth PMOS transistors M8 and M9 are further included. As a selection control signal is applied through the eighth PMOS transistor M8, as shown in FIG. 15, selection signals output from odd- and even-numbered stages may be output.

[0122] That is, this example has advantages in that it may adjust a pulse width and a swing of a boost signal, and may reduce the number of drive units.

[0123] FIG. 16 is a block diagram showing a configuration of a first scan driver of a scan driving circuit according to a second complementary example.

[0124] In this embodiment, it is unnecessary to input control signals D1, D2, D3, and D4 in each stage.

[0125] FIG. 17 is a circuit diagram of a stage in a first scan driver of the scan driving circuit, which shows a detailed circuit arrangement of an odd-numbered stage of the first and second scan/boost drive units. FIG. 18 is an input/output waveform diagram of the stage shown in FIG. 17.

[0126] As shown in FIG. 17 and FIG. 18, scan/boost drive unit 600 has the same construction as that shown in FIG. 14.

[0127] The difference is that a third power supply VL in place of control signals D1, D2, D3, and D4 is applied to an input terminal of a sixth PMOS transistor M6. The third power supply VL supplies a negative voltage corresponding to a low level value of the control signal. In this case, as shown in FIG. 18, the second complementary example can still obtain an output waveform similar to that of the first complementary example.

[0128] As apparent from the above description, in accordance with a scan driving circuit with a first scan driver for providing a selection signal and/or a boost signal, and a second scan driver for providing an emission signal, by freely adjusting a pulse width and a swing of the boost signal, an electric current I_{OLED} supplied to an organic light emitting diode can be set at a desired value.

[0129] Furthermore, a flow path of a static current is removed from the scan driving circuit that allows power consumption to be reduced.

[0130] In addition, when the scan driving circuit outputs a high-level signal, an output terminal is not charged, thereby minimizing a leakage current. When the scan driving circuit outputs a low-level signal, a reduction of an electric current charging the output terminal is minimized to increase an operation speed.

[0131] Although a few embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes might be made in this embodiment without departing from the scope of the claims.

Claims

1. A scan driving circuit for a display device comprising n pixel rows, n boost signal lines and n emission control signal lines, wherein n is an integer greater than 1, the scan driving circuit comprising a first scan driver (310) and a second scan driver (320):

   wherein the first scan driver (310) comprises:

   a scan drive unit (312) comprising n stages and configured to receive first and second clock signals having a phase shift with respect to each other and sequentially output selection signals (S1-Sn) to selection lines of the pixel rows of the display device; and
   a boost drive unit comprising n stages configured to sequentially output boost signals (B1-Bn) to respective boost signal lines of the display device;
   wherein the boost drive unit comprises:

a first boost drive unit (314) comprising n/2 stages configured to receive third and fourth clock signals having a phase shift with respect to each other and sequentially output boost signals to the odd-numbered boost signal lines; and
a second boost drive unit (316) comprising n/2 stages configured to receive fifth and sixth clock signals having a phase shift with respect to each other and sequentially output boost signals to the even-numbered boost signal lines;

wherein the second scan driver (320) comprises n stages configured to sequentially output emission signals to emission lines of respective pixel rows,
wherein each stage of the first scan driver (312), the first boost drive unit (314) and the second boost drive unit (316) comprises first and second clock input terminals, each for receiving one of the clock signals, an input terminal for receiving either an input signal or an output signal of a previous stage and an output terminal to output a signal to a corresponding line,
characterised in that each stage further comprises:

a first transistor (m1) with an input terminal configured to receive an output voltage of a previous stage or a first input voltage from the input terminal of the stage and a gate terminal configured to receive the clock signal from the first clock input terminal;
a second transistor (m2) configured to receive the clock signal from the second clock input terminal as input and to provide a signal to the output terminal, and comprising a gate terminal configured to receive a signal from the output terminal of the first transistor;
a third transistor (m3) configured to receive a signal from a second power supply and to provide a signal to a first node, and comprising a gate terminal configured to receive the clock signal from the first clock input terminal;
a fourth transistor (m4) configured to receive the clock signal from the first clock input terminal and to provide an output signal to the first node, and comprising a gate terminal configured to receive a signal from the output terminal of the first transistor (m1); and
a fifth transistor (m5) configured to receive a signal from a first power supply and to provide a signal to the output line, and comprising a gate terminal configured to receive a signal from the first node.

2. A scan driving circuit according to claim 1,
wherein when the stage is an odd numbered stage of the scan drive unit, the first clock signal is supplied to the first clock terminal, and the second clock signal is supplied to the second clock terminal and when the stage is an even numbered stage of the scan drive unit, the second clock signal is supplied to the first clock terminal, and the first clock signal is supplied to the second clock terminal;
when the stage is an odd numbered stage of the first boost drive unit, the third clock signal is supplied to the first clock terminal, and the fourth clock signal is supplied to the second clock terminal, and when the stage is an even numbered stage of the first boost drive unit, the fourth clock signal is supplied to the first clock terminal, and the third clock signal is supplied to the second clock terminal; and
when the stage is an odd numbered stage of the second boost drive unit, the fifth clock signal is supplied to the first clock terminal, and the sixth clock signal is supplied to the second clock terminal, and when the stage is an even numbered stage of the second boost drive unit, the sixth clock signal is supplied to the first clock terminal, and the fifth clock signal is supplied to the second clock terminal.

3. A scan driving circuit according to claim 1 or 2, further comprising a first capacitor (c1) coupled between the output terminal of the first transistor (m1) and the output line.

4. A scan driving circuit according to any one of the preceding claims, wherein each stage of the first and second boost drive units (314, 316) further comprises:

a sixth transistor (m6) configured to receive a signal from a control signal input line (D1, D3) and to provide a signal to a boost signal output line, comprising a gate terminal configured to receive a signal from an output terminal of the first transistor (m1); and
a seventh transistor (m7) configured to receive a signal from the first power supply and to provide a signal to the boost signal output line, comprising a gate terminal configured to receive a signal from the first node.

5. A scan driving circuit according to claim 4, further comprising first and third control signal lines configured to supply first and third control signals to odd-numbered stages of the first and second boost drive units (314, 316), and second

and fourth control signal lines configured to supply second and fourth control signals to even-numbered stages of the first and second boost drive units (314, 316).

6. An organic light emitting display comprising:

a pixel portion comprising a plurality of pixels coupled to selection signal lines, data lines, emission signal lines, and boost signal lines;
a data driving circuit configured to provide a data signal to the data lines; and
a scan driving circuit according to any one of the preceding Claims.

Patentansprüche

1. Zeilenansteuerungsschaltung für eine Anzeigevorrichtung, die n Bildpunktzeilen, n Boostsignalleitungen und n Emissionssteuerungssignalleitungen umfasst, wobei n eine ganze Zahl größer als 1 ist, wobei die Zeilenansteuerungsschaltung einen ersten Zeilentreiber (310) und einen zweiten Zeilentreiber (320) umfasst;
worin der erste Zeilentreiber (310) umfasst:

eine Zeilenansteuerungseinheit (312), die n Stufen umfasst und dafür konfiguriert ist, ein erstes und ein zweites Taktsignal mit einer Phasenverschiebung in Bezug aufeinander zu empfangen und der Reihe nach Auswahlsignale (S1-Sn) an Auswahlleitungen der Bildpunktzeilen der Anzeigevorrichtung auszugeben; und
eine Boostansteuerungseinheit, die n Stufen umfasst, die dafür konfiguriert sind, Boostsignale (B1-Bn) an entsprechende Boostsignalleitungen der Anzeigevorrichtung auszugeben;
worin die Boostansteuerungseinheit umfasst:

eine erste Boostansteuerungseinheit (314), die n/2 Stufen umfasst, die dafür konfiguriert sind, ein drittes und ein viertes Taktsignal mit einer Phasenverschiebung in Bezug aufeinander zu empfangen und der Reihe nach Boostsignale an die ungeradzahligen Boostsignalleitungen auszugeben; und
eine zweite Boostansteuerungseinheit (316), die n/2 Stufen umfasst, die dafür konfiguriert sind, ein fünftes und ein sechstes Taktsignal mit einer Phasenverschiebung in Bezug aufeinander zu empfangen und der Reihe nach Boostsignale an die geradzahligen Boostsignalleitungen auszugeben;

worin der zweite Zeilentreiber (320) n Stufen umfasst, die dafür konfiguriert sind, der Reihe nach Emissionssignale an Emissionsleitungen entsprechender Bildpunktzeilen auszugeben,
worin jede Stufe des ersten Zeilentreibers (312), der ersten Boostansteuerungseinheit (314) und der zweiten Boostansteuerungseinheit (316) umfasst: einen ersten und einen zweiten Takteingangsanschluss, jeder zum Empfangen eines der Taktsignale, einen Eingangsanschluss zum Empfangen entweder eines Eingangssignals oder eines Ausgangssignals einer vorherigen Stufe und einen Ausgangsanschluss, um ein Signal an eine entsprechende Leitung auszugeben,
dadurch gekennzeichnet, dass jede Stufe ferner umfasst:

einen ersten Transistor (m1) mit einem Eingangsanschluss, der dafür konfiguriert ist, eine Ausgangsspannung einer vorherigen Stufe oder eine erste Eingangsspannung vom Eingangsanschluss der Stufe zu empfangen, und einem Gateanschluss, der dafür konfiguriert ist, das Taktsignal vom ersten Takteingangsanschluss zu empfangen;
einen zweiten Transistor (m2), der dafür konfiguriert ist, das Taktsignal vom zweiten Takteingangsanschluss als Eingang zu empfangen und ein Signal an den Ausgangsanschluss zu übergeben, und einen Gateanschluss umfasst, der dafür konfiguriert ist, ein Signal vom Ausgangsanschluss des ersten Transistors zu empfangen;
einen dritten Transistor (m3), der dafür konfiguriert ist, ein Signal von einer zweiten Stromversorgung zu empfangen und ein Signal an einen ersten Knoten zu übergeben, und einen Gateanschluss umfasst, der dafür konfiguriert ist, das Taktsignal vom ersten Takteingangsanschluss zu empfangen;
einen vierten Transistor (m4), der dafür konfiguriert ist, das Taktsignal vom ersten Takteingangsanschluss zu empfangen und ein Ausgangssignal an den ersten Knoten zu übergeben, und einen Gateanschluss umfasst, der dafür konfiguriert ist, ein Signal vom Ausgangsanschluss des ersten Transistors (m1) zu empfangen; und
einen fünften Transistor (m5), der dafür konfiguriert ist, ein Signal von einer ersten Stromversorgung zu empfangen und ein Signal an die Ausgangsleitung zu übergeben, und einen Gateanschluss umfasst, der

dafür konfiguriert ist, ein Signal vom ersten Knoten zu empfangen.

2. Zeilenansteuerungsschaltung nach Anspruch 1,
worin, wenn die Stufe eine ungeradzahlige Stufe der Zeilenansteuerungseinheit ist, das erste Taktsignal an den ersten Taktanschluss angelegt wird und das zweite Taktsignal an den zweiten Taktanschluss angelegt wird, und, wenn die Stufe eine geradzahlige Stufe der Zeilenansteuerungseinheit ist, das zweite Taktsignal an den ersten Taktanschluss angelegt wird und das erste Taktsignal an den zweiten Taktanschluss angelegt wird;
worin, wenn die Stufe eine ungeradzahlige Stufe der ersten Boostansteuerungseinheit ist, das dritte Taktsignal an den ersten Taktanschluss angelegt wird und das vierte Taktsignal an den zweiten Taktanschluss angelegt wird, und, wenn die Stufe eine geradzahlige Stufe der ersten Boostansteuerungseinheit ist, das vierte Taktsignal an den ersten Taktanschluss angelegt wird und das dritte Taktsignal an den zweiten Taktanschluss angelegt wird; und
worin, wenn die Stufe eine ungeradzahlige Stufe der zweiten Boostansteuerungseinheit ist, das fünfte Taktsignal an den ersten Taktanschluss angelegt wird und das sechste Taktsignal an den zweiten Taktanschluss angelegt wird, und, wenn die Stufe eine geradzahlige Stufe der zweiten Boostansteuerungseinheit ist, das sechste Taktsignal an den ersten Taktanschluss angelegt wird und das fünfte Taktsignal an den zweiten Taktanschluss angelegt wird.

3. Zeilenansteuerungsschaltung nach Anspruch 1 oder 2, ferner einen ersten Kondensator (c1) umfassend, der zwischen den Ausgangsanschluss des ersten Transistors (m1) und die Ausgangsleitung gekoppelt ist.

4. Zeilenansteuerungsschaltung nach einem der vorhergehenden Ansprüche, worin jede Stufe der ersten und der zweiten Boostansteuerungseinheit (314, 316) ferner umfasst:

einen sechsten Transistor (m6), der dafür konfiguriert ist, ein Signal von einer Steuersignaleingangsleitung (D1, D3) zu empfangen und ein Signal an eine Boostsignalausgangsleitung zu übergeben, und einen Gateanschluss umfasst, der dafür konfiguriert ist, ein Signal von einem Ausgangsanschluss des ersten Transistors (m1) zu empfangen; und
einen siebenten Transistor (m7), der dafür konfiguriert ist, ein Signal von der ersten Stromversorgung zu empfangen und ein Signal an die Boostsignalausgangsleitung zu übergeben, und einen Gateanschluss umfasst, der dafür konfiguriert ist, ein Signal vom ersten Knoten zu empfangen.

5. Zeilenansteuerungsschaltung nach Anspruch 4, ferner umfassend: eine erste und eine dritte Steuersignalleitung, die dafür konfiguriert sind, ein erstes und ein drittes Steuersignal an ungeradzahlige Stufen der ersten und der zweiten Boostansteuerungseinheit (314, 316) anzulegen, und eine zweite und eine vierte Steuersignalleitung, die dafür konfiguriert sind, ein zweites und ein viertes Steuersignal an geradzahlige Stufen der ersten und der zweiten Boostansteuerungseinheit (314, 316) anzulegen.

6. Organische Leuchtanzeige, umfassend:

einen Bildpunktabschnitt, der eine Vielzahl von Bildpunkten umfasst, die mit Auswahlsignalleitungen, Datenleitungen, Emissionssignalleitungen und Boostsignalleitungen gekoppelt sind;
eine Datenansteuerungsschaltung, die dafür konfiguriert ist, ein Datensignal an die Datenleitungen zu übergeben; und
eine Zeilenansteuerungsschaltung nach einem der vorhergehenden Ansprüche.

Revendications

1. Circuit de commande de balayage pour un dispositif d'affichage comprenant n rangées de pixel, n lignes de signal d'amplification et n lignes de signal de commande d'émission, dans lequel n est un nombre entier supérieur à 1, le circuit de commande de balayage comprenant un premier dispositif de commande de balayage (310) et un second dispositif de commande de balayage (320) :

dans lequel le premier dispositif de commande de balayage (310) comprend :

une unité de commande de balayage (312) comprenant n étages et configurée pour recevoir des premier et deuxième signaux d'horloge présentant un décalage de phase l'un par rapport à l'autre et produire de manière séquentielle des signaux de sélection (S1 à Sn) vers des lignes de sélection des rangées de pixel du dispositif d'affichage ; et

une unité de commande d'amplification comprenant n étages configurée pour produire de manière séquentielle des signaux d'amplification (B1 à Bn) vers des lignes de signal d'amplification respectives du dispositif d'affichage ;

dans lequel l'unité de commande d'amplification comprend :

une première unité de commande d'amplification (314) comprenant n/2 étages configurés pour recevoir des troisième et quatrième signaux d'horloge présentant un décalage de phase l'un par rapport à l'autre et produire de manière séquentielle des signaux d'amplification vers les lignes de signal d'amplification impaires ; et
une seconde unité de commande d'amplification (316) comprenant n/2 étages configurés pour recevoir des cinquième et sixième signaux d'horloge présentant un décalage de phase l'un par rapport à l'autre et produire de manière séquentielle des signaux d'amplification vers les lignes de signal d'amplification paires ;

dans lequel le second dispositif de commande de balayage (320) comprend n étages configurés pour produire de manière séquentielle des signaux d'émission vers des lignes d'émission de rangées de pixels respectives, dans lequel chaque étage du premier dispositif de commande de balayage (312), de la première unité de commande d'amplification (314) et de la seconde unité de commande d'amplification (316) comprend des première et seconde bornes d'entrée d'horloge, permettant respectivement de recevoir un des signaux d'horloge, une borne d'entrée permettant de recevoir un signal d'entrée ou un signal de sortie d'un étage précédent et une borne de sortie permettant de produire un signal vers une ligne correspondante,
caractérisé en ce que chaque étage comprend en outre :

un premier transistor (m1) avec une borne d'entrée configurée pour recevoir une tension de sortie d'un étage précédent ou une première tension d'entrée provenant de la borne d'entrée de l'étage et une borne de gâchette configurée pour recevoir le signal d'horloge provenant de la première borne d'entrée d'horloge ;
un deuxième transistor (m2) configuré pour recevoir le signal d'horloge provenant de la seconde borne d'entrée d'horloge en tant qu'entrée et pour fournir un signal vers la borne de sortie, et comprenant une borne de gâchette configurée pour recevoir un signal provenant de la borne de sortie du premier transistor ;
un troisième transistor (m3) configuré pour recevoir un signal provenant d'une seconde alimentation électrique et pour fournir un signal vers un premier noeud, et comprenant une borne de gâchette configurée pour recevoir le signal d'horloge provenant de la première borne d'entrée d'horloge ;
un quatrième transistor (m4) configuré pour recevoir le signal d'horloge provenant de la première borne d'entrée d'horloge et pour fournir un signal de sortie vers le premier noeud, et comprenant une borne de gâchette configurée pour recevoir un signal provenant de la borne de sortie du premier transistor (m1); et
un cinquième transistor (m5) configuré pour recevoir un signal provenant d'une première alimentation électrique et pour fournir un signal vers la ligne de sortie, et comprenant une borne de gâchette configurée pour recevoir un signal provenant du premier noeud.

2. Circuit de commande de balayage selon la revendication 1,
dans lequel, lorsque l'étage est un étage impair de l'unité de commande de balayage, le premier signal d'horloge est fourni vers la première borne d'horloge, et le deuxième signal d'horloge est fourni vers la seconde borne d'horloge et, lorsque l'étage est un étage pair de l'unité de commande de balayage, le deuxième signal d'horloge est fourni vers la première borne d'horloge, et le premier signal d'horloge est fourni vers la seconde borne d'horloge ;
lorsque l'étage est un étage impair de la première unité de commande d'amplification, le troisième signal d'horloge est fourni vers la première borne d'horloge, et le quatrième signal d'horloge est fourni vers la seconde borne d'horloge, et, lorsque l'étage est un étage pair de la première unité de commande d'amplification, le quatrième signal d'horloge est fourni vers la première borne d'horloge, et le troisième signal d'horloge est fourni vers la seconde borne d'horloge ; et
lorsque l'étage est un étage impair de la seconde unité de commande d'amplification, le cinquième signal d'horloge est fourni vers la première borne d'horloge, et le sixième signal d'horloge est fourni vers la seconde borne d'horloge, et, lorsque l'étage est un étage pair de la seconde unité de commande d'amplification, le sixième signal d'horloge est fourni vers la première borne d'horloge, et le cinquième signal d'horloge est fourni vers la seconde borne d'horloge.

3. Circuit de commande de balayage selon la revendication 1 ou 2, comprenant en outre un premier condensateur (c1) couplé entre la borne de sortie du premier transistor (m1) et la ligne de sortie.

4. Circuit de commande de balayage selon l'une quelconque des revendications précédentes, dans lequel chaque

étage des première et deuxième unités de commande d'amplification (314, 316) comprend en outre :

un sixième transistor (m6) configuré pour recevoir un signal provenant d'une ligne d'entrée de signal de commande (D1, D3) et pour fournir un signal vers une ligne de sortie de signal d'amplification, comprenant une borne de gâchette configurée pour recevoir un signal provenant d'une borne de sortie du premier transistor (m1); et
un septième transistor (m7) configuré pour recevoir un signal provenant de la première alimentation électrique et pour fournir un signal vers la ligne de sortie de signal d'amplification, comprenant une borne de gâchette configurée pour recevoir un signal provenant du premier noeud.

5. Circuit de commande de balayage selon la revendication 4, comprenant en outre des première et troisième lignes de signal de commande configurées pour fournir des premier et troisième signaux de commande vers des étages impairs des première et seconde unités de commande d'amplification (314, 316), et des deuxième et quatrième lignes de signal de commande configurées pour fournir des deuxième et quatrième signaux de commande vers des étages pairs des première et seconde unités de commande d'amplification (314, 316).

6. Affichage électroluminescent organique comprenant :

une partie pixel comprenant une pluralité de pixels couplés à des lignes de signal de sélection, des lignes de données, des lignes de signal d'émission, et des lignes de signal d'amplification ;
un circuit de commande de données configuré pour fournir un signal de données vers lesdites lignes de données ; et
un circuit de commande de balayage selon l'une quelconque des revendications précédentes.

FIG. 1
(PRIOR ART)

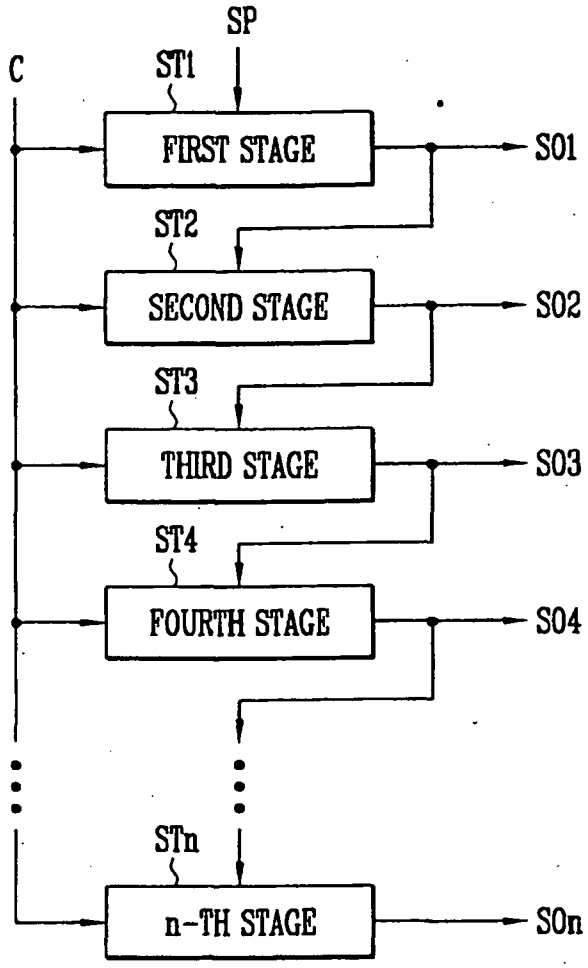


FIG. 2
(PRIOR ART)

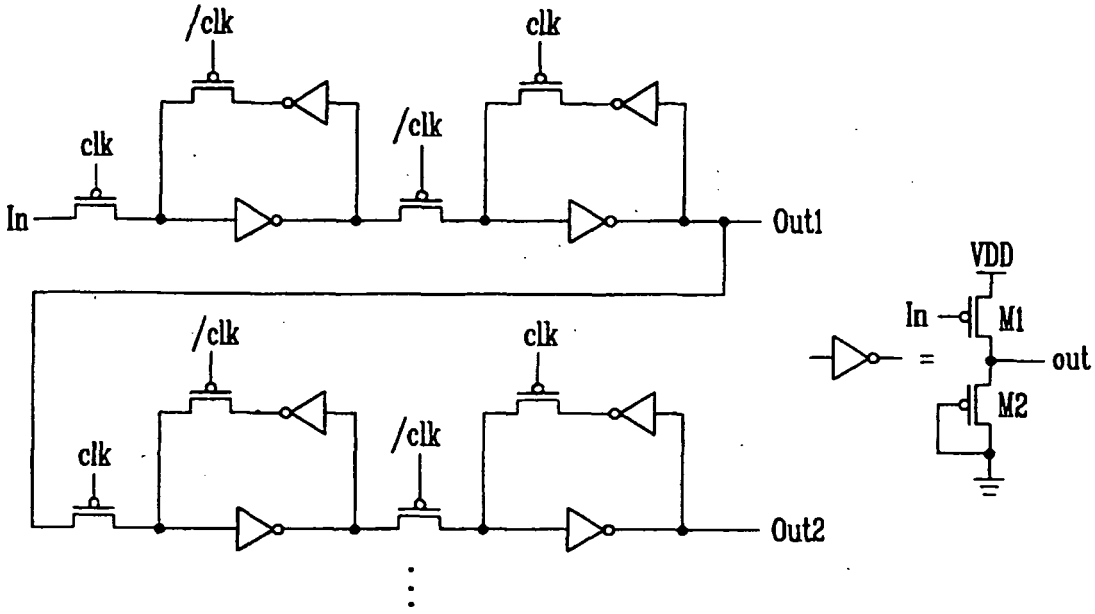


FIG. 3
(PRIOR ART)

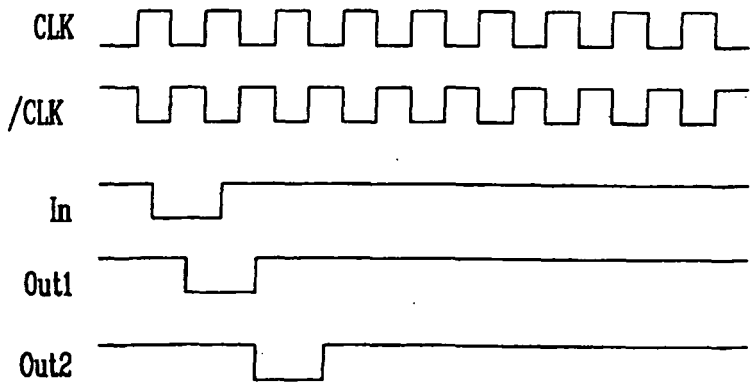


FIG. 4

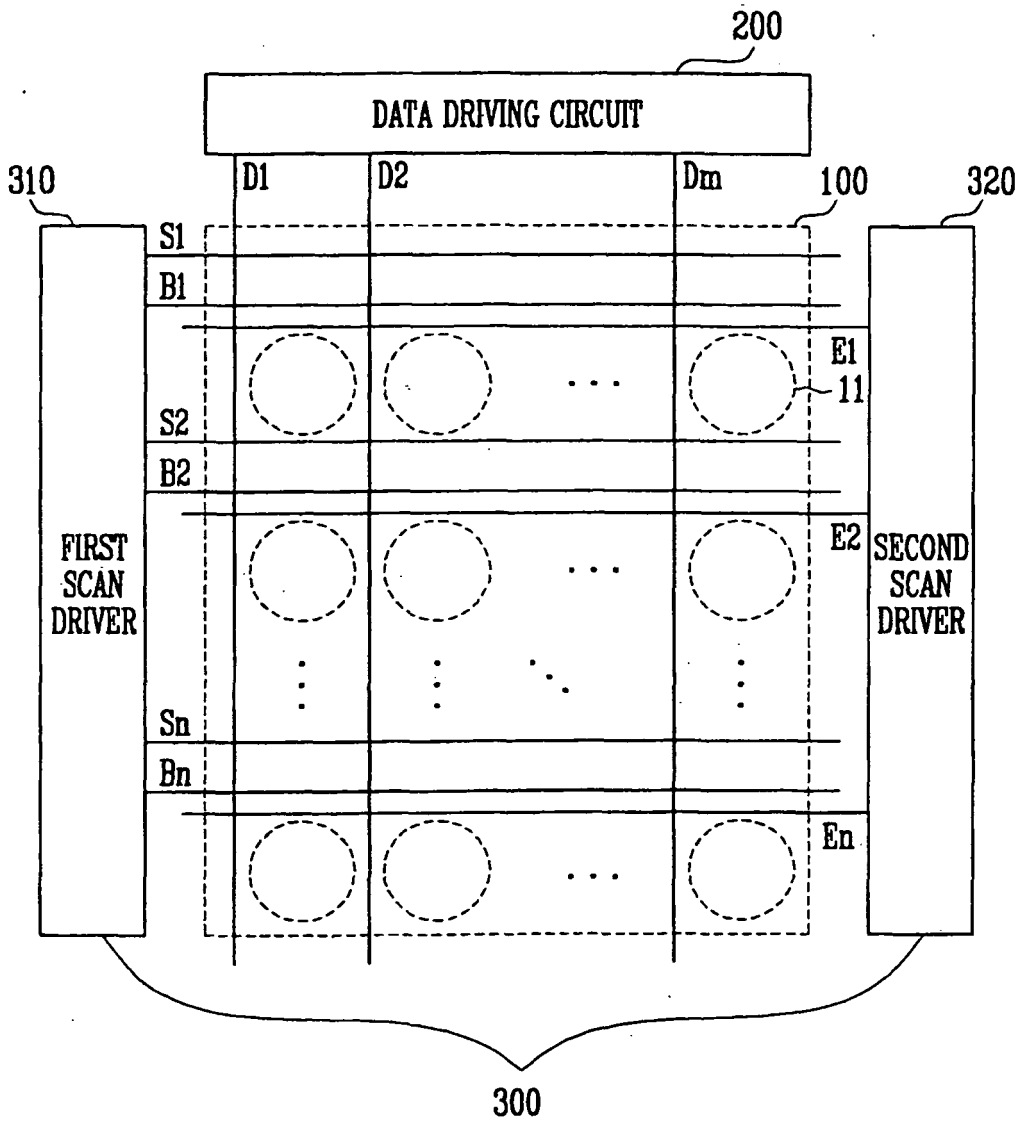

200
DATA DRIVING CIRCUIT
310
D1
D2
Dm
100
320
S1
B1
E1
11
S2
B2
E2
FIRST SCAN DRIVER
SECOND SCAN DRIVER
Sn
Bn
En
300

FIG. 5

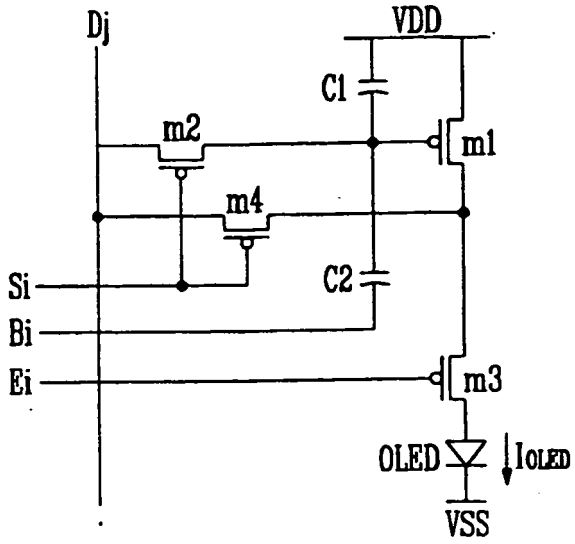

Dj
VDD
C1
m2
m1
m4
C2
Si
Bi
Ei
m3
OLED
IOLED
VSS

FIG. 6

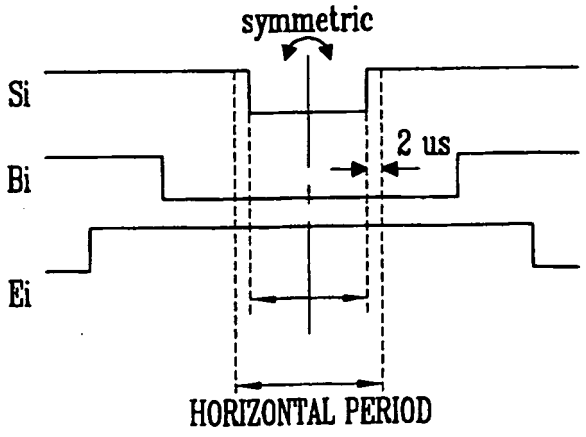

symmetric
Si
2 us
Bi
Ei
HORIZONTAL PERIOD

FIG. 7

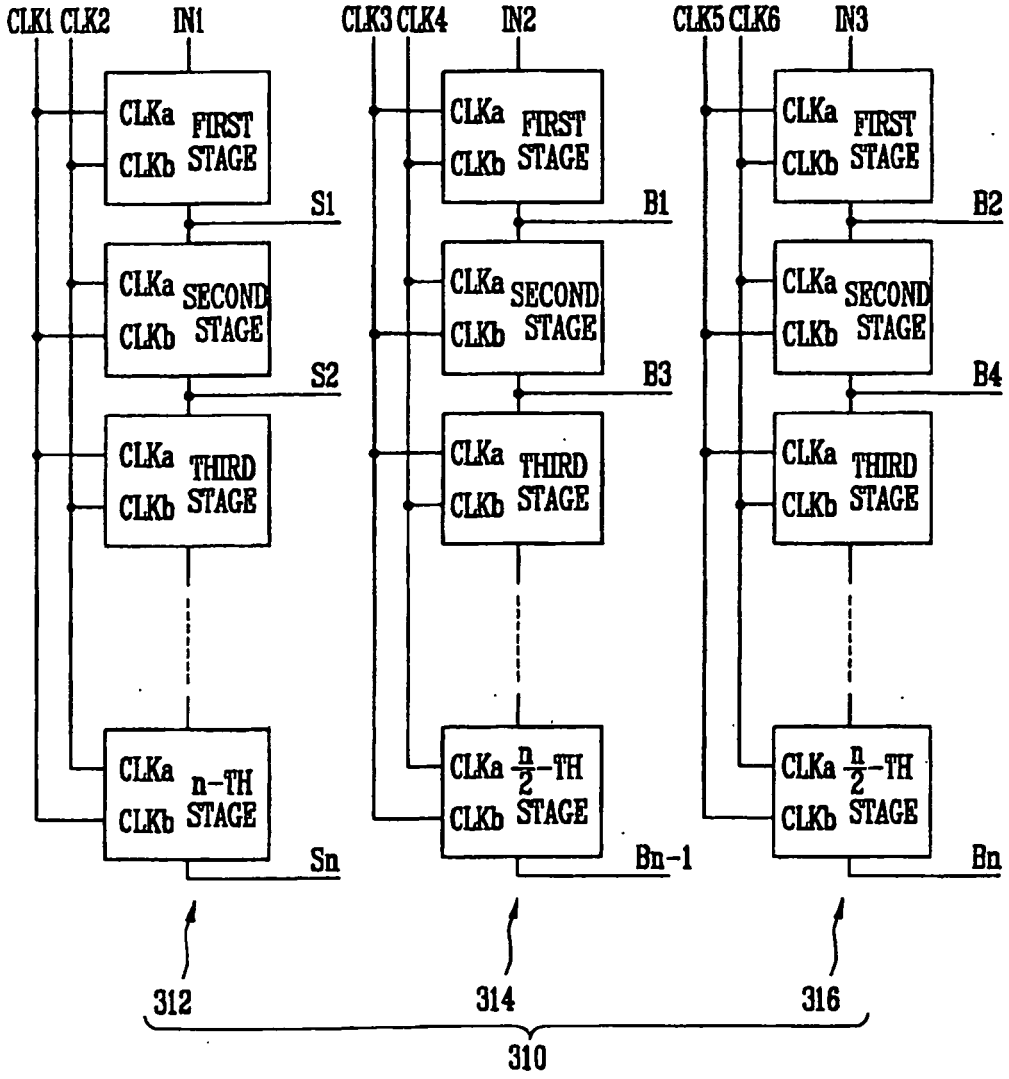

CLK1 CLK2
IN1
CLK3 CLK4
IN2
CLK5 CLK6
IN3
CLKa
CLKb
FIRST STAGE
SECOND STAGE
THIRD STAGE
n-TH STAGE
n/2-TH STAGE
S1
S2
Sn
B1
B2
B3
B4
Bn-1
Bn
312
314
316
310

FIG. 8

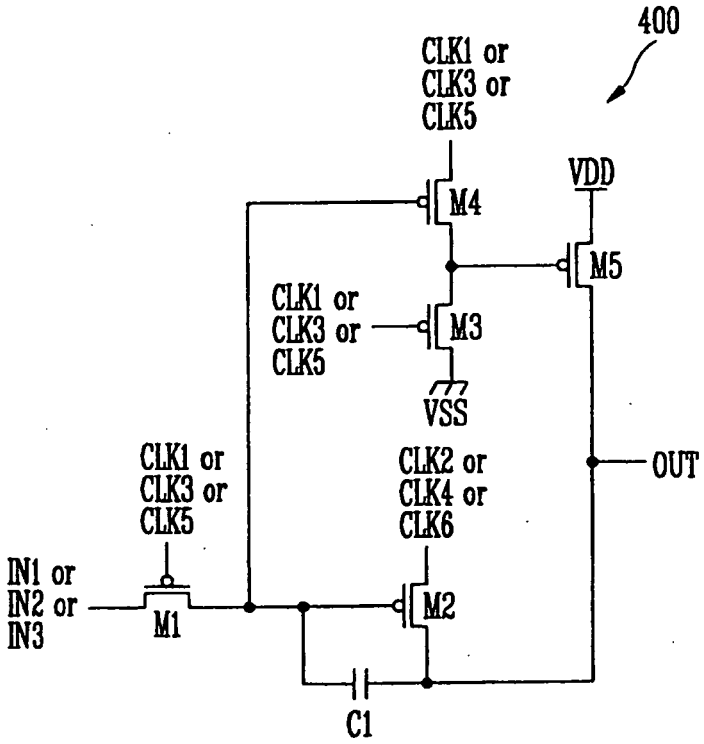

400
CLK1 or
CLK3 or
CLK5
VDD
M4
M5
CLK1 or
CLK3 or
CLK5
M3
VSS
CLK1 or
CLK3 or
CLK5
CLK2 or
CLK4 or
CLK6
OUT
IN1 or
IN2 or
IN3
M1
M2
C1

FIG. 9

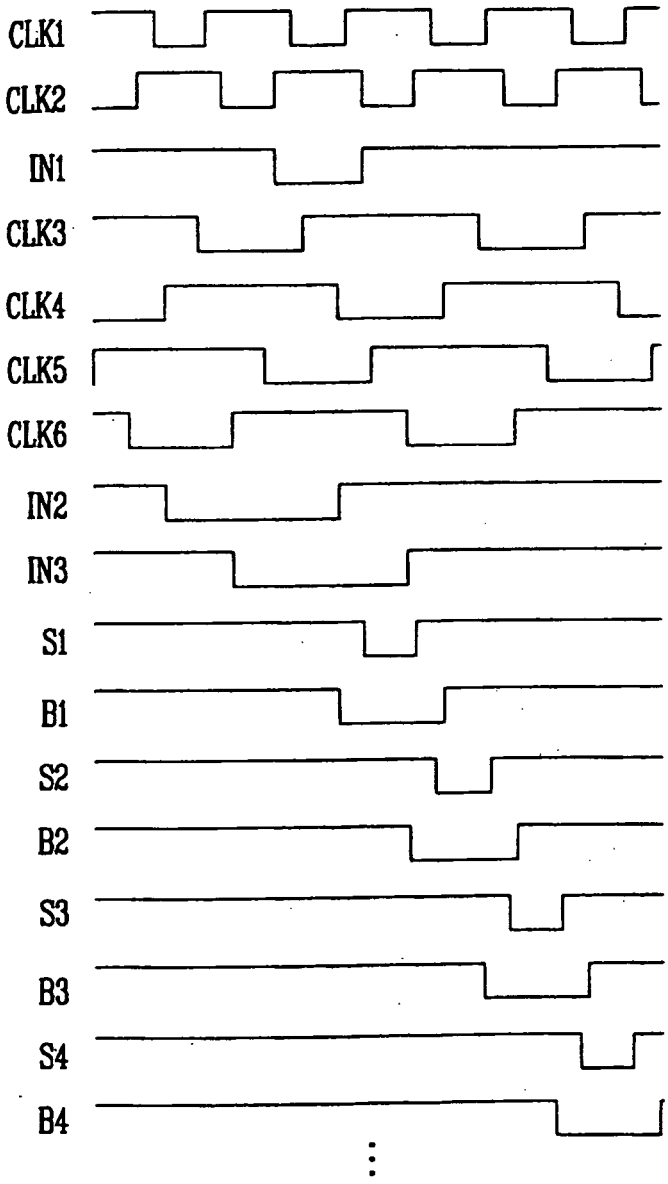


FIG. 10

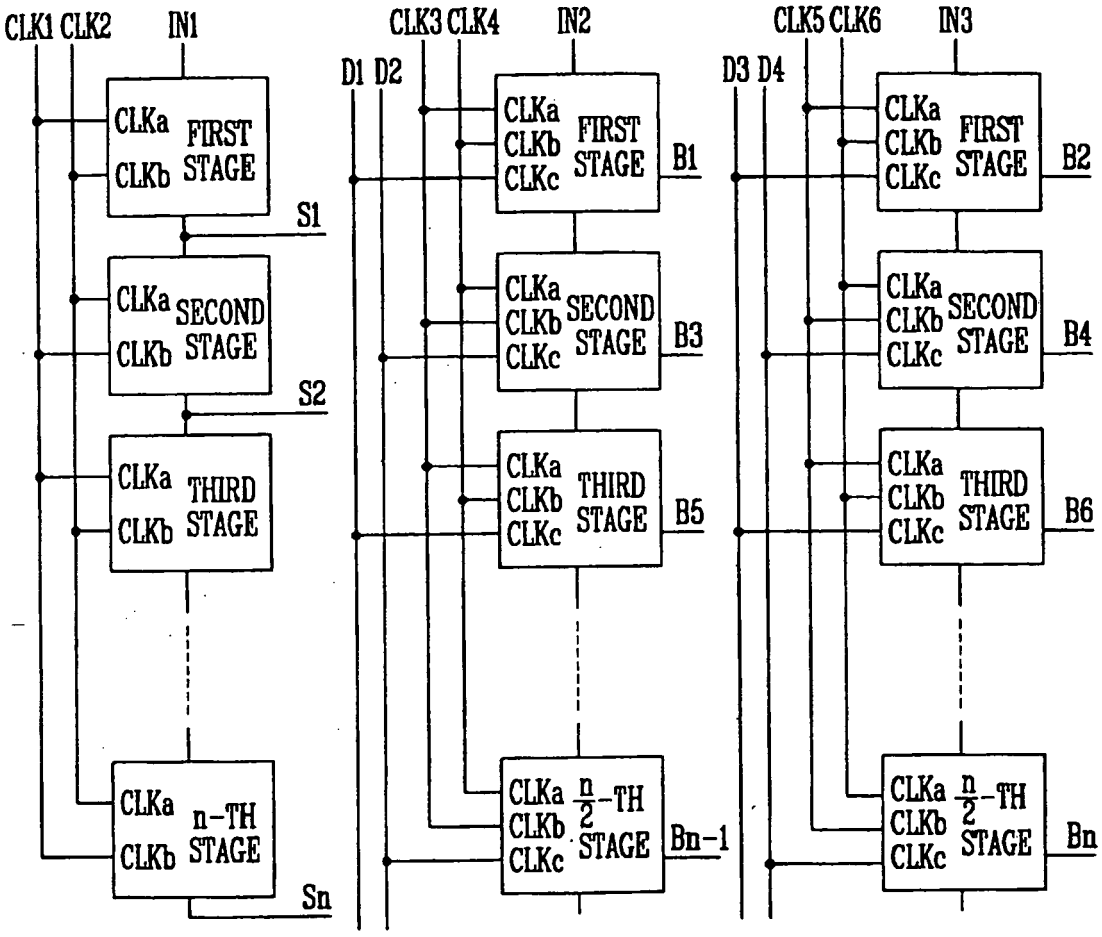

CLK1 CLK2
IN1
CLKa
CLKb
FIRST STAGE
S1
SECOND STAGE
S2
THIRD STAGE
n-TH STAGE
Sn
CLK3 CLK4
IN2
D1 D2
CLKc
B1
B3
B5
n/2-TH STAGE
Bn-1
CLK5 CLK6
IN3
D3 D4
B2
B4
B6
Bn

FIG. 11

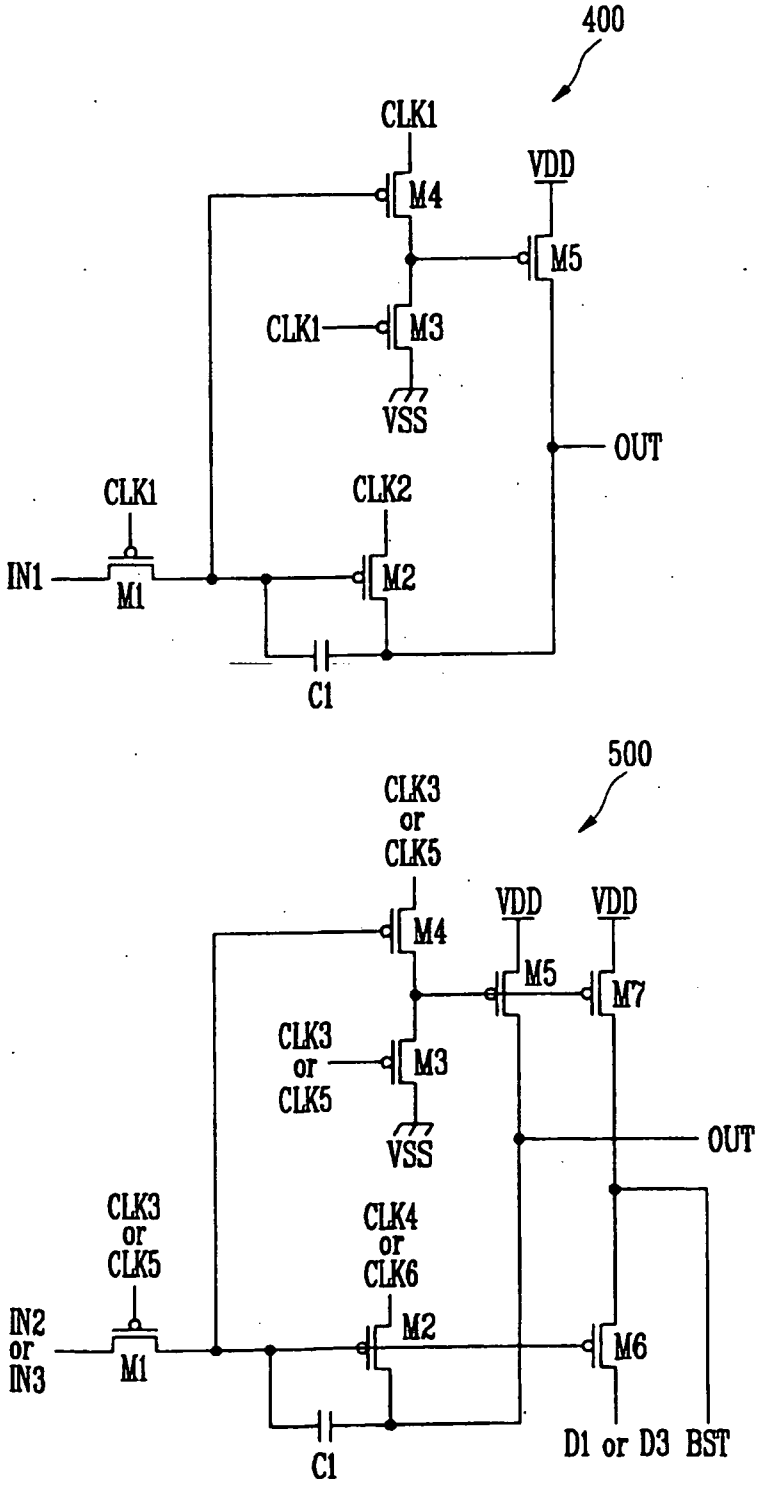

400
CLK1
VDD
M4
M5
CLK1
M3
VSS
OUT
CLK1
CLK2
IN1
M1
M2
C1
500
CLK3
or
CLK5
VDD
VDD
M4
M5
M7
CLK3
or
CLK5
M3
VSS
OUT
CLK3
or
CLK5
CLK4
or
CLK6
IN2
or
IN3
M1
M2
M6
C1
D1 or D3
BST

FIG. 12

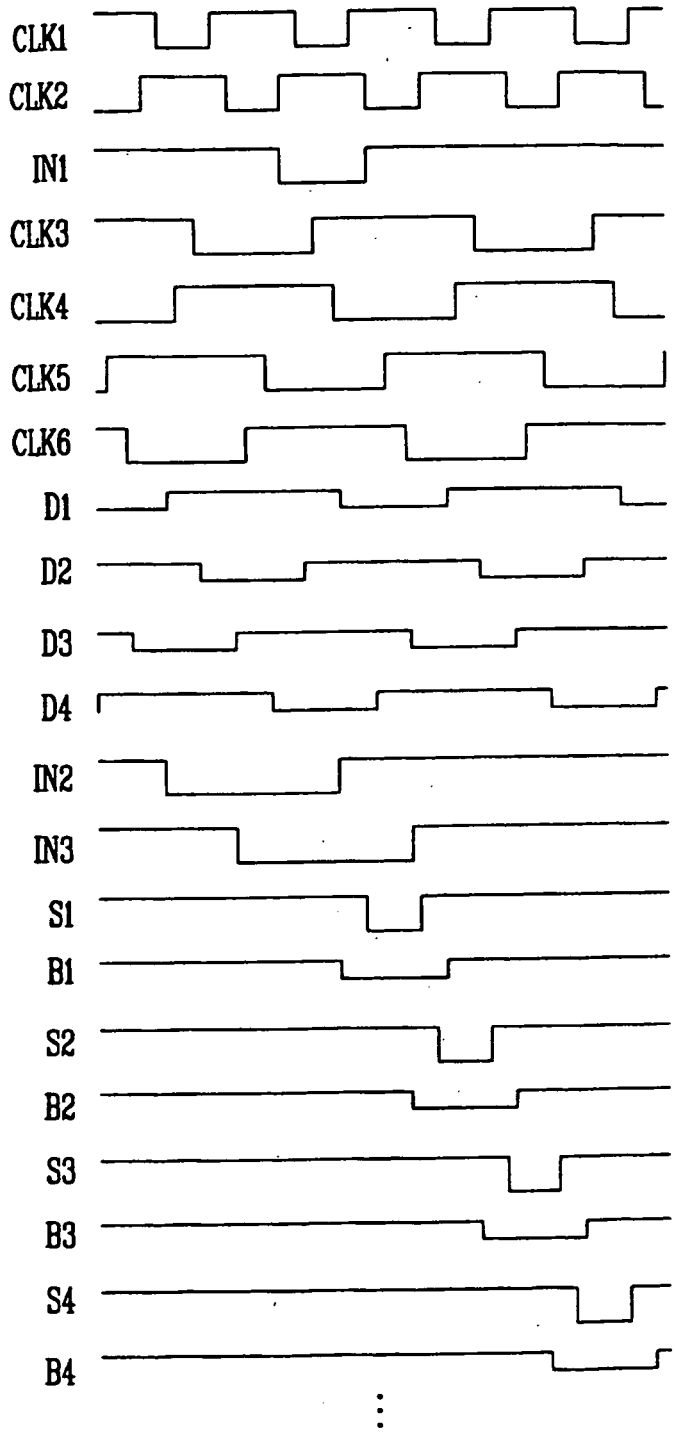

CLK1
CLK2
IN1
CLK3
CLK4
CLK5
CLK6
D1
D2
D3
D4
IN2
IN3
S1
B1
S2
B2
S3
B3
S4
B4

FIG. 13

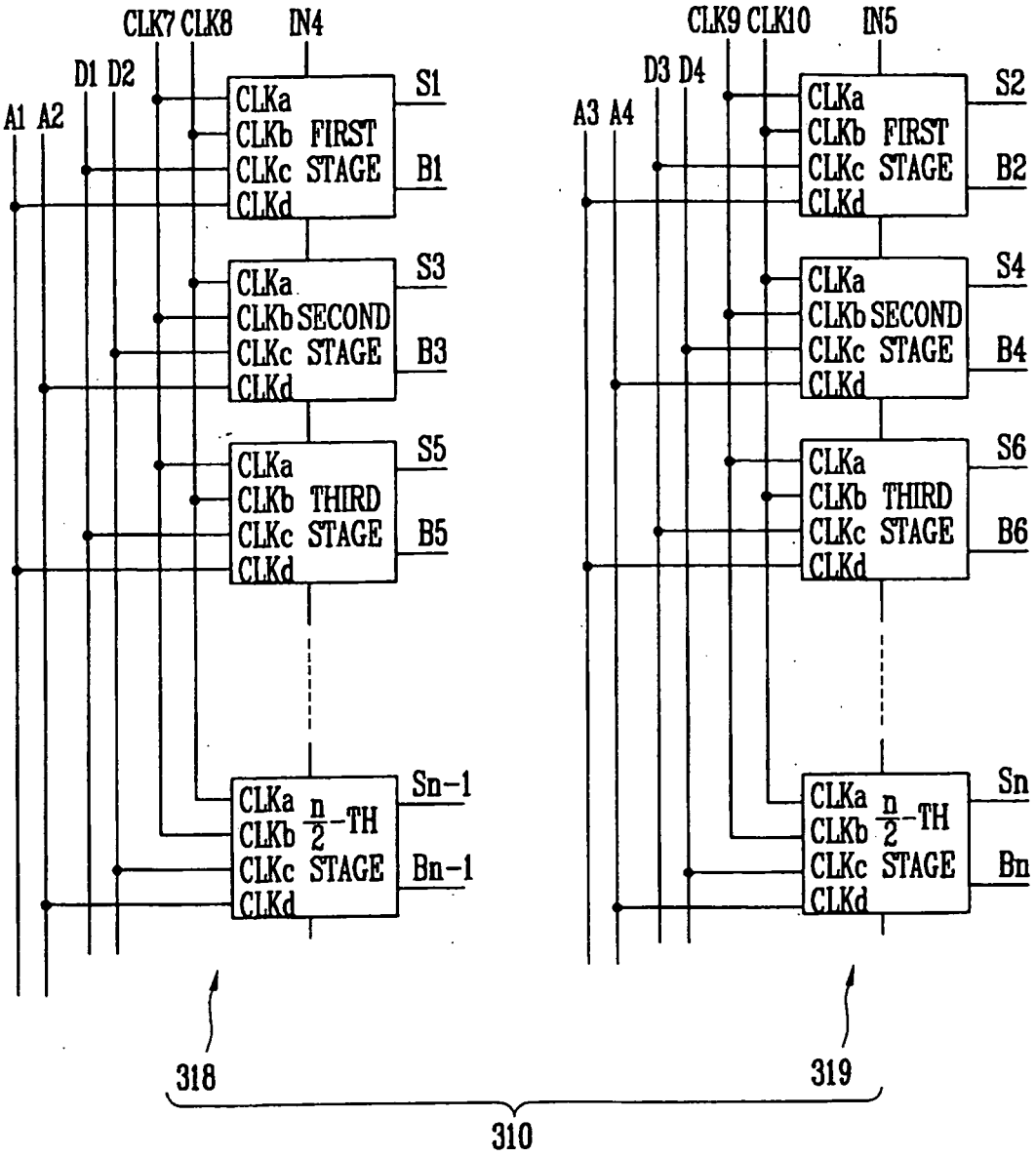

CLK7 CLK8
IN4
D1 D2
A1 A2
CLKa
CLKb FIRST
CLKc STAGE
CLKd
S1
B1
CLKa
CLKb SECOND
CLKc STAGE
CLKd
S3
B3
CLKa
CLKb THIRD
CLKc STAGE
CLKd
S5
B5
CLKa n/2-TH
CLKb
CLKc STAGE
CLKd
Sn-1
Bn-1
CLK9 CLK10
IN5
D3 D4
A3 A4
CLKa
CLKb FIRST
CLKc STAGE
CLKd
S2
B2
CLKa
CLKb SECOND
CLKc STAGE
CLKd
S4
B4
CLKa
CLKb THIRD
CLKc STAGE
CLKd
S6
B6
CLKa n/2-TH
CLKb
CLKc STAGE
CLKd
Sn
Bn
318
319
310

FIG. 14

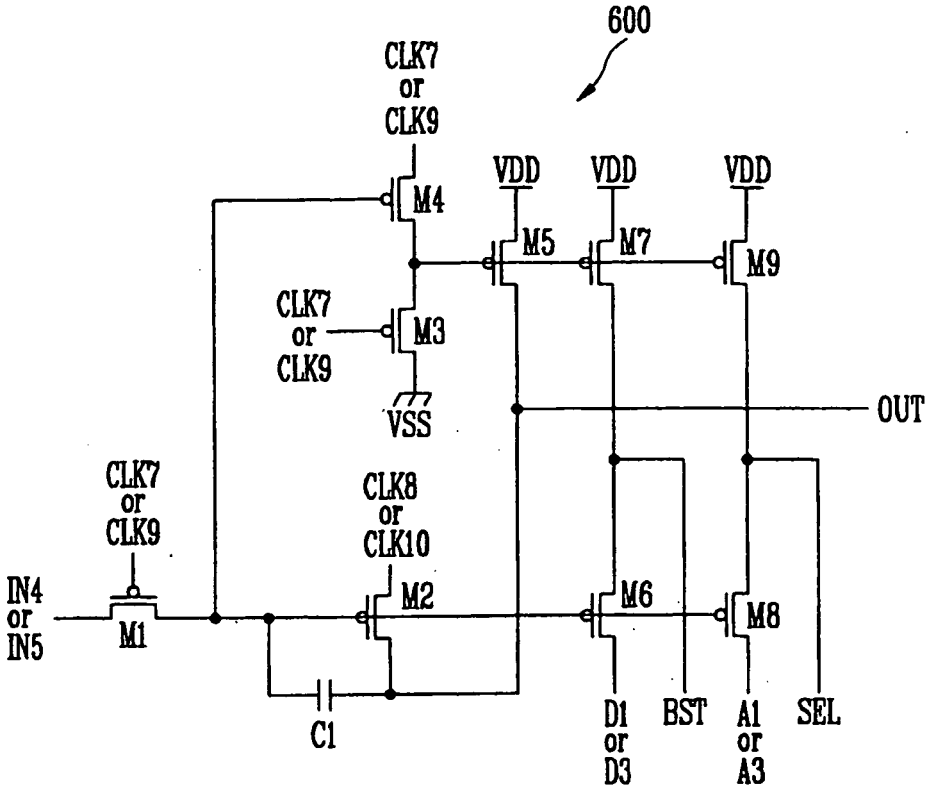

600
CLK7 or CLK9
VDD
VDD
VDD
M4
M5
M7
M9
CLK7 or CLK9
M3
VSS
OUT
CLK7 or CLK9
CLK8 or CLK10
IN4 or IN5
M1
M2
M6
M8
C1
D1 or D3
BST
A1 or A3
SEL

FIG. 15

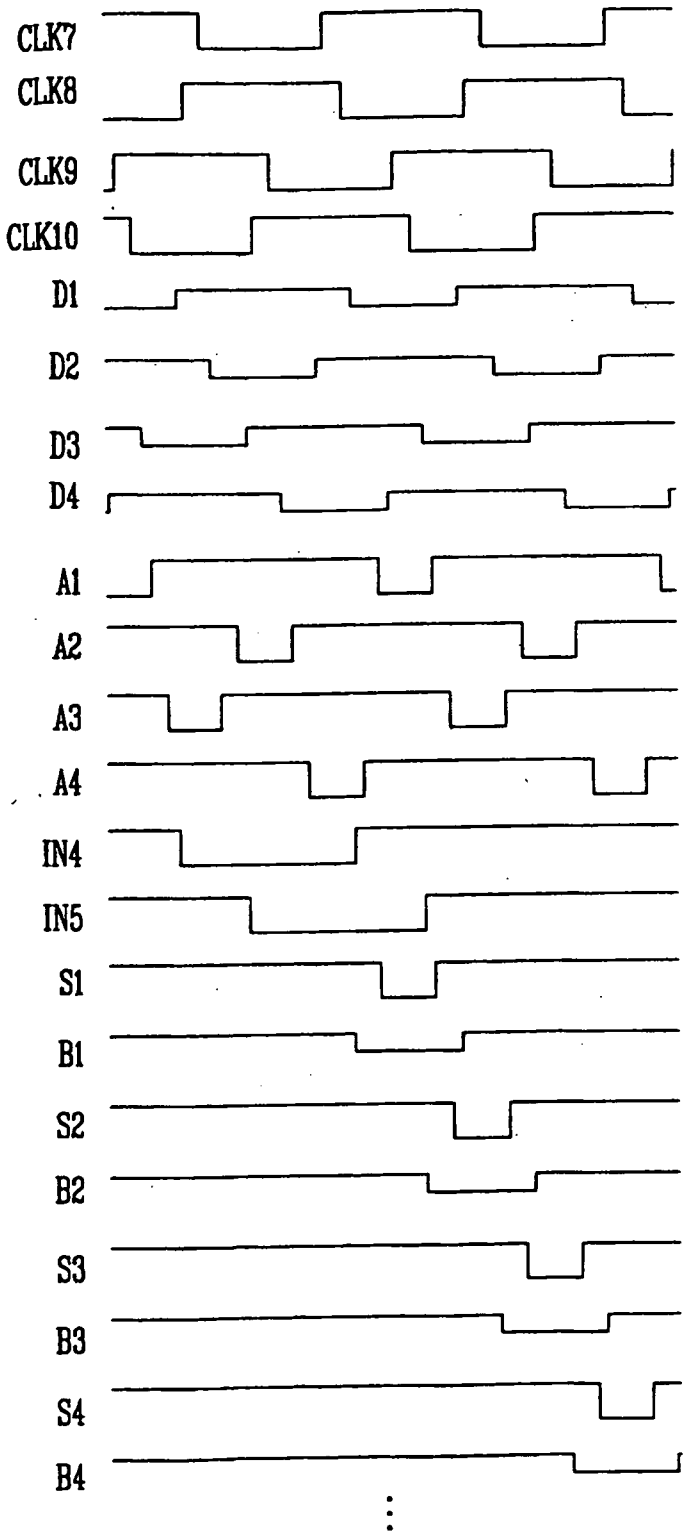

CLK7
CLK8
CLK9
CLK10
D1
D2
D3
D4
A1
A2
A3
A4
IN4
IN5
S1
B1
S2
B2
S3
B3
S4
B4

FIG. 16

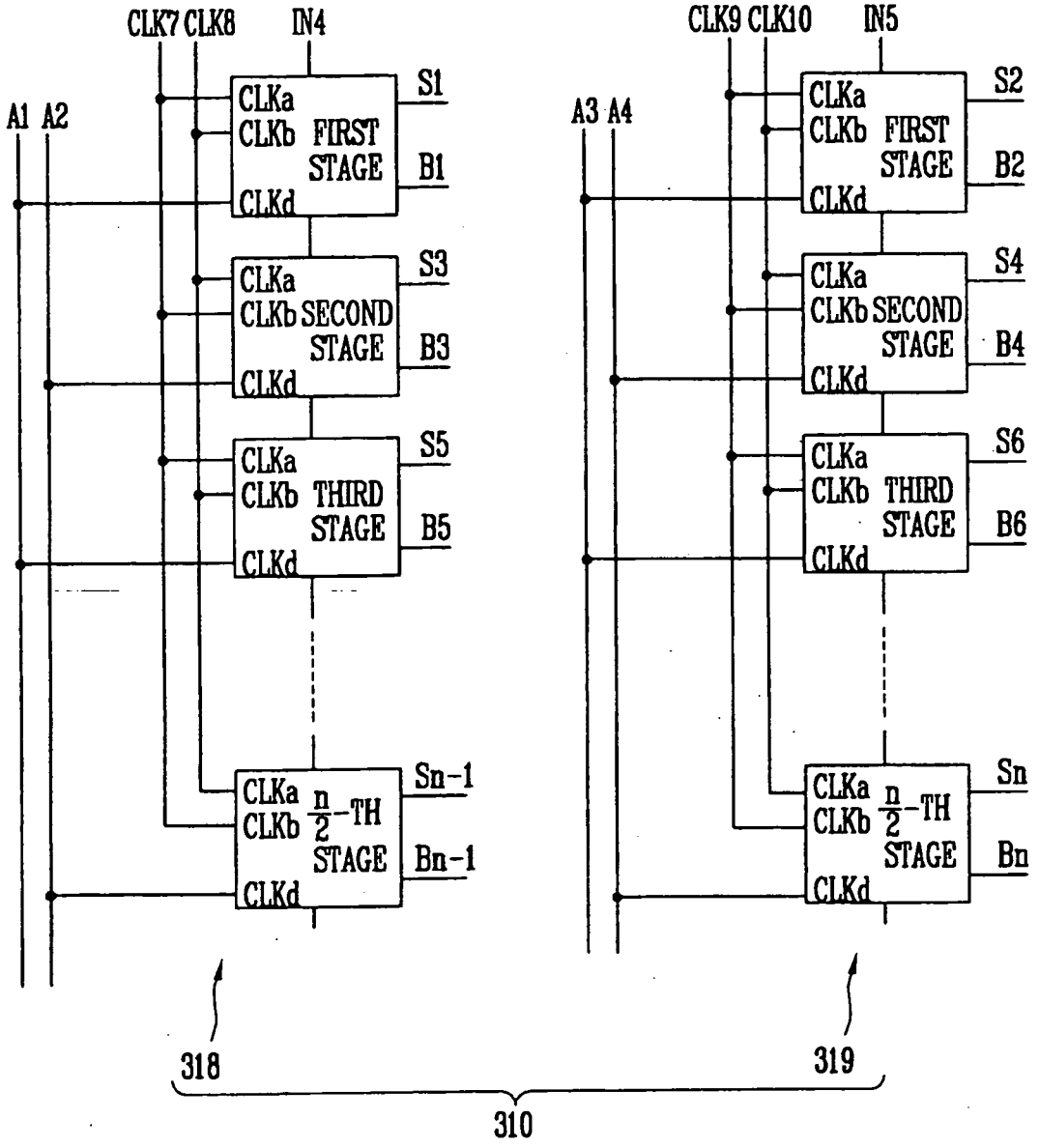

CLK7 CLK8 IN4
CLK9 CLK10 IN5
A1 A2
A3 A4
CLKa
CLKb
CLKd
FIRST STAGE
SECOND STAGE
THIRD STAGE
n/2-TH STAGE
S1
S2
S3
S4
S5
S6
Sn-1
Sn
B1
B2
B3
B4
B5
B6
Bn-1
Bn
318
319
310

FIG. 17

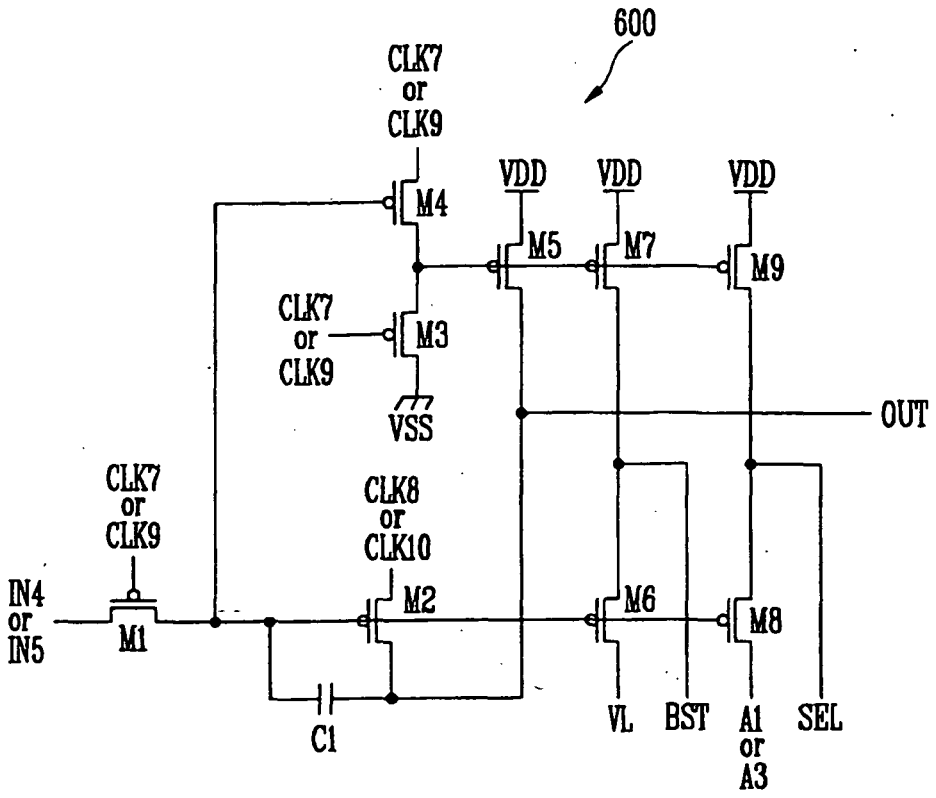
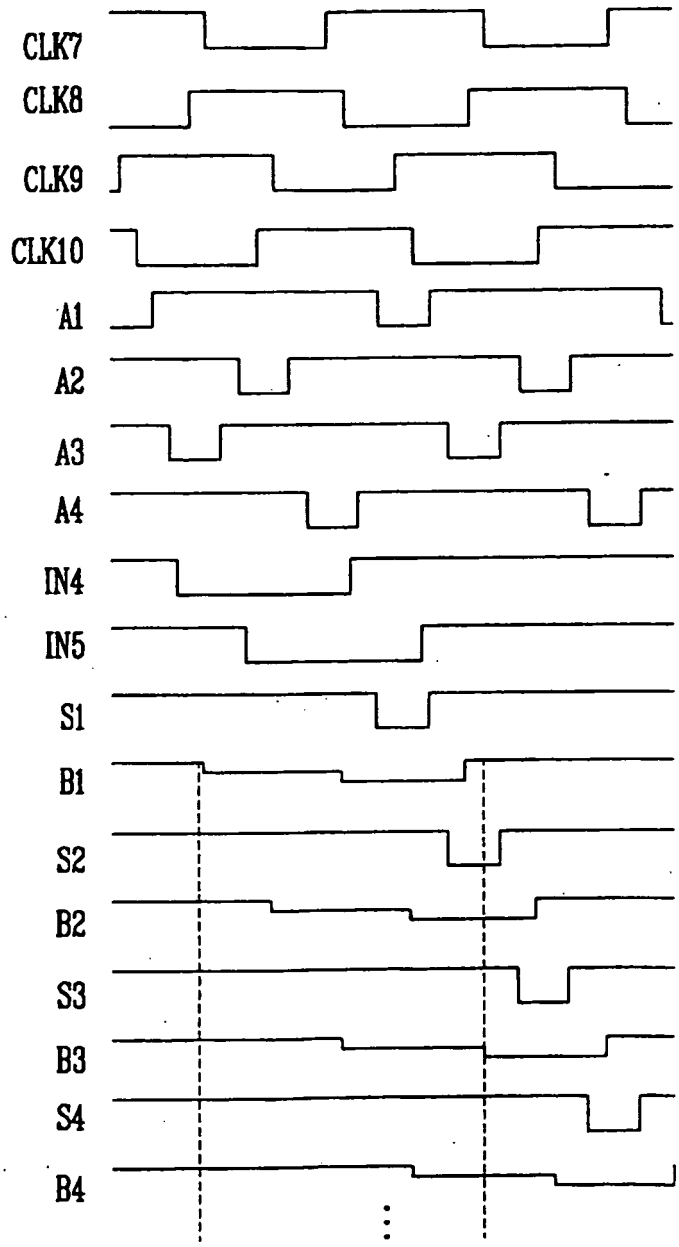

600
CLK7 or CLK9
VDD
VDD
VDD
M4
M5
M7
M9
CLK7 or CLK9
M3
VSS
OUT
CLK7 or CLK9
CLK8 or CLK10
IN4 or IN5
M1
M2
M6
M8
C1
VL
BST
A1 or A3
SEL

FIG. 18



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20050093464 A **[0013]**
- US 6339631 B **[0014]**
- US 20040227718 A **[0015]**
- US 5517543 A **[0016]**
- US 20050078076 A **[0017]**

专利名称(译)	扫描驱动电路和使用其的有机发光显示器		
公开(公告)号	EP1764773B1	公开(公告)日	2015-04-08
申请号	EP2006254876	申请日	2006-09-20
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	SHIN DONG YONG LEGAL & IP TEAM		
发明人	SHIN, DONG YONG LEGAL & IP TEAM		
IPC分类号	G09G3/32		
CPC分类号	G11C19/184 G09G3/20 G09G2300/0426 G09G2300/043 G09G2300/0809 G09G2310/0262 G09G2310/0267 G09G2310/0286 G09G2330/021 G11C19/28		
优先权	1020050087426 2005-09-20 KR		
其他公开文献	EP1764773A3 EP1764773A2		
外部链接	Espacenet		

摘要(译)

公开了一种扫描驱动电路和使用该扫描驱动电路的有机发光显示器。该电路通过从每个单元的级移除静态电流的流动路径来有效地降低功耗。扫描驱动电路与前级的输入信号线或输出电压线耦合，并包括与两相时钟信号输入线耦合的多个级，第一扫描驱动器依次输出选择信号和/或通过多个阶段的增强信号。第二扫描驱动器通过多个级顺序输出发射信号。第一扫描驱动器包括用于输出选择信号的扫描驱动单元，用于输出奇数编号的升压信号的第一升压驱动单元，以及用于输出偶数编号的升压信号的第二升压驱动单元。

$$\Delta V_G = \frac{\Delta V_B C_2}{C_1 + C_2} \quad (1)$$