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(54) **Data driver, organic light emitting display device using the same, and method of driving the organic light emitting display device**

Datentreiber, organische lichtemittierende Anzeigevorrichtung damit und Verfahren zur Ansteuerung der organischen lichtemittierenden Anzeigevorrichtung

Dispositif de pilotage de données, dispositif d'affichage électroluminescent organique comprenant celui-ci et son procédé de commande

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- **MATSUEDA Y ET AL: "35.1: 2.5-in. AMOLED with Integrated 6-Bit Gamma Compensated Digital Data Driver" 2004 SID INTERNATIONAL SYMPOSIUM. SEATTLE, WA, MAY 25 - 27, 2004, SID INTERNATIONAL SYMPOSIUM, SAN JOSE, CA : SID, US, 25 May 2004 (2004-05-25), pages 1116-1119, XP007011917**

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Description

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a data driver, an organic light emitting display device using the same, and a method of driving the organic light emitting display device, and more particularly to, a data driver capable of displaying images with a substantially uniform brightness, an organic light emitting display device using the same, and a method of driving the organic light emitting display device.

2. Discussion of Related Art

[0002] Recently, various types of flat panel displays (FPDs) have been developed that reduced weight and volume compared to cathode ray tubes (CRT). The FPDs include liquid crystal displays (LCDs), field emission displays (FEDs), plasma display panels (PDPs), and organic light emitting display devices.

[0003] Among the FPDs, the organic light emitting display devices display images using organic light emitting diode devices that generate light by re-combination of electrons and holes. The organic light emitting display device has high response speed and is driven with low power consumption.

[0004] FIG. 1 illustrates the structure of a conventional organic light emitting display device.

[0005] Referring to FIG. 1, the conventional organic light emitting display device includes a display region 30 including a plurality of pixels 40 coupled to scan lines S1 to Sn and data lines D1 to Dm, a scan driver 10 for driving the scan lines S1 to Sn, a data driver 20 for driving the data lines D1 to Dm, and a timing controller 50 for controlling the scan driver 10 and the data driver 20.

[0006] The timing controller 50 generates data driving control signals DCS and scan driving control signals SCS in response to synchronizing signals supplied from the outside.

[0007] The data driving control signals DCS generated by the timing controller 50 are supplied to the data driver 20 and the scan driving control signals SCS generated by the timing controller 50 are supplied to the scan driver 10. The timing controller 50 supplies the data Data supplied from the outside to the data driver 20.

[0008] The scan driver 10 receives the scan driving control signals SCS from the timing controller 50. The scan driver 10 then generates the scan signals to sequentially supply the generated scan signals to the scan lines S1 to Sn.

[0009] The data driver 20 receives the data driving control signals DCS from the timing controller 50. The data driver 20 then generates data signals and supplies the generated data signals to the data lines D1 to Dm in synchronization with the scan signals.

[0010] The display region 30 receives first and second power from a first power source ELVDD and a second power source ELVSS from the outside, respectively, and supplies the first and second power to the pixels 40. The pixels 40 then control the currents that flow from the first power source ELVDD to the second power source ELVSS via an organic light emitting diode devices in response to the data signals to generate light components corresponding to the data signals.

[0011] That is, according to the conventional organic light emitting display device, each of the pixels 40 generates light with predetermined brightness in response to each of the data signals. However, according to the conventional organic light emitting display device, due to non-uniformity in the threshold voltages of transistors included in the pixels 40 and deviation in electron mobility, it may not be possible to display images with desired brightness. While the threshold voltages of the transistors included in the pixels 40 may be compensated for by controlling the structure of the pixel circuits included in the pixels 40, the deviation in the electron mobility is not compensated for. Therefore, an organic light emitting display device capable of displaying images with a substantially uniform brightness regardless of the deviation in the electron mobility is desired.

[0012] Furthermore, HAI-JUNG IN, JOON-HO BAE, JIN-SUNG KANG, AN OHKYONG KWON: "A Novel Voltage-Programming Pixel with Current-Correction Method for Large-Size and High-Resolution AMOLEDS on Poly-Si Back-plane" IMID 05 DIGEST, [Online] 23 July 2005 (2005-07-23), pages 901-904, XP002405123 Retrieved from the Internet: URL:http://pddocserv/specdocs/datalhandbooks/IMID/2005/28.6.pdf> [retrieved of 2006-10-20] discloses a new driving method and a pixel circuit for large-area large-size and high-resolution AMOLEDS (active matrix organic light diodes). The maximum error of emission currents in the proposed voltage-programming pixel structure with current correction method are 1.536%, 2.45%, and 2.97% for 30-inch, 40-inch, and 50-inch HDTVS, respectively, when $\pm$12.5% variation of mobility and $\pm$0.3V variation threshold voltage are assumed. The proposed pixel improves emission current uniformity by compensating not only threshold voltage but also mobility of pixel driving TFTs and overcomes the charging problem because it basically uses voltage programming methods. It is expected that proposed driving method can be applicable at large-area full HDTV application.

[0013] Furthermore, MATSUEDA Y ET AL:"35.1:2.5-in. AMOLED with Integrated 6-Bit Gamma Compensated Digital

Data Driver" 2004 SID INTERNATIONAL SYMPOSIUM. SEATTLE, WA, MAY 25-27, 2004, SID INTERNATIONAL SYMPOSIUM, SAN JOSE, CA : SID, US, 25 May 2004 (2004-05-25), pages 1116-1119, XP07011917 discloses a teaching of how to compensate the threshold voltage using a pixel circuit, comprising capacitors and transistors.

[0014] Furthermore, US 2004/124780 A1 discloses an electro-luminescence display device and driving method thereof. The electro-luminescence display device includes a supply voltage source; a data driver for driving a plurality of data lines arranged within a panel; a gamma voltage generator for generating gamma voltages to generate analog data voltages corresponding to externally inputted data signals provided to the data driver; and a threshold voltage generator and the supply voltage source for controlling a supply voltage of the supply voltage source and to apply the controlled voltage to the gamma voltage generator.

SUMMARY OF THE INVENTION

[0015] Accordingly, it is an aspect of the present invention to provide a data driver for driving an organic light emitting display device capable of displaying images with a substantially uniform brightness. It is further an aspect of the present invention to provide a display region comprising a pixel circuit allowing for compensation of variations of a transistor's electron mobility, an organic light emitting display device comprising such a data driver and such a display region, and a method of driving the organic light emitting display device.

[0016] The invention is set forth in claims 1 and 2.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] These and/or other aspects and features of the invention will become apparent and more readily appreciated from the following description of the exemplary embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 illustrates a conventional organic light emitting display device;
FIG. 2 illustrates an organic light emitting display device according to an embodiment of the present invention;
FIG. 3 is a circuit diagram illustrating an example of a pixel illustrated in FIG. 2;
FIG. 4 illustrates waveforms that describe a method of driving the pixel illustrated in FIG. 3;
FIG. 5 is a circuit diagram illustrating another example of the pixel illustrated in FIG. 2;
FIG. 6 is a block diagram illustrating an example of the data driver illustrated in FIG. 2;
FIG. 7 is a block diagram illustrating another example of the data driver illustrated in FIG. 2;
FIG. 8 illustrates an example of a connection among a voltage generator, a digital-to-analog converter, a first buffer, a second buffer, a switching unit, a current sink unit, and a pixel;
FIG. 9 illustrates a method of driving the pixel, the switching unit, and the current sink unit illustrated in FIG. 8;
FIG. 10 illustrates another example of the switching unit illustrated in FIG. 8;
FIG. 11 illustrates another example of the connection among the voltage generator, the digital-to-analog converter, the first buffer, the second buffer, the switching unit, the current sink unit, and the pixel;
FIG. 12 illustrates still another example of the data driver illustrated in FIG. 2;
FIG. 13 illustrates the connection among the voltage generator, the digital-to-analog converter, the first buffer, the second buffer, the switching unit, the current sink unit, and the pixel illustrated in FIG. 12; and
FIG. 14 illustrates waveforms that describe a method of driving the voltage generator, the switching unit, and the current sink unit illustrated in FIG. 13.

DETAILED DESCRIPTION

[0018] Hereinafter, exemplary embodiments of the present invention will be described with reference to FIGs. 2 to 5 and 12 to 14.

[0019] FIG. 2 illustrates an organic light emitting display device according to an embodiment of the present invention.

[0020] Referring to FIG. 2, the organic light emitting display device according to one embodiment of the present invention includes a display region 130 including a plurality of pixels 140 coupled to scan lines S1 to Sn, emission control lines E1 to En, and data lines D1 to Dm, a scan driver 110 for driving the scan lines S1 to Sn and the emission control lines E1 to En, a data driving part 120 for driving the data lines D1 to Dm, and a timing controller 150 for controlling the scan driver 110 and the data driving part 120. The display region 130 includes the pixels 140 formed in the regions partitioned by the scan lines S1 to Sn, the emission control lines E1 to En, and the data lines D1 to Dm. The pixels 140 receive a first voltage from a first power source ELVDD, a second voltage from a second power source ELVSS, and a reference voltage from a reference power source Vref from the outside. The pixels 140 then compensate for drop of the voltage of the first power source ELVDD using a difference between the reference voltage of the reference power source

Vref and the first voltage of the first power source ELVDD. The pixels 140 supply predetermined currents from the first power source ELVDD to the second power source ELVSS via organic light emitting diode devices (not shown) in response to data signals. Each of the pixels 140 may have the structure illustrated in FIG. 3 or 5. Detailed description of the structure of the pixel 140 illustrated in FIG. 3 or 5 will follow.

[0021] The timing controller 150 generates data driving control signals DCS and scan driving control signals SCS in response to synchronizing signals supplied from the outside. The data driving control signals DCS generated by the timing controller 150 are supplied to the data driving part 120 and the scan driving control signals SCS generated by the timing controller 150 are supplied to the scan driver 110. The timing controller 150 supplies data Data supplied from the outside to the data driving part 120. The scan driver 110 receives the scan driving control signals SCS. The scan driver 110 then sequentially supplies scan signals to the scan lines S1 to Sn. The scan driver 110 also sequentially supplies emission control signals to the emission control lines E1 to En. Each of the emission control signals is supplied to overlap two scan signals. Therefore, a width of the emission control signals is equal to or larger than a width of the scan signals.

[0022] The data driving part 120 receives the data driving control signals DCS from the timing controller 150. The data driving part 120 then generates the data signals to be supplied to the data lines D1 to Dm. The data driving part 120 supplies predetermined currents to the data lines D1 to Dm in a first period of a horizontal period H and supplies predetermined voltages (representing the data signals) to the data lines D1 to Dm in a second period following the first period of the horizontal period H. Therefore, the data driving part 120 includes at least one data driver 200.

[0023] FIG. 3 illustrates pixel 1401 which is an example of the pixel 140 illustrated in FIG. 2. In FIG. 3, for the sake of convenience, the pixel coupled to the mth data line Dm, the (n-1)th and nth scan lines Sn-1 and Sn, and the nth emission control line En is illustrated.

[0024] Referring to FIG. 3, the pixel 1401 in one embodiment of the present invention includes an organic light emitting diode (OLED) and a pixel circuit 1421 for supplying current to the OLED.

[0025] The OLED generates light of a predetermined color in response to the current supplied from the pixel circuit 1421.

[0026] The pixel circuit 1421 compensates for drop in the first voltage from the first power source ELVDD and a threshold voltage of a fourth transistor M4 when a scan signal is supplied to the (n-1)th scan line Sn-1 (the previous scan line) and charges the voltage corresponding to the data signal when the scan signal is supplied to the nth scan line Sn (the current or the present scan line). Therefore, the pixel circuit 1421 includes first, second, third, fourth, fifth, sixth transistors M1, M2, M3, M4, M5, and M6, a first capacitor C1, and a second capacitor C2. Each transistor has first and second electrodes and a gate electrode.

[0027] The first electrode of the first transistor M1 is coupled to the data line Dm and the second electrode of the first transistor M1 is coupled to a first node N1. The gate electrode of the first transistor M1 is coupled to the nth scan line Sn. The first transistor M1 is turned on when the scan signal is supplied to the nth scan line Sn to electrically connect the data line Dm and the first node N1 to each other.

[0028] The first electrode of the second transistor M2 is coupled to the data line Dm and the second electrode of the second transistor M2 is coupled to the second electrode of the fourth transistor M4. The gate electrode of the second transistor M2 is coupled to the nth scan line Sn. The second transistor M2 is turned on when the scan signal is supplied to the nth scan line Sn to electrically connect the data line Dm and the second electrode of the fourth transistor M4 to each other.

[0029] The first electrode of the third transistor M3 is coupled to the reference power source Vref and the second electrode of the third transistor M3 is coupled to the first node N1. The gate electrode of the third transistor M3 is coupled to the (n-1)th scan line Sn-1. The third transistor M3 is turned on when the scan signal is supplied to the (n-1)th scan line Sn-1 to electrically connect the reference power source Vref and the first node N1 to each other.

[0030] The first electrode of the fourth transistor M4 is coupled to the first power source ELVDD and the second electrode of the fourth transistor M4 is coupled to the first electrode of the sixth transistor M6. The gate electrode of the fourth transistor M4 is coupled to a second node N2. The fourth transistor M4 supplies the current corresponding to the voltage applied to the second node N2, that is, the voltage charged in the first and second capacitors C1 and C2, to the first electrode of the sixth transistor M6.

[0031] The second electrode of the fifth transistor M5 is coupled to the second node N2 and the first electrode of the fifth transistor M5 is coupled to the second electrode of the fourth transistor M4. The gate electrode of the fifth transistor M5 is coupled to the (n-1)th scan line Sn-1. The fifth transistor M5 is turned on when the scan signal is supplied to the (n-1)th scan line Sn-1 so that current flows through the fourth transistor M4 and that the fourth transistor M4 operates as a diode.

[0032] The first electrode of the sixth transistor M6 is coupled to the second electrode of the fourth transistor M4 and the second electrode of the sixth transistor M6 is coupled to the anode electrode of the OLED. The gate electrode of the sixth transistor M6 is coupled to the nth emission control line En. The sixth transistor M6 is turned off when an emission control signal is supplied to the nth emission control line En and is turned on when no emission control signal is supplied. Here, the emission control signal supplied to the nth emission control line En is supplied to overlap the scan

signals supplied to the (n-1)th scan line Sn-1 and the nth scan line Sn. Therefore, the sixth transistor M6 is turned off when the scan signal is supplied to the (n-1)th scan line Sn-1 and the nth scan line Sn so that predetermined voltage is charged in the first and second capacitors C1 and C2 and is turned on in the other cases to electrically connect the fourth transistor M4 and the OLED to each other. While in FIG. 3, for the sake of convenience, the transistors M1 to M6 are shown as PMOS transistors, the present invention is not limited to a circuit including PMOS transistors but could e.g. include NMOS transistors instead of or together with PMOS transistors.

[0033] In the pixel 1401 illustrated in FIG. 3, the reference power source Vref does not supply current to the OLED. Since the reference power source Vref is not loaded resistively and does not supply current to the pixel 1401, a drop in voltage in Vref is not generated. Therefore, it is possible to maintain the voltage value of the reference power source Vref uniform regardless of the positions of the pixels 140. The voltage value of the reference power source Vref may be equal to or different from the voltage of the first power source ELVDD.

[0034] FIG. 4 illustrates waveforms that describe a method of driving the pixel illustrated in FIG. 3. In FIG. 4, a horizontal period H is divided into a first period and a second period to be driven. In the first period, a predetermined current (PC) flows to the data lines D1 to Dm. In the second period, a data signal DS is supplied to the data lines D1 to Dm. The PC is pulled from the pixel 1401 to one of the data drivers 200 which operates as a current sink.

[0035] The data signal DS is supplied from the data driver 200 to the pixel 1401. Hereinafter, for the sake of convenience, it is assumed that the initial voltage value of the reference power source Vref is equal to the initial voltage value of the first power source ELVDD. Operation processes will be described in detail with reference to FIGs. 3 and 4. First, the scan signal is supplied to the (n-1)th scan line Sn-1. When the scan signal is supplied to the (n-1)th scan line Sn-1, the third and fifth transistors M3 and M5 are turned on. When the fifth transistor M5 is turned on, current flows through the fourth transistor M4 and the fourth transistor M4 operates as a diode. When the fourth transistor M4 operates as a diode, the voltage value obtained by subtracting the threshold voltage of the fourth transistor M4 from the first power source ELVDD is applied to the second node N2.

[0036] When the third transistor M3 is turned on, the voltage of the reference power source Vref is applied to the first node N1. At this time, the second capacitor C2 is charged with the voltage corresponding to difference between the first node N1 and the second node N2. In this case, when it is assumed that the reference power source Vref is equal to the voltage value of the first power source ELVDD, the voltage corresponding to the threshold voltage of the fourth transistor M4 is charged in the second capacitor C2. When a predetermined drop in voltage is generated in the first power source ELVDD, e.g. due to a contact resistance in the supply line or such, the threshold voltage of the fourth transistor M4 and the voltage corresponding to the voltage drop of the first power source ELVDD are charged in the second capacitor C2. That is, according to the present invention, in the period where the scan signal is supplied to the (n-1)th scan line Sn-1, the voltage corresponding to the voltage drop of the first power source ELVDD and the threshold voltage of the fourth transistor M4 are charged in the second capacitor C2. Accordingly, it is possible to compensate for the voltage drop of the first power source ELVDD.

[0037] After a predetermined voltage is charged in the second capacitor C2, the scan signal is supplied to the nth scan line Sn. When the scan signal is supplied to the nth scan line Sn, the first and second transistors M1 and M2 are turned on. When the second transistor M2 is turned on, in the first period of the horizontal period H, the PC is pulled from the pixel 1401 to the data driver 200 via the data line Dm. In more detail, the PC is supplied to the data driver 200 via the first power source ELVDD, the fourth transistor M4, the second transistor M2, and the data line Dm. The voltages in the node N1 and the node that connects the second electrode of transistor M4 to the first electrode of transistor M6 drop in response to the PC until transistor M4 can supply the current pulled to the data driver 200. At this time, a predetermined voltage is charged in the first and second capacitors C1 and C2 in response to the PC. These voltages depend on the electrical characteristics of transistor M4 such as its individual electron mobility and may be used to calibrate the data driver 200 to compensate for variations in electron mobility when supplying a data signal to the pixel 1401.

[0038] On the other hand, the data driver 200 resets the voltage of a gamma voltage unit (not shown) using a compensation voltage generated when the PC sinks to generate the data signal DS using the reset voltage of the gamma voltage unit. Then, the data signal DS is supplied to the first node N1 via the first transistor M1 in the second period of the horizontal period H. Then, the voltage corresponding to a difference between the data signal DS and the voltage of the first power source ELVDD is charged in the first capacitor C1. At this time, since the second node N2 floats, the second capacitor C2 maintains the previously charged voltage.

[0039] That is, according to the described embodiment of the present invention, in the period where the scan signal is supplied to one of the scan lines, called a previous scan line (i.e., Sn-1), the threshold voltage of the fourth transistor M4 and the voltage corresponding to the voltage drop of the first power source ELVDD are charged in the second capacitor C2 so that it is possible to compensate for the voltage drop of the first power source ELVDD and the threshold voltage of the fourth transistor M4. According to the described embodiment of the present invention, the voltage of the gamma voltage unit is reset so that the electron mobility of the transistors included in the pixel 1401 is compensated for during the period in which the scan signal is supplied to the next scan line, called a current or a present scan line (i.e., Sn), and the generated data signal is supplied using the reset gamma voltage. Therefore, according to the described

embodiment of the present invention, non-uniformity in the threshold voltages of the transistors and the electron mobility is compensated for, so that it is possible to display images with a substantially uniform brightness. Processes of resetting the voltage of the gamma voltage unit will be described later.

[0040] FIG. 5 illustrates a pixel 1402 which is another example of the pixel 140 illustrated in FIG. 2. The pixel 1402 includes a pixel circuit 1422 that includes first, second, third, fourth, fifth, and sixth transistors M1', M2', M3', M4', M5', and M6', a first capacitor C1', and a second capacitor C2'. Each transistor has first and second electrodes and a gate electrode. The structure of the pixel 1402 illustrated in FIG. 5 is the same as the structure of the pixel 1401 illustrated in FIG. 3 except that the first capacitor C1' is now provided between the second node N2' and the first power source ELVDD.

[0041] Operation processes will be described in detail with reference to FIGs. 4 and 5. First, the scan signal is supplied to the (n-1)th scan line Sn-1. When the scan signal is supplied to the (n-1)th scan line Sn-1, the third and fifth transistors M3' and M5' are turned on. When the fifth transistor M5' is turned on, current flows through the fourth transistor M4' so that the fourth transistor M4' operates as a diode. When the fourth transistor M4' operates as a diode, the voltage value obtained by subtracting the threshold voltage of the fourth transistor M4' from the first power source ELVDD is applied to the second node N2'. Therefore, the voltage corresponding to the threshold voltage of the fourth transistor M4' is charged in the first capacitor C1'.

[0042] When the third transistor M3' is turned on, the voltage of the reference power source Vref is applied to the first node N1'. Then, the second capacitor C2' charges the voltage corresponding to a difference between the first node N1' and the second node N2'. Here, since the first and second transistors M1' and M2' are turned off in the period where the scan signal is supplied to the (n-1)th scan line Sn-1, the data signal DS is not supplied to the pixel 1402.

[0043] Then, the scan signal is supplied to the nth scan line Sn so that the first and second transistors M1' and M2' are turned on. When the second transistor M2' is turned on, in the first period of the horizontal period H, the PC is supplied from the pixel 1402 to the data driver 200 via the data line Dm. Actually, the PC is supplied to the data driver 200 via the first power source ELVDD, the fourth transistor M4', the second transistor M2', and the data line Dm. At this time, a predetermined voltage is charged in the first and second capacitors C1' and C2' in response to a first data signal DS1.

[0044] The data driver 200 resets the voltage of the gamma voltage unit (not shown) using the compensation voltage applied in response to the PC to generate the data signal DS using the reset voltage of the gamma voltage unit. Then, in the second period of the horizontal period H, the data signal DS is supplied to the first node N1'. Then, the predetermined voltage corresponding to the data signal DS is charged in the first and second capacitors C1' and C2'.

[0045] Actually, when the data signal DS is supplied, the voltage of the first node N1' falls from the voltage of the reference power source Vref to the voltage of the data signal DS. Since the second node N2' floats, the voltage at the second node N2' is reduced in response to the amount of voltage drop of the first node N1'. The amount of reduction in the voltage of the second node N2' is determined by the capacitance values of the first and second capacitors C1' and C2'.

[0046] When the voltage of the second node N2' falls, the predetermined voltage corresponding to the voltage value of the second node N2' is charged in the first capacitor C1'. Here, since the voltage value of the reference power source Vref is fixed, the voltage charged in the first capacitor C1' is determined by the data signal DS. That is, since the voltage values charged in the capacitors C1' and C2' are determined by the reference power source Vref and the data signal DS in the pixel 1402 illustrated in FIG. 5, it is possible to charge a desired voltage regardless of the voltage drop of the first power source ELVDD.

[0047] According to the described embodiments of the present invention, the voltage of the gamma voltage unit is reset to compensate for the electron mobility of the transistors included in the pixel 1402 and to supply the generated data signal using the reset gamma voltage. Therefore, according to the described embodiments of the present invention, non-uniformity in the threshold voltages of the transistors and deviation in the electron mobility of the transistors is compensated for so that it is possible to display images with a substantially uniform brightness.

[0048] FIG. 6 is a block diagram illustrating an exemplary embodiment of a data driver 201, which is an example of the data driver 200 illustrated in FIG. 2. In FIG. 6, for the sake of convenience, it is assumed that the data driver 201 has j (j is a natural number not less than 2) channels.

[0049] Referring to FIG. 6, the data driver 201 according to the exemplary embodiment includes a shift register unit 210, a sampling latch unit 220, a holding latch unit 230, a gamma voltage unit 240, a digital-to-analog converter unit (hereinafter, referred to as a DAC) 250, a first buffer unit 270, a second buffer unit 260, a current supplying unit 280, and a selector 290.

[0050] The shift register unit 210 receives a source shift clock SSC and a source start pulse SSP from the timing controller 150. The shift register unit 210 then sequentially generates j sampling signals while shifting the source start pulse SSP every one period of the source shift clock SSC. Therefore, the shift register unit 210 includes j shift registers 2101 to 210j.

[0051] The sampling latch unit 220 sequentially stores the data Data in response to the sampling signals sequentially supplied from the shift register unit 210. Here, the sampling latch unit 220 includes j sampling latches 2201 to 220j in order to store the j data Data. Each of the sampling latches 2201 to 220j has the magnitude corresponding to the number

of bits of the data Data. For example, when the data Data is composed of k bits, each of the sampling latches 2201 to 220j has the magnitude of k bits.

[0052] The holding latch unit 230 receives the data Data from the sampling latch unit 220 to store the data Data when a source output enable signal SOE is input. The holding latch unit 230 supplies the data Data stored therein to the DAC unit 250, when the source output enable signal SOE is input. Here, the holding latch unit 230 includes j holding latches 2301 to 230j in order to store the j data Data. Each of the holding latches 2301 to 230j has the magnitude corresponding to the number of bits of the data Data. For example, each of the holding latches 2301 to 230j has the magnitude of k bits to store the data Data.

[0053] The gamma voltage unit 240 includes j voltage generators 2401 to 240j for generating predetermined gray scale voltage in response to the data Data of k bits. As illustrated in FIG. 8, each of the voltage generators 2401 to 240j is composed of a plurality of voltage dividing resistors R(1) to R(I) to generate 2^k gray scale voltages. Here, the voltage generators 2401 to 240j reset the values of the gray scale voltages using the compensation voltage supplied from the second buffer unit 260 to supply the reset gray scale voltages to the DACs 2501 to 250j.

[0054] The DAC unit 250 includes j DACs 2501 to 250j that generate the data signal DS in response to the bit values of the data Data. Each of the DACs 2501 to 250j selects one of the plurality of gray scale voltages in response to the bit values of the data Data supplied from the holding latch unit 230 to generate a second data signal DS2.

[0055] The first buffer unit 270 supplies the data signals DS supplied from the DAC unit 250 to the selector 290. Therefore, the first buffer unit 270 includes j first buffers 2701 to 270j. The selector 290 controls electrical connection between the data lines D1 to Dj and the first buffers 2701 to 270j. Actually, the selector 290 electrically connects the data lines D1 to Dj and the first buffers 2701 to 270j to each other only in the second period of the horizontal period H and does not connect the data lines D1 to Dj and the first buffers 2701 to 270j to each other in the other period. Therefore, the selector 290 includes j switching units 2901 to 290j.

[0056] The current supplying unit 280 sinks the PC from the pixels 140 coupled to the data lines D1 to Dj in the first period of the horizontal period H. Actually, the current supplying unit 280 sinks the maximum current that can flow through each of the pixels 140, that is, the current to be supplied to the OLED when the pixel 140 emits light with the maximum brightness. The current supplying unit 280 supplies a predetermined compensation voltage generated when the current sinks to the second buffer unit 260. Therefore, the current supplying unit 280 includes j current sink units 2801 to 280j.

[0057] The second buffer unit 260 supplies the compensation voltage supplied from the current supplying unit 280 to the gamma voltage unit 240. Therefore, the second buffer unit 260 includes j second buffers 2601 to 260j.

[0058] On the other hand, as illustrated in FIG. 7, a data driver 202, which is an example of the data driver 200 according to one exemplary embodiment may further include a level shifter unit 310 after the holding latch unit 230. The level shifter unit 310 increases the voltage levels of the data Data supplied from the holding latch unit 230 to supply the data Data to the DAC unit 250. When the data Data having a high voltage level are supplied from an external system to the data driver 200, circuit parts having a high voltage resistant property must be provided in response to the voltage level so that manufacturing cost increases. Therefore, the data Data having a low voltage level are supplied from the outside of the data driver 200 and the low voltage level is transited to a high voltage level by the level shifter unit 310.

[0059] FIG. 8 illustrates a connection among the voltage generator, the DAC, the first buffer, the second buffer, the switching unit, the current sink unit, and the pixel circuit provided in a specific channel. In FIG. 8, for the sake of convenience, a jth channel is illustrated and it is assumed that the data line Dj is coupled to the pixel circuit 1421 of the pixel 1401 illustrated in FIG. 3.

[0060] Referring to FIG. 8, the voltage generator 240j includes a plurality of voltage dividing resistors R(1) to R(I). The voltage dividing resistors R(1) to R(I) are positioned between the reference power source Vref and the second buffer 260j. The voltage dividing resistors R(1) to R(I) divide the voltage between the voltage of the reference power source Vref and the compensation voltage supplied from the second buffer 260j to generate a plurality of gray scale voltages to V(0) to V(2^k-1) and to supply the generated gray scale voltages to the DAC 250j.

[0061] The DAC 250j selects one gray scale voltage among the gray scale voltages V(0) to V(2^k-1) in response to the bit values of the data Data to supply the selected gray scale voltage to the first buffer 270j. Here, the gray scale voltage selected by the DAC 250j is used as the data signal DS.

[0062] The first buffer 270j transmits the data signal DS supplied from the DAC 250j to the switching unit 290j.

[0063] The switching unit 290j includes an 11^{th} transistor M11. The 11^{th} transistor M11 is controlled by the first control signal CS1 illustrated in FIG. 9. That is, the 11^{th} transistor M11 is turned on in the second period of the horizontal period H and is turned off in the first period. Therefore, the data signal DS is supplied to the data line Dj in the second period of the horizontal period H and is not supplied in the other period.

[0064] The current sink unit 280j includes 12^{th} and 13^{th} transistors M12 and M13 controlled by the second control signal CS2, a current source Imax coupled to the first electrode of the 13^{th} transistor M13, and a third capacitor C3 coupled between a third node N3 and a ground voltage source GND. The 12^{th} and 13^{th} transistors M12 and M13 each have a gate electrode and first and second electrodes.

[0065] The gate electrode of the 12^{th} transistor M12 is coupled to the gate electrode of the 13^{th} transistor M13 and

the second electrode of the 12th transistor M12 is coupled to the second electrode of the 13th transistor M13 and the data line Dj. The first electrode of the 12th transistor M12 is coupled to the second buffer 260j. The 12th transistor M12 is turned on in the first period of the horizontal period H by the second control signal CS2 and is turned off in the second period.

[0066] The first electrode of the 13th transistor M13 is coupled to the current source Imax. The 13th transistor M13 is also turned on by the second control signal CS2 in the first period of the horizontal period H and is turned off in the second period.

[0067] The current source Imax receives the current to be supplied to the OLED when the pixel 1401 emits light with a maximum brightness in the first period where the 12th and 13th transistors M12 and M13 are turned on.

[0068] The third capacitor C3 stores the compensation voltage applied to the third node N3 when the current source Imax operates as a current sink for the current from the pixel 1401. The third capacitor C3 that has been charged with the compensation voltage in the first period, maintains the compensation voltage of the third node N3 uniform even when the 12th and 13th transistors M12 and M13 are turned off in the second period. The second buffer 260j transmits the compensation voltage applied to the third node N3, that is, the voltage charged in the third capacitor C3 to the voltage generator 240j. Then, the voltage generator 240j divides the voltage between the voltage of the reference power source Vref and the compensation voltage supplied from the second buffer 260j. Here, the compensation voltage applied to the third node N3 is set to be the same or to vary in each pixel 140 in accordance with the electron mobility of the transistors included in the pixel 140. The compensation voltage supplied to the j voltage generators 2401 to 240j is determined by the currently coupled pixel 140.

[0069] On the other hand, when different compensation voltages are supplied to the j voltage generators 2401 to 240j, the values of the gray scale voltages V(0) to V(2^k-1) supplied to the DACs 2501 to 250j provided in the j channels are set to be different from each other. Here, since the gray scale voltages V(0) to V(2^k-1) are controlled by the pixels 140 to which the data lines D1 to Dj are currently coupled, although the electron mobility of the transistors included in the pixels 140 is non-uniform, the display region 130 can display images with a substantially uniform brightness.

[0070] FIG. 9 illustrates driving waveforms supplied to the switching unit, the current sink unit, and the pixel illustrated in FIG. 8.

[0071] The voltage value of the data signal DS supplied to the pixel 140 will be described in detail with reference to FIGs. 8 and 9. First, the scan signal is supplied to the (n-1)th scan line Sn-1. When the scan signal is supplied to the (n-1)th scan line Sn-1, the third and fifth transistors M3 and M5 are turned on. Then, the voltage value obtained by subtracting the threshold voltage of the fourth transistor M4 from the first power source ELVDD is applied to the second node N2 and the voltage of the reference power source Vref is applied to the first node N1. At this time, the voltage corresponding to the voltage drop of the first power source ELVDD and the threshold voltage of the fourth transistor M4 are charged in the second capacitor C2.

[0072] Actually, the voltages applied to the first node N1 and the second node N2 are represented by EQUATION 1.

[EQUATION1]

$$V_{N1} = Vref$$

$$V_{N2} = ELVDD - V_{thM4}$$

wherein, V_{N1}, V_{N2}, and V_{thM4} represent the voltage applied to the first node N1, the voltage applied to the second node N2, and the threshold voltage of the fourth transistor M4, respectively.

[0073] On the other hand, in a period between the point of time when the scan signal supplied to the (n-1)th scan line Sn-1 is turned off and the point of time when the scan signal is supplied to the nth scan line Sn, the first and second nodes N1 and N2 float. Therefore, the voltage value charged in the second capacitor C2 does not change. Then, the scan signal is supplied to the nth scan line Sn so that the first and second transistors M1 and M2 are turned on. While the scan signal is supplied to the nth scan line Sn, in the first period, the 12th and 13th transistors M12 and M13 are also turned on. When the 12th and 13th transistors M12 and M13 are turned on, a current flows through the current source Imax via the first power source ELVDD, the fourth transistor M4, the second transistor M2, the data line Dj, and the 13th transistor M13 and the current source Imax operates as a current sink for this current.

[0074] At this time, since the current of the current source Imax flows through the fourth transistor M4, EQUATION 2 is obtained.

[EQUATION 2]

$$I_{max} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(ELVDD - V_{N2} - V_{thM4})^2$$

wherein, μ, Cox, W, and L represent electron mobility, the capacity of an oxide layer, the width of a channel, and the length of a channel, of the fourth transistor M4, respectively.

[0075] The voltage applied to the second node N2 when the current obtained by EQUATION 2 flows through the fourth transistor M4 may be represented by EQUATION 3.

[EQUATION 3]

$$V_{N2} = ELVDD - \sqrt{\frac{2Imax}{\mu_p C_{ox}}\frac{L}{W}} - |V_{thM4}|$$

[0076] The voltage applied to the first node N1 may be represented by EQUATION 4 by the coupling of the second capacitor C2.

[EQUATION 4]

$$V_{N1} = Vref - \sqrt{\frac{2Imax}{\mu_p C_{ox}}\frac{L}{W}} = V_{N3} = V_{N4}$$

wherein, the voltage V_{N1} applied to the first node N1 may be equal to the voltage V_{N3} applied to the third node N3 and the voltage V_{N4} applied to a fourth node N4 formed between the second buffer 260j and the voltage generator 240j. That is, when the current is sunk by the current source Imax, the voltage obtained by EQUATION 4 is applied to the fourth node N4.

[0077] However, as illustrated by EQUATION 4, the voltage applied to the third node N3 and the fourth node N4 is affected by the electron mobility of the transistors included in the pixel 140 the current from which sinks into the current source Imax. Therefore, the value of the voltage applied at the third node N3 and the fourth node N4 when the current is sunk by the current source Imax varies in each of the pixels 140 according to the electron mobility of each of the pixels 140.

[0078] When the voltage obtained by EQUATION 4 is applied to the fourth node N4, a voltage V_{diff} across the voltage generator 240j may be represented by EQUATION 5.

[EQUATION 5]

$$V_{diff} = Vref - \left(Vref - \sqrt{\frac{2Imax}{\mu_p C_{OX}}\frac{L}{W}}\right)$$

[0079] When the DAC 250j selects the hth (h is a natural number) gray scale voltage among f (f is a natural number greater than or equal to h) gray scale voltages in response to the data Data, the voltage Vb supplied to the first buffer 270j may be represented by EQUATION 6.

[EQUATION 6]

$$Vb = Vref - \frac{h}{f}\sqrt{\frac{2Imax}{\mu_p C_{OX}}\frac{L}{W}}$$

[0080] After the current sinks in the first period so that the voltage obtained by EQUATION 4 is charged in the third capacitor C3, the 12th and 13th transistors M12 and M13 are turned off in the second period and the 11th transistor M11 is turned on. At this time, the third capacitor C3 maintains the voltage value charged therein. Therefore, the voltage value of the third node N3 may be maintained as illustrated in EQUATION 4. Since the 11th transistor M11 is turned on in the second period, the voltage supplied to the first buffer 270j is supplied to the first node N1 via the 11th transistor M11, the data line Dj, and the first transistor M1. That is, the voltage obtained by EQUATION 6 is supplied to the first node N1. The voltage applied to the second node N2 by the coupling of the second capacitor C2 may be represented by EQUATION 7.

[EQUATION 7]

$$V_{N2} = ELVDD - \frac{h}{f}\sqrt{\frac{2Imax}{\mu_p C_{OX}}\frac{L}{W}} - |V_{thM4}|$$

[0081] At this time, the current that flows via the fourth transistor M4 may be represented by EQUATION 8.

[EQUATION 8]

$$I_{M4} = \frac{1}{2}\mu_p C_{OX}\frac{W}{L}(ELVDD - V_{N2} - |V_{thM4}|)^2$$

$$= \frac{1}{2}\mu_p C_{OX}\frac{W}{L}\left(ELVDD - \left(ELVDD - \frac{h}{f}\sqrt{\frac{2Imax}{\mu_p C_{OX}}\frac{L}{W}} - |V_{thM4}|\right) - V_{thM4}\right)^2$$

$$= \left(\frac{h}{f}\right)^2 Imax$$

[0082] Referring to EQUATION 8, according to the present invention, the current that flows through the fourth transistor M4 is determined by the gray scale voltage generated by the voltage generator 240j. That is, according to the present

invention, the current determined by the gray scale voltage can flow to the fourth transistor M4 regardless of the threshold voltage and electron mobility of the fourth transistor M4. Therefore, it is possible to display images with a substantially uniform brightness.

[0083] On the other hand, according to the present invention, the structure of the switching unit 290j may vary. For example, in the switching unit 290j', as illustrated in FIG. 10, the 11th transistor M11 and a 14th transistor M14 may be coupled to each other in the form of a transmission gate. The 14th transistor M14 formed of PMOS receives a second control signal CS2. The 11th transistor M11 formed of NMOS receives the first control signal CS1. As shown in FIG. 9, since the polarity of the first control signal CS1 is opposite to the polarity of the second control signal CS2, the 11th and 14th transistors M11 and M14 are turned on and off at the same time.

[0084] On the other hand, when the 11th and 14th transistors M11 and M14 are coupled to each other in the form of the transmission gate, a voltage-current characteristic curve is in the form of a straight line so that it is possible to minimize switching error.

[0085] FIG. 11 illustrates another example of the connection among the voltage generator, the DAC, the first buffer, the second buffer, the switching unit, the current sink unit, and the pixel provided in the specific channel. The structure of FIG. 11 is the same as the structure of FIG. 8 except that the pixel 1402 is coupled to the data line Dj instead of the first exemplary pixel 1401. Therefore, the voltage supplied to the pixel 1402 will be simply described.

[0086] Referring to FIGs. 9 and 11, first, when the scan signal is supplied to the (n-1)th scan line Sn-1, the voltage obtained by EQUATION 1 is applied to the first and second nodes N1' and N2'.

[0087] The current that flows through the fourth transistor M4' in the first period when the scan signal is supplied to the nth scan line Sn and the 12th and 13th transistors M12' and M13' are turned on is also represented by EQUATION 2 that pertained to the fourth transistor M4 of the first exemplary pixel circuit 1421 and the voltage applied to the second node N2' in the first period is also represented by EQUATION 3.

[0088] The voltage applied to the first node N1' by the coupling of the second capacitor C2' may be represented by EQUATION 9.

[EQUATION 9]

$$V_{N1'} = Vref\text{-}\left(\frac{C1'+C2'}{C2'}\right)\sqrt{\frac{2Imax}{\mu_p C_{ox}}\frac{L}{W}} = V_{N3'} = V_{N4'}$$

[0089] Since the voltage applied to the first node N1' is also supplied to the third node N3 and the fourth node N4, the voltage V_{diff} across the voltage generator 240j may be represented by EQUATION 10.

[EQUATION 10]

$$V_{diff} = Vref\text{-}\left(Vref\text{-}\left(\frac{C1'+C2'}{C2'}\right)\sqrt{\frac{2Imax}{\mu_p C_{OX}}\frac{L}{W}}\right)$$

[0090] When the DAC 250j selects the hth gray scale voltage among f gray scale voltages, the voltage Vb supplied to the first buffer 270j may be represented by EQUATION 11.

[EQUATION 11]

$$Vb = Vref - \frac{h}{f}\left(\frac{C1'+C2'}{C2'}\right)\sqrt{\frac{2Imax}{\mu_p C_{OX}}\frac{L}{W}}$$

[0091] The voltage supplied to the first buffer 270j is supplied to the first node N1'. At this time, the voltage applied to the second node N2' may be represented also by EQUATION 7. Therefore, the current that flows through the fourth transistor M4' may be represented by EQUATION 8. That is, according to the present invention, the current supplied to the OLED via the fourth transistor M4' is determined by the gray scale voltage regardless of the threshold voltage and electron mobility of the fourth transistor M4'. Therefore, it is possible to display images with a substantially uniform brightness.

[0092] On the other hand, in the pixel 1402 illustrated in FIG. 5, the voltage of the second node N2' gradually changes although the voltage of the first node N1' rapidly changes because it changes proportionally to (C1'+C2')/C2'. Therefore, when the pixel 1402 illustrated in FIG. 5 is used, it is possible to set the voltage range of the voltage generator 240j larger than in the case where the pixel 1401 illustrated in FIG. 3 is applied. As described above, when the voltage range of the voltage generator 240j is set to be larger, it is possible to reduce the influence of the switching error of the 11^{th} transistor M11' and the first transistor M1'.

[0093] FIG. 12 illustrates another example 203 of the data driver 200 illustrated in FIG. 2.

[0094] Referring to FIG. 12, the data driver 203 according to an embodiment of the present invention further includes a voltage supply unit 300 provided between the first buffer unit 270 and the DAC unit 250 when compared with the data driver 201 shown in FIG. 6.

[0095] The voltage supply unit 300 supplies a precharging voltage Vp to the first buffer unit 270 every horizontal period. Therefore, each horizontal period is divided into a 0^{th} period, a first period, and a second period as illustrated in FIG. 14. Here, the voltage supply unit 300 supplies the precharging voltage Vp to the first buffer unit 270 in the 0^{th} period of each horizontal period H. That is, the voltage supply unit 300 supplies the precharging voltage before the PC sinks into the current sink Imax. Therefore, it is possible to reduce the time required for sinking the PC.

[0096] The voltage supply unit 300 electrically connects the DAC unit 250 and the first buffer unit 270 to each other in the second period of each horizontal period H. Therefore, the voltage supply unit 300 includes j precharging units 3001 to 300j.

[0097] The first buffer unit 270 supplies the precharging voltage supplied from the precharging units 3001 to 300j and the data signals DS supplied from the DAC unit 250 to the switching unit 290j.

[0098] The selector 290 controls electrical connection between the data lines D1 to Dj and the first buffers 2701 to 270j. The selector 290 electrically couples the data lines D1 to Dj and the first buffers 2701 to 270j to one another in the 0^{th} period in which the precharging voltage Vp is supplied and in the second period in which the data signals DS are supplied and does not connect the data lines D1 to Dj and the first buffers 2701 to 270j to each other in the first period.

[0099] FIG. 13 illustrates the connection among the voltage generator, the DAC unit, the precharging unit, the first buffer, the second buffer, the switching unit, the current sink unit, and the pixel provided in one specific channel of the data driver illustrated in FIG. 12.

[0100] Referring to FIG. 13, the voltage generator 240j includes a plurality of voltage dividing resistors R(1) to R(I). The voltage dividing resistors R(1) to R(I) are provided between the reference power source Vref and the second buffer 260j to divide a voltage. Actually, the voltage dividing resistors R(1) to R(I) divide the voltage between the voltage of the reference power source Vref and the compensation voltage supplied from the second buffer 260j to generate the plurality of gray scale voltages V(0) to V(2^k-1) and to supply the generated gray scale voltages V(0) to V(2^k-1) to the DAC 250j.

[0101] The DAC 250j selects one gray scale voltage among the gray scale voltages V(0) to V(2^k-1) in response to the bit values of the data Data to supply the selected gray scale voltage to the precharging unit 300j. Here, the gray scale voltage selected by the DAC 250j is used as the data signal DS.

[0102] The precharging unit 300j includes the 14^{th} and 15^{th} transistors M14 and M15. The 14^{th} transistor M14 is provided between the DAC 250j and the first buffer 270j to be controlled by a third control signal CS3 illustrated in FIG. 14. The 14^{th} transistor M14 is turned on in the second period of the horizontal period H to supply the data signal DS supplied from the DAC 250j to the first buffer 270j.

[0103] The 15^{th} transistor M15 is provided between the precharging voltage source Vp and the first buffer 270j to be controlled by the fourth control signal CS4. That is, the 15^{th} transistor M15 is turned on in the 0^{th} period of the horizontal period H to supply the precharging voltage Vp to the first buffer 270j.

[0104] The first buffer 270j transmits the precharging voltage Vp and the data signal DS supplied from the precharging unit 300j to the switching unit 290j.

[0105] The switching unit 290j includes the 11th transistor M11. The 11th transistor M11 is controlled by the first control signal CS1. That is, the 11th transistor M11 is turned on in the 0th and second periods of the horizontal period H to supply the precharging voltage Vp and the data signal DS to the data line Dj.

[0106] The current sink unit 280j includes the 12th and 13th transistors M12 and M13 controlled by the second control signal CS2, the current source Imax coupled to the first electrode of the 13th transistor M13, and the third capacitor C3 coupled between the third node N3 and the ground voltage source GND.

[0107] The gate electrode of the 12th transistor M12 is coupled to the gate electrode of the 13th transistor M13. The second electrode of the 12th transistor M12 is coupled to the second electrode of the 13th transistor M13 and the data line Dj. The first electrode of the 12th transistor M12 is coupled to the second buffer 260j. The 12th transistor M12 is turned on by the second control signal CS2 in the first period of the horizontal period H. The first electrode of the 13th transistor M13 is coupled to the current source Imax. The 13th transistor M13 is also turned on by the second control signal CS2 in the first period of the horizontal period H.

[0108] The current source Imax receives the current to be supplied to the OLED when the pixel 1401 emits light with the maximum brightness in the second period when the 12th and 13th transistors M12 and M13 are turned on.

[0109] The third capacitor C3 stores the compensation voltage applied to the third node N3 when the 12th and 13th transistors M12 and M13 are on and the current from the pixel 1401 is sunk by the current source Imax that is operating as a current sink. The third capacitor C3 that has been charged with the compensation voltage, maintains the compensation voltage of the third node N3 uniform even when the 12th and 13th transistors M12 and M13 are turned off in the second period.

[0110] The second buffer 260j supplies the compensation voltage applied to the third node N3 to the voltage generator 240j at the fourth node N4. The voltage generator 240j divides the voltage difference between the voltage of the reference power source Vref and the compensation voltage into a number of different gray scale voltages V(0) to V(2^k-1). The compensation voltage applied to the third node N3 may be the same or may vary in each pixel 1401 due to the electron mobility of the transistors included in the pixel 1401. The compensation voltages supplied to the j voltage generators 2401 to 240j at each point in time are determined by the pixels 1401 to which the data lines D1 to Dj are coupled at that point in time.

[0111] On the other hand, if different compensation voltages are supplied to the j voltage generators 2401 to 240j, the values of the gray scale voltages V(0) to V(2^k-1) supplied to the DACs 2501 to 250j provided in the j channels are also different from one another. Since the gray scale voltages V(0) to V(2^k-1) are controlled by the pixels to which the data lines D1 to Dj are currently coupled, although the mobility of the transistors included in the pixels 1401 or 1402 is non-uniform, the display region 130 can display images with a substantially uniform brightness.

[0112] FIG. 14 illustrates driving waveforms supplied to the switching unit, the current sink unit, the precharging unit, and the pixel illustrated in FIG. 13.

[0113] The voltage value of the data signal DS supplied to the pixel 140 will be described in detail with reference to FIGs. 13 and 14. First, the scan signal is supplied to the (n-1)th scan line Sn-1. When the scan signal is supplied to the (n-1)th scan line Sn-1, the third and fifth transistors M3 and M5 are turned on. Then, the voltage value obtained by subtracting the threshold voltage of the fourth transistor M4 from the first power source ELVDD is applied to the second node N2 and the voltage of the reference power source Vref is applied to the first node N1. At this time, the voltage corresponding to the voltage drop of the first power source ELVDD and the threshold voltage of the fourth transistor M4 are charged in the second capacitor C2.

[0114] The voltages applied to the first node N1 and the second node N2 may be represented by EQUATION 1. However, in a period between the point of time where the scan signal supplied to the (n-1)th scan line Sn-1 is turned off and the point of time where the scan signal is supplied to the nth scan line Sn, the first and second nodes N1 and N2 float. Therefore, the value of the voltage charged in the second capacitor C2 does not change.

[0115] Then, the scan signal is supplied to the nth scan line Sn so that the first and second transistors M1 and M2 are turned on. In the portion of the 0th period when the scan signal is supplied to the nth scan line Sn, the 15th and 11th transistors M15 and M11 are also turned on by their respective control signals CS4 and CS1. When the 15th and 11th transistors M15 and M11 are turned on, the precharging voltage Vp is supplied to the first node N1 via the 15th transistor M15, the first buffer 270j, the 11th transistor M11, the data line Dj, and the first transistor M1. As a result, the voltage corresponding to the precharging voltage Vp is charged in the first capacitor C1.

[0116] Here, the value of the precharging voltage Vp is determined to correspond to the value of the current source Imax. The value of the precharging voltage Vp is set so that a current corresponding to the current source Imax can flow through the fourth transistor M4. That is, the value of the precharging voltage Vp is set so that the current obtained when the pixel 1401 emits light with the maximum brightness flows through the fourth transistor M4.

[0117] Then, the 12th and 13th transistors M12 and M13 are turned on in the first period of the horizontal period H by their common control signal CS2. When the 12th and 13th transistors M12 and M13 are turned on, the current that flows

through the current source Imax via the first power source ELVDD, the fourth transistor M4, the second transistor M2, the data line Dj, and the 13th transistor M13 sinks into this current source.

[0118] At this time, the current of the current source Imax through the fourth transistor M4, is obtained by EQUATION 2. The voltage applied to the second node N2 when the current obtained by EQUATION 2 flows through the fourth transistor M4 may be represented by EQUATION 3.

[0119] The voltage applied to the first node N1 by the coupling of the second capacitor C2 may be represented by EQUATION 4.

[0120] The voltage V_{N1} applied to the first node N1 is ideally the same as the voltage V_{N3} applied to the third node N3 and the voltage V_{N4} applied to the fourth node N4. That is, when the current is sunk by the current source Imax, the voltage obtained by EQUATION 4 is applied to the fourth node N4. On the other hand, since a predetermined voltage is charged in the first capacitor C1 by the precharging voltage Vp in the 0th period, it is possible to minimize the length of time for which the voltage obtained by EQUATION 4 is applied to the fourth node N4.

[0121] As illustrated in EQUATION 4, the voltage applied to the third and fourth nodes N3 and N4 is affected by the electron mobility of the transistors included in the pixel 140 the current from which sinks. Therefore, the voltage value applied to the third and fourth nodes N3 and N4 when the current is sunk by the current source Imax varies in each of the pixels 140 (or 1401 or 1402).

[0122] On the other hand, when the voltage obtained by EQUATION 4 is applied to the fourth node N4, the voltage V_{diff} across the voltage generator 240j may be represented by EQUATION 5.

[0123] When the DAC 250j selects the hth (h is a natural number no more than f) gray scale voltage among f (f is a natural number) gray scale voltages in response to the data Data, the voltage Vb supplied to the first buffer 270j may be represented by EQUATION 6.

[0124] However, after the current sinks in the first period so that the voltage obtained by EQUATION 4 is charged in the third capacitor C3, the 12th and 13th transistors M12 and M13 are turned off and the 14th and 11th transistors M14 and M11 are turned on in the second period. At this time, the third capacitor C3 maintains the voltage charged in the capacitor. Therefore, the voltage value of the third node N3 may be maintained as illustrated in EQUATION 4.

[0125] Since the 14th and 11th transistors M14 and M11 are turned on in the second period of the horizontal period H, the data signal selected by the DAC 250j is supplied to the first node N1 via the first buffer 270j, the data line Dj, and the first transistor M1. That is, the voltage obtained by EQUATION 6 is supplied to the first node N1. The voltage applied to the second node N2 by the coupling of the second capacitor C2 may be represented by EQUATION 7.

[0126] At this time, the current that flows via the fourth transistor M4 may be represented by EQUATION 8.

[0127] Referring to EQUATION 8, according to the present invention, the current that flows through the fourth transistor M4 is determined by the gray scale voltage generated by the voltage generator 240j. That is, according to the present invention, the current determined by the gray scale voltage can flow to the fourth transistor M4 regardless of the threshold voltage and electron mobility of the fourth transistor M4. Therefore, it is possible to display images with a substantially uniform brightness. Also, according to the present invention, since the precharging voltage Vp is supplied to the pixel 140 (or pixel 1401 or pixel 1402) in the 0th period, it is possible to reduce the driving time of the first period in which the current sinks.

[0128] As described above, according to the data driver of the embodiments of the present invention, the organic light emitting display device using the data driver, and the method of driving the organic light emitting display device, since the values of the gray scale voltages generated by the voltage generator are reset using the compensation voltage generated when the current from the pixel sinks and the reset gray scale voltages are supplied to the pixel the current from which sinks, it is possible to display images with a substantially uniform brightness regardless of the electron mobility of the transistors. According to the present invention, since the precharging voltage is supplied before the currents sink, it is possible to reduce the time for which the currents sink and to stably drive the organic light emitting display device.

Claims

1. A organic light emitting display device comprising a plurality of pixels (140), each pixel (140, 1421) comprising:

first to sixth transistors (M1, M2, M3, M4, M5, M6), first and second capacitors (C1, C2), first and second nodes (N1, N2),
wherein each of the transistors (M1, M2, M3, M4, M5, M6) comprises a gate electrode and first and second main electrodes and each of the capacitors (C1, C2) comprises a first and a second connector,
the gate electrodes of the first and second transistor (M1,M2) being connected to a scan line (Sn),
the gate electrodes of the third and fifth transistors (M3, M5) being connected to the previous scan line (Sn-1),
the gate electrode of the sixth transistor (M6) being connected to an emission control line (En),
the second node (N2) being connected to the second connector of the second capacitor (C2), the gate electrode

of the fourth transistor (M4) and the first main electrode of the fifth transistor (M5),
the first node (N1) being connected to the first connector of the first capacitor (C1), the first connector of the second capacitor (C2), the first main electrode of the third transistor (M3) and the second main electrode of the first transistor (M1),
the first main electrode of the first transistor (M1) and the first main electrode of the second transistor (M2) being connected to a data line (Dj),
the second main electrode of the second transistor (M2) being connected to the second main electrode of the sixth transistor (M6), the second main electrode of the fifth transistor (M5) and the first main electrode of the fourth transistor (M4),
the second main electrode of the third transistor (M3) configured to be connected to a reference power source (Vref),
the second main electrode of the fourth transistor (M4) being connected to the second connector of the first capacitor (C1) and configured to be connected to a first power source (ELVDD),
the first main electrode of the sixth transistor (M6) being connected to an organic light emitting diode (OLED) which is configured to be connected to a second power source (ELVSS);
a data driver comprising:

a current sink unit (280j) adapted to control flow of a predetermined current being generated by a current source (Imax) through a data line (Dj) connected to the current sink unit (280j) and to generate a compensation voltage in response to the predetermined current;
a voltage generator (240j) directly or indirectly connected to the current sink unit (280j) and adapted to supply gray scale voltages in response to the compensation voltage;
a digital-to-analog converter (250j) being adapted to select one gray scale voltage among the gray scale voltages as a data signal in response to a k-bit data supplied from outside to the data driver; and

a precharging unit (300j) for supplying a precharging voltage to a pixel coupled to the data line in a 0^{th} period before a first period, the precharging unit (300j) being located between the digital-to-analog converter (250j) and a switching unit (290j) and comprising:

a precharging voltage source (Vp);
a fifteenth transistor (M15) located between the precharging voltage source (Vp) and the switching unit (290j); and
a fourteenth transistor (M14) located between the digital-to-analog converter (250j) and the switching unit (290j) and for being turned on in a second period of each horizontal period (H),
wherein each horizontal period includes the 0^{th} period, the first period, and the second period;
the digital-to-analog converter (250j) being connected to the voltage generator (240j) and further being connected directly or indirectly to the switching unit (290j); and
the switching unit (290j) adapted to supply the data signal to the data line (Dj),the switching unit (290j) being directly or indirectly connected to the digital-to-analog converter (250j) and the data line (Dj);

the current sink unit (280j) comprising:

twelfth and thirteenth transistor (M12, M13), the current source (Imax), a third node (N3) and a third capacitor (C3),
each of the twelfth and thirteenth transistor (M12,M13) comprising a gate electrode and first and second main electrodes,
the current source (Imax) being adapted to receive the predetermined current and being connected to the first main electrode of the thirteenth transistor (M13),
the third capacitor (C3) being adapted to store the compensation voltage,
the third capacitor (C3) being connected to the third node (N3) and a ground voltage source (GND),
the gate electrode of the twelfth transistor (M12) being connected to the gate electrode of the thirteenth transistor (M13) and a command signal line (CS2) being adapted to switch on the twelfth and thirteenth transistor during the first period being part of the horizontal period (H),
the third node (N3) being connected to the first main electrode of the twelfth transistor (M12), the third capacitor (C3) and the voltage generator (240j),
the second main electrode of the twelfth transistor (M12) being connected to the second main electrode of the thirteenth transistor (M13) and the data line (Dj),
the data line (Dj) connecting the switching unit (290j) and the current sink unit (280j).

2. A organic light emitting display device comprising a plurality of pixels (140), each pixel (140, 1422) comprising:

first to sixth transistors (M1', M2', M3', M4', M5', M6'), first and second capacitors (C1', C2'), first and second nodes (N1', N2'),
wherein each of the transistors (M1', M2', M3', M4', M5', M6') comprises a gate electrode and first and second main electrodes and each of the capacitors (C1', C2') comprises a first and second connector,
the gate electrodes of the first and second transistor (M1',M2') being connected to a scan line (Sn),
the gate electrodes of the third and fifth transistors (M3', M5') being connected to the previous scan line (Sn-1),
the gate electrode of the sixth transistor (M6') being connected to an emission control line (En),
the second node (N2') being connected to the first connector of the first capacitor (C1'), the second connector of the second capacitor (C2'), the gate electrode of the fourth transistor (M4') and the first main electrode of the fifth transistor (M5'),
the first node (N1') being connected to the first connector of the second capacitor (C2'), the first main electrode of the third transistor (M3') and
the second main electrode of the first transistor (M1'),
the first main electrode of the first transistor (M1') and the second main electrode of the second transistor (M2') being connected to a data line (Dj),
the first main electrode of the second transistor (M2') being connected to the second main electrode of the sixth transistor (M6'), the second main electrode of the fifth transistor (M5') and the first main electrode of the fourth transistor (M4'),
the second main electrode of the third transistor (M3') configured to be connected to a reference power source (Vref),
the second main electrode of the fourth transistor (M4') being connected to the second connector of the first capacitor (C1') and being configured to be connected to an first power source (ELVDD),
the first main electrode of the sixth transistor (M6') being connected to an organic light emitting diode (OLED) which is configured to be connected to an second power source (ELVSS);
a data driver comprising:

a current sink unit (280j) adapted to control flow of a predetermined current being generated by a current source (Imax) through a data line (Dj) connected to the current sink unit (280j) and to generate a compensation voltage in response to the predetermined current,
a voltage generator (240j) directly or indirectly connected to the current sink unit (280j) and adapted to supply gray scale voltages in response to the compensation voltage,
a digital-to-analog converter (250j) being adapted to select one gray scale voltage among the gray scale voltages as a data signal in response to a k-bit supplied from outside to the data driver; and

a precharging unit (300j) for supplying a precharging voltage to a pixel coupled to the data line in a 0^{th} period before a first period, the precharging unit (300j) being located between the digital-to-analog converter (250j) and a switching unit (290j) and comprising:

a precharging voltage source (Vp);
a fifteenth transistor (M15) located between the precharging voltage source (Vp) and the switching unit (290j); and
a fourteenth transistor (M14) located between the digital-to-analog converter (250j) and the switching unit (290j) and for being turned on in a second period of each horizontal period (H),
wherein each horizontal period includes the 0^{th} period, the first period, and the second period;
the digital-to-analog converter (250j) being connected to the voltage generator (240j) and further being connected directly or indirectly to the switching unit (290j); and
the switching unit (290j) adapted to supply the data signal to the data line (Dj),
the switching unit (290j) being directly or indirectly connected to the digital-to-analog converter (250j) and the data line (Dj);

the current sink unit (280j) comprising:

twelfth and thirteenth transistor (M12, M13), the current source (Imax), a third node (N3) and a third capacitor (C3),
each of the twelfth and thirteenth transistor (M12,M13) comprising a gate electrode and first and second main electrodes,

the current source (Imax) being adapted to receive the predetermined current and being connected to the first main electrode of the thirteenth transistor (M13),
the third capacitor (C3) being adapted to store the compensation voltage,
the third capacitor (C3) being connected to the third node (N3) and a ground voltage source (GND),
the gate electrode of the twelfth transistor (M12) being connected to the gate electrode of the thirteenth transistor (M13) and a command signal line (CS2) being adapted to switch on the twelfth and thirteenth transistor during the first period being part of the horizontal period (H),
the third node (N3) being connected to the first main electrode of the twelfth transistor (M12), the third capacitor (C3) and the voltage generator (240j),
the second main electrode of the twelfth transistor (M12) being connected to the second main electrode of the thirteenth transistor (M13) and the data line (Dj),
the data line (Dj) connecting the switching unit (290j) and the current sink unit (280j).

3. The data driver as claimed in one of claims 1 or 2, wherein the current sink unit (280) is adapted to receive the predetermined current in the first period, the first period being a part of the horizontal period (H).

4. The data driver as claimed in one of claims 1 through 3, wherein a value of the predetermined current is equal to a value of a current that flows when a pixel connected to the data line (Dj) emits light with a maximum brightness.

5. The data driver as claimed in one of claims 3 or 4, wherein the switching unit (290j) is adapted to couple the data line (Dj) and the digital-to-analog converter (250j) to each other in the second period of the horizontal period (H) occurring after the first period.

6. The data driver as claimed in claim 5,
wherein the switching unit (290j') comprises two transistors (M11,M14) being
coupled to each other in a form of a transmission gate or wherein the switching unit comprises an eleventh transistor (M11) which is controlled by a control signal (CS1).

7. The data driver as claimed in one of the preceding claims, wherein the voltage generator (240j) comprises a plurality of voltage dividing resistors coupled between a first terminal and a second terminal for generating the gray scale voltages.

8. The data driver as claimed in claim 7,
wherein the first terminal is connected to a reference power source (Vref) adapted to provide a reference voltage to the first terminal, and
wherein the second terminal is connected to the current sink unit (280j) adapted to provide the compensation voltage to the second terminal.

9. The data driver as claimed in one of the preceding claims, further comprising:

a first buffer (270j) located between the digital-to-analog converter (250j) and the switching unit (290j); and
a second buffer (260j) located between the current sink (280j) unit and the voltage generator (240j).

10. The data driver as claimed in one of the preceding claims, further comprising:

a shift register unit (210) including shift registers adapted to generate sampling signals;
a sampling latch unit (220) including a plurality of sampling latches adapted to receive the data supplied to the data driver in response to the sampling signals; and
a holding latch unit (230) including holding latches adapted to receive and store the data stored in the sampling latches and to supply the data stored in the holding latches to the digital-to-analog converter (250).

11. The data driver as claimed in claim 10, further comprising a level shifter unit (310) for increasing a voltage level of the data stored in the holding latches to supply the data to the digital-to-analog converter (250).

12. The data driver as claimed in one of the preceding claims, wherein the precharging voltage source (Vp) is adapted to provide the precharge voltage that corresponds to a voltage value of the data line (Dj) resulting from the predetermined current being pulled from a pixel.

13. The data driver as claimed in one of the claims 1 to 5 or 7 to 12, wherein the switching unit (290j) comprises an eleventh transistor (M11) for electrically coupling the data line (Dj) and the precharging unit (300j) to each other in the 0^{th} period and the second period.

14. A method of driving an organic light emitting display device according to one of the claims 1 or 2, the method comprising the steps of:

controlling predetermined currents to flow in data lines (Dj) coupled to pixels (140, 1421, 1422);
generating compensation voltages corresponding to the predetermined currents;
resetting values of gray scale voltages using the compensation voltages;
selecting one voltage among the gray scale voltages corresponding to bit values of data supplied to the data driver from the outside;
and supplying the selected voltage to the data lines (Dj),
the method being **characterised by** a step of supplying a predetermined precharging voltage to a pixel (140, 1421, 1422) selected by a scan signal.

15. The method as claimed in claim 15, wherein the predetermined currents are equal to currents that flow through organic light emitting diodes (OLED) within the pixels (140, 1421, 1422) when the pixels emit light with a maximum brightness.

16. The method as claimed in one of the claims 15 or 16, wherein the precharging voltage (Vp) corresponds to a voltage value of the data line (Dj) connected to the pixel (140, 1421, 1422) selected by a scan signal resulting from the predetermined current being pulled from the pixel (140, 1421, 1422).

Patentansprüche

1. Organische lichtemittierende Anzeigevorrichtung umfassend eine Vielzahl von Pixeln (140), wobei jedes Pixel (140, 1421) umfasst:

erste bis sechste Transistoren (M1, M2, M3, M4, M5, M6), erste und zweite Kondensatoren (C1, C2), erste und zweite Knoten (N 1, N2),
wobei jeder der Transistoren (M1, M2, M3, M4, M5, M6) eine Gate-Elektrode sowie erste und zweiten Hauptelektroden umfasst und jeder der Kondensatoren (C1, C2) einen ersten und einen zweiten Verbinder umfasst,
die Gate-Elektroden des ersten und zweiten Transistors (M1, M2) mit einer Abtastzeile (Sn) verbunden sind,
die Gate-Elektroden des dritten und fünften Transistors (M3, M5) mit der vorherigen Abtastzeile (Sn-1) verbunden sind,
die Gate-Elektrode des sechsten Transistors (M6) mit einer Emissionssteuerleitung (En) verbunden ist,
der zweiten Knoten (N2) mit dem zweiten Verbinder des zweiten Kondensators (C2),
der Gate-Elektrode des vierten Transistors (M4) und der ersten Hauptelektrode des fünften Transistors (M5) verbunden ist,
der erste Knoten (N1) mit dem ersten Verbinder des ersten Kondensators (C1), dem ersten Verbinder des zweiten Kondensators (C2), der ersten Hauptelektrode des dritten Transistors (M3) und der zweiten Hauptelektrode des ersten Transistors (M1) verbunden ist,
die erste Hauptelektrode des ersten Transistors (M1) und die erste Hauptelektrode des zweiten Transistors (M2) mit einer Datenleitung (Dj) verbunden sind,
die zweite Hauptelektrode des zweiten Transistors (M2) mit der zweiten Hauptelektrode des sechsten Transistors (M6), der zweiten Hauptelektrode des fünften Transistors (M5) und der ersten Hauptelektrode des vierten Transistors (M4) verbunden ist,
die zweite Hauptelektrode des dritten Transistors (M3) derart ausgebildet ist, dass sie mit einer Referenzstromquelle (Vref) verbunden ist,
die zweite Hauptelektrode des vierten Transistors (M4) mit dem zweiten Verbinder des ersten Kondensators (C1) verbunden und derart ausgebildet ist, dass sie mit einer ersten Stromquelle (ELVDD) verbunden ist,
die erste Hauptelektrode des sechsten Transistors (M6) mit einer organischen lichtemittierenden Diode (OLED) verbunden ist, die derart ausgebildet ist, dass sie mit einer zweiten Stromquelle (ELVSS) verbunden ist;
einen Datentreiber, umfassend:

eine Stromsenkeeinheit (280j), die ausgebildet ist zum Steuern eines Flusses eines vorbestimmten, von

einer Stromquelle (Imax) erzeugten Stroms durch eine mit der Stromsenkeeinheit (280j) verbundene Datenleitung (Dj) sowie zum Erzeugen einer Ausgleichsspannung als Reaktion auf den vorbestimmten Strom;
einen Spannungsgenerator (240j), der direkt oder indirekt mit der Stromsenkeeinheit (280j) verbunden und zum Zuführen von Grauskala-Spannungen als Reaktion auf die Ausgleichsspannung ausgebildet ist,
einen Digital-Analog-Wandler (250j), der ausgebildet ist zum Auswählen einer Grauskala-Spannung unter den Grauskala-Spannungen als ein Datensignal als Reaktion auf k-Bit-Daten, die dem Datentreiber von außen zugeführt werden; und

eine Voraufladungseinheit (300j) zum Zuführen einer Voraufladungsspannung an ein Pixel, das mit der Datenleitung in einer 0'ten Periode vor einer ersten Periode gekoppelt ist, wobei sich die Voraufladungseinheit (300j) zwischen dem Digital-Analog-Wandler (250j) und einer Schalteinheit (290j) befindet und umfasst:

eine Voraufladungsspannungsquelle (Vp);
einen fünfzehnten Transistor (M 15), der sich zwischen der Voraufladungsspannungsquelle (Vp) und der Schalteinheit (290j) befindet; und
einen vierzehnten Transistor (M14), der sich zwischen dem Digital-Analog-Wandler (250j) und der Schalteinheit (290j) befindet und in einer zweiten Periode jeder Horizontalperiode (H) eingeschaltet wird,
wobei jede Horizontalperiode die 0'te Periode, die erste Periode und die zweite Periode umfasst;
der Digital-Analog-Wandler (250j) mit dem Spannungsgenerator (240j) verbunden ist und weiter direkt oder indirekt mit der Schalteinheit (290j) verbunden ist; und
die Schalteinheit (290j) ausgebildet ist zum Zuführen des Datensignals an die Datenleitung (Dj), wobei die Schalteinheit (290j) direkt oder indirekt mit dem Digital-Analog-Wandler (250j) und der Datenleitung (Dj) verbunden ist;

wobei die Stromsenkeeinheit (280j) umfasst:

einen zwölften und dreizehnten Transistor (M12, M13), die Stromquelle (Imax), einen dritten Knoten (N3) und einen dritten Kondensator (C3),
wobei der zwölfte und dreizehnte Transistor (M12, M13) jeweils eine Gate-Elektrode sowie erste und zweite Hauptelektroden umfasst,
die Stromquelle (Imax) ausgebildet ist zum Empfangen des vorbestimmten Stroms und mit der ersten Hauptelektrode des dreizehnten Transistors (M13) verbunden ist,
der dritte Kondensator (C3) ausgebildet ist zum Speichern der Ausgleichsspannung,
der dritte Kondensator (C3) mit dem dritten Knoten (N3) und einer Erdspannungsquelle (GND) verbunden ist,
die Gate-Elektrode des zwölften Transistors (M12) mit der Gate-Elektrode des dreizehnten Transistors (M13) verbunden ist und eine Befehlssignalleitung (CS2) ausgebildet ist zum Einschalten des zwölften und dreizehnten Transistors während der ersten Periode, die Teil der Horizontalperiode (H) ist,
der dritte Knoten (N3) mit der ersten Hauptelektrode des zwölften Transistors (M12),
dem dritten Kondensator (C3) und dem Spannungsgenerator (240j) verbunden ist,
die zweite Hauptelektrode des zwölften Transistors (M12) mit der zweiten Hauptelektrode des dreizehnten Transistors (M13) und der Datenleitung (Dj) verbunden ist,
wobei die Datenleitung (Dj) die Schalteinheit (290j) und die Stromsenkeeinheit (280j) verbindet.

2. Organische lichtemittierende Anzeigevorrichtung umfassend eine Vielzahl von Pixeln (140), wobei jedes Pixel (140, 1422) umfasst:

erste bis sechste Transistoren (M1', M2', M3', M4', M5', M6'), erste und zweite Kondensatoren (C1', C2'), erste und zweite Knoten (N1', N2'),
wobei jeder der Transistoren (M1', M2', M3', M4', M5', M6') eine Gate-Elektrode sowie erste und zweiten Hauptelektroden umfasst und jeder der Kondensatoren (C1', C2') einen ersten und einen zweiten Verbinder umfasst,
die Gate-Elektroden des ersten und zweiten Transistors (M1', M2') mit einer Abtastzeile (Sn) verbunden sind,
die Gate-Elektroden des dritten und fünften Transistors (M3', M5') mit der vorherigen Abtastzeile (Sn-1) verbunden sind,
die Gate-Elektrode des sechsten Transistors (M6') mit einer Emissionssteuerleitung (En) verbunden ist,
der zweiten Knoten (N2') mit dem ersten Verbinder des ersten Kondensators (C1'),
dem zweiten Verbinder des zweiten Kondensators (C2'), der Gate-Elektrode des vierten Transistors (M4') und der ersten Hauptelektrode des fünften Transistors (M5') verbunden ist,

der erste Knoten (N1') mit dem ersten Verbinder des zweiten Kondensators (C2'),
der ersten Hauptelektrode des dritten Transistors (M3') und der zweiten Hauptelektrode des ersten Transistors (M1') verbunden ist,
die erste Hauptelektrode des ersten Transistors (M1') und die zweite Hauptelektrode des zweiten Transistors (M2') mit einer Datenleitung (Dj) verbunden sind,
die erste Hauptelektrode des zweiten Transistors (M2') mit der zweiten Hauptelektrode des sechsten Transistors (M6'), der zweiten Hauptelektrode des fünften Transistors (M5') und der ersten Hauptelektrode des vierten Transistors (M4') verbunden ist,
die zweite Hauptelektrode des dritten Transistors (M3') derart ausgebildet ist, dass sie mit einer Referenzstromquelle (Vref) verbunden ist,
die zweite Hauptelektrode des vierten Transistors (M4') mit dem zweiten Verbinder des ersten Kondensators (C1') verbunden und derart ausgebildet ist, dass sie mit einer ersten Stromquelle (ELVDD) verbunden ist,
die erste Hauptelektrode des sechsten Transistors (M6') mit einer organischen lichtemittierenden Diode (OLED) verbunden ist, die derart ausgebildet ist, dass sie mit einer zweiten Stromquelle (ELVSS) verbunden ist;
einen Datentreiber, umfassend:

eine Stromsenkeeinheit (280j), die ausgebildet ist zum Steuern eines Flusses eines vorbestimmten, von einer Stromquelle (Imax) erzeugten Stroms durch eine mit der Stromsenkeeinheit (280j) verbundene Datenleitung (Dj) sowie zum Erzeugen einer Ausgleichsspannung als Reaktion auf den vorbestimmten Strom;
einen Spannungsgenerator (240j), der direkt oder indirekt mit der Stromsenkeeinheit (280j) verbunden und zum Zuführen von Grauskala-Spannungen als Reaktion auf die Ausgleichsspannung ausgebildet ist,
einen Digital-Analog-Wandler (250j), der ausgebildet ist zum Auswählen einer Grauskala-Spannung unter den Grauskala-Spannungen als ein Datensignal als Reaktion auf ein k-Bit, das dem Datentreiber von außen zugeführt wird; und

eine Voraufladungseinheit (300j) zum Zuführen einer Voraufladungsspannung an ein Pixel, das mit der Datenleitung in einer 0'ten Periode vor einer ersten Periode gekoppelt ist, wobei sich die Voraufladungseinheit (300j) zwischen dem Digital-Analog-Wandler (250j) und einer Schalteinheit (290j) befindet und umfasst:

eine Voraufladungsspannungsquelle (Vp);
einen fünfzehnten Transistor (M 15), der sich zwischen der Voraufladungsspannungsquelle (Vp) und der Schalteinheit (290j) befindet; und
einen vierzehnten Transistor (M14), der sich zwischen dem Digital-Analog-Wandler (250j) und der Schalteinheit (290j) befindet und in einer zweiten Periode jeder Horizontalperiode (H) eingeschaltet wird,
wobei jede Horizontalperiode die 0'te Periode, die erste Periode und die zweite Periode umfasst;
der Digital-Analog-Wandler (250j) mit dem Spannungsgenerator (240j) verbunden ist und weiter direkt oder indirekt mit der Schalteinheit (290j) verbunden ist; und
die Schalteinheit (290j) ausgebildet ist zum Zuführen des Datensignals an die Datenleitung (Dj), wobei die Schalteinheit (290j) direkt oder indirekt mit dem Digital-Analog-Wandler (250j) und der Datenleitung (Dj) verbunden ist;

wobei die Stromsenkeeinheit (280j) umfasst:

einen zwölften und dreizehnten Transistor (M12, M13), die Stromquelle (Imax), einen dritten Knoten (N3) und einen dritten Kondensator (C3),
wobei der zwölfte und dreizehnte Transistor (M12, M13) jeweils eine Gate-Elektrode sowie erste und zweite Hauptelektroden umfasst,
die Stromquelle (Imax) ausgebildet ist zum Empfangen des vorbestimmten Stroms und mit der ersten Hauptelektrode des dreizehnten Transistors (M13) verbunden ist,
der dritte Kondensator (C3) ausgebildet ist zum Speichern der Ausgleichsspannung,
der dritte Kondensator (C3) mit dem dritten Knoten (N3) und einer Erdspannungsquelle (GND) verbunden ist,
die Gate-Elektrode des zwölften Transistors (M12) mit der Gate-Elektrode des dreizehnten Transistors (M13) verbunden ist und eine Befehlssignalleitung (CS2) ausgebildet ist zum Einschalten des zwölften und dreizehnten Transistors während der ersten Periode, die Teil der Horizontalperiode (H) ist,
der dritte Knoten (N3) mit der ersten Hauptelektrode des zwölften Transistors (M12),
dem dritten Kondensator (C3) und dem Spannungsgenerator (240j) verbunden ist,
die zweite Hauptelektrode des zwölften Transistors (M12) mit der zweiten Hauptelektrode des dreizehnten Transistors (M13) und der Datenleitung (Dj) verbunden ist,

wobei die Datenleitung (Dj) die Schalteinheit (290j) und die Stromsenkeeinheit (280j) verbindet.

3. Datentreiber nach einem der Ansprüche 1 oder 2, wobei die Stromsenkeeinheit (280) ausgebildet ist, den vorbestimmten Strom in der ersten Periode zu empfangen, wobei die erste Periode ein Teil der Horizontalperiode (H) ist.

4. Datentreiber nach einem der Ansprüche 1 bis 3, wobei ein Wert des vorbestimmten Stroms gleich einem Wert eines Stroms ist, der fließt, wenn ein mit der Datenleitung (Dj) verbundenes Pixel Licht mit einer maximalen Helligkeit abgibt.

5. Datentreiber nach einem der Ansprüche 3 oder 4, wobei die Schalteinheit (290j) ausgebildet ist, die Datenleitung (Dj) und den Digital-Analog-Wandler (250j) in der nach der ersten Periode erfolgenden zweiten Periode der Horizontalperiode (H) miteinander zu koppeln.

6. Datentreiber nach Anspruch 5,
wobei die Schalteinheit (290j) zwei Transistoren (M11, M14) umfasst, die in Form eines Übertragungsgatters miteinander gekoppelt sind,
oder wobei die Schalteinheit einen elften Transistor (M11) umfasst, der von einem Steuersignal (CS1) gesteuert wird.

7. Datentreiber nach einem der vorstehenden Ansprüche, wobei der Spannungsgenerator (240j) eine Vielzahl von spannungsteilenden Widerständen umfasst, die zwischen einen ersten Anschluss und einen zweiten Anschluss zum Erzeugen der Grauskala-Spannungen geschaltet sind.

8. Datentreiber nach Anspruch 7,
wobei der erste Anschluss mit einer Referenzstromquelle (Vref) verbunden ist, die ausgebildet ist, dem ersten Anschluss eine Referenzspannung bereitzustellen, und wobei der zweite Anschluss mit der Stromsenkeeinheit (280j) verbunden ist, die ausgebildet ist, dem zweiten Anschluss die Ausgleichsspannung bereitzustellen.

9. Datentreiber nach einem der vorstehenden Ansprüche, weiterhin umfassend:

einen ersten Puffer (270j), der sich zwischen dem Digital-Analog-Wandler (250j) und der Schalteinheit (290j) befindet; und
einen zweiten Puffer (260j), der sich zwischen der Stromsenkeeinheit (280j) und dem Spannungsgenerator (240j) befindet.

10. Datentreiber nach einem der vorstehenden Ansprüche, weiterhin umfassend:

eine Schieberegistereinheit (210) enthaltend Schieberegister, die zum Erzeugen von Abtastsignalen ausgebildet sind;
eine Abtast-Latch-Einheit (220) enthaltend eine Vielzahl von Abtast-Latches, die zum Empfangen der dem Datentreiber als Reaktion auf die Abtastsignale zugeführten Daten ausgebildet sind; und
eine Halte-Latch-Einheit (230) enthaltend Halte-Latches, die zum Empfangen und Speichern der in den Abtast-Latches gespeicherten Daten sowie zum Zuführen der in den Halte-Latches gespeicherten Daten an den Digital-Analog-Wandler (250) ausgebildet sind.

11. Datentreiber nach Anspruch 10, weiterhin umfassend eine Pegelumsetzereinheit (310) zum Erhöhen eines Spannungspegels der in den Halte-Latches gespeicherten Daten zum Zuführen der Daten an den Digital-Analog-Wandler (250).

12. Datentreiber nach einem der vorstehenden Ansprüche, wobei die Voraufladungsspannungsquelle (Vp) ausgebildet ist, die Voraufladungsspannung bereitzustellen, die einem Spannungswert der Datenleitung (Dj), der sich aus dem von einem Pixel abgezogenen vorbestimmten Strom ergibt, entspricht.

13. Datentreiber nach einem der Ansprüche 1 bis 5 oder 7 bis 12, wobei die Schalteinheit (290j) einen elften Transistor (M11) zum elektrischen Koppeln der Datenleitung (Dj) und der Voraufladungseinheit (300j) miteinander in der 0'ten Periode und der zweiten Periode umfasst.

14. Verfahren zum Ansteuern einer organischen lichtemittierenden Anzeigevorrichtung nach einem der Ansprüche 1 oder 2, wobei das Verfahren folgende Schritte umfasst:

Steuern vorbestimmter Ströme zum Fließen in mit Pixeln (140, 1421, 1422) gekoppelten Datenleitungen (Dj);
Erzeugen von Ausgleichsspannungen entsprechend den vorbestimmten Strömen;
Zurücksetzen von Werten von Grauskala-Spannungen unter Verwendung der Ausgleichsspannungen;
Auswählen einer Spannung unter den Grauskala-Spannungen entsprechend Bit-Werten von Daten, die dem Datentreiber von außen zugeführt werden;
und Zuführen der ausgewählten Spannung an die Datenleitungen (Dj),
wobei das Verfahren **gekennzeichnet ist durch** einen Schritt des Zuführens einer vorbestimmten Voraufladungsspannung an ein von einem Abtastsignal ausgewähltes Pixel (140, 1421, 1422).

15. Verfahren nach Anspruch 14, wobei die vorbestimmten Ströme gleich Strömen sind, die durch organische lichtemittierende Dioden (OLED) innerhalb der Pixel (140, 1421, 1422) fließen, wenn die Pixel Licht mit einer maximalen Helligkeit abgeben.

16. Verfahren nach einem der Ansprüche 14 oder 15, wobei die Voraufladungsspannung (Vp) einem Spannungswert der Datenleitung (Dj) entspricht, die mit dem Pixel (140, 1421, 1422) verbunden ist, das von einem Abtastsignal ausgewählt wird, das sich aus dem von dem Pixel (140, 1421, 1422) abgezogenen vorbestimmten Strom ergibt.

Revendications

1. Dispositif d'affichage électroluminescent organique comprenant une pluralité de pixels (140), chaque pixel (140, 1421) comprenant :

d' un premier à un sixième transistor (M1, M2, M3, M4, M5, M6), un premier et un deuxième condensateur (C1, C2), un premier et un deuxième noeud (N1, N2),
dans lequel chacun des transistors (M1, M2, M3, M4, M5, M6) comprend une électrode de grille et des première et deuxième électrodes principales et chacun des condensateurs (C1, C2) comprend des premier et deuxième connecteurs,
les électrodes de grille des premier et deuxième transistors (M1, M2) étant reliées à une ligne (Sn) de balayage,
les électrodes de grille des troisième et cinquième transistors (M3, M5) étant reliées à une ligne de balayage précédente (Sn-1),
l'électrode grille du sixième transistor (M6) étant reliée à une ligne (En) de commande d'émission ;
le deuxième noeud (N2) étant relié au deuxième connecteur du deuxième condensateur (C2), à l'électrode de grille du quatrième transistor (M4) et à la première électrode principale du cinquième transistor (M5),
le premier noeud (N1) étant relié au premier connecteur du premier condensateur (C1), au premier connecteur du deuxième condensateur (C2), à la première électrode principale du troisième transistor (M3) et à la deuxième électrode principale du premier transistor (M1),
la première électrode principale du premier transistor (M1) et la première électrode principale du deuxième transistor (M2) étant reliées à une ligne (Dj) de données,
la deuxième électrode principale du deuxième transistor (M2) étant reliée à la deuxième électrode principale du sixième transistor (M6), à la deuxième électrode principale du cinquième transistor (M5) et à la première électrode principale du quatrième transistor (M4),
la deuxième électrode principale du troisième transistor (M3) configurée pour être reliée à un bloc d'alimentation de référence (Vref),
la deuxième électrode principale du quatrième transistor (M4) étant reliée au deuxième connecteur du premier condensateur (C1) et configurée pour être reliée à un premier bloc d'alimentation (ELVDD),
la première électrode principale du sixième transistor (M6) étant reliée à une diode électroluminescente organique (OLED) qui est configurée pour être reliée à un deuxième bloc d'alimentation (ELVSS) ;
un circuit d'attaque de données comprenant :

une unité (280j) de circulation de courant adaptée pour commander un passage d'un courant prédéterminé qui est généré par une source de courant (Imax) à travers une ligne (Dj) de données reliée à l'unité (280j) de circulation de courant et pour générer une tension de compensation en réponse au courant prédéterminé ;
un générateur (240j) de tension relié directement ou indirectement à l'unité (280j) de circulation de courant et adapté pour fournir des tensions d'échelle de gris en réponse à la tension de compensation ;
un convertisseur numérique-analogique (250j) étant adapté pour sélectionner une tension d'échelle de gris parmi les tensions d'échelle de gris comme étant un signal de données en réponse à des données d'un kilobit fournies de l'extérieur du circuit d'attaque de données ; et

une unité (300j) de précharge destinée à fournir une tension de précharge à un pixel associé à la ligne de données dans une 0ème période avant une première période, l'unité (300j) de précharge étant située entre le convertisseur numérique-analogique (250j) et une unité (290j) de commutation et comprenant :

une source (Vp) de tension de précharge ;

un quinzième transistor (M15) situé entre la source (Vp) de tension de précharge et l'unité (290j) de commutation ; et
un quatorzième transistor (M14) situé entre le convertisseur numérique-analogique (250j) et l'unité (290j) de commutation et destiné à être activé dans une deuxième période de chaque période horizontale (H), dans lequel chaque période horizontale comporte la 0ème période, la première période et la deuxième période ;
le convertisseur numérique-analogique (250j) étant relié au générateur (240j) de tension et étant en outre relié directement ou indirectement à l'unité (290j) de commutation ; et
l'unité (290j) de commutation adaptée pour fournir le signal de données à la ligne (Dj) de données, l'unité (290j) de commutation étant reliée directement ou indirectement au convertisseur numérique-analogique (250j) et à la ligne (Dj) de données ;

l'unité (280j) de circulation de courant comprenant :

des douzième et treizième transistors (M12, M13), la source de courant (Imax), un troisième noeud (N3) et un troisième condensateur (C3),
chacun des douzième et treizième transistors (M12, M13) comprenant une électrode de grille et des première et deuxième électrodes principales,
la source de courant (Imax) étant adaptée pour recevoir le courant prédéterminé et étant reliée à la première électrode principale du treizième transistor (M13),
le troisième condensateur (C3) étant adapté pour stocker la tension de compensation,
le troisième condensateur (C3) étant relié au troisième noeud (N3) et à une source de tension de terre (GND),
l'électrode de grille du douzième transistor (M12) étant reliée à l'électrode de grille du treizième transistor (M13) et une ligne (CS2) de signal de commande étant adaptée pour commuter sur les douzième et treizième transistors durant la première période qui est une partie de la période horizontale (H),
le troisième noeud (N3) étant relié à la première électrode principale du douzième transistor (M12), au troisième condensateur (C3) et au générateur de tension (240j),
la deuxième électrode principale du douzième transistor (M12) étant reliée à la deuxième électrode principale du treizième transistor (M13) et à la ligne (Dj) de données,
la ligne (Dj) de données reliant l'unité (290j) de commutation et l'unité (280j) de circulation du courant.

2. Dispositif d'affichage électroluminescent organique comprenant une pluralité de pixels (140), chaque pixel (140, 1422) comprenant :

d'un premier à un sixième transistor (M1' , M2', M3', M4', M5', M6'), un premier et un deuxième condensateur (C1', C2'), un premier et un deuxième noeud (N1', N2'),
dans lequel chacun des transistors (M1', M2', M3', M4', M5', M6') comprend une électrode de grille et des première et deuxième électrodes principales et chacun des condensateurs (C1', C2') comprend un premier et un deuxième connecteur,
les électrodes de grille des premier et deuxième transistors (M1', M2') étant reliées à une ligne (Sn) de balayage,
les électrodes de grille des troisième et cinquième transistors (M3', M5') étant reliées à la ligne de balayage précédente (Sn-1),
l'électrode de grille du sixième transistor (M6') étant reliée à une ligne (En) de commande d'émission,
le deuxième noeud (N2') étant relié au premier connecteur du premier condensateur (Cl'), au deuxième connecteur du deuxième condensateur (C2'), à l'électrode grille du quatrième transistor (M4') et à la première électrode principale du cinquième transistor (M5'),
le premier noeud (N1') étant relié au premier connecteur du deuxième condensateur (C2'), à la première électrode principale du troisième transistor (M3') et à la deuxième électrode principale du premier transistor (M1'),
la première électrode principale du premier transistor (M1') et la deuxième électrode principale du deuxième transistor (M2') étant reliées à une ligne (Dj) de données,
la première électrode principale du deuxième transistor (M2') étant reliée à la deuxième électrode principale du sixième transistor (M6'), à la deuxième électrode principale du cinquième transistor (M5') et à la première

électrode principale du quatrième transistor (M4'),
la deuxième électrode principale du troisième transistor (M3') étant configurée pour être reliée à un bloc d'alimentation de référence (Vref),
la deuxième électrode principale du quatrième transistor (M4') étant reliée au deuxième connecteur du premier condensateur (C1') et étant configurée pour être reliée à un premier bloc d'alimentation (ELVDD),
la première électrode principale du sixième transistor (M6') étant reliée à une diode électroluminescente organique (OLED) qui est configurée pour être reliée à un deuxième bloc d'alimentation (ELVSS) ;
un circuit d'attaque de données comprenant :

une unité (280j) de circulation de courant adaptée pour commander un passage d'un courant prédéterminé qui est généré par une source de courant (Imax) à travers une ligne (Dj) de données reliée à l'unité (280j) de circulation du courant et pour générer une tension de compensation en réponse au courant prédéterminé,
un générateur de tension (240j) relié directement ou indirectement à l'unité (280j) de circulation du courant et adapté pour fournir des tensions d'échelle de gris en réponse à la tension de compensation,
un convertisseur numérique-analogique (250j) étant adapté pour sélectionner une tension d'échelle de gris entre les tensions d'échelle de gris comme étant un signal de données en réponse à un kilobit fourni de l'extérieur au circuit d'attaque de données ; et

une unité (300j) de précharge destinée à fournir une tension de précharge à un pixel couplé à la ligne de données dans une $0^{éme}$ période avant une première période, l'unité (300j) de précharge étant située entre le convertisseur numérique-analogique (250j) et l'unité (290j) de commutation et comprenant :

une source (Vp) de tension de précharge ;
un quinzième transistor (M15) situé entre la source (Vp) de tension de précharge et l'unité (290j) de commutation ; et
un quatorzième transistor (M14) situé entre le convertisseur numérique-analogique (250j) et l'unité (290j) de commutation et destiné à être activé dans une deuxième période de chaque période horizontale (H),
dans lequel chaque période horizontale comporte la $0^{ème}$ période, la première période et la deuxième période ;
le convertisseur numérique-analogique (250j) étant relié au générateur de tension (240j) et étant en outre relié directement ou indirectement à l'unité (290j) de commutation ; et
l'unité (290j) de commutation étant adaptée pour fournir le signal de données à la ligne (Dj) de données,
l'unité (290j) de commutation étant reliée directement ou indirectement au convertisseur numérique-analogique (250j) et à la ligne (Dj) de données ;

l'unité (280j) de circulation de courant comprenant :

des douzième et treizième transistors (M12, M13), la source de courant (Imax), un troisième noeud (N3) et un troisième condensateur (C3),
chacun des douzième et treizième transistors (M12, M13) comprenant une électrode grille et des première et deuxième électrodes principales,
la source de courant (Imax) étant adaptée pour recevoir le courant prédéterminé et étant reliée à la première électrode principale du treizième transistor (M13),
le troisième condensateur (C3) étant adapté pour stocker la tension de compensation,
le troisième condensateur (C3) étant relié au troisième noeud (N3) et à une source de tension de terre (GND),
l'électrode de grille du douzième transistor (M12) étant reliée à l'électrode de grille du treizième transistor (M13) et une ligne de signal de commande (CS2) étant adaptée pour commuter sur les douzième et treizième transistors durant la première période qui est une partie de la période horizontale (H),
le troisième noeud (N3) étant relié à la première électrode principale du douzième transistor (M12), au troisième condensateur (C3) et au générateur de tension (240j),
la deuxième électrode principale du douzième transistor (M12) étant reliée à la deuxième électrode principale du treizième transistor (M13) et à la ligne (Dj) de données,
la ligne (Dj) de données reliant l'unité (290j) de commutation et l'unité (280j) de circulation du courant.

3. Circuit d'attaque de données tel que revendiqué dans l'une des revendications 1 ou 2, dans lequel l'unité (280) de circulation du courant est adaptée pour recevoir le courant prédéterminé dans la première période, la première période étant une partie de la période horizontale (H).

4. Circuit d'attaque de données tel que revendiqué dans l'une des revendications 1 à 3, dans lequel une valeur du courant prédéterminé est égale à une valeur d'un courant qui circule lorsqu'un pixel relié à la ligne (Dj) de données émet de la lumière avec une luminosité maximale.

5. Circuit d'attaque de données tel que revendiqué dans l'une des revendications 3 ou 4, dans lequel l'unité (290j) de commutation est adaptée pour coupler la ligne (Dj) de données et le convertisseur numérique-analogique (250j) l'un à l'autre dans la deuxième période de la période horizontale (H) survenant après la première période.

6. Circuit d'attaque de données tel que revendiqué dans la revendication 5,
dans lequel l'unité (290j') de commutation comprend deux transistors (M11, M14) couplés l'un à l'autre sous forme d'une grille de transmission ou dans lequel l'unité de commutation comprend un onzième transistor (M11) qui est commandé par un signal de commande (CS1).

7. Circuit d'attaque de données tel que revendiqué dans l'une des revendications précédentes, dans lequel le générateur de tension (240j) comprend une pluralité de résistances de division de tension couplées entre une première borne et une deuxième borne pour générer les tensions d'échelle de gris.

8. Circuit d'attaque de données tel que revendiqué dans la revendication 7,
dans lequel la première borne est reliée à un bloc d'alimentation de référence (Vref) adapté pour fournir une tension de référence à la première borne, et
dans lequel la deuxième borne est reliée à l'unité (280j) de circulation du courant adaptée pour fournir la tension de compensation à la deuxième borne.

9. Circuit d'attaque de données tel que revendiqué dans l'une des revendications précédentes, comprenant en outre :

une première porte de transfert (270j) située entre le convertisseur numérique-analogique (250j) et l'unité (290j) de commutation ; et
une deuxième porte de transfert (260j) située entre l'unité (280j) de circulation du courant et le générateur de tension (240j).

10. Circuit d'attaque de données tel que revendiqué dans l'une des revendications précédentes, comprenant en outre :

une unité (210) de registre à décalage comportant des registres à décalage adaptés pour générer des signaux d'échantillonnage ;
une unité (220) de verrous d'échantillonnage comportant une pluralité de verrous d'échantillonnage adaptés pour recevoir les données fournies au circuit d'attaque de données en réponse aux signaux d'échantillonnage ; et
une unité (230) de verrous de retenue comportant des verrous de retenue adaptés pour recevoir et stocker les données stockées dans les verrous d'échantillonnage et pour fournir les données stockées dans les verrous de retenue au convertisseur numérique-analogique (250).

11. Circuit d'attaque de données tel que revendiqué dans la revendication 10, comprenant en outre une unité (310) de décalage de niveau destinée à augmenter un niveau de tension des données stockées dans les verrous de retenue pour fournir les données au convertisseur numérique analogique (250).

12. Circuit d'attaque de données tel que revendiqué dans l'une des revendications précédentes, dans lequel
la source (Vp) de tension de précharge est adaptée pour fournir la tension de précharge qui correspond à une valeur de tension de la ligne (Dj) de données résultant du courant prédéterminé tiré d'un pixel.

13. Circuit d'attaque de données tel que revendiqué dans l'une des revendications 1 à 5 ou 7 à 12, dans lequel
l'unité (290j) de commutation comprend un onzième transistor (M11) pour coupler électriquement la ligne (Dj) de données et l'unité (300j) de précharge l'une à l'autre dans la $0^{ème}$ période et la deuxième période.

14. Procédé de pilotage d'un dispositif d'affichage électroluminescent organique selon l'une des revendications 1 et 2, le procédé comprenant les étapes qui consistent :

à commander des courants prédéterminés pour qu'ils circulent dans des lignes (Dj) de données couplées à des pixels (140, 1421, 1422) ;
à générer des tensions de compensation correspondant aux courants prédéterminés ;

à réinitialiser des valeurs de tensions d'échelle de gris en utilisant les tensions de compensation ;
à sélectionner une tension parmi les tensions d'échelle de gris correspondant aux valeurs de bit de données fournies au circuit d'attaque de données depuis l'extérieur ;
et à fournir la tension sélectionnée aux lignes (Dj) de données,
le procédé étant **caractérisé par** une étape qui consiste à fournir une tension de précharge prédéterminée à un pixel (140, 1421, 1422) sélectionné par un signal de balayage.

15. Procédé tel que revendiqué dans la revendication 14, dans lequel les courants prédéterminés sont égaux aux courants qui circulent à travers des diodes électroluminescentes organiques (OLED) à l'intérieur des pixels (140, 1421, 1422) lorsque les pixels émettent de la lumière avec une luminosité maximale.

16. Procédé tel que revendiqué dans l'une des revendications 14 et 15, dans lequel la tension de précharge (Vp) correspond à une valeur de tension de la ligne (Dj) de données reliée au pixel (140, 1421, 1422) sélectionné par un signal de balayage résultant du courant prédéterminé tiré du pixel (140, 1421, 1422).

FIG. 1
(PRIOR ART)

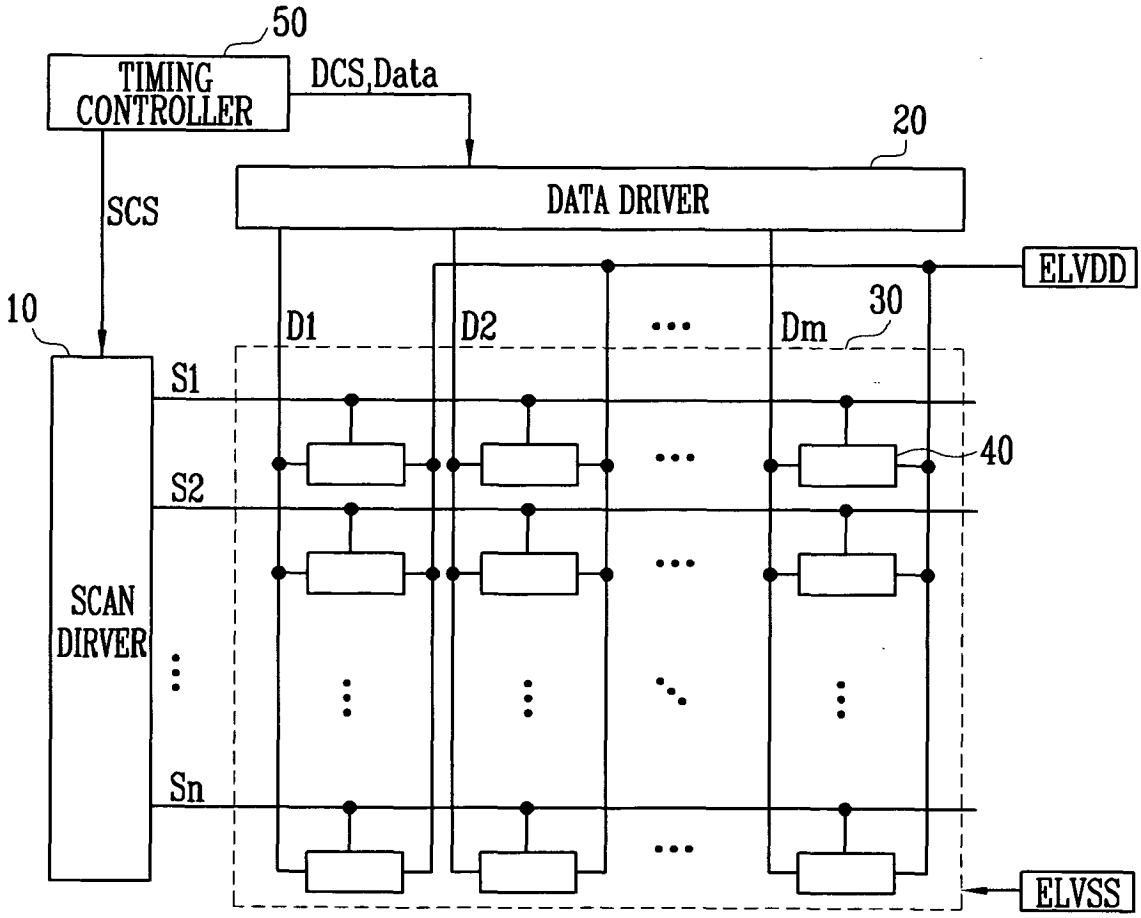


FIG. 2

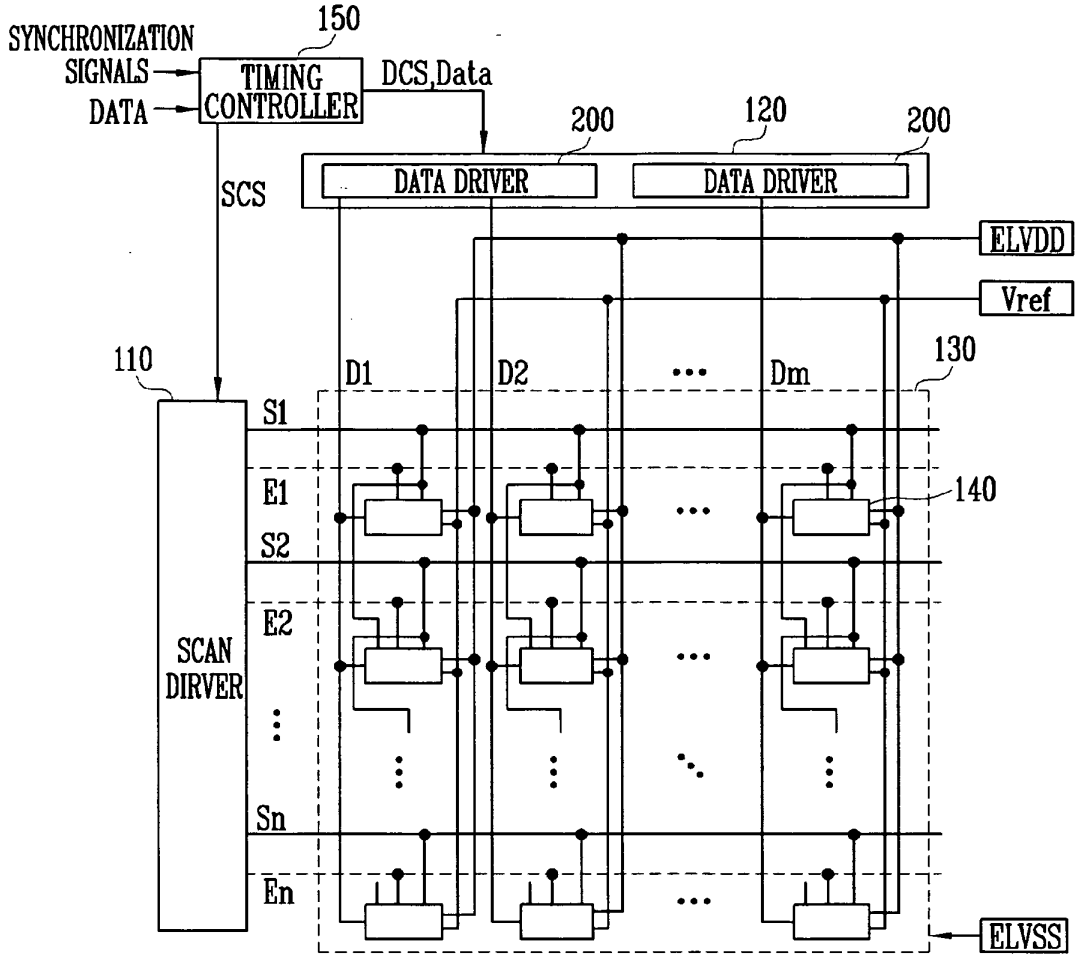

SYNCHRONIZATION
SIGNALS
DATA
150
TIMING
CONTROLLER
DCS,Data
200
120
200
DATA DRIVER
DATA DRIVER
SCS
ELVDD
Vref
110
D1
D2
Dm
130
S1
E1
S2
E2
140
SCAN
DIRVER
Sn
En
ELVSS

FIG. 3

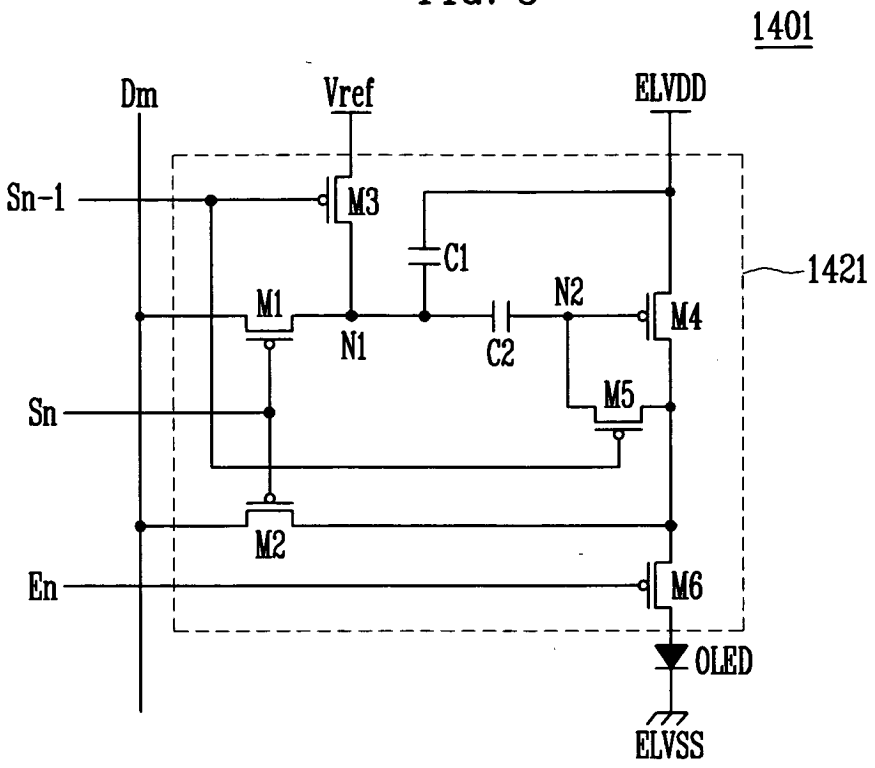

1401
Dm
Vref
ELVDD
Sn-1
M3
C1
1421
M1
N2
M4
N1
C2
Sn
M5
M2
En
M6
OLED
ELVSS

FIG. 4

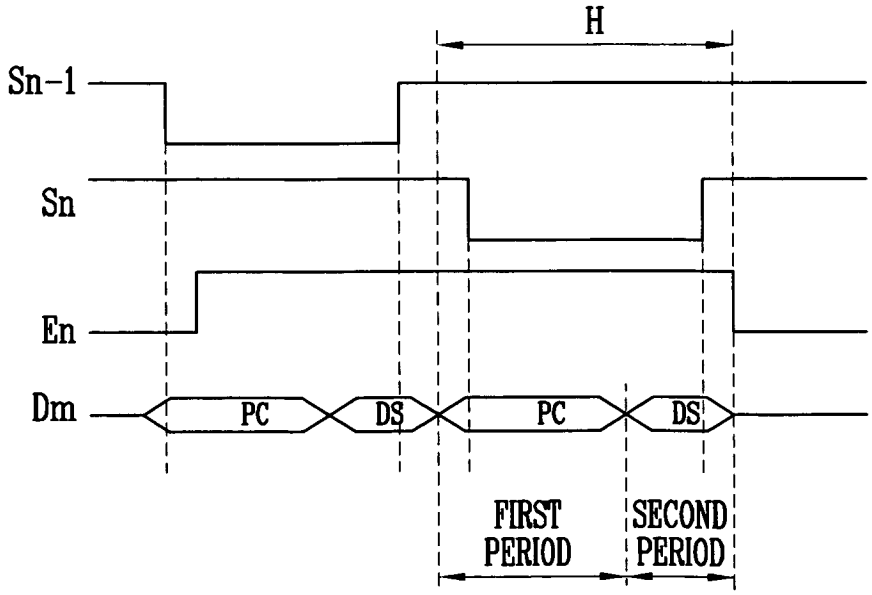

H
Sn-1
Sn
En
Dm
PC
DS
PC
DS
FIRST PERIOD
SECOND PERIOD

FIG. 5

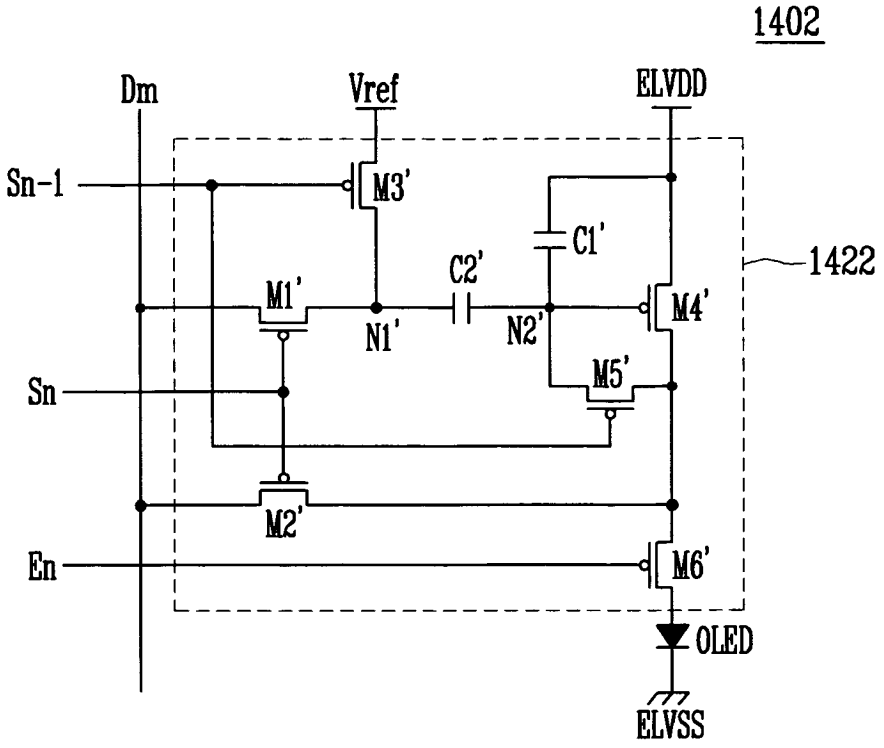

1402
Dm
Vref
ELVDD
Sn-1
M3'
C1'
C2'
1422
M1'
N1'
N2'
M4'
M5'
Sn
M2'
En
M6'
OLED
ELVSS

FIG. 6

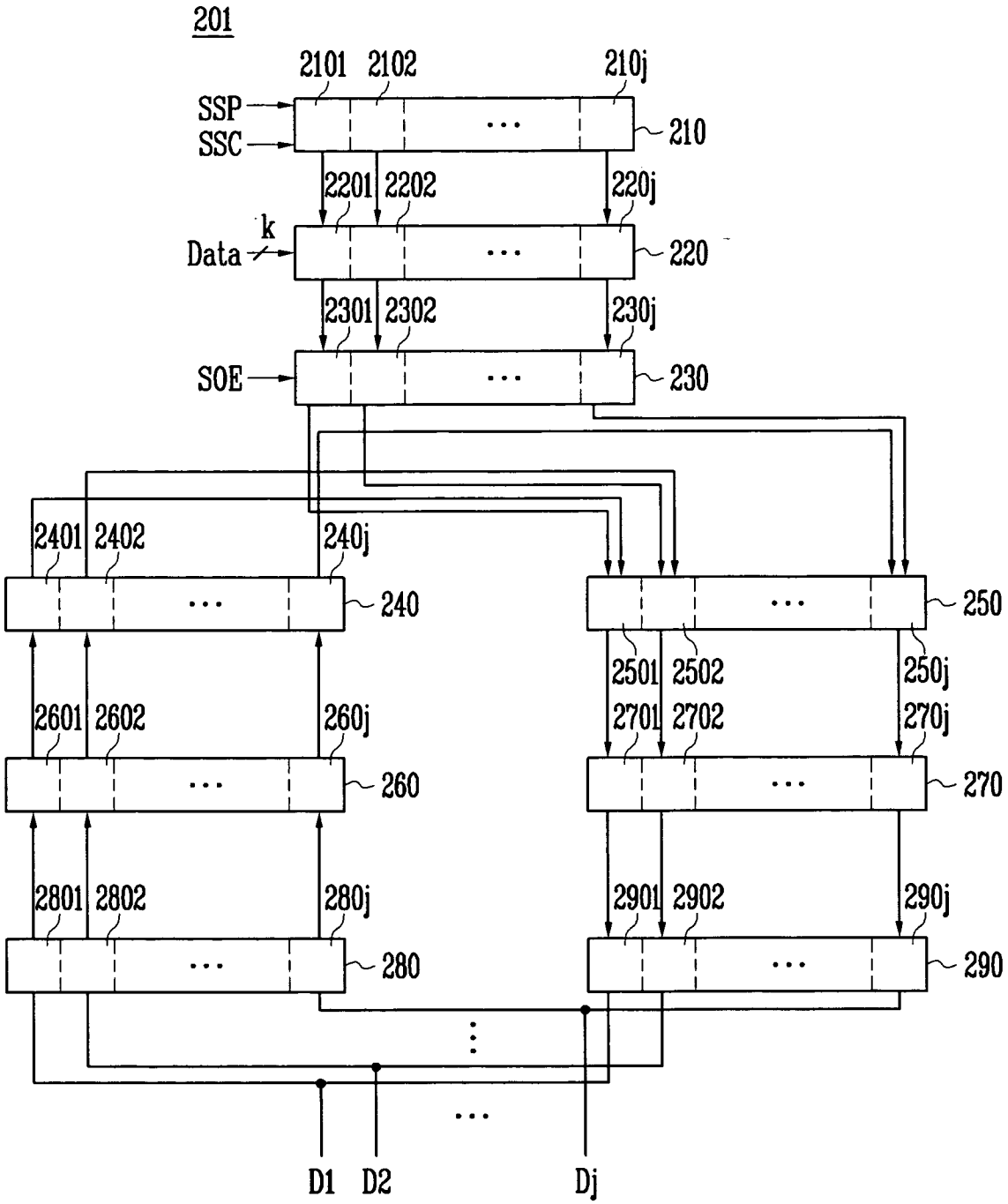

201
2101
2102
210j
SSP
SSC
210
2201
2202
220j
k
Data
220
2301
2302
230j
SOE
230
2401
2402
240j
240
250
2501
2502
250j
2601
2602
260j
2701
2702
270j
260
270
2801
2802
280j
2901
2902
290j
280
290
D1
D2
Dj

FIG. 7

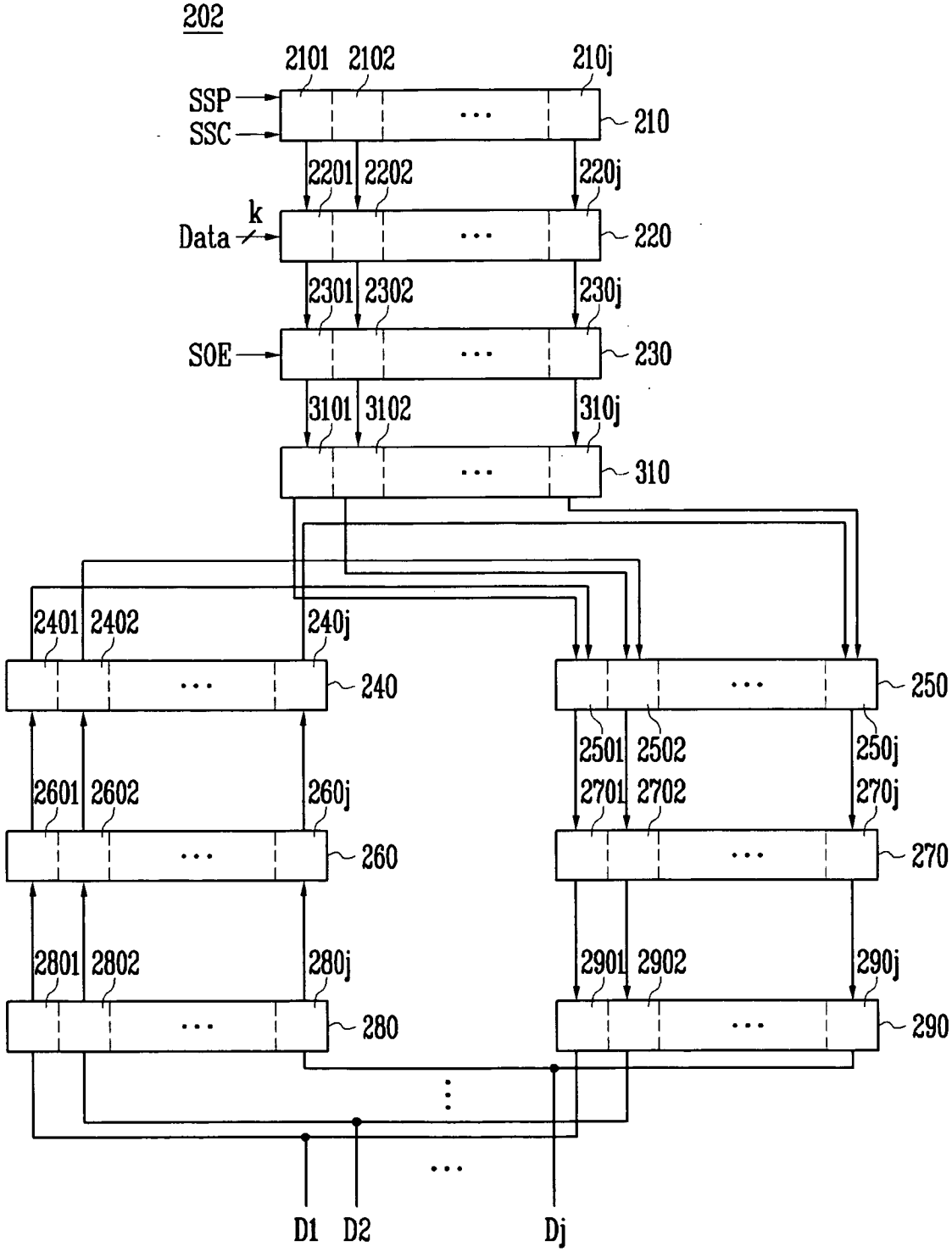

202
2101
2102
210j
SSP
SSC
210
2201
2202
220j
k
Data
220
2301
2302
230j
SOE
230
3101
3102
310j
310
2401
2402
240j
240
250
2501
2502
250j
2601
2602
260j
2701
2702
270j
260
270
2801
2802
280j
2901
2902
290j
280
290
D1
D2
Dj

FIG. 8

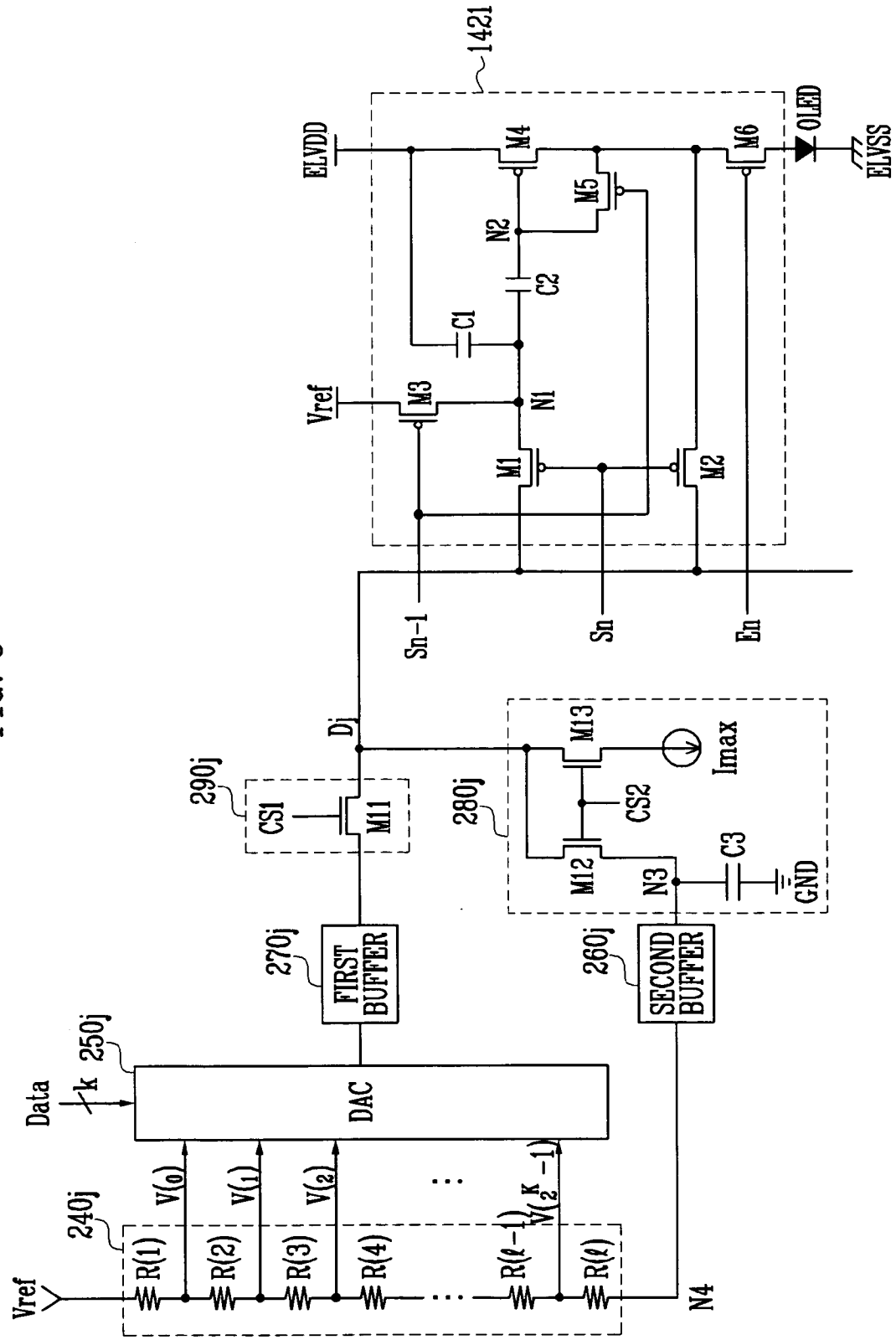

1421
ELVDD
M4
M5
M6
OLED
ELVSS
N2
C2
C1
Vref
M3
N1
M1
M2
Sn-1
Sn
En
Dj
290j
CS1
M11
280j
M13
Imax
CS2
M12
N3
C3
GND
270j
FIRST BUFFER
260j
SECOND BUFFER
Data
k
250j
DAC
240j
V(0)
V(1)
V(2)
V(2^K-1)
R(1)
R(2)
R(3)
R(4)
R(ℓ-1)
R(ℓ)
Vref
N4

FIG. 9

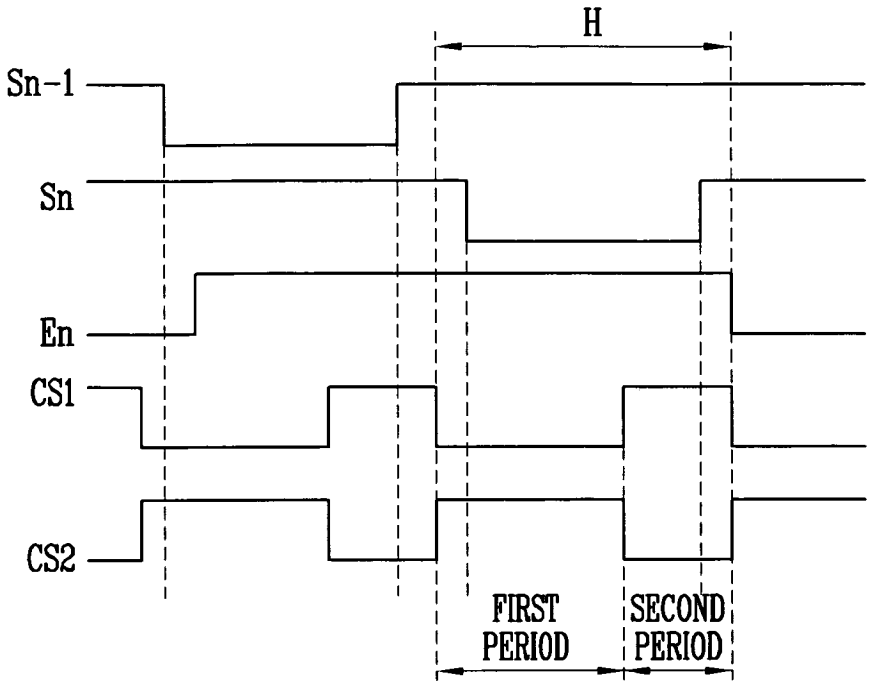


FIG. 10

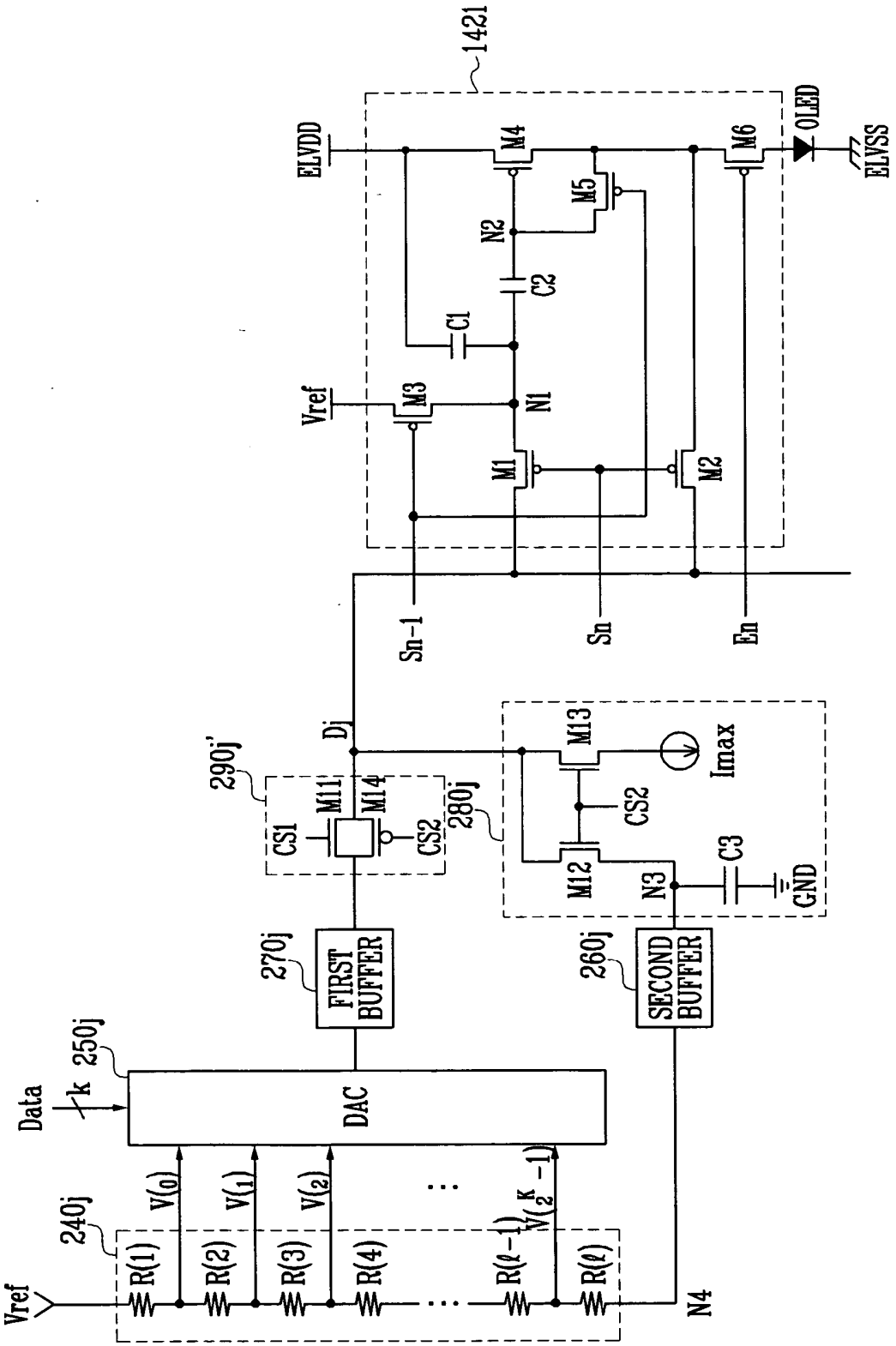

1421
ELVDD
M4
M6
OLED
ELVSS
M5
N2
C2
C1
Vref
M3
N1
M1
M2
Sn-1
Sn
En
290j'
Dj
M13
Imax
CS1
M11
M14
CS2
280j
CS2
M12
N3
C3
GND
270j
FIRST BUFFER
260j
SECOND BUFFER
250j
Data
k
DAC
240j
V(0)
V(1)
V(2)
V(2^K -1)
R(1)
R(2)
R(3)
R(4)
R(ℓ-1)
R(ℓ)
Vref
N4

FIG. 11

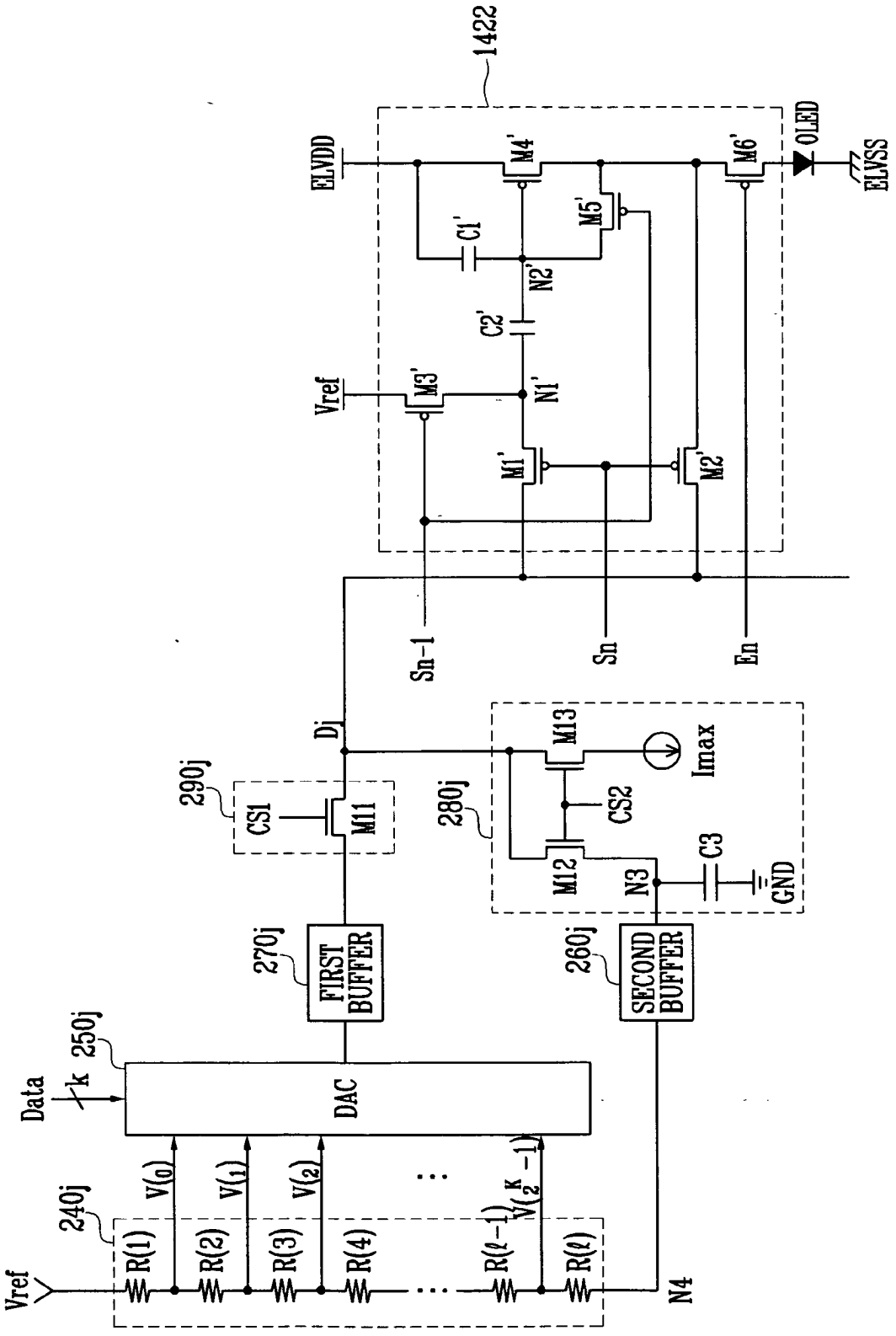

1422
ELVDD
M4'
M6'
OLED
ELVSS
M5'
C1'
N2'
C2'
Vref
M3'
N1'
M1'
M2'
Sn-1
Sn
En
Dj
290j
CS1
M11
280j
M13
Imax
CS2
M12
N3
C3
GND
270j
FIRST BUFFER
260j
SECOND BUFFER
Data
k
250j
DAC
240j
V(0)
V(1)
V(2)
V(2^K-1)
R(1)
R(2)
R(3)
R(4)
R(ℓ-1)
R(ℓ)
Vref
N4

FIG. 12

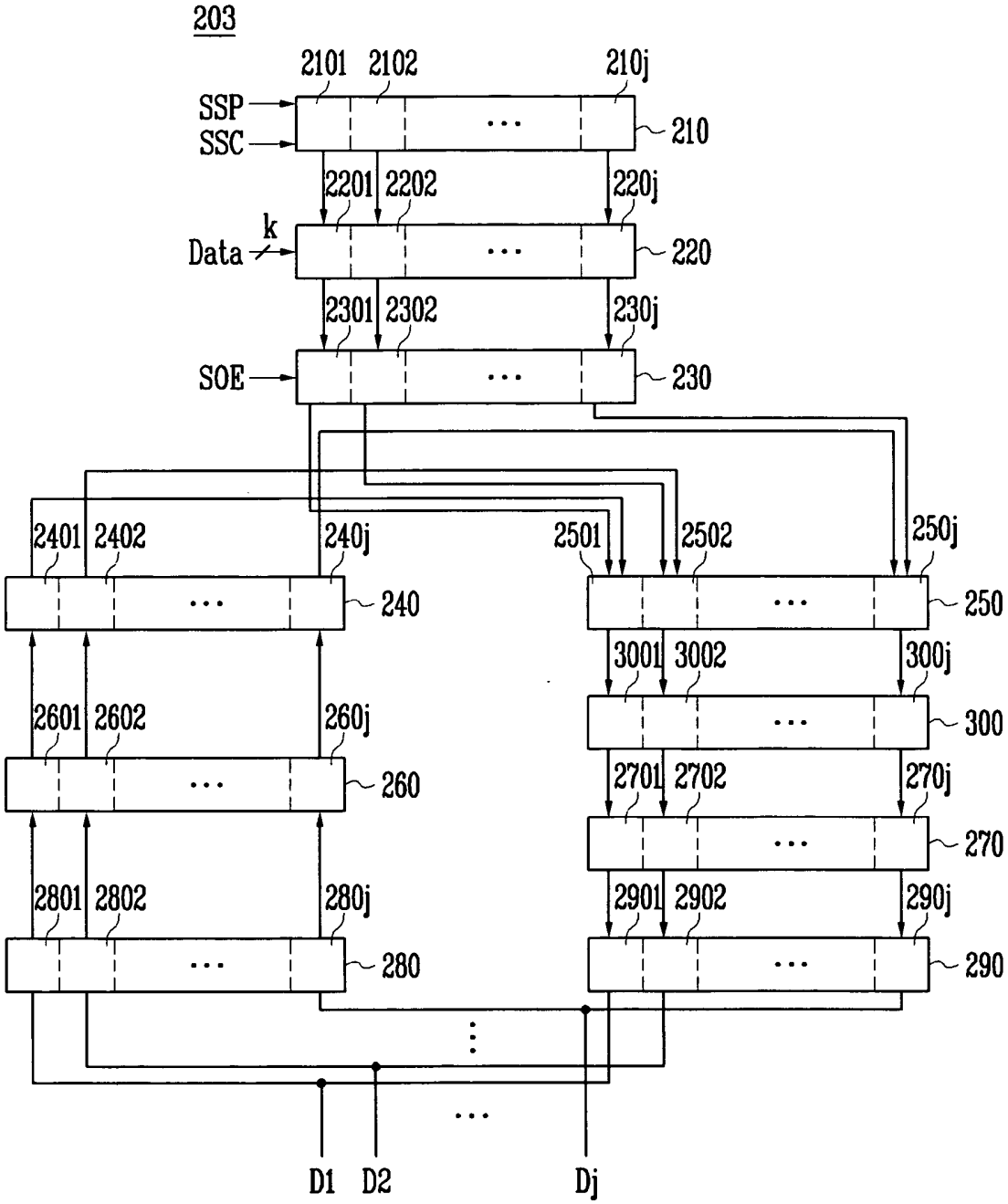

203
2101
2102
210j
SSP
SSC
210
2201
2202
220j
k
Data
220
2301
2302
230j
SOE
230
2401
2402
240j
240
2501
2502
250j
250
3001
3002
300j
300
2601
2602
260j
260
2701
2702
270j
270
2801
2802
280j
280
2901
2902
290j
290
D1
D2
Dj

FIG. 13

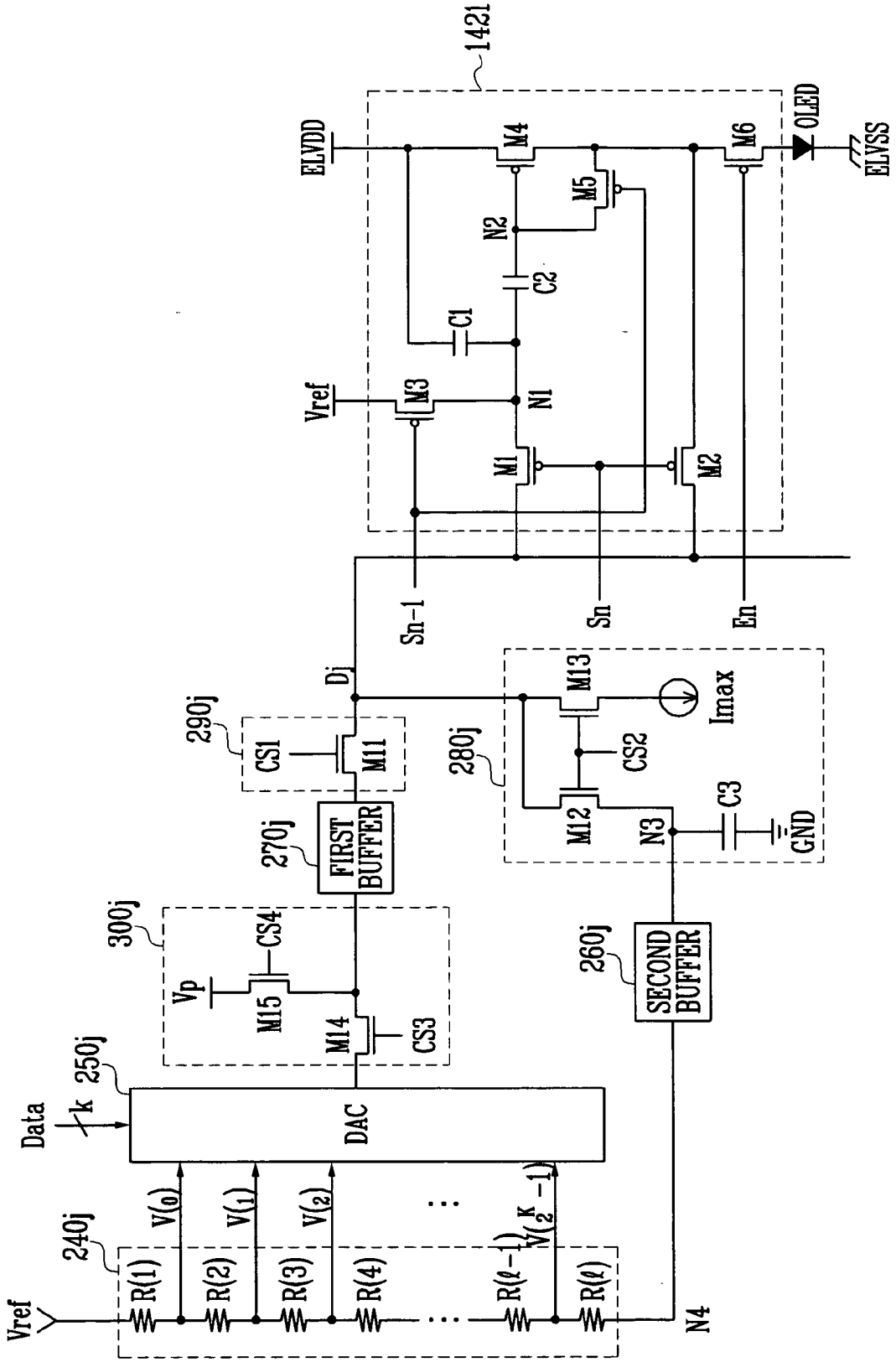
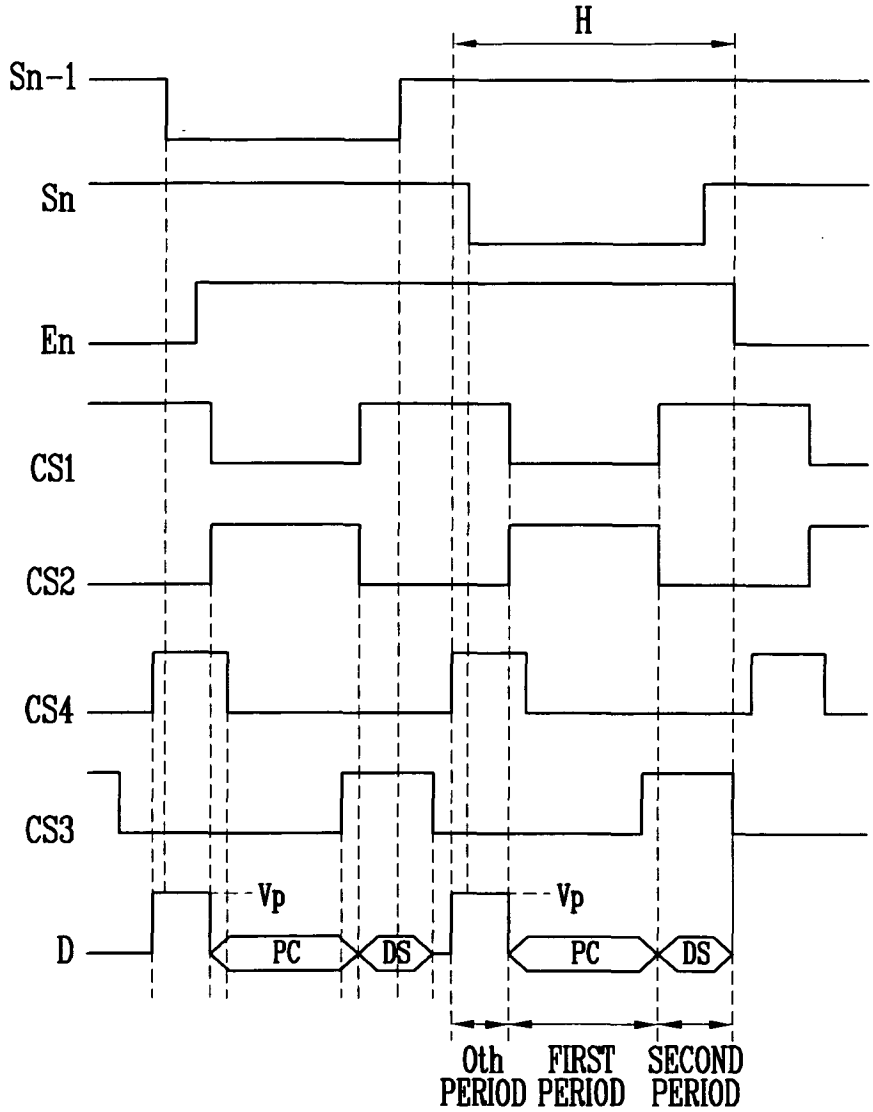

1421
ELVDD
M4
M5
M6
OLED
ELVSS
N2
C2
C1
Vref
M3
N1
M1
M2
Sn-1
Sn
En
Dj
290j
CS1
M11
280j
M13
Imax
CS2
M12
N3
C3
GND
270j
FIRST BUFFER
300j
Vp
CS4
M15
M14
CS3
260j
SECOND BUFFER
250j
Data
k
DAC
240j
V(0)
V(1)
V(2)
V(2^K-1)
R(1)
R(2)
R(3)
R(4)
R(ℓ-1)
R(ℓ)
Vref
N4

FIG. 14


H
Sn-1
Sn
En
CS1
CS2
CS4
CS3
Vp
Vp
D
PC
DS
PC
DS
0th PERIOD
FIRST PERIOD
SECOND PERIOD

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2004124780 A1 **[0014]**

Non-patent literature cited in the description

- **HAI-JUNG IN ; JOON-HO BAE ; JIN-SUNG KANG ; AN OHKYONG KWON.** A Novel Voltage-Programming Pixel with Current-Correction Method for Large-Size and High-Resolution AMOLEDS on Poly-Si Backplane. *IMID 05 DIGEST,* 23 July 2005, 901-904, http://pddocserv/specdocs/datalhandbooks/IMID/2005/28.6.pdf **[0012]**
- **MATSUEDA Y et al.** 35.1:2.5-in. AMOLED with Integrated 6-Bit Gamma Compensated Digital Data Driver. *2004 SID INTERNATIONAL SYMPOSIUM. SEATTLE, WA, MAY 25-27, 2004, SID INTERNATIONAL SYMPOSIUM,* 25 May 2004, 1116-1119 **[0013]**

专利名称(译)	数据驱动器，使用其的有机发光显示装置，以及驱动有机发光显示装置的方法		
公开(公告)号	EP1752955B1	公开(公告)日	2011-10-19
申请号	EP2006118729	申请日	2006-08-10
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司 汉阳大学校产学协力团		
申请(专利权)人(译)	三星SDI CO.，LTD. IUCF-HYU（产学合作基金会汉阳大学）		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
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发明人	RYU, DO HYUNG LEGAL & IP TEAM CHUNG, BO YONG LEGAL & IP TEAM KIM, HONG KWON LEGAL & IP TEAM KWON, OH KYONG LEGAL & IP TEAM		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3291 G09G3/3233 G09G2300/0819 G09G2300/0852 G09G2300/0861 G09G2310/0251 G09G2320/0276 G09G2320/043 G09G2352/00		
代理机构(译)	hengelhaupt，Jürgen		
优先权	1020050073048 2005-08-10 KR 1020050073047 2005-08-10 KR		
其他公开文献	EP1752955A1		
外部链接	Espacenet		

摘要(译)

能够显示具有基本均匀亮度的图像的数据驱动器，使用该数据驱动器的有机发光显示装置，以及驱动该有机发光显示装置的方法。数据驱动器包括：电流吸收单元，用于控制流过数据线的预定电流;电压发生器，用于使用在预定电流s时产生的补偿电压来重置灰度级电压的值;数字 - 模拟转换器，用于响应于从外部提供的数据的比特值，选择灰度级电压中的一个灰度级电压作为数据信号，以及用于将数据信号提供给数据线的开关单元。可以将预定电流设置为等于对应于最大亮度的像素电流。

[EQUATION1]

$$V_{N1} = Vref$$

$$V_{N2} = ELVDD - V_{thM4}$$