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(54) **Data driving circuit, organic light emitting diode display using the same, and method of driving the organic light emitting diode display**

Datentreiberschaltung, organische lichtemittierende Diodenanzeige damit und Verfahren zur Ansteuerung der organischen lichtemittierenden Diodenanzeige

Circuit de commande de données, affichage à diodes électroluminescentes organiques l'utilisant, et procédé de commande de l'affichage à diodes électroluminescentes organiques

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**EP-A- 1 675 093**

- **HAI-JUNG IN ET AL: "A Novel Voltage-Programming Pixel with Current-Correction Method for Large-Size and High-Resolution AMOLEDs on Poly-Si Backplane" INTERNATIONAL MEETING ON INFORMATION DISPLAY, XX, XX, no. 286, 23 July 2005 (2005-07-23), pages 901-904, XP002405123**
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**EP 1 750 246 B1**

**Description****BACKGROUND**5 **1. Field of the Invention**

[0001] The present invention relates to a data driving circuit, a light emitting display employing such a data driving circuit, and a method of driving the light emitting display. More particularly, the invention relates to a data driving circuit capable of displaying images with uniform brightness, a light emitting display using such a data driving circuit, and a method of driving the light emitting display to display images with uniform brightness.

10 **2. Discussion of Related Art**

[0002] Flat panel displays (FPDs), which are generally lighter and more compact than cathode ray tubes (CRTs), are being developed. FPDs include liquid crystal displays (LCDs), field emission displays (FEDs), plasma display panels (PDPs) and light emitting displays.

[0003] Light emitting displays may display images using organic light emitting diodes (OLEDs) that generate light when electrons and holes re-combine. Light emitting displays generally have fast response times and consume relatively low amounts of power.

20 [0004] FIG. 1 illustrates a schematic of the structure of a known light emitting display.

[0005] As shown in FIG. 1, the light emitting display includes a pixel unit 30, a scan driver 10, a data driver 20 and a timing controller 50. The pixel unit 30 may include a plurality of pixels 40 connected to scan lines S1 to Sn and data lines D1 to Dm. The scan driver 10 may drive the scan lines S1 to Sn. The data driver 20 may drive the data lines D1 to Dm. The timing controller 50 may control the scan driver 10 and the data driver 20.

25 [0006] The timing controller 50 may generate data driving control signals DCS and scan driving control signals SCS based on externally supplied synchronizing signals (not shown). The data driving control signals DCS are supplied to the data driver 20 and the scan driving control signals SCS are supplied to the scan driver 10. The timing controller 50 may supply data DATA to the data driver 20 in accordance with externally supplied data (not shown).

30 [0007] The scan driver 10 receives the scan driving control signals SCS from the timing controller 50. The scan driver 10 generates scan signals (not shown) based on the received scan driving control signals SCS. The generated scan signals may be sequentially supplied to the pixel unit 30 via the scan lines S1 to Sn.

[0008] The data driver 20 receives the data driving control signals DCS from the timing controller 50. The data driver 20 generates data signals (not shown) based on the received data DATA and data driving control signals DCS. Corresponding ones of the generated data signals may be supplied to the data lines D1 to Dm in synchronization with respective ones of the scan signals being supplied to the scan lines S1 to Sn.

35 [0009] The pixel unit 30 may be connected to a first power source ELVDD for supplying a first voltage VDD and a second power source ELVSS for supplying a second voltage VSS to the pixels 40. The pixels 40, together with the first voltage VDD signal and the second voltage VSS signal, control the currents that flow through respective OLEDs in accordance with the corresponding data signals. The pixels 40 thereby generate light based on the first voltage VDD signal, the second voltage VSS signal and the data signals.

40 [0010] In known light emitting displays, each of the pixels 40 may include a pixel circuit including at least one transistor for selectively supplying the respective data signal and the respective scan signal for selectively turning on and turning off the respective pixel 40 of the light emitting display.

45 [0011] It is desired for each pixel 40 of a light emitting display to generate light of predetermined brightness in response to various values of the respective data signals. For example, when the same data signal is applied to all the pixels 40 of the display, it is generally desired for all the pixels 40 of the display to generate the same brightness. The brightness generated by each pixel 40 is not, however, only dependent on the data signal. The brightness generated by each pixel 40 is also dependent on characteristics of each pixel 40, such as the characteristics, e.g., threshold voltage, of each transistor of the pixel circuit.

50 [0012] Generally, there are variations in threshold voltage and/or electron mobility from transistor to transistor such that different transistors have different threshold voltages and electron mobilities. The characteristics of transistors may also change over time and/or usage. For example, the threshold voltage and electron mobility of a transistor may be dependent on the on/off history of the transistor.

55 [0013] Therefore, in a light emitting display, the brightness generated by each pixel in response to respective data signals depends on the characteristics of the transistor(s) that may be included in the respective pixel circuit. Such variations in threshold voltage and electron mobility may prevent and/or hinder the uniformity of images being displayed. Thus, such variations in threshold voltage and electron mobility may also prevent the display of an image with a desired brightness.

**[0014]** Although it may be possible to at least partially compensate for differences between threshold voltages of the transistors included in the pixels by controlling the structure of the pixel circuits of the pixels 40, circuits and methods capable of compensating for the variations in electron mobility are needed and desired. OLEDs that are capable of displaying images with uniform brightness irrespective of variations in electron mobility are also desired.

5 **[0015]** EP-A-1675093 describes a data driving circuit including: a voltage digital-analog converter adapted to generate a first gradation voltage corresponding to external data; a current digital-analog converter adapted to generate a gradation current corresponding to the external data; a voltage control unit adapted to receive a feedback pixel current from a pixel via a data line and to generate a second gradation voltage by increasing or decreasing a level of the first gradation voltage in accordance with the feedback pixel current; a buffer unit adapted to selectively supply the first or second gradation voltage to the data line; and a selection unit adapted to selectively connect the data line to either the buffer unit or the voltage control unit. With this configuration, an image is displayed with a desired brightness.

10 **[0016]** HAI-JUNG IN ET AL: "A Novel Voltage-Programming Pixel with Current-Correction Method for Large-Size and High-Resolution AMOLEDs on Poly-Si Backplane" INTERNATIONAL MEETING ON INFORMATION DISPLAY, XX, XX, no. 286, 23 July 2005, pages 901-904, describes an active matrix OLED voltage-programming pixel structure with current-correction method.

15 **[0017]** US2005/088103A1 discloses an image display device that reduces variations in brightness of light emitting elements included in the device due to a voltage drop on the power source line of the device and TFT threshold voltage variations. The image display device is equipped with a pixel circuit voltage detecting means to selectively output a voltage internal to a pixel circuit included in each of a plurality of pixels of the device to a signal line to which the pixel circuit connects. Its drive circuit is equipped with a voltage addition means to add the signal line voltage and a signal voltage corresponding to image data to be displayed and output a sum voltage to the signal line again.

20 **[0018]** The present invention is therefore directed to a light emitting display using the same, which substantially overcomes one or more of the problems due to the limitations and disadvantages of the related art.

25 **[0019]** It is therefore a feature of an embodiment of the present invention to provide a light emitting display driven by a data driving circuit to display images with uniform brightness and a method of driving the light emitting display.

30 **[0020]** A data driving circuit for driving at least one pixel of a light emitting display based on externally supplied data for the pixel is described, wherein the pixel is electrically connectable to the driving circuit via at least one data line. The data driving circuit may include at least one current sink that may receive a predetermined current from the pixel via the data line, a voltage generator that may respectively set values of a plurality of gray scale voltages based on a compensation voltage generated by the pixel when the predetermined current flows through the pixel, at least one digital-analog converter that may select, as a data signal for the pixel, one of the plurality of set gray scale voltages based on a bit value of a portion of the externally supplied data associated with the pixel, at least one switching unit that may supply the selected data signal to the data line. A value of the predetermined current may be equal to or higher than a value of a minimum current employable by the pixel to emit light of maximum brightness. The maximum brightness may correspond to a brightness of the pixel when a highest one of the plurality of set gray scale voltages is applied to the pixel.

35 **[0021]** The voltage generator may include a plurality of voltage dividing resistors between a first terminal for receiving a reference power source and a second terminal for receiving the compensation voltage to set the gray scale voltages. A compensation resistor may be connected between the second terminal and the voltage dividing resistors to reduce a value of the compensation voltage. The compensation resistor may compensate for the value of the predetermined current being higher than the value of the minimum current employable by the pixel to emit light of maximum brightness by reducing the value of the compensation voltage such that a voltage corresponding to the minimum current may be supplied to the voltage dividing resistors. The current sink may receive the predetermined current from the pixel during a first partial period of one complete period for driving the pixel based on the selected gray scale voltage, the first partial period may occur before a second partial period in the one complete period for driving the pixel.

40 **[0022]** The current sink may include a current source for receiving the predetermined current, a first transistor between the data line and the voltage generator, the first transistor may be turned on during the first partial period, a second transistor between the data line and the current source, the second transistor may be turned on during the first partial period, and a capacitor that may charge the compensation voltage. The switching unit may include at least one transistor that may selectively connect the data line and the digital-analog converter to each other only during any partial period of a complete period, for driving the pixel based on the selected gray scale voltage, which occurs after a first partial period of the complete period. The switching unit may include two transistors that are connected to each other so as to form a transmission gate- The data driving circuit may include a first buffer provided between the digital-analog converter and the switching unit and/or a second buffer provided between the current sink and the voltage generator.

45 **[0023]** Each channel of the data driving circuit may include a respective one of each of the current sink, the voltage generator, the digital-analog converter and the switching unit. The data driving circuit may include at least one shift register for generating sampling pulses, at least one sampling latch for receiving the data in response to the sampling pulses, and at least one holding latch for temporarily storing the data stored in the sampling latch before the temporarily stored data is supplied to the digital-analog converter. The data driving circuit may include a level shifter for modifying

a voltage level of the data stored in the holding latch before the temporarily stored data is supplied to the digital-analog converter.

5 [0024] At least one of the above and other features and advantages of embodiments of the present invention may be realized by providing a light emitting display, comprising: pixel unit including a plurality of pixels connected to n scan lines, a plurality of data lines and a plurality of emission control lines, wherein each pixel comprises a driving transistor; a scan driver for respectively and sequentially supplying, during each scan cycle, n scan signals to the n scan lines, and for sequentially and respectively supplying emission control signals to the plurality of emission control lines; a data driving circuit, for respectively setting values of and generating a plurality of gray scale voltages for driving a said pixel via the respective data lines, wherein the plurality of gray scale voltages are set and generated based on a compensation voltage generated by said pixel when a predetermined current is flowing in said pixel during a first partial period of one complete period for driving said pixel wherein a value of the predetermined current is equal to or greater than a value of a minimum current employable by said pixel to emit light of maximum brightness, the data driving circuit comprising a current sink for sinking the predetermined current flowing through the pixel via the data line, the current sink comprising: a current source for receiving the predetermined current; a first current source transistor provided between the data line and the voltage generator, the first current source transistor being arranged to be turned on during the first partial period; a second current source transistor provided between the data line and the current source, the second current source transistor being arranged to be turned on during the first partial period; and a capacitor for charging the compensation voltage; and wherein the compensation voltage is arranged to compensate for at least variations in threshold voltage and/or electron mobility of the driving transistor of said pixel.

10 [0025] Each of the pixels may be connected to two of the n scan lines, and during each of the scan cycles, a first scan line of the two scan lines may receive a respective one of the n scan signals before a second scan line of the two scan lines receives a respective one of the n scan signals, and each of the pixels may include a first power source, an organic light emitting diode the organic light emitting diode receiving current from the first power source, first and second transistors, each of which may have a first electrode connected to the respective one of the data lines associated with the pixel, the first and second transistors may be turned on when the second of the two scan signals is supplied, a third transistor having a first electrode connected to a reference power source and a second electrode connected to a second electrode of the first transistor, the third transistor may be turned on when the first of the two scans signal is supplied, a fourth transistor, the fourth transistor may control an amount of current supplied to the organic light emitting diode, a first terminal of the fourth transistor may be connected to the first power source, and a fifth transistor having a first electrode connected to a gate electrode of the fourth transistor and a second electrode connected to a second electrode of the fourth transistor, the fifth transistor may be turned on when the first of the two scan signals is supplied such that the fourth transistor may operate as a diode.

15 [0026] Each of the pixels may include a first capacitor having a first electrode connected to one of a second electrode of the first transistor and the gate electrode of the fourth transistor and a second electrode connected to the first power source, and a second capacitor having a first electrode connected to the second electrode of the first transistor and a second electrode connected to the gate electrode of the fourth transistor.

20 [0027] Each of the pixels may include a sixth transistor having a first terminal connected to the second electrode of the fourth transistor and a second terminal connected to the organic light emitting diode, the sixth transistor may be turned off when the respective emission control signal is supplied. The current sink may receive the predetermined current from the pixel during the first partial period of one complete period for driving the pixel based on the selected gray scale voltage, the first partial period occurring before a second partial period in the complete period for driving the pixel, and the sixth transistor may be turned off during the second partial period of the complete period for driving the pixel.

25 [0028] At least one of the above and other features and advantages of embodiments of the present invention may be separately realized by providing a method of driving a light emitting display comprising a pixel unit including a plurality of pixels connected to n scan lines, a plurality of data lines and a plurality of emission control lines, each pixel comprising a driving transistor, a scan driver and a data driving circuit, the data driving circuit comprising a current sink for sinking a predetermined current flowing through the pixel via the data line, the current sink comprising: a current source for receiving the predetermined current; a first current source transistor provided between the data line and the voltage generator, the first current source transistor being arranged to be turned on during the first partial period; a second current source transistor provided between the data line and the current source, the second current source transistor being arranged to be turned on during the first partial period; and a capacitor for charging the compensation voltage; the method comprising: sequentially and respectively supplying, during each scan cycle, n scan signals to the n scan lines; sequentially and respectively supplying emission control signals to the plurality of emission control lines; and respectively setting values of and generating a plurality of gray scale voltages for driving a said pixel via the respective data lines, wherein the plurality of gray scale voltages are set and generated based on a compensation voltage generated by said pixel when the predetermined current flows in said pixel wherein a value of the predetermined current is equal to or greater than a value of a minimum current employable by said pixel to emit light of maximum brightness, and wherein the compensation voltage is arranged to compensate for at least variations in threshold voltage and/or electron

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mobility of the driving transistor of said pixel.

**[0029]** Flowing the predetermined current and generating the compensation voltage may occur during a first partial period of a complete period for driving the pixel based on the selected gray scale voltage. Supplying the selected data signal may occur during any partial period of the complete period, for driving the pixel, other than the first partial period that occurs after the first partial period. When the value of the predetermined current flowing from the respective pixel to the current sink of the light emitting display is greater than the value of the minimum current employable by the respective pixel to emit light of maximum brightness, the step of generating the compensation voltage may include generating an initial compensation voltage and a first compensation voltage based on the initial compensation voltage before the step of setting values of the plurality of gray scale voltages. The first compensation voltage may be less than the initial generated compensation voltage and the first compensation voltage may correspond to a highest one of the plurality of gray scale voltages and the compensation voltage generated when the predetermined current that flows is equal to or substantially equal to the minimum current employable by the pixel to emit light of maximum brightness. Setting values of the plurality of gray scale voltages may include supplying the compensation voltage to a plurality of voltage dividing resistors.

**[0030]** At least one of the above and other features and advantages of embodiments of the present invention may be separately realized by providing a data driving circuit employable by a light emitting display for driving at least one pixel of the light emitting display based on externally supplied data for the pixel, the pixel may be electrically connectable to at least one data line, at least one scan line and at least one emission line of the light emitting display. The data driving circuit may include means for sinking a predetermined current flowing through the pixel via the data line during a first partial period of a complete period based on the selected gray scale voltage, means for generating a compensation voltage using the predetermined current, means for generating and setting values for a plurality of gray scale voltages based on the compensation voltage generated by the pixel when the predetermined current flows through the pixel, means for selecting, as a data signal for the pixel, one of the plurality of set gray scale voltages based on a bit value of a portion of the externally supplied data associated with the pixel, and means for supplying the selected data signal to the data line, wherein a value of the predetermined current may be equal to or higher than a value of a minimum current employable by the pixel to emit light of maximum brightness, and the maximum brightness may correspond to a brightness of the pixel when a highest one of the plurality of set gray scale voltages is applied to the pixel.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0031]** These and other features and advantages of embodiments of the invention will become apparent to those of ordinary skill in the art by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 illustrates a schematic diagram of a known light emitting display;  
 FIG. 2 illustrates a schematic diagram of a light emitting display according to an embodiment of the present invention;  
 FIG. 3 illustrates a circuit diagram of an exemplary pixel employable in the light emitting display illustrated in FIG. 2;  
 FIG. 4 illustrates exemplary waveforms employable for driving the pixel illustrated in FIG. 3;  
 FIG. 5 illustrates a circuit diagram of another exemplary pixel employable in the light emitting display illustrated in FIG. 2;  
 FIG. 6 illustrates a block diagram of a first embodiment of the data driving circuit illustrated in FIG. 2;  
 FIG. 7 illustrates a block diagram of a second embodiment of the data driving circuit illustrated in FIG. 2;  
 FIG. 8 illustrates a schematic diagram of a first embodiment of a connection scheme connecting a voltage generator, a digital-analog converter, a first buffer, a second buffer, a switching unit and a current sink unit illustrated in FIG. 6, and the pixel illustrated in FIG. 3;  
 FIG. 9 illustrates exemplary waveforms employable for driving the pixel, the switching unit and the current sink unit illustrated in FIG. 8;  
 FIG. 10 illustrates the connection scheme illustrated in FIG. 8 employing another embodiment of a switching unit;  
 FIG. 11 illustrates a schematic diagram of a second embodiment of a connection scheme connecting the voltage generator, the digital-analog converter, the first buffer, the second buffer, the switching unit and the current sink unit illustrated in FIG. 6, and the pixel illustrated in FIG. 5;  
 FIG. 12 illustrates a schematic diagram of a third embodiment of a connection scheme connecting the voltage generator, the digital-analog converter, the first buffer, the second buffer, the switching unit and the current sink unit illustrated in FIG. 6, and the pixel illustrated in FIG. 3; and  
 FIG. 13 illustrates a schematic diagram of a fourth embodiment of a connection scheme connecting the voltage generator, the digital-analog converter, the first buffer, the second buffer, the switching unit and the current sink unit illustrated in FIG. 6, and the pixel illustrated in FIG. 5.

## DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

**[0032]** The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

**[0033]** Hereinafter, exemplary embodiments of the present invention will be described with reference to FIGS. 2 to 13.

**[0034]** FIG. 2 illustrates a schematic diagram of a light emitting display according to an embodiment of the present invention.

**[0035]** As shown in FIG. 2, the light emitting display may include a scan driver 110, a data driver 120, a pixel unit 130 and a timing controller 150. The pixel unit 130 may include a plurality of pixels 140. The pixel unit 130 may include  $n \times m$  pixels 140 arranged, for example, in  $n$  rows and  $m$  columns, where  $n$  and  $m$  may each be integers. The pixels 140 may be connected to scan lines  $S1$  to  $S_n$ , emission control lines  $E1$  to  $E_n$  and data lines  $D1$  to  $D_m$ . The pixels 140 may be respectively formed in the regions partitioned by the emission control lines  $E1$  to  $E_n$  and the data lines  $D1$  to  $D_m$ . The scan driver 110 may drive the scan lines  $S1$  to  $S_n$  and the emission control lines  $E1$  to  $E_n$ . The data driver 120 may drive the data lines  $D1$  to  $D_m$ . The timing controller 150 may control the scan driver 110 and the data driver 120. The data driver 120 may include one or more data driving circuits 200.

**[0036]** The timing controller 150 may generate data driving control signals DCS and scan driving control signals SCS in response to externally supplied synchronizing signals (not shown). The data driving control signals DCS generated by the timing controller 150 may be supplied to the data driver 120. The scan driving control signals SCS generated by the timing controller 150 may be supplied to the scan driver 110. The timing controller 150 may supply data DATA to the data driver 120 in accordance with the externally supplied data (not shown).

**[0037]** The scan driver 110 may receive the scan driving control signals SCS from the timing controller 150. The scan driver 110 may generate scan signals  $SS1$  to  $SS_n$  based on the received scan driving control signals SCS and may sequentially and respectively supply the scan signals  $SS1$  to  $SS_n$  to the scan lines  $S1$  to  $S_n$ . The scan driver 110 may sequentially supply emission control signals  $ES1$  to  $ES_n$  to the emission control lines  $E1$  to  $E_n$ . Each of the emission control signals  $ES1$  to  $ES_n$  may be supplied, e.g., changed from a low voltage signal to a high voltage signal, such that an "on" emission control signal, e.g., a high voltage signal, at least partially overlaps at least two of the scan signals  $SS1$  to  $SS_n$ . Therefore, in embodiments of the invention, a pulse width of the emission control signals  $ES1$  to  $ES_n$  may be equal to or larger than a pulse width of the scan signals  $SS1$  to  $SS_n$ .

**[0038]** The data driver 120 may receive the data driving control signals DCS from the timing controller 150. The data driver 120 may generate data signals  $DS1$  to  $DS_m$  based on the received data driving control signals DCS and the data DATA. The generated data signals  $DS1$  to  $DS_m$  may be supplied to the data lines  $D1$  to  $D_m$  in synchronization with the scan signals  $SS1$  to  $SS_n$  supplied to the scan lines  $S1$  to  $S_n$ . For example, when the 1<sup>st</sup> scan signal  $SS1$  is supplied, the generated data signals  $DS1$  to  $DS_m$  corresponding to the pixels 140(1)(1 to  $m$ ) may be synchronously supplied to the 1<sup>st</sup> to the  $m$ -th pixels in the 1<sup>st</sup> row via the data lines  $D1$  to  $D_m$ , and when the  $n$ th scan signal  $SS_n$  is supplied, the generated data signals  $DS1$  to  $DS_m$  corresponding to the pixels 140( $n$ )(1 to  $m$ ) may be synchronously supplied to the 1<sup>st</sup> to the  $m$ -th pixels in the  $n$ -th row via the data lines  $D1$  to  $D_m$ .

**[0039]** The data driver 120 may supply predetermined currents to the data lines  $D1$  to  $D_m$  during a first period of one horizontal period 1H for driving one or more of the pixels 140. For example, one horizontal period 1H may correspond to a complete period associated with one of the scan signals  $SS1$  to  $SS_n$  and a corresponding one of the data signals  $DS1$  to  $DS_m$  being supplied to the respective pixel 140 in order to drive the respective pixel 140. The data driver 120 may supply predetermined voltages to the data lines  $D1$  to  $D_m$  during a second period of the one horizontal period. For example, one horizontal period 1H may correspond to a complete period associated with one of the scan signals  $SS1$  to  $SS_n$  and a corresponding one of the data signals  $DS1$  to  $DS_m$  being supplied to the respective pixel 140 in order to drive the respective pixel 140. In embodiments of the invention, the data driver 120 may include at least one data driving circuit 200 for supplying such predetermined currents and predetermined voltages during the first and second periods of one horizontal period 1H. In the following description, the predetermined voltages that may be supplied to the data lines  $D1$  to  $D_m$  during the second period will be referred to as the data signals  $DS1$  to  $DS_m$ .

**[0040]** The pixel unit 130 may be connected to a first power source ELVDD for supplying a first voltage VDD, a second power source ELVSS for supplying a second voltage VSS and a reference power source ELVref for supplying a reference voltage Vref to the pixels 140. The first power source ELVDD, the second power source ELVSS and the reference power source ELVref may be externally provided. The pixels 140 may receive the first voltage VDD signal and the second voltage VSS signal, and may control the currents that flow through respective light emitting devices/materials, e.g., OLEDs, in accordance with the data signals  $DS1$  to  $DS_m$  that may be supplied by the data driver 120 to the pixels 140. The pixels 140 may thereby generate light components corresponding to the received data DATA.

**[0041]** Some or all of the pixels 140 may receive the first voltage VDD signal, the second voltage VSS signal and the

reference voltage Vref signal from the respective first, second and reference power sources ELVDD, ELVSS and ELVref. The pixels 140 may compensate for a voltage drop in the first voltage VDD signal and/or threshold voltage(s) using the reference voltage Vref signal. The amount of compensation may be based on a difference between voltage values of the reference voltage Vref signal and the first voltage VDD signal respectively supplied by the reference power source ELVref and the first power source ELVDD. The pixels 140 may supply respective currents from the first power source ELVDD to the second power source ELVSS via, for example, the OLEDs in response to the respective data signals DS1 to DS<sub>m</sub>. In embodiments of the invention, each of the pixels 140 may have, for example, the structure illustrated in FIG. 3 or 5.

**[0042]** FIG. 3 illustrates a circuit diagram of an nm-th exemplary pixel 140nm employable in the light emitting display illustrated in FIG. 2. For simplicity, FIG. 3 illustrates the nm-th pixel that may be the pixel provided at the intersection of the n-th row of scan lines S<sub>n</sub> and the m-th row of data lines D<sub>m</sub>. The nm-th pixel 140nm may be connected to the m-th data line D<sub>m</sub>, the n-1th and nth scan lines S<sub>n-1</sub> and S<sub>n</sub> and the nth emission control line E<sub>n</sub>. For simplicity, FIG. 3 only illustrates one exemplary pixel 140nm. In embodiments of the invention, the structure of the exemplary pixel 140nm may be employed for all or some of the pixels 140 of the light emitting display.

**[0043]** Referring to FIG. 3, the nm-th pixel 140nm may include a light emitting material/device, e.g., OLED<sub>nm</sub>, and an nm-th pixel circuit 142nm for supplying current to the associated light emitting material/device.

**[0044]** The nm-th OLED<sub>nm</sub> may generate light of a predetermined color in response to the current supplied from the nm-th pixel circuit 142nm. The nm-th OLED<sub>nm</sub> may be formed of organic material, phosphor and/or inorganic material.

**[0045]** In embodiments of the invention, the nm-th pixel circuit 142nm may generate a compensation voltage for compensating for variations within and/or among the pixels 140 such that the pixels 140 may display images with uniform brightness. The nm-th pixel circuit 142nm may generate the compensation voltage using a previously supplied scan signal of the scan signals SS1 to SS<sub>n</sub> during each scan cycle. In embodiments of the invention, one scan cycle may correspond to scan signals SS1 to SS<sub>n</sub> being sequentially supplied. Thus, in embodiments of the invention, during each cycle, the n-1th scan signal SS<sub>n-1</sub> may be supplied prior to the nth scan signal SS<sub>n</sub> and when the n-1th scan signal SS<sub>n-1</sub> is being supplied to the n-1th scan line of the light emitting display, the nm-th pixel circuit 142nm may employ the n-1th scan signal SS<sub>n-1</sub> to generate a compensation voltage. For example, the second pixel in the second column, i.e., the 2-2 pixel 140<sub>22</sub>, may generate a compensation voltage using the first scan signal SS1.

**[0046]** The compensation voltage may compensate for a voltage drop in a source voltage signal and/or a voltage drop resulting from a threshold voltage of the transistor of the nm-th pixel circuit 142nm. For example, the nm-th pixel circuit 142nm may compensate for a voltage drop of the first voltage VDD signal and/or a threshold voltage of a transistor, e.g., a threshold voltage of the fourth transistor M4<sub>nm</sub> of the pixel circuit 142nm based on the compensation voltage that may be generated using a previously supplied scan line during the same scan cycle.

**[0047]** In embodiments of the invention, the pixel circuit 142nm may compensate for a drop in the voltage of the first power source ELVDD and the threshold voltage of a fourth transistor M4<sub>nm</sub> when the n-1th scan signal SS<sub>n-1</sub> is supplied to the n-1th scan line S<sub>n-1</sub>, and may charge the voltage corresponding to the data signal when the nth scan signal SS<sub>n</sub> is supplied to the nth scan line S<sub>n</sub>. In embodiments of the invention, the pixel circuit 142nm may include first to sixth transistors M1<sub>nm</sub> to M6<sub>nm</sub>, a first capacitor C1<sub>nm</sub> and a second capacitor C2<sub>nm</sub> to help generate the compensation voltage and to drive the light emitting material/device.

**[0048]** A first electrode of the first transistor M1<sub>nm</sub> may be connected to the data line D<sub>m</sub> and a second electrode of the first transistor M1<sub>nm</sub> may be connected to a first node N1<sub>nm</sub>. A gate electrode of the first transistor M1<sub>nm</sub> may be connected to the nth scan line S<sub>n</sub>. The first transistor M1<sub>nm</sub> may be turned on when the nth scan signal SS<sub>n</sub> is supplied to the nth scan line S<sub>n</sub>. When the first transistor M1<sub>nm</sub> is turned on, the data line D<sub>m</sub> may be electrically connected to the first node N1<sub>nm</sub>.

**[0049]** A first electrode of the first capacitor C1<sub>nm</sub> may be connected to the first node N1<sub>nm</sub> and a second electrode of the first capacitor C1<sub>nm</sub> may be connected to the first power source ELVDD.

**[0050]** A first electrode of the second transistor M2<sub>nm</sub> may be connected to the data line D<sub>m</sub> and a second electrode of the second transistor M2<sub>nm</sub> may be connected to a second electrode of the fourth transistor M4<sub>nm</sub>. A gate electrode of a second transistor M2<sub>nm</sub> may be connected to the nth scan line S<sub>n</sub>. The second transistor M2<sub>nm</sub> may be turned on when the nth scan signal SS<sub>n</sub> is supplied to the nth scan line S<sub>n</sub>. When the second transistor M2<sub>nm</sub> is turned on, the data line D<sub>m</sub> may be electrically connected to the second electrode of the fourth transistor M4<sub>nm</sub>.

**[0051]** A first electrode of the third transistor M3<sub>nm</sub> may be connected to the reference power source ELVref and a second electrode of the third transistor M3<sub>nm</sub> may be connected to the first node N1<sub>nm</sub>. A gate electrode of the third transistor M3<sub>nm</sub> may be connected to the n-1th scan line S<sub>n-1</sub>. The third transistor M3<sub>nm</sub> may be turned on when the n-1th scan signal SS<sub>n-1</sub> is supplied to the n-1th scan line S<sub>n-1</sub>. When the third transistor M3<sub>nm</sub> is turned on, the reference voltage Vref may be electrically connected to the first node N1<sub>nm</sub>.

**[0052]** A first electrode of the fourth transistor M4<sub>nm</sub> may be connected to the first power source ELVDD and the second electrode of the fourth transistor M4<sub>nm</sub> may be connected to a first electrode of the sixth transistor M6<sub>nm</sub>. A gate electrode of the fourth transistor M4<sub>nm</sub> may be connected to the second node N2<sub>nm</sub>.

**[0053]** A first electrode of the second capacitor C2nm may be connected to the first node N1nm and a second electrode of the second capacitor C2nm may be connected to the second node N2nm.

**[0054]** In embodiments of the invention, the first and second capacitors C1nm and C2nm may be charged when the n-1th scan signal SSn-1 is supplied. In particular, the first and second capacitors C1nm and C2nm may be charged and the fourth transistor M4nm may supply a current corresponding to a voltage at the second node N2nm to the first electrode of the sixth transistor M6nm.

**[0055]** A second electrode of the fifth transistor M5nm may be connected to the second node N2nm and a first electrode of the fifth transistor M5nm may be connected to the second electrode of the fourth transistor M4nm. A gate electrode of the fifth transistor M5nm may be connected to the n-1th scan line Sn-1. The fifth transistor M5nm may be turned on when the n-1th scan signal SSn-1 is supplied to the n-1th scan line Sn-1 so that current flows through the fourth transistor M4nm. Therefore, the fourth transistor M4nm may operate as a diode.

**[0056]** The first electrode of the sixth transistor M6nm may be connected to the second electrode of the fourth transistor M4nm and a second electrode of the sixth transistor M6nm may be connected to an anode electrode of the nm-th OLEDnm. A gate electrode of the sixth transistor M6nm may be connected to the nth emission control line En. The sixth transistor M6nm may be turned off when an emission control signal ESn is supplied, e.g., a high voltage signal, to the nth emission control line En and may be turned on when no emission control signal, e.g., a low voltage signal, is supplied to the nth emission control line En.

**[0057]** In embodiments of the invention, the emission control signal ESn supplied to the nth emission control line En may be supplied to at least partially overlap both the n-1th scan signal SSn-1 that may be supplied to the n-1th scan line Sn-1 and the nth scan signal SSn that may be supplied to nth scan line Sn. Therefore, the sixth transistor M6nm may be turned off when the n-1th scan signal SSn-1 is supplied, e.g., a low voltage signal is supplied, to the n-1th scan line Sn-1 and the n-th scan signal SSn is supplied, e.g., a low voltage signal is supplied, to the nth scan line Sn so that a predetermined voltage may be charged in the first and second capacitors C1nm and C2nm. The sixth transistor M6nm may be turned on during other times to electrically connect the fourth transistor M4nm and the nm-th OLEDnm to each other. In the exemplary embodiment shown in FIG. 3, the transistors M1nm to M6nm are PMOS transistors, which may turn on when a low voltage signal is supplied to the respective gate electrode and may turn on when a high voltage signal is supplied to the respective gate electrode. However, embodiments of the present invention are not limited to the use of PMOS devices.

**[0058]** In the pixel illustrated in FIG. 3, the reference voltage Vref signal is not supplied to the respective OLEDs. Because the reference power source ELVref does not supply current to the pixels 140, a drop in the voltage of the reference voltage Vref may not occur. Therefore, it is possible to maintain the voltage value of the reference voltage Vref signal uniform regardless of the positions of the pixels 140. In embodiments of the invention, the voltage value of the reference voltage Vref may be equal to or different from the first voltage ELVDD.

**[0059]** FIG. 4 illustrates exemplary waveforms that may be employed for driving the exemplary nm-th pixel 140nm illustrated in FIG. 3. As shown in FIG. 4, each horizontal period 1H (complete period) for driving the nm-th pixel 140nm may be divided into a first period and a second period. During the first period (first partial period), predetermined currents (PC) may respectively flow through the data lines D1 to Dm. During the second period, the data signals DS1 to DSm may be supplied to the respective pixels 140 via the data lines D1 to Dm. During the first period (first partial period), the respective PCs may be supplied from each of the pixel(s) 140 to a data driving circuit 200 that may be capable of functioning, at least in part, as a current sink. During the second period (second partial period), the data signals DS1 to DSm may be supplied from the data driving circuit 200 to the pixel(s) 140. For simplicity, in the following description, it will be assumed that, at least initially, i.e., prior to any voltage drop that may result during operation of the pixels 140, the voltage value of the reference voltage Vref signal is equal to the voltage value of the first voltage VDD signal.

**[0060]** Exemplary methods of operating the nm-th pixel circuit 142nm of the nm-th pixel 140nm of the pixels 140 will be described in detail with reference to FIGS. 3 and 4. First, the n-1th scan signal SSn-1 may be supplied to the n-1th scan line Sn-1 to control the on/off operation of the m pixels that may be connected to the n-1th scan line Sn-1. When the scan signal SSn-1 is supplied to the n-1th scan line Sn-1, the third and fifth transistors M3nm and M5nm of the nm-th pixel circuit 142nm of the nm pixel 140nm may be turned on. When the fifth transistor M5nm is turned on, current may flow through the fourth transistor M4nm so that the fourth transistor M4nm may operate as a diode. When the fourth transistor M4nm operates as a diode, the voltage value of the second node N2nm may correspond to a difference between the threshold voltage of the fourth transistor M4nm and the voltage of the first voltage VDD signal being supplied by the first power source ELVDD.

**[0061]** More particularly, when the third transistor M3nm is turned on, the reference voltage Vref signal from the reference power source ELVref may be applied to the first node N1nm. The second capacitor C2nm may be charged with a voltage corresponding to the difference between the first node N1nm and the second node N2nm. In embodiments of the invention in which the reference voltage Vref signal from the reference power source ELVref and the first voltage VDD from the first power source ELVDD may, at least initially, i.e., prior to any voltage drop that may result during operation of the pixels 140, be equal, the voltage corresponding to the threshold voltage of the fourth transistor M4nm

may be charged in the second capacitor C2nm. In embodiments of the invention in which a predetermined drop in voltage of the first voltage VDD signal occurs, the threshold voltage of the fourth transistor M4nm and a voltage corresponding to the magnitude of the voltage drop of the first power source ELVDD may be charged in the second capacitor C2nm.

5 [0062] In embodiments of the invention, during the period where the n-1th scan signal SSn-1 may be supplied to the n-1th scan line Sn-1, a predetermined voltage corresponding to the sum of the voltage corresponding to the voltage drop of the first voltage VDD signal and the threshold voltage of the fourth transistor M4nm may be charged in the second capacitor C2nm. By storing the voltage corresponding to a sum of the voltage drop of the first voltage VDD signal from the first power source ELVDD and the threshold voltage of the fourth transistor M4nm during operation of the respective n-1 pixel of in the m-th column, it is possible to later utilize the stored voltage to compensate for both the voltage drop of the first voltage VDD signal and the threshold voltage during operation of the respective nm-th pixel 140nm.

10 [0063] In embodiments of the invention, the voltage corresponding to the sum of the threshold voltage of the fourth transistor M4nm and the difference between the reference voltage signal Vref and the first voltage VDD signal may be charged in the second capacitor C2nm before the nth scan signal SSn is supplied to the nth scan line Sn. When the nth scan signal SSn is supplied to the nth scan line Sn, the first and second transistors M1nm and M2nm may be turned on. During the first period of one horizontal period, when the second transistor M2nm of the pixel circuit 142nm of the nm-th pixel 140nm is turned on, the PC may be supplied from the nm-th pixel 140nm to the data driving circuit 200 via the data line Dm. In embodiments of the invention, the PC may be supplied to the data driving circuit 200 via the first power source ELVDD, the fourth transistor M4nm, the second transistor M2nm and the data line Dm. A predetermined voltage may then be charged in the first and second capacitors C1nm and C2nm in response to the supplied PC.

15 [0064] The data driving circuit 200 may reset a voltage of a gamma voltage unit (not shown) based on a predetermined voltage value, i.e., compensation voltage that may be generated when the PC sinks, as described above. The reset voltage from the gamma voltage unit (not shown) may be used to generate the data signals DS1 to DSm to be respectively supplied to the data lines D 1 to Dm.

20 [0065] In embodiments of the invention, the generated data signals DS1 to DSm may be respectively supplied to the respective data lines D1 to Dm during the second period of the one horizontal period. More particularly, e.g., the respective generated data signal DSm may be supplied to the respective first node N1nm via the first transistor M1nm during the second period of the one horizontal period. Then, the voltage corresponding to difference between the data signal DSm and the first power source ELVDD may be charged in the first capacitor C1nm. The second node N2nm may then float and the second capacitor C2nm may maintain the previously charged voltage.

25 [0066] In embodiments of the invention, during the period when the n-1 pixel in the m-th column is being controlled and the scan signal SSn-1 is being supplied to the previous scan line Sn-1, a voltage corresponding to the threshold voltage of the fourth transistor M4nm and the voltage drop of the first voltage VDD signal from the first power source ELVDD may be charged in the second capacitor C2nm of the nm-th pixel 140nm to compensate for the voltage drop of the first voltage VDD signal from the first power source ELVDD and the threshold voltage of the fourth transistor M4nm.

30 [0067] In embodiments of the invention, during the period when the n-th scan signal Sn is supplied to the n-th scan line Sn, the voltage of the gamma voltage unit (not shown) may be reset so that the electron mobility of the transistors included in the respective n-th pixels 140n associated with each data line D1 to Dm may be compensated for and the respective generated data signals DS1 to DSm may be supplied to the n-th pixels 140n using the respective reset gamma voltages. Therefore, in embodiments of the invention, non-uniformity in the threshold voltages of the transistors and the electron mobility may be compensated, and images with uniform brightness may be displayed. Processes for resetting the voltage of the gamma voltage unit will be described below.

35 [0068] FIG. 5 illustrates another exemplary embodiment of an nm-th pixel 140nm' employable by the light emitting display illustrated in FIG. 2. The structure of the nm-th pixel 140nm' illustrated in FIG. 5 is substantially the same as the structure of the nm-th pixel 140nm illustrated in FIG. 3, but for the arrangement of a first capacitor C1nm' in a pixel circuit 142nm' and respective connections to a first node N1nm' and a second node N2nm'. In the exemplary embodiment illustrated in FIG. 5, a first electrode of the first capacitor C1nm' may be connected to the first node N1nm' and a second electrode of the first capacitor C1nm' may be connected to the first power source ELVDD. A first electrode of the second capacitor C2nm may be connected to the first node N1nm' and a second electrode of the second capacitor C2nm may be connected to the second node N2nm'. The first node N1nm' may be connected to the second electrode of the first transistor M1nm, the second electrode of the third transistor M3nm and the first electrode of the second capacitor C2nm. The second node N2nm' may be connected to the gate electrode of the fourth transistor M4nm, the second electrode of the fifth transistor M5nm, the first electrode of the first capacitor C1nm' and the second electrode of the second capacitor C2nm.

40 [0069] In the following description, the same reference numerals employed above in the description of the nm-th pixel 140nm shown in FIG. 3 will be employed to describe like features in the exemplary embodiment of the nm-th pixel 140nm' illustrated in FIG. 5.

45 [0070] Exemplary methods for operating the nm-th pixel circuit 142nm' of the nm-th pixel 140nm' of the pixels 140 will be described in detail with reference to FIGS. 4 and 5. First, during a horizontal period for driving the n-1 pixels 140(n-

1)(1 to m), i.e., the pixels arranged in the (n-1)th row, when the n-1th scan signal SS<sub>n-1</sub> is supplied to the n-1th scan line Sn-1, the third and fifth transistors M3<sub>nm</sub> and M5<sub>nm</sub> of the n-th pixel(s) 140(n)(1 to m), i.e., the pixels arranged in the n-th row, may be turned on.

5 **[0071]** When the fifth transistor M5<sub>nm</sub> is turned on, current may flow through the fourth transistor M4<sub>nm</sub> so that the fourth transistor M4<sub>nm</sub> may operate as a diode. When the fourth transistor M4<sub>nm</sub> operates as a diode, a voltage corresponding to a value obtained by subtracting the threshold voltage of the fourth transistor M4<sub>nm</sub> from the first power source ELVDD may be applied to a second node N2<sub>nm</sub>'. The voltage corresponding to the threshold voltage of the fourth transistor M4<sub>nm</sub> may be charged in the first capacitor C1<sub>nm</sub>'. As shown in FIG. 5, the first capacitor C1<sub>nm</sub>' may be provided between the second node N2<sub>nm</sub>' and the first power source ELVDD.

10 **[0072]** When the third transistor M3<sub>nm</sub> is turned on, the voltage of the reference power source ELVref may be applied to the first node N1<sub>nm</sub>'. Then, the second capacitor C2<sub>nm</sub> may be charged with the voltage corresponding to difference between a first node N1<sub>nm</sub>' and the second node N2<sub>nm</sub>'. During the period where the n-1th scan signal SS<sub>n-1</sub> is supplied to the n-1th scan line Sn-1 and the first and second transistors M1<sub>nm</sub> and M2<sub>nm</sub> may be turned off, the data signal DS<sub>m</sub> may not be supplied to the nm-th pixel 140<sub>nm</sub>'.

15 **[0073]** Then, during the first period of the one horizontal period for driving the nm-th pixel 140<sub>nm</sub>', the scan signal SS<sub>n</sub> may be supplied to the nth scan line Sn and the first and second transistors M1<sub>nm</sub> and M2<sub>nm</sub> may be turned on. When the second transistor M2<sub>nm</sub> is turned on, during the first period of the one horizontal period, the respective PC may be supplied from the nm-th pixel 140<sub>nm</sub>' to the data driving circuit 200 via the data line D<sub>m</sub>. The PC may be supplied to the data driving circuit 200 via the first power source ELVDD, the fourth transistor M4<sub>nm</sub>, the second transistor M2<sub>nm</sub> and the data line D<sub>m</sub>. In response to the PC, predetermined voltage may be charged in the first and second capacitors C1<sub>nm</sub>' and C2<sub>nm</sub>.

**[0074]** The data driving circuit 200 may reset the voltage of the gamma voltage unit using the compensation voltage applied in response to the PC to generate the data signal DS using the respectively reset voltage of the gamma voltage unit.

25 **[0075]** Then, during the second period of the one horizontal period for driving the nm-th pixel 140<sub>nm</sub>', the data signal DS<sub>m</sub> may be supplied to the first node N1<sub>nm</sub>'. The predetermined voltage corresponding to the data signal DS<sub>m</sub> may be charged in the first and second capacitors C1<sub>nm</sub>' and C2<sub>nm</sub>.

30 **[0076]** When the data signal DS<sub>m</sub> is supplied, the voltage of the first node N1<sub>nm</sub>' may fall from the voltage Vref of the reference power source ELVref to the voltage of the data signal DS<sub>m</sub>. At this time, as the second node N2<sub>nm</sub>' may be floating, the voltage value of the second node N2<sub>nm</sub>' may be reduced in response to the amount of voltage drop of the first node N1<sub>nm</sub>'. The amount of reduction in voltage that may occur at the second node N2<sub>nm</sub>' may be determined by the capacitances of the first and second capacitors C1<sub>nm</sub>' and C2<sub>nm</sub>.

35 **[0077]** When the voltage of the second node N2<sub>nm</sub>' falls, the predetermined voltage corresponding to the voltage value of the second node N2<sub>nm</sub>' may be charged in the first capacitor C1<sub>nm</sub>'. When the voltage value of the reference power source ELVref is fixed, the amount of voltage charged in the first capacitor C1<sub>nm</sub>' may be determined by the data signal DS<sub>m</sub>. That is, in the nm-th pixel 140<sub>nm</sub>' illustrated in FIG. 5, because the voltage values charged in the capacitors C1<sub>nm</sub>' and C2<sub>nm</sub> may be determined by the reference power source ELVref and the data signal DS<sub>m</sub>, it may be possible to charge a desired voltage irrespective of the voltage drop of the first power source ELVDD.

40 **[0078]** In embodiments of the invention, the voltage of the gamma voltage unit may be reset so that the electron mobility of the transistors included in each of the pixels 140 may be compensated for and the respective generated data signal may be supplied using the reset gamma voltage. In embodiments of the invention, non-uniformity among the threshold voltages of the transistors and deviation in the electron mobility of the transistors may be compensated for, thereby enabling images with uniform brightness to be displayed.

45 **[0079]** FIG. 6 illustrates a block diagram of a first exemplary embodiment of the data driving circuit illustrated in FIG. 2. For simplicity, in FIG. 6, it is assumed that the data driving circuit 200 has j channels, where j is a natural number equal to or greater than 2.

**[0080]** As shown in FIG. 6, the data driving circuit 200 may include a shift register unit 210, a sampling latch unit 220, a holding latch unit 230, a gamma voltage unit 240, a digital-analog converter unit (hereinafter, referred to as a DAC) 250, a first buffer unit 270, a second buffer unit 260, a current supply unit 280 and a selector 290.

50 **[0081]** The shift register unit 210 may receive a source shift clock SSC and a source start pulse SSP from the timing controller 150. The shift register unit 210 may utilize the source shift clock SSC and the source start pulse SSP to sequentially generate j sampling signals while shifting the source start pulse SSP every one period of the source shift clock SSC. The shift register unit 210 may include j shift registers 2101 to 210j.

55 **[0082]** The sampling latch unit 220 may sequentially store the respective data DATA in response to sampling signals sequentially supplied from the shift register unit 210. The sampling latch unit 220 may include j sampling latches 2201 to 220j in order to store the j data DATA. Each of the sampling latches 2201 to 220j may have the magnitude corresponding to the number of bits of the data DATA. For example, when the data DATA is composed of k bits, each of the sampling latches 2201 to 220j may have the magnitude of k bits.

**[0083]** The holding latch unit 230 may receive the data DATA from the sampling latch unit 220 to store the data DATA

when a source output enable SOE signal is input. The holding latch unit 230 may supply the data DATA stored therein when the SOE signal is input to the DAC unit 250. The holding latch unit 230 may include j holding latches 2301 to 230j in order to store the j data DATA. Each of the holding latches 2301 to 230j may have a magnitude corresponding to the number of bits of the data DATA. For example, each of the holding latches 2301 to 230j may have the magnitude of k bits so that the respective data DATA may be stored.

**[0084]** The gamma voltage unit 240 may include j voltage generators 2401 to 240j for generating a predetermined gray scale voltage in response to the data DATA of k bits. As illustrated in FIG. 8, each of the voltage generators 2401 to 240j may include a plurality of voltage dividing resistors R1 to R/ for generating  $2^k$  gray scale voltages. The voltage generators 2401 to 240j may reset values of the gray scale voltages using the compensation voltage supplied from the second buffer 260 and may supply the reset gray scale voltages to the DACs 2501 to 250j.

**[0085]** The DAC unit 250 may include j DACs 2501 to 250j that may generate the data signals DS in response to the bit values of the data DATA. Each of the DACs 2501 to 250j may select one of the plurality of gray scale voltages in response to the bit values of the data DATA supplied from the holding latch unit 230 to generate respective data signals DS1 to DSj.

**[0086]** The first buffer unit 270 may supply the data signals DS supplied from the DAC unit 250 to the selector 290. The first buffer unit 270 may include j first buffers 2701 to 270j.

**[0087]** The selector 290 may control electrical connections between the data lines D1 to Dj and the first buffers 2701 to 270j. The selector 290 may electrically connect the data lines D1 to Dj and the first buffers 2701 to 270j to each other during the second period of the one horizontal period. In embodiments of the invention, the selector 290 may electrically connect the data lines D1 to Dj and the first buffers 2701 to 270j to each other only during the second period. During periods other than the second period, the selector 290 may keep the data lines D1 to Dj and the first buffers 2701 to 270j electrically disconnected from each other.

**[0088]** The selector 290 may include j switching units 2901 to 290j. The generated respective data signals DS1 to DSj may be respectively supplied from the first buffers 2701 to 270j to the data lines D1 to Dj via the switching units 2901 to 290j. In embodiments of the invention, the selector 290 may employ other types of switching units. Fig. 10 illustrates another exemplary embodiment of a switching unit switching unit 291j that may be employed by the selector 290.

**[0089]** The current supply unit 280 may sink the PC from the pixels 140 connected to the data lines D1 to Dj during the first period of the one horizontal period. For example, the current supply unit 280 may sink the current from each of the pixels 140. As discussed below, the amount of current that each pixel may sink to the current supply unit 280 may correspond to or may be greater than a minimum amount of current to be supplied to the respective OLED for the respective one of the pixels 140 to emit light with the maximum brightness. The current supply unit 280 may help enable predetermined compensation voltages to be respectively generated when the respective currents sink to the second buffer unit 260. The current supply unit 280 may include j current sink units 2801 to 280j.

**[0090]** The second buffer unit 260 may supply the compensation voltage supplied from the current supply unit 280 to the gamma voltage unit 240. Therefore, the second buffer unit 260 may include j second buffers 2601 to 260j.

**[0091]** In embodiments of the invention, as illustrated in FIG. 7, the data driving circuit 200 may further include a level shifter unit 300. The level shifter unit 300 may be connected to the holding latch unit 230 and the DAC unit 250. The level shifter unit 300 may increase or decrease voltage levels of the data DATA supplied from the holding latch unit 230 before supplying the data DATA to the DAC unit 250. When the data DATA being supplied from an external system to the data driving circuit 200 has high voltage levels, circuit components with high voltage resistant properties should generally be provided in response to the voltage levels, thereby increasing the manufacturing cost. In embodiments of the invention, the data DATA being supplied from an external system to the data driving circuit 200 may have low voltage levels and the low voltage level may be transitioned to a high voltage level by the level shifter unit 300.

**[0092]** FIG. 8 illustrates a first embodiment of a connection scheme for connecting the voltage generator 240j, the DAC 250j, the first buffer 270j, the second buffer 260j, the switching unit 290j, the current sink unit 280j and a pixel 140nj in a specific channel. For simplicity, FIG. 8 only illustrates one channel, i.e., the jth channel and it is assumed that the data line Dj is connected to an nj-th pixel 140nj according to the exemplary embodiment of the nm-th pixel 140nm illustrated in FIG. 3.

**[0093]** As shown in FIG. 8, the voltage generator 240j may include a plurality of voltage dividing resistors R1 to R/. The voltage dividing resistors R1 to R/ may be positioned between the reference power source ELVref and the second buffer 260j and may divide voltages supplied thereto. The voltage dividing resistors R1 to R/ may divide the voltage between the voltage of the reference power source ELVref and the compensation voltage supplied from the second buffer 260j and may generate a plurality of gray scale voltages V0 to  $2^{k-1}$ . The generated plurality of gray scale voltages V0 to  $2^{k-1}$  may be supplied to the generated gray scale voltages V0 to  $2^{k-1}$  to the DAC 250j.

**[0094]** The DAC 250j may select one gray scale voltage among the gray scale voltages V0 to  $2^{k-1}$  in response to the bit values of the data DATA and may supply the selected gray scale voltage to the first buffer 270j. The gray scale voltage selected by the DAC 250j may be used as the respective data signal DSj. The first buffer 270j may transmit the data signal DSj supplied from the DAC 250j to the switching unit 290j.

**[0095]** The switching unit 290j may include an 11<sup>th</sup> transistor M11j. The 11<sup>th</sup> transistor M11j may be controlled by a first control signal CS1, as illustrated in FIG. 8. As shown in FIG. 9, in embodiments of the invention, the 11<sup>th</sup> transistor M11j may be turned on during the second period of the one horizontal period 1H and may be turned off during the first period of the one horizontal period 1H via the first control signal CS1. The data signal DSj may be supplied to the data line Dj during the second period of the one horizontal period 1H. In embodiments of the invention, the data signal DS may only be supplied to the data line Dj during the second period of the one horizontal period and may not be supplied during the first period or other period(s).

**[0096]** The current sink unit 280j may include 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j, a current source I<sub>maxj</sub> and a third capacitor C3j. The current source I<sub>maxj</sub> may be connected to a first electrode of the 13<sup>th</sup> transistor M13j. The third capacitor C3j may be connected between a third node N3j and a ground voltage source GND. The 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j may be controlled by a second control signal CS2. A first electrode of the 12<sup>th</sup> transistor M12 may also be connected to the third node N3j.

**[0097]** A gate electrode of the 12<sup>th</sup> transistor M12j may be connected to a gate electrode of the 13<sup>th</sup> transistor M13j. The gate electrodes of the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j, M13j may receive the second control signal CS2. A second electrode of the 12<sup>th</sup> transistor M12j may be connected to a second electrode of the 13<sup>th</sup> transistor M13j and the data line Dj. The first electrode of the 12<sup>th</sup> transistor M12j may be connected to the second buffer 260j. The 12<sup>th</sup> transistor M12j may be turned on during the first period of the one horizontal period 1H by the second control signal CS2 and may be turned off during the second period of the one horizontal period 1H.

**[0098]** The gate electrode of the 13<sup>th</sup> transistor M13j may be connected to the gate electrode of the 12<sup>th</sup> transistor M12j and the second electrode of the 13<sup>th</sup> transistor may be connected to the data line Dj. The first electrode of the 13<sup>th</sup> transistor M13j may be connected to the current source I<sub>maxj</sub>. The 13<sup>th</sup> transistor M13j may be turned on by the second control signal CS2 during the first period of the one horizontal period 1H and may be turned off during the second period of the one horizontal period 1H.

**[0099]** During the first period when the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j may be turned on, the current source I<sub>maxj</sub> may receive, from the respective pixel 140nj, the minimum current that may be required by the OLED to enable the pixel 140nj to emit light with the maximum brightness.

**[0100]** The third capacitor C3j may store the compensation voltage applied to the third node N3j when the current is being supplied by the respective pixel 140nj to the current source I<sub>maxj</sub>. The third capacitor C3j may charge the compensation voltage applied to the third node N3j during the first period and may maintain the compensation voltage of the third node N3j uniform even if the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j may be turned off.

**[0101]** The second buffer 260j may transmit the compensation voltage applied to the third node N3j to the voltage generator 240j. In particular, the second buffer 260j may transmit the voltage charged in the third capacitor C3j to the voltage generator 240j. The voltage generator 240j may divide the voltage between the voltage of the reference voltage V<sub>ref</sub> supplied by the reference power source ELV<sub>ref</sub> and the compensation voltage supplied from the second buffer 260j. The compensation voltage applied to the third node N3j may be set based on the electron mobility and/or threshold voltages of the transistors respectively included in those pixels of the pixels 140 associated with the j-th data line Dj. The compensation voltage supplied to the j voltage generators 2401 to 240j may be determined by the pixel 140nj currently receiving the respective data signal DSj via data line Dj.

**[0102]** In embodiments of the invention in which different compensation voltages are supplied to the j voltage generators 2401 to 240j, the values of the gray scale voltages V<sub>0</sub> to V<sub>2<sup>k</sup>-1</sub> supplied to the DACs 2501 to 250j provided in the j channels may be set to be different from each other. In embodiments of the invention, the gray scale voltages V<sub>0</sub> to V<sub>2<sup>k</sup>-1</sub> may be controlled by the pixels 140 connected to the data lines D1 to Dj and the pixel unit 130 may display images having uniform brightness even when the electron mobility of the transistors included in the pixels 140 is not uniform. In embodiments of the invention, the pixels 140 may emit light of maximum brightness when the highest of the gray scale voltages V<sub>0</sub> to V<sub>2<sup>k</sup>-1</sub> is employed as the respective data signal DS.

**[0103]** FIG. 9 illustrates exemplary driving waveforms that may be supplied to the switching unit 290j, the current sink unit 280j and the pixel 140nj illustrated in FIG. 8.

**[0104]** Processes for controlling the respective voltages of the data signals DS supplied to the pixels 140 will be described in detail with reference to FIGS. 8 and 9. In the exemplary embodiment illustrated in FIG. 8, the pixel 140nj and the pixel circuit 142nj, according to the exemplary embodiment illustrated in FIG. 3 is provided. In the following description, the same reference numerals employed above in the description of the nm-th pixel 140nm shown in FIG. 3 will be employed to describe like features in the exemplary embodiment of the nj-th pixel 140nj illustrated in FIG. 8.

**[0105]** First, the scan signal SS<sub>n-1</sub> may be supplied to the n-1th scan line S<sub>n-1</sub>. When the scan signal SS<sub>n-1</sub> is supplied to the n-1th scan line S<sub>n-1</sub>, the third and fifth transistors M3nj and M5nj may be turned on. The voltage value obtained by subtracting the threshold voltage of the fourth transistor M4nj from the first power source ELVDD may then be applied to a second node N2nj and the voltage of the reference power source ELV<sub>ref</sub> may be applied to a first node N1nj. The voltage corresponding to the voltage drop of the first power source ELVDD and the threshold voltage of the fourth transistor M4nj may then be charged in the second capacitor C2nj.

[0106] The voltages applied to the first node N1nj and the second node N2nj may be represented by EQUATION1 and EQUATION2.

[EQUATION1]

$$V_{N1} = V_{ref}$$

[EQUATION2]

$$V_{N2} = ELVDD - |V_{thM4}|$$

[0107] In EQUATION1 and EQUATION2,  $V_{N1}$ ,  $V_{N2}$ , and  $V_{thM4}$  represent the voltage applied to the first node N1nj, the voltage applied to the second node N2nj, and the threshold voltage of the fourth transistor M4nj, respectively.

[0108] From the time when the scan signal SSn-1 is supplied to the n-1th scan line Sn-1 is turned off to the time when the scan signal SSn is supplied to the nth scan line Snj, the first and second nodes N1nj and N2nj may be floating. Therefore, the voltage value charged in the second capacitor C2nj may not change during that time.

[0109] The n-th scan signal SSn may then be supplied to the nth scan line Sn so that the first and second transistors M1nj and M2nj may be turned on. When the scan signal SSn is being supplied to the nth scan line Sn, during the first period of the one horizontal period when the n-th scan line Sn is being driven, the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j may be turned on. When the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j are turned on, the current that may flow through the current source Imaxj via the first power source ELVDD, the fourth transistor M4nj, the second transistor M2nj, the data line Dj, and the 13<sup>th</sup> transistor M13j may sink.

[0110] When current flows through the current source Imaxj via the first power source ELVDD, the fourth transistor M4nj and the second transistor M2nj, EQUATION3 may apply.

[EQUATION3]

$$I_{max} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (ELVDD - V_{N2} - |V_{thM4}|)^2$$

[0111] In EQUATION3,  $\mu$ ,  $C_{ox}$ ,  $W$ , and  $L$  represent the electron mobility, the capacitance of an oxide layer, the width of a channel, and the length of a channel, respectively.

[0112] The voltage applied to the second node N2nj when the current obtained by EQUATION3 flows through the fourth transistor M4nj may be represented by EQUATION4.

[EQUATION4]

$$V_{N2} = ELVDD - \sqrt{\frac{2I_{max}}{\mu_p C_{ox}} \frac{L}{W}} - |V_{thM4}|$$

[0113] The voltage applied to the first node N1nj may be represented by EQUATION5 by the coupling of the second capacitor C2nj.

[EQUATION5]

$$V_{N1} = V_{ref} - \sqrt{\frac{2I_{max}}{\mu_p C_{ox}} \frac{L}{W}} = V_{N3} = V_{N4}$$

[0114] In EQUATION5, the voltage  $V_{N1}$  may correspond to the voltage applied to the first node N1nj, the voltage  $V_{N3}$  may correspond to the voltage applied to the third node N3j and the voltage  $V_{N4}$  may correspond to the voltage applied to a fourth node N4j. In embodiments of the invention, the voltage  $V_{N1}$  applied to the first node N1nj may be equal to the voltage  $V_{N3}$  applied to the third node N3 and the voltage  $V_{N4}$  applied to the fourth node N4j. When the current is being supplied to the current source  $I_{maxj}$ , the voltage value obtained by EQUATION5 may be applied to the fourth node N4j.

[0115] As seen in EQUATION5, the voltage applied to the third node N3j and the fourth node N4j may be affected by the electron mobility of the transistors included in the pixel 140nj, which is supplying current to the current source  $I_{maxj}$ . Therefore, the voltage value applied to the third node N3j and the fourth node N4j when the current is being supplied to the current source  $I_{maxj}$  may vary in each of the pixels 140 (when the electron mobility varies in each of the pixels 140).

[0116] On the other hand, when the voltage obtained by EQUATION5 is applied to the fourth node N4j, the voltage  $V_{diff}$  of the voltage generator 240j may be represented by EQUATION6.

[EQUATION6]

$$V_{diff} = V_{ref} - \left( V_{ref} - \sqrt{\frac{2I_{max}}{\mu_p C_{ox}} \frac{L}{W}} \right)$$

[0117] When the DAC 250j selects the hth gray scale voltage among f gray scale voltages in response to the data DATA, the voltage  $V_b$  supplied to the first buffer 270j may be represented by EQUATION7. In EQUATION7, h may be a natural number equal to or less than f and f may be a natural number.

[EQUATION7]

$$V_b = V_{ref} - \frac{h}{f} \sqrt{\frac{2I_{max}}{\mu_p C_{ox}} \frac{L}{W}}$$

[0118] In embodiments of the invention in which current sink corresponding to a minimum amount of current required by the respective light emitting material/device for displaying light of a maximum brightness sinks to the respective current source during the first period, after the current sinks during the first period, the voltage  $V_b$  obtained by EQUATION5 may be charged and supplied to the first buffer 270j. During the second period, the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j may be turned off, and the 11<sup>th</sup> transistor M11j may be turned on. During this time, the third capacitor C3j may maintain the voltage amount charged therein and, therefore, the voltage value of the third node N3j may be maintained, as illustrated in EQUATION5.

[0119] In embodiments of the invention, the 11<sup>th</sup> transistor M11 may be turned on during the second period and the voltage supplied to the first buffer 270j may be supplied to the first node N1nj via the 11<sup>th</sup> transistor M11j, the data line Dj, and the first transistor M1nj. In such embodiments of the invention, the voltage obtained by EQUATION7 may be supplied to the first node N1nj. The voltage applied to the second node N2nj by the coupling of the second capacitor C2nj may be represented by EQUATION8.

[EQUATION8]

$$V_{N2} = ELVDD - \frac{h}{f} \sqrt{\frac{2I_{max}}{\mu_p C_{OX}} \frac{L}{W}} - |V_{thM4}|$$

[0120] In embodiments of the invention, the current flowing via the fourth transistor M4nj may be represented by EQUATION9.

[EQUATION9]

$$\begin{aligned} I_{N4} &= \frac{1}{2} \mu_p C_{OX} \frac{W}{L} (ELVDD - V_{N2} - |V_{thM4}|)^2 \\ &= \frac{1}{2} \mu_p C_{OX} \frac{W}{L} \left( ELVDD - \left( ELVDD - \frac{h}{f} \sqrt{\frac{2I_{max}}{\mu_p C_{OX}} \frac{L}{W}} - |V_{thM4}| \right) - V_{thM4} \right)^2 \\ &= \left( \frac{h}{f} \right)^2 I_{max} \end{aligned}$$

[0121] Referring to EQUATION9, in embodiments of the invention, the current flowing through the fourth transistor M4nj may be determined by the gray scale voltage generated by the voltage generator 240j. In embodiments of the invention, the current corresponding to the gray scale voltage selected by the DAC 250j may flow to the fourth transistor M4nj irrespective of the threshold voltage and electron mobility of the fourth transistor M4nj. As discussed above, embodiments of the invention enable the display of images with uniform brightness.

[0122] In embodiments of the invention, as discussed above, different switching units may be employed. FIG. 10 illustrates the connection scheme illustrated in FIG. 8 employing another embodiment of a switching unit 291j. The exemplary connection scheme illustrated in FIG. 10 is substantially the same as the exemplary connection scheme illustrated in FIG. 8, but for another exemplary embodiment of the switching unit 291j. In the following description, the same reference numerals employed above will be employed to describe like features in the exemplary embodiment illustrated in FIG. 10.

[0123] As shown in FIG. 10, another exemplary switching unit 291j may include 11<sup>th</sup> and 14<sup>th</sup> transistors M11j, M14j that may be connected to each other in the form of a transmission gate. The 14<sup>th</sup> transistor M14j, which may be a PMOS type transistor, may receive the second control signal CS2. The 11<sup>th</sup> transistor M11j, which may be a NMOS type transistor, may receive the first control signal CS1. In such embodiments, when the polarity of the first control signal CS1 is opposite to the polarity of the second control signal CS2, the 11<sup>th</sup> and 14<sup>th</sup> transistors M11j and M14j may be turned on and off at the same time.

[0124] In embodiments of the invention in which the 11<sup>th</sup> and 14<sup>th</sup> transistors M11j and M14j are connected to each other in the form of the transmission gate, a voltage-current characteristic curve may be in the form of a straight line and switching error may be minimized.

[0125] FIG. 11 illustrates a second exemplary embodiment of a connection scheme for connecting voltage generator 240j, the DAC 250j, the first buffer 270j, the second buffer 260j, the switching unit 290j, the current sink unit 280j and the pixel 140 in a specific channel. The exemplary connection scheme illustrated in FIG. 11 is substantially the same as the exemplary connection scheme illustrated in FIG. 8. The exemplary connection scheme illustrate in FIG. 11 employs an exemplary pixel 140nj', according to the exemplary pixel 140nm' shown in FIG. 5. In the following description, the same reference numerals employed above will be employed to describe like features in the exemplary embodiment illustrated in FIG. 11. Therefore, the voltage supplied to the pixel 140nj' will be only briefly described below.

[0126] Referring to FIGS. 9 and 11, when the scan signal Ssn-1 is supplied to the n-1<sup>th</sup> scan line Sn-1, the voltages

obtained by EQUATION and EQUATION2 may be respectively applied to the first and second nodes N1nj' and N2nj' of pixel circuit 142nj'.

[0127] The current that may flow through the fourth transistor M4nj during the first period when the scan signal SSn may be supplied to the nth scan line Sn and the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j may be turned on may be represented by EQUATION3. The voltage that may be applied to the second node N2nj' during the first period when the scan signal SSn is supplied to the nth scan line Sn and the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j may be turned on may be represented by EQUATION4.

[0128] The voltage applied to the first node N1nj' by the coupling of the second capacitor C2nj may be represented by EQUATION10.

[EQUATION10]

$$V_{M1} = V_{ref} - \left( \frac{C1+C2}{C2} \right) \sqrt{\frac{2I_{max}}{\mu_p C_{ox}} \frac{L}{W}} = V_{N3} = V_{N4}$$

[0129] In embodiments of the invention, the voltage applied to the first node N1nj' may be supplied to the third node N3j and the fourth node N4j and the voltage V<sub>diff</sub> of the voltage generator 240j may be represented by EQUATION11.

[EQUATION11]

$$V_{diff} = V_{ref} - \left( V_{ref} - \left( \frac{C1+C2}{C2} \right) \sqrt{\frac{2I_{max}}{\mu_p C_{ox}} \frac{L}{W}} \right)$$

[0130] When the DAC 250j selects the hth gray scale voltage among f gray scale voltages, the voltage Vb supplied to the first buffer 270j may be represented by EQUATION12.

[EQUATION12]

$$Vb = V_{ref} - \frac{h}{f} \left( \frac{C1+C2}{C2} \right) \sqrt{\frac{2I_{max}}{\mu_p C_{ox}} \frac{L}{W}}$$

[0131] The voltage supplied to the first buffer 270j may be supplied to the first node N1nj'. The voltage applied to the second node N2nj' may be represented by EQUATION8. The current that flows through the fourth transistor M4nj may be represented by EQUATION9.

[0132] In embodiments of the invention, the current supplied to the respective OLEDnj via the fourth transistor M4nj may be determined by the gray scale voltage regardless of the threshold voltage and electron mobility of the fourth transistor M4nj. Embodiments of the invention enable images with uniform brightness to be displayed.

[0133] In some embodiments of the invention, e.g., embodiments employing the pixel 140nj' illustrated in FIG. 11, the voltage of the second node N2nj' may change gradually although the voltage of the first node N1nj' may change rapidly, i.e., (C1+C2)/C2. When the pixel 140nj' illustrated in FIG. 11 is employed, a greater voltage range may be set for the voltage generator 240j than a voltage range that may be set for the voltage generator 240j when the pixel 140nj illustrated in FIG. 8 is employed. As discussed above, when the voltage range of the voltage generator 240j is set to be larger, it is possible to reduce the influence of the switching error of the 11<sup>th</sup> transistor M11j and the first transistor M1nj.

[0134] In embodiments of the invention, to stably drive the above-described pixels 140, the generated compensation voltage should be stably applied to the pixels. More particularly, for example, the generated compensation voltage should be stably applied to the third node N3 during the first period. However, because the current that sinks during the first

period may be a micro current, e.g., several tens of  $\mu\text{A}$ , a desired compensation voltage may not be applied during the first period of the one horizontal period. If the first period of the one horizontal period is set to be large enough to solve such a problem, the second period may be shortened. Such a shortened second period may not allow the pixels 140 to be charged as desired.

5 **[0135]** In embodiments of the invention, as illustrated in FIG. 12, a current source  $I_{\text{max}2}$  for sinking current higher than the current to be supplied to the OLED for the pixel 140 to emit light with the maximum brightness may be provided. The current source  $I_{\text{max}2j}$  may be provided in the current sink unit 280j. FIG. 12 illustrates the connection scheme illustrated in FIG. 8 employing the current source  $I_{\text{max}2j}$ . The exemplary connection scheme illustrated in FIG. 12 is substantially the same as the exemplary connection scheme illustrated in FIG. 8, except for the current source  $I_{\text{max}2}$  replacing  $I_{\text{max}}$ , and another exemplary embodiment of a voltage generator 240j'. In the following description, the same reference numerals employed above will be employed to describe like features in the exemplary embodiment illustrated in FIG. 12.

10 **[0136]** FIG. 12 illustrates another exemplary embodiment of a connection scheme among the voltage generator 240j', the DAC 250j, the first buffer 270j, the second buffer 260j, the switching unit 290j, the current sink unit 280j and the pixel 140nj in a specific channel. In the exemplary embodiment illustrated in FIG. 12, for simplicity, the jth channel is illustrated, and it is assumed that the data line  $D_j$  is connected to the pixel 140nj. In the following description, the same reference numerals employed above in the description of the exemplary embodiment illustrated in FIG. 8 will be employed to describe like features in the exemplary embodiment of the connection scheme illustrated in FIG. 12.

15 **[0137]** As shown in FIG. 12, the current sink unit 280j may include 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j that may be controlled by the second control signal CS2, the current source  $I_{\text{max}2j}$  that may be connected to the first electrode of the 13<sup>th</sup> transistor M13j, and a third capacitor C3j that may be connected between a third node N3j and a ground voltage source GND.

20 **[0138]** The gate electrode of the 12<sup>th</sup> transistor M12j may be connected to the gate electrode of the 13<sup>th</sup> transistor M13j and the second electrode of the 12<sup>th</sup> transistor M12j may be connected to the second electrode of the 13<sup>th</sup> transistor M13j and the data line  $D_j$ . The first electrode of the 12<sup>th</sup> transistor M12j may be connected to the second buffer 260j. The 12<sup>th</sup> transistor M12j may be turned on during the first period of the one horizontal period 1H by the second control signal CS2 and may be turned off during the second period.

25 **[0139]** The gate electrode of the 13<sup>th</sup> transistor M13 may be connected to the gate electrode of the 12<sup>th</sup> transistor M12j and the second electrode of the 13<sup>th</sup> transistor M13j may be connected to the data line  $D_j$ . The first electrode of the 13<sup>th</sup> transistor M13j may be connected to the current source  $I_{\text{max}2j}$ . The 13<sup>th</sup> transistor M13j may be turned on by the second control signal CS2 during the first period of the one horizontal period 1H and may be turned off during the second period.

30 **[0140]** The current source  $I_{\text{max}2j}$  may receive, during the first period for driving the nj-th pixel 140nj when the 12<sup>th</sup> and 13<sup>th</sup> transistors M12 and M13 may be turned on, a current higher than a minimum current that may be required by the OLEDnj for the respective nj-th pixel 140nj to emit light with maximum brightness. In embodiments of the invention employing the current source  $I_{\text{max}2j}$ , which may receive the relatively higher, i.e., minimum current relatively greater than the current required by the respective nj-th pixel to emit light with the maximum brightness, it may be possible to reduce a time for which a predetermined voltage may be applied to the third node N3j and may thereby reduce driving time of the nj-th pixel 140nj.

35 **[0141]** The third capacitor C3j may store the first compensation voltage that is applied to the third node N3j by the current source  $I_{\text{max}2j}$  during the first period for driving the nj-th pixel 140nj. More particularly, for example, the third capacitor C3j may charge the first compensation voltage applied to the third node N3j during the first period and may maintain the first compensation voltage of the third node N3j uniform during the second period where the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j may be turned off.

40 **[0142]** In embodiments of the invention, the second buffer 260j may supply the first compensation voltage applied to the third node N3j to the voltage generator 240j'.

**[0143]** The voltage generator 240j' may include voltage dividing resistors R1 to R/ for generating the plurality of gray scale voltages  $V_0$  to  $V_{2^k-1}$  and a compensation resistor  $R_c$  for reducing the value of the first compensation voltage.

45 **[0144]** A compensation resistor  $R_c$  may be provided between a fifth node N5j and the fourth node N4j so that a second compensation voltage lower than the first compensation voltage, which may be applied to the fourth node N4j, may be applied to the fifth node N5j. The value of the second compensation voltage to be applied at the fifth node N5j, may be set, for example, to be equal to the value of the voltage that may be applied to the third node N3j when the current sinking to the current source  $I_{\text{max}2j}$  equals the minimum current required by the OLEDnj to emit light with maximum brightness.

50 **[0145]** The voltage dividing resistors R1 to R/ may divide the voltage between the voltage of the reference power source  $ELV_{\text{ref}}$  and the second compensation voltage to generate the plurality of gray scale voltages  $V_0$  to  $V_{2^k-1}$  and may supply the generated gray scale voltages  $V_0$  to  $V_{2^k-1}$  to the DAC 250j.

55 **[0146]** The DAC 250j may select one gray scale voltage among the gray scale voltages  $V_0$  to  $V_{2^k-1}$  based on the bit

values of the data DATA and may supply the selected gray scale voltage to the first buffer 270j. In embodiments of the invention, the gray scale voltage selected by the DAC 250j may be used as the data signal DSj.

[0147] The first buffer 270j may transmit the data signal DSj supplied from the DAC 250j to the switching unit 290j.

[0148] The switching unit 290j may supply the data signal DS to the data line Dj during the second period. The switching unit 290j may refrain from supplying the data signal DS to the data line Dj during the first period of the one horizontal period 1H.

[0149] Exemplary methods for operating the n-th pixel circuit 142nj of the nj-th pixel 140nj of the pixels 140 will be described in detail with reference to FIGS. 9 and 12. When the scan signal SSn-1 is supplied to the n-1th scan line Sn-1, the voltages obtained by EQUATION1 and EQUATION2 may be respectively applied to the first and second nodes N1nj and N2nj.

[0150] Then, when the scan signal SSn is supplied to the nth scan line Sn, the first and second transistors M1nj and M2nj are turned on. The 12<sup>th</sup> and 13<sup>th</sup> transistors M12nj and M13nj may be turned on during the first period of the one horizontal period when the scan signal SSn is supplied to the nth scan line Sn. Then, the voltage obtained by EQUATION13 may be applied to the third node N3j by the current that is sinking via the current source Imax2j.

[EQUATION13]

$$V_{N3} = V_{ref} - \sqrt{\frac{2I_{max}}{\mu_p C_{ox}} \frac{L}{W}} + \Delta V$$

[0151] When the current sinking to the current source Imax2 corresponds to at least the minimum amount of current the respective OLEDnj requires for the respective pixel 140nj to emit light with the maximum brightness, the voltage obtained by EQUATION4 may be applied to the third node N3j. However, in the exemplary embodiment illustrated in FIG. 12, because the current sinking to the current source Imax2j may be higher than the amount of current the respective OLED requires for the respective pixel 140 to emit light with the maximum brightness sinks, the respective increase in current may be addressed as  $\Delta V$ , and the voltage obtained by EQUATION 13 may be applied to the third node N3j.

[0152] The voltage applied to the third node N3j may be applied to the fourth node N4j via the second buffer 260j. The compensation resistor Rc may reduce the value of the voltage applied to the fourth node N4j by a predetermined value and may supply the reduced voltage to the fifth node N5j. The compensation resistor Rc may reduce the value of the voltage by  $\Delta V$  in EQUATION13 and may supply the voltage obtained by EQUATION5 to the fifth node N5j.

[0153] When the voltage obtained by EQUATION5 is applied to the fifth node N5, the voltage between the fifth node N5j and the reference power source ELVref may be represented by EQUATION6. When the DAC 250j selects the hth gray scale voltage among the f gray scale voltages, the voltage Vb supplied to the first buffer 270j may be represented by EQUATION7.

[0154] Then, the voltage supplied to the first buffer 270j may be supplied to the first node N1 during the second period when the 11<sup>th</sup> transistor M11j may be turned on. More particularly, in embodiments of the invention, the voltage obtained by EQUATION7 may be supplied to the first node N1nj. The voltage applied to the second node N2nj may be represented by EQUATION8 by the coupling of the second capacitor C2nj. As can be understood from EQUATION9, in embodiments of the invention, the respective current depending on the gray scale voltage may flow to the fourth transistor M4nj regardless of the threshold voltage and electron mobility of the fourth transistor M4nj.

[0155] FIG. 13 illustrates a fourth embodiment of a connection connecting among the voltage generator 240j', the DAC 250j, the first buffer 270j, the second buffer 260j, the switching unit 290j, the current sink unit 280j and the pixel 140nj' in a specific channel. The exemplary embodiment illustrated in FIG.13 is similar to the exemplary embodiment illustrated in FIG. 12. In particular, in the exemplary embodiment illustrated in FIG. 13, the embodiment of the nm-th pixel 140nm' described above with reference to FIG. 5 is employed instead of the exemplary embodiment of the nm-th pixel 140nm described above with reference to FIG. 3. Therefore, the voltage supplied to the pixel 140 will be only briefly described below. In embodiments of the invention, the switching unit 291j illustrated in FIG. 10 may be employed instead of the one or all of the switching units 290j illustrated in FIGS. 12 and 13.

[0156] As can be understood from FIGS. 9 and 13, when the scan signal SSn-1 is supplied to the n-1 scan line Sn-1, the voltages obtained by EQUATION1 and EQUATION3 may be respectively applied to the first and second nodes N1nj and N2nj.

[0157] Then, the 12<sup>th</sup> and 13<sup>th</sup> transistors M12j and M13j may be turned on in the first period of the period where the scan signal SSn is supplied to the nth scan line Sn. The voltage obtained by EQUATION14 may then be applied to the

third node N3j by the current that is sinking to the current source I<sub>max2j</sub>.

[EQUATION14]

$$V_{M1} = V_{ref} - \left( \frac{C1 + C2}{C2} \right) \sqrt{\frac{2I_{max}}{\mu_p C_{ox}} \frac{L}{W}} + \Delta V$$

[0158] In embodiments of the invention in which the current sinking to the current source I<sub>max</sub> is the same as the required current flow to the respective light emitting element/material, e.g., OLED<sub>nm</sub>, of the respective pixel 140nm, 140nm' to emit light with the maximum brightness, the voltage obtained by EQUATION10 may be applied to the third node N3j. In embodiments of the invention, e.g., the embodiment illustrated in FIG. 13, in which a current flow that is higher than the current flow required by the OLED<sub>nj</sub>' for the pixel 140nj' to emit light with the maximum brightness may sink to the current source I<sub>max2j</sub>, the voltage obtained by EQUATION14, accounting for a change in voltage ΔV due to the increased current flow, may be applied to the third node N3j.

[0159] The voltage applied to the third node N3j may be applied to the fourth node N4j via the second buffer 260j. The compensation resistor R<sub>c</sub> may then reduce the value of the voltage applied to the fourth node N4j by a predetermined value and may supply the reduced voltage to the fifth node N5j. In embodiments of the invention, the compensation resistor R<sub>c</sub> may reduce the value of the voltage applied to the fourth node N4j by ΔV of EQUATION14 and may supply the voltage obtained by EQUATION10 to the fifth node N5j. As discussed above, ΔV may correspond to the voltage difference that may result when a current flow that is different from the current flow required by the OLED<sub>nj</sub> for the pixel 140nj' to emit light of maximum brightness sinks to the current source I<sub>max2j</sub>.

[0160] When the voltage obtained by EQUATION10 is applied to the fifth node N5j, the voltage between the fifth node N5j and the reference power source ELV<sub>ref</sub> may be represented by EQUATION11. When the DAC 250j selects the h<sup>th</sup> gray scale voltage among the f gray scale voltages, the voltage V<sub>b</sub> supplied to the first buffer 270j may be represented by EQUATION12.

[0161] Then, the voltage supplied to the first buffer 270j may be supplied to the first node N1nj' during the second period where the 11<sup>th</sup> transistor M11j is turned on. At this time, the voltage applied to the second node N2nj' may be represented by EQUATION8. Therefore, the current that flows through the fourth transistor M4nj may be represented by EQUATION9. In embodiments of the invention, the current corresponding to the gray scale voltage selected by the DAC 250j may flow to the fourth transistor M4nj irrespective of the threshold voltage and electron mobility of the fourth transistor M4nj. As discussed above, embodiments of the invention enable the display of images with uniform brightness.

[0162] As described above, data driving circuits employing one or more aspects of the invention, light emitting display using such data driving circuits, and methods of driving such light emitting displays, enable values of the gray scale voltages generated by the voltage generator to be reset using the compensation voltage generated when the current from the respective pixel sinks. The reset gray scale voltages may then be supplied to the respective pixel, and in embodiments of the invention it is possible to display images with uniform brightness regardless of the electron mobility of the transistors. In embodiments of the invention, because a current flow that is higher than the current flow required by the OLED for the respective pixel to emit light with the maximum brightness may sink to a current source, it is possible to stably drive the light emitting display during each of the horizontal periods.

[0163] Exemplary embodiments of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

## Claims

1. A data driving circuit (200) for driving a pixel (140j) of a light emitting display based on externally supplied data for the pixel, the pixel being electrically connectable to the data driving circuit via a data line, the data driving circuit comprising:

a current supply unit (280) including a current sink (280j) configured to sink a predetermined current flowing through the pixel via the data line for generating a compensation voltage using the predetermined current;  
 a voltage generator (240j) configured to generate and set values for a plurality of gray scale voltages ( $V_{0-2^{k-1}}$ ) based on the compensation voltage generated by the pixel when the predetermined current flows through the

pixel, wherein the voltage generator (240j) comprises a plurality of voltage dividing resistors (R1-R1) provided between a first terminal for receiving a reference power source (Vref) and a second terminal for receiving the compensation voltage to set the gray scale voltages;

a digital-analog converter (250j) for selecting, as a data signal for the pixel, one of the plurality of set gray scale voltages based on a bit value of a portion of the externally supplied data associated with the pixel; and

at least one switching unit (290j) for supplying the selected data signal to the data line, wherein a value of the predetermined current being equal to or higher than a value of a minimum current employable by the pixel to emit light of maximum brightness, and the maximum brightness corresponds to a brightness of the pixel when a highest one of the plurality of set gray scale voltages is applied to the pixel;

wherein the current sink (280j) comprises:

a current source (Imaxj) configured to receive the predetermined current, wherein the current sink is arranged to receive the predetermined current from the pixel during a first partial period of one complete period for driving the pixel based on the selected gray scale voltage, the first partial period occurring before a second partial period in the one complete period for driving the pixel based on the selected gray scale voltage;

a first transistor (M12j) provided between the data line and the voltage generator (240j), the first transistor being arranged to be turned on during the first partial period;

a second transistor (M13j) provided between the data line and the current source (Imaxj), the second transistor being arranged to be turned on during the first partial period; and

a capacitor (C3j) for charging the compensation voltage.

2. A data driving circuit according to claim 1, further comprising a compensation resistor (Rc) connected between the second terminal and the voltage dividing resistors to reduce a value of the compensation voltage, wherein the compensation resistor is arranged to compensate for the value of the predetermined current being higher than the value of the minimum current employable by the pixel to emit light of maximum brightness by reducing the value of the compensation voltage such that a voltage corresponding to the minimum current is supplied to the voltage dividing resistors.

3. A data driving circuit according to claim 1 or 2, further comprising:

a first buffer (270j) provided between the digital-analog converter (250j) and the switching unit (290j); and  
a second buffer (260j) provided between the current sink (280j) and the voltage generator (240j).

4. A data driving circuit according to any one of the preceding claims, wherein each channel of the data driving circuit includes a respective one of each of the current sink, the voltage generator, the digital-analog converter and the switching unit.

5. A data driving circuit according to any one of the preceding claims, further comprising:

a shift register (210j) configured to generate sampling pulses;  
a sampling latch (220j) configured to receiving the data in response to the sampling pulses; and  
a holding latch (230j) configured to temporarily store the data stored in the sampling latch before the temporarily stored data is supplied to the digital-analog converter (250j).

6. A data driving circuit according to claim 5, further comprising a level shifter (300j) configured to modify a voltage level of the data stored in the holding latch before the temporarily stored data is supplied to the digital-analog converter (250j).

7. A light emitting display, comprising:

a pixel unit including a plurality of pixels connected to n scan lines(S1-Sn), a plurality of data lines (D1-Dm) and a plurality of emission control lines(E1-En);

a scan driver (110) configured to respectively and sequentially supply, during each scan cycle, n scan signals to the n scan lines, and to sequentially and respectively supply emission control signals to the plurality of emission control lines; and

a data driving circuit according to any one of the preceding claims.

8. A light emitting display according to claim 7, wherein each of the pixels is connected to two of the n scan lines, and

during each of the scan cycles, a first scan line of the two scan lines is arranged to receive a respective one of the n scan signals before a second scan line of the two scan lines is arranged to receive a respective one of the n scan signals, and each of the pixels comprises:

- 5 a first power source (ELVDD);  
 an organic light emitting diode (OLED<sub>nm</sub>, OLED<sub>nj</sub>) arranged to receive current from the first power source;  
 first and second transistors (M1<sub>nm</sub>, M1<sub>nj</sub>, M2<sub>nm</sub>, M2<sub>nj</sub>) each having a first electrode connected to the respective  
 one of the data lines associated with the pixel, the first and second transistors being arranged to be turned on  
 when the first of the two scan signals is supplied;  
 10 a third transistor (M3<sub>nm</sub>, M3<sub>nj</sub>) having a first electrode connected to a reference power source (V<sub>ref</sub>) and a  
 second electrode connected to a second electrode of the first transistor, the third transistor being arranged to  
 be turned on when the first of the two scans signal is supplied;  
 a fourth transistor (M4<sub>nm</sub>, M4<sub>nj</sub>), arranged to control an amount of current supplied to the organic light emitting  
 diode, a first terminal of the fourth transistor being connected to the first power source; and  
 15 a fifth transistor (M5<sub>nm</sub>, M5<sub>nj</sub>) having a first electrode connected to a gate electrode of the fourth transistor and  
 a second electrode connected to a second electrode of the fourth transistor, the fifth transistor being arranged  
 to be turned on when the first of the two scan signals is supplied such that the fourth transistor operates as a diode.

9. A light emitting display according to claim 8, wherein each of the pixels comprises:

- 20 a first capacitor (C1<sub>nm</sub>, C1<sub>nj</sub>) having a first electrode connected to one of a second electrode of the first transistor  
 and the gate electrode of the fourth transistor and a second electrode connected to the first power source; and  
 a second capacitor (C2<sub>nm</sub>, C2<sub>nj</sub>) having a first electrode connected to the second electrode of the first transistor  
 and a second electrode connected to the gate electrode of the fourth transistor.

10. A light emitting display according to claim 8 or 9, wherein each of the pixels further comprises a sixth transistor  
 (M6<sub>nm</sub>, M6<sub>nj</sub>) having a first terminal connected to the second electrode of the fourth transistor and a second terminal  
 connected to the organic light emitting diode, the sixth transistor being arranged to be turned off when the respective  
 emission control signal is supplied,

- 30 wherein the current sink is arranged to receive the predetermined current from the pixel during the first partial period  
 of one complete period (H) for driving the pixel based on the selected gray scale voltage, the first partial period  
 being arranged to occur before a second partial period of the complete period for driving the one pixel based on the  
 selected gray scale voltage, and the sixth transistor is arranged to be turned on during the second partial period of  
 the complete period for driving the one pixel.

11. A method of driving a pixel of a light emitting display based on externally supplied data for the pixel, wherein the  
 pixel is electrically connectable to a driving circuit via a data line, the method comprising:

- 40 flowing a predetermined current from the pixel to a current sink (280j) of the light emitting display via the data  
 line during a first partial period of a complete period for driving the pixel based on a selected gray scale voltage,  
 a value of the predetermined current being equal to or greater than a value of a minimum current employable  
 by the pixel to emit light of maximum brightness;  
 generating a compensation voltage when the predetermined current flows through the pixel;  
 setting values of and generating a plurality of gray scale voltages based on the generated compensation voltage  
 45 by supplying the compensation voltage to a plurality of voltage dividing resistors;  
 selecting, as a data signal for the pixel, the selected gray scale voltage as one of the plurality of gray scale  
 voltages ( $V_{0-2}^{k-1}$ ) based on a bit value of a portion of the externally supplied data associated with the pixel; and  
 supplying the selected data signal to the pixel via the data line, wherein the maximum brightness corresponds  
 to a brightness of the pixel when a highest one of the plurality of set gray scale voltages is applied to the pixel.

12. A method according to claim 11, wherein supplying the selected data signal occurs during any partial period of the  
 complete period, for driving the pixel, other than the first partial period that occurs after the first partial period.

13. A method according to claims 11 or 12, wherein when the value of the predetermined current flowing from the  
 respective one the pixels to the current sink of the light emitting display is greater than the value of the minimum  
 current employable by the respective pixel to emit light of maximum brightness, and generating the compensation  
 voltage comprises generating an initial compensation voltage and a first compensation voltage based on the initial  
 compensation voltage before the step of setting values of the plurality of gray scale voltages.

14. A method according to claim 13, wherein the first compensation voltage is less than the initial generated compensation voltage and the first compensation voltage corresponds to a highest one of the plurality of gray scale voltages and the compensation voltage generated when the predetermined current that flows is equal to the minimum current employable by the pixel to emit light of maximum brightness.

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## Patentansprüche

1. Datentreiberschaltung (200) zum Ansteuern eines Pixels (140j) einer Leuchtanzeige auf der Basis von extern zugeführten Daten für das Pixel, wobei das Pixel mit der Datentreiberschaltung über eine Datenleitung elektrisch verbunden werden kann, wobei die Datentreiberschaltung Folgendes umfasst:

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eine Stromzuführungseinheit (280) mit einer Stromsenke (280j), die zum Abführen von durch das Pixel über die Datenleitung fließendem vorbestimmtem Strom zum Erzeugen einer Kompensationsspannung mit dem vorbestimmten Strom konfiguriert ist;

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einen Spannungsgenerator (240j), der zum Erzeugen und Einstellen von Werten für mehrere Graustufenspannungen ( $V_{0,2^{k-1}}$ ) auf der Basis der von dem Pixel erzeugten Kompensationsspannung konfiguriert ist, wenn der vorbestimmte Strom durch das Pixel fließt, wobei der Spannungsgenerator (240j) mehrere Spannungsteilungswiderstände (R1-RI) umfasst, die zwischen einem ersten Anschluss zum Empfangen einer Referenzstromquelle ( $V_{ref}$ ) und einem zweiten Anschluss zum Empfangen der Kompensationsspannung vorgesehen sind, um die Graustufenspannungen einzustellen;

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einen Digital-Analog-Wandler (250j) zum Auswählen, als Datensignal für das Pixel, von einer der mehreren eingestellten Graustufenspannungen auf der Basis eines Bitwertes eines Teils der mit dem Pixel assoziierten extern zugeführten Daten; und

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wenigstens eine Schalteinheit (290j) zum Zuführen des gewählten Datensignals zur Datenleitung, wobei ein Wert des vorbestimmten Stroms gleich oder höher als ein Wert eines Mindeststroms ist, der von dem Pixel benutzt werden kann, um Licht von maximaler Helligkeit zu emittieren, und die maximale Helligkeit einer Helligkeit des Pixels entspricht, wenn eine höchste der mehreren eingestellten Graustufenspannungen an das Pixel angelegt wird;

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wobei die Stromsenke (280j) Folgendes umfasst:

eine Stromquelle ( $I_{maxj}$ ), die zum Empfangen des vorbestimmten Stroms konfiguriert ist, wobei die Stromsenke zum Empfangen des vorbestimmten Stroms von dem Pixel während einer ersten Teilperiode einer kompletten Periode ausgelegt ist, um das Pixel auf der Basis der gewählten Graustufenspannung anzusteuern, wobei die erste Teilperiode vor einer zweiten Teilperiode in der einen kompletten Periode auftritt, um das Pixel auf der Basis der gewählten Graustufenspannung anzusteuern;

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einen ersten Transistor (M12j), der zwischen der Datenleitung und dem Spannungsgenerator (240j) vorgesehen ist, wobei der erste Transistor zum Einschalten während der ersten Teilperiode ausgelegt ist;

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einen zweiten Transistor (M13j), der zwischen der Datenleitung und der Stromquelle ( $I_{maxj}$ ) vorgesehen ist, wobei der zweite Transistor zum Einschalten während der ersten Teilperiode ausgelegt ist; und einen Kondensator (C3j) zum Laden der Kompensationsspannung.

2. Datentreiberschaltung nach Anspruch 1, die ferner einen Kompensationswiderstand ( $R_c$ ) umfasst, der zwischen dem zweiten Anschluss und den Spannungsteilungswiderständen geschaltet ist, um einen Wert der Kompensationsspannung zu reduzieren, wobei der Kompensationswiderstand so ausgelegt ist, dass er den Umstand, dass der Wert des vorbestimmten Stroms höher ist als der Wert des Mindeststroms, der von dem Pixel benutzt werden kann, um Licht von maximaler Helligkeit zu emittieren, dadurch kompensiert, dass er den Wert der Kompensationsspannung so reduziert, dass eine dem Mindeststrom entsprechende Spannung an die Spannungsteilungswiderstände angelegt wird.

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3. Datentreiberschaltung nach Anspruch 1 oder 2, die ferner Folgendes umfasst:

einen ersten Puffer (270j), der zwischen dem Digital-Analog-Wandler (250j) und der Schalteinheit (290j) vorgesehen ist; und

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einen zweiten Puffer (260j), der zwischen der Stromsenke (280j) und dem Spannungsgenerator (240j) vorgesehen ist.

4. Datentreiberschaltung nach einem der vorherigen Ansprüche, wobei jeder Kanal der Datentreiberschaltung jeweils

eines aus Stromsenke, Spannungsgenerator, Digital-Analog-Wandler und Schalteinheit beinhaltet.

5. Datentreiberschaltung nach einem der vorherigen Ansprüche, die ferner Folgendes umfasst:

5 ein Schieberegister (210j), das zum Erzeugen von Abtastimpulsen konfiguriert ist;  
einen Abtast-Latch (220j), der zum Empfangen der Daten als Reaktion auf die Abtastimpulse konfiguriert ist; und  
einen Halte-Latch (230j), der zum vorübergehenden Speichern der im Abtast-Latch gespeicherten Daten konfiguriert ist, bevor die vorübergehend gespeicherten Daten dem Digital-Analog-Wandler (250j) zugeführt werden.

- 10 6. Datentreiberschaltung nach Anspruch 5, die ferner einen Pegelschieber (300j) umfasst, der zum Modifizieren eines Spannungspegels der im Halte-Latch gespeicherten Daten konfiguriert ist, bevor die vorübergehend gespeicherten Daten dem Digital-Analog-Wandler (250j) zugeführt werden.

7. Leuchtanzeige, die Folgendes umfasst:

15 eine Pixeleinheit mit mehreren Pixeln, die mit n Scan-Leitungen (S1-Sn), mehreren Datenleitungen (D1-Dm) und mehreren Emissionssteuerleitungen (E1-En) verbunden sind;  
einen Scan-Treiber (110), der so konfiguriert ist, dass er den n Scan-Leitungen jeweils und sequentiell bei jedem Scan-Zyklus n Scan-Signale zuführt und den mehreren Emissionssteuerleitungen sequentiell und jeweils Emissionssteuersignale zuführt; und  
20 eine Datentreiberschaltung nach einem der vorherigen Ansprüche.

8. Leuchtanzeige nach Anspruch 7, wobei jedes der Pixel mit zwei der n Scan-Leitungen verbunden ist und bei jedem der Scan-Zyklen eine erste Scan-Leitung der beiden Scan-Leitungen zum Empfangen von jeweils einem der n Scan-Signale ausgelegt ist, bevor eine zweite Scan-Leitung der beiden Scan-Leitungen zum Empfangen jeweils eines der n Scan-Signale ausgelegt ist, und wobei jedes der Pixel Folgendes umfasst:

25 eine erste Stromquelle (ELVDD);  
eine organische Leuchtdiode (OLEDnm, OLEDnj), die zum Empfangen von Strom von der ersten Stromquelle ausgelegt ist;  
30 erste und zweite Transistoren (M1nm, M1nj, M2nm, M2nj) jeweils mit einer ersten Elektrode, die mit jeweils einer der mit dem Pixel assoziierten Datenleitungen verbunden ist, wobei der erste und zweite Transistor so ausgelegt sind, dass sie einschalten, wenn das erste der beiden Scan-Signale angelegt wird;  
einen dritten Transistor (M3nm, M3nj) mit einer ersten Elektrode, die mit einer Referenzstromquelle (Vref) verbunden ist, und einer zweiten Elektrode, die mit einer zweiten Elektrode des ersten Transistors verbunden ist, wobei der dritte Transistor so ausgelegt ist, dass er einschaltet, wenn das erste der beiden Scan-Signale angelegt wird;  
35 einen vierten Transistor (M4nm, M4nj), der zum Regeln einer der organischen Leuchtdiode zugeführten Strommenge ausgelegt ist, wobei ein erster Anschluss des vierten Transistors mit der ersten Stromquelle verbunden ist; und  
40 einen fünften Transistor (M5nm, M5nj) mit einer ersten Elektrode, die mit einer Gate-Elektrode des vierten Transistors verbunden ist, und einer zweiten Elektrode, die mit einer zweiten Elektrode des vierten Transistors verbunden ist, wobei der fünfte Transistor so ausgelegt ist, dass er einschaltet, wenn das erste der beiden Scan-Signale angelegt wird, so dass der vierte Transistor als Diode arbeitet.

9. Leuchtanzeige nach Anspruch 8, wobei jedes der Pixel Folgendes umfasst:

45 einen ersten Kondensator (C1nm, C1nj) mit einer ersten Elektrode, die mit einer zweiten Elektrode des ersten Transistors oder mit der Gate-Elektrode des vierten Transistors verbunden ist, und einer mit der ersten Stromquelle verbundenen zweiten Elektrode; und  
50 einen zweiten Kondensator (C2nm, C2nj) mit einer ersten Elektrode, die mit der zweiten Elektrode des ersten Transistors verbunden ist, und einer zweiten Elektrode, die mit der Gate-Elektrode des vierten Transistors verbunden ist.

10. Leuchtanzeige nach Anspruch 8 oder 9, wobei jedes der Pixel ferner einen sechsten Transistor (M6nm, M6nj) mit einem ersten Anschluss, der mit der zweiten Elektrode des vierten Transistors verbunden ist, und einem zweiten Anschluss umfasst, der mit der organischen Leuchtdiode verbunden ist, wobei der sechste Transistor so ausgelegt ist, dass er abschaltet, wenn das jeweilige Emissionssteuersignal angelegt wird,

wobei die Stromsenke so ausgelegt ist, dass sie den vorbestimmten Strom von dem Pixel während der ersten Teilperiode einer kompletten Periode (H) empfängt, um das Pixel auf der Basis der gewählten Graustufenspannung anzusteuern, wobei die erste Teilperiode so ausgelegt ist, dass sie vor einer zweiten Teilperiode der kompletten Periode auftritt, um das eine Pixel auf der Basis der gewählten Graustufenspannung anzusteuern, und der sechste Transistor so ausgelegt ist, dass er während der zweiten Teilperiode der kompletten Periode zum Ansteuern des einen Pixels einschaltet.

11. Verfahren zum Ansteuern eines Pixels einer Leuchtanzeige auf der Basis von extern zugeführten Daten für das Pixel, wobei das Pixel über eine Datenleitung mit einer Treiberschaltung elektrisch verbunden werden kann, wobei das Verfahren Folgendes beinhaltet:

Leiten eines vorbestimmten Stroms von dem Pixel zu einer Stromsenke (280j) der Leuchtanzeige über die Datenleitung während einer ersten Teilperiode einer kompletten Periode zum Ansteuern des Pixels auf der Basis einer gewählten Graustufenspannung, wobei ein Wert des vorbestimmten Stroms gleich oder größer als ein Wert eines Mindeststroms ist, der von dem Pixel zum Emittieren von Licht von maximaler Helligkeit benutzt werden kann;

Erzeugen einer Kompensationsspannung, wenn der vorbestimmte Strom durch das Pixel fließt;

Einstellen von Werten von und Erzeugen mehrerer Graustufenspannungen auf der Basis der erzeugten Kompensationsspannung durch Anlegen der Kompensationsspannung an mehrere Spannungsteilungswiderstände; Auswählen, als Datensignal für das Pixel, der gewählten Graustufenspannung als eine der mehreren Graustufenspannungen ( $V_{0-2}^{k-1}$ ) auf der Basis eines Bitwertes eines Teils der mit dem Pixel assoziierten extern zugeführten Daten; und

Anlegen des gewählten Datensignals an das Pixel über die Datenleitung, wobei die maximale Helligkeit einer Helligkeit des Pixels entspricht, wenn eine höchste der mehreren eingestellten Graustufenspannungen an das Pixel angelegt wird.

12. Verfahren nach Anspruch 11, wobei das Anlegen des gewählten Datensignals während einer beliebigen Teilperiode der kompletten Periode zum Ansteuern des Pixels außer der ersten Teilperiode erfolgt, die nach der ersten Teilperiode auftritt.

13. Verfahren nach Anspruch 11 oder 12, wobei wenn der Wert des von dem jeweils einen der Pixel zur Stromsenke der Leuchtanzeige fließenden vorbestimmten Stroms größer ist als der Wert des Mindeststroms, der von dem jeweiligen Pixel zum Emittieren von Licht von maximaler Helligkeit benutzt werden kann, und das Erzeugen der Kompensationsspannung das Erzeugen einer anfänglichen Kompensationsspannung und einer ersten Kompensationsspannung auf der Basis der anfänglichen Kompensationsspannung vor dem Schritt des Einstellens von Werten der mehreren Graustufenspannungen beinhaltet.

14. Verfahren nach Anspruch 13, wobei die erste Kompensationsspannung geringer ist als die anfängliche erzeugte Kompensationsspannung und die erste Kompensationsspannung einer höchsten der mehreren Graustufenspannungen und der Kompensationsspannung entspricht, die erzeugt wird, wenn der fließende vorbestimmte Strom gleich dem Mindeststrom ist, der von dem Pixel zum Emittieren von Licht von maximaler Helligkeit benutzt werden kann.

## Revendications

1. Circuit de commande de données (200) permettant de commander un pixel (140j) d'un affichage électroluminescent en se basant sur des données fournies de manière externe concernant le pixel, le pixel pouvant être raccordé de manière électrique au circuit de commande de données par l'intermédiaire d'une ligne de données, le circuit de commande de données comprenant :

une unité d'alimentation électrique (280) comprenant un puits de courant (280j) configuré pour dissiper un courant prédéterminé circulant à travers le pixel par l'intermédiaire de la ligne de données pour générer une tension de compensation utilisant le courant prédéterminé ;

un générateur de tension (240j) configuré pour générer et définir des valeurs pour une pluralité de tensions d'échelle de gris ( $V_{0-2}^{k-1}$ ) en se basant sur la tension de compensation générée par le pixel lorsque le courant prédéterminé circule à travers le pixel, dans lequel le générateur de tension (240j) comprend une pluralité de résistances de division de tension (R1-RI) fournies entre une première borne permettant de recevoir une source

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d'énergie de référence ( $V_{ref}$ ) et une seconde borne permettant de recevoir la tension de compensation afin de définir les tensions d'échelle de gris ;

un convertisseur numérique-analogique (250j) permettant de sélectionner, en tant que signal de données pour le pixel, une tension parmi la pluralité de tensions d'échelle de gris définies en se basant sur une valeur binaire d'une partie des données fournies de manière externe associées au pixel ; et

au moins une unité de commutation (290j) permettant de fournir le signal de données sélectionné à la ligne de données, dans lequel une valeur du courant prédéterminé est supérieure ou égale à une valeur d'un courant minimum pouvant être utilisé par le pixel pour émettre de la lumière à luminosité maximum, et la luminosité maximum correspond à une luminosité du pixel lorsqu'une tension la plus élevée parmi la pluralité de tensions d'échelle de gris définies est appliquée au pixel ;  
dans lequel le puits de courant (280j) comprend :

une source de courant ( $I_{maxj}$ ) configuré pour recevoir le courant prédéterminé, dans lequel le puits de courant est agencé pour recevoir le courant prédéterminé en provenance du pixel pendant une première période partielle parmi une période complète permettant de commander le pixel en se basant sur la tension d'échelle de gris sélectionnée, la première période partielle survenant avant une seconde période partielle parmi ladite période complète permettant de commander le pixel en se basant sur la tension d'échelle de gris sélectionnée ;

un premier transistor (M12j) fourni entre la ligne de données et le générateur de tension (240j), le premier transistor étant agencé pour être rendu passant pendant la première période partielle ;

un deuxième transistor (M13j) fourni entre la ligne de données et la source de courant ( $I_{maxj}$ ), le deuxième transistor étant agencé pour être rendu passant pendant la première période partielle ; et

un condensateur (C3j) permettant de charger la tension de compensation.

2. Circuit de commande de données selon la revendication 1, comprenant en outre une résistance de compensation ( $R_c$ ) raccordée entre la seconde borne et les résistances de division de tension afin de réduire une valeur de la tension de compensation, dans lequel la résistance de compensation est agencée pour compenser la valeur du courant prédéterminé lorsqu'elle est supérieure à la valeur du courant minimum pouvant être utilisé par le pixel pour émettre de la lumière à luminosité maximale en réduisant la valeur de la tension de compensation de telle manière qu'une tension correspondant au courant minimum est fournie aux résistances de division de tension.

3. Circuit de commande de données selon la revendication 1 ou 2, comprenant en outre :

un premier séparateur (270j) fourni entre le convertisseur numérique-analogique (250j) et l'unité de commutation (290j) ; et

un second séparateur (260j) fourni entre le puits de courant (280j) et le générateur de tension (240j).

4. Circuit de commande de données selon l'une quelconque des revendications précédentes, dans lequel chaque canal du circuit de commande de données comprend un élément respectif parmi respectivement le puits de courant, le générateur de tension, le convertisseur numérique-analogique et l'unité de commutation.

5. Circuit de commande de données selon l'une quelconque des revendications précédentes, comprenant en outre :

un registre à décalage (210j) configuré pour générer des impulsions d'échantillonnage ;

un verrou d'échantillonnage (220j) configuré pour recevoir les données en réaction aux impulsions d'échantillonnage ; et

un verrou de retenue (230j) configuré pour stocker de manière temporaire les données stockées dans le verrou d'échantillonnage avant que les données stockées de manière temporaire soient fournies au convertisseur numérique-analogique (250j).

6. Circuit de commande de données selon la revendication 5, comprenant en outre un dispositif de décalage de niveau (300j) configuré pour modifier un niveau de tension des données stockées dans le verrou de retenue avant que les données stockées de manière temporaire soient fournies au convertisseur numérique-analogique (250j).

7. Affichage électroluminescent, comprenant :

une unité de pixel comprenant une pluralité de pixels raccordées à  $n$  lignes de balayage ( $S_1$  à  $S_n$ ), à une pluralité de lignes de données ( $D_1$  à  $D_m$ ) et à une pluralité de lignes de commande d'émission ( $E_1$  à  $E_n$ ) ;

un dispositif de commande de balayage (110) configuré pour fournir respectivement et de manière séquentielle, pendant chaque cycle de balayage, n signaux de balayage à n lignes de balayage, et pour fournir de manière séquentielle et respectivement des signaux de commande d'émission à la pluralité de lignes de commande d'émission ; et

5 un circuit de commande de données selon l'une quelconque des revendications précédentes.

8. Affichage électroluminescent selon la revendication 7, dans lequel chacun des pixels est raccordé à deux parmi les n lignes de balayage, et, pendant chacun des cycles de balayage, une première ligne de balayage parmi les deux lignes de balayage est agencée pour recevoir un signal respectif parmi les n signaux de balayage avant qu'une seconde ligne de balayage parmi les deux lignes de balayage soit agencée pour recevoir un signal respectif parmi les n signaux de balayage, et chacun des pixels comprend :

une première source d'énergie (ELVDD) ;

15 une diode électroluminescente organique (OLEDnm, OLEDnj) agencée pour recevoir du courant en provenance de la première source d'énergie ;

des premier et deuxième transistors (M1nm, M1nj, M2nm, M2nj) présentant respectivement une première électrode raccordée à la ligne respective parmi les lignes de données associées au pixel, les premier et deuxième transistors étant agencés pour être rendus passant lorsque le premier parmi les deux signaux de balayage est fourni ;

20 un troisième transistor (M3nm, M3nj) présentant une première électrode raccordée à une source d'énergie de référence (Vref) et une seconde électrode raccordée à une seconde électrode du premier transistor, le troisième transistor étant agencé de manière à être rendu passant lorsque le premier parmi les deux signaux de balayage est fourni ;

25 un quatrième transistor (M4nm, M4nj), agencé pour commander une quantité de courant fournie à la diode électroluminescente organique, une première borne du quatrième transistor étant raccordée à la première source d'énergie ; et

30 un cinquième transistor (M5nm, M5nj) présentant une première électrode raccordée à une électrode de grille du quatrième transistor et une seconde électrode raccordée à une seconde électrode du quatrième transistor, le cinquième transistor étant agencé de manière à être rendu passant lorsque le premier parmi les deux signaux de balayage est fourni, de sorte que le quatrième transistor fonctionne comme une diode.

9. Affichage électroluminescent selon la revendication 8, dans lequel chacun des pixels comprend :

35 un premier condensateur (C1nm, C1nj) présentant une première électrode raccordée à une première électrode du premier transistor et l'électrode de grille du quatrième transistor et une seconde électrode raccordée à la première source d'énergie ; et

un second condensateur (C2nm, C2nj) présentant une première électrode raccordée à la seconde électrode du premier transistor et une seconde électrode raccordée à l'électrode de grille du quatrième transistor.

- 40 10. Affichage électroluminescent selon la revendication 8 ou 9, dans lequel chacun des pixels comprend en outre un sixième transistor (M6nm, M6nj) présentant une première borne raccordée à la seconde électrode du quatrième transistor et une seconde borne raccordée à la diode électroluminescente organique, le sixième transistor étant agencé de manière à être rendu non passant lorsque le signal de commande d'émission respectif est fourni, dans lequel le puits de courant est agencé pour recevoir le courant prédéterminé en provenance du pixel pendant la première période partielle parmi une période complète (H) permettant de commander le pixel en se basant sur la tension d'échelle de gris sélectionnée, la première période partielle étant agencée de manière à survenir avant une seconde période partielle parmi la période complète permettant de commander ledit pixel en se basant sur la tension d'échelle de gris sélectionnée, et le sixième transistor est agencé de manière à être rendu passant pendant la seconde période partielle parmi la période complète permettant de commander ledit pixel.

- 50 11. Procédé de commande d'un pixel d'un affichage électroluminescent en se basant sur des données concernant le pixel fournies de manière externe, dans lequel le pixel peut être raccordé électriquement à un circuit de commande par l'intermédiaire d'une ligne de données, le procédé comprenant l'étape consistant à :

55 faire circuler un courant prédéterminé depuis le pixel vers un puits de courant (280j) de l'affichage électroluminescent par l'intermédiaire de la ligne de données pendant une première période partielle parmi une période complète permettant de commander le pixel en se basant sur une tension d'échelle de gris sélectionnée, une valeur du courant prédéterminé étant supérieure ou égale à une valeur d'un courant minimum pouvant être

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utilisé par le pixel pour émettre de la lumière à luminosité maximum ;  
générer une tension de compensation lorsque le courant prédéterminé circule à travers le pixel ;  
définir des valeurs d'une pluralité de tensions d'échelle de gris, et générer ladite pluralité, en se basant sur la  
tension de compensation générée, en fournissant la tension de compensation à une pluralité de résistances  
de division de tension ;  
sélectionner, en tant que signal de données pour le pixel, la tension d'échelle de gris sélectionnée, qui est une  
parmi la pluralité de tensions d'échelle de gris ( $V_{0-2^{k-1}}$ ) en se basant sur une valeur binaire d'une partie des  
données fournies de manière externe associées au pixel ; et  
fournir le signal de données sélectionné au pixel par l'intermédiaire de la ligne de données, dans lequel la  
luminosité maximum correspond à une luminosité du pixel lorsqu'une tension la plus élevée parmi la pluralité  
de tensions d'échelle de gris définies est appliquée au pixel.

- 12.** Procédé selon la revendication 11, dans lequel l'étape de fourniture du signal de données sélectionné survient pendant une quelconque période partielle parmi la période complète, permettant de commander le pixel, autre que la première période partielle qui survient après la première période partielle.
- 13.** Procédé selon la revendication 11 ou 12, dans lequel, lorsque la valeur du courant prédéterminé circulant depuis le pixel respectif parmi les pixels vers le puits de courant de l'affichage électroluminescent est supérieure à la valeur du courant minimum pouvant être utilisée par le pixel respectif pour émettre de la lumière à luminosité maximum, et l'étape de génération de la tension de compensation comprend une étape consistant à générer une tension de compensation initiale et une première tension de compensation en se basant sur la tension de compensation initiale avant l'étape de définition des valeurs de la pluralité de tensions d'échelle de gris.
- 14.** Procédé selon la revendication 13, dans lequel la première tension de compensation est inférieure à la tension de compensation générée initiale et la première tension de compensation correspond à une tension la plus élevée parmi la pluralité de tensions d'échelle de gris et la tension de compensation générée lorsque le courant prédéterminé qui circule est égal au courant minimum pouvant être utilisé par le pixel pour émettre de la lumière à luminosité maximum.

FIG. 1  
(RELATED ART)

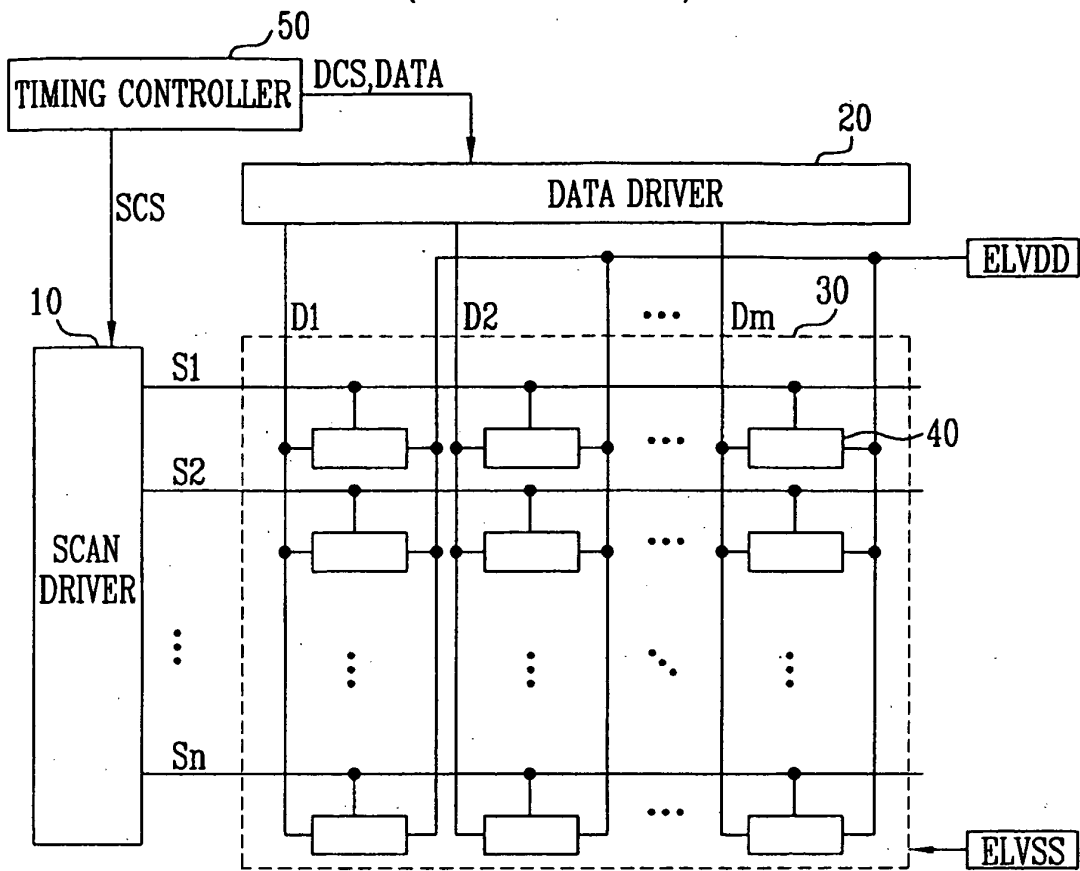




FIG. 3

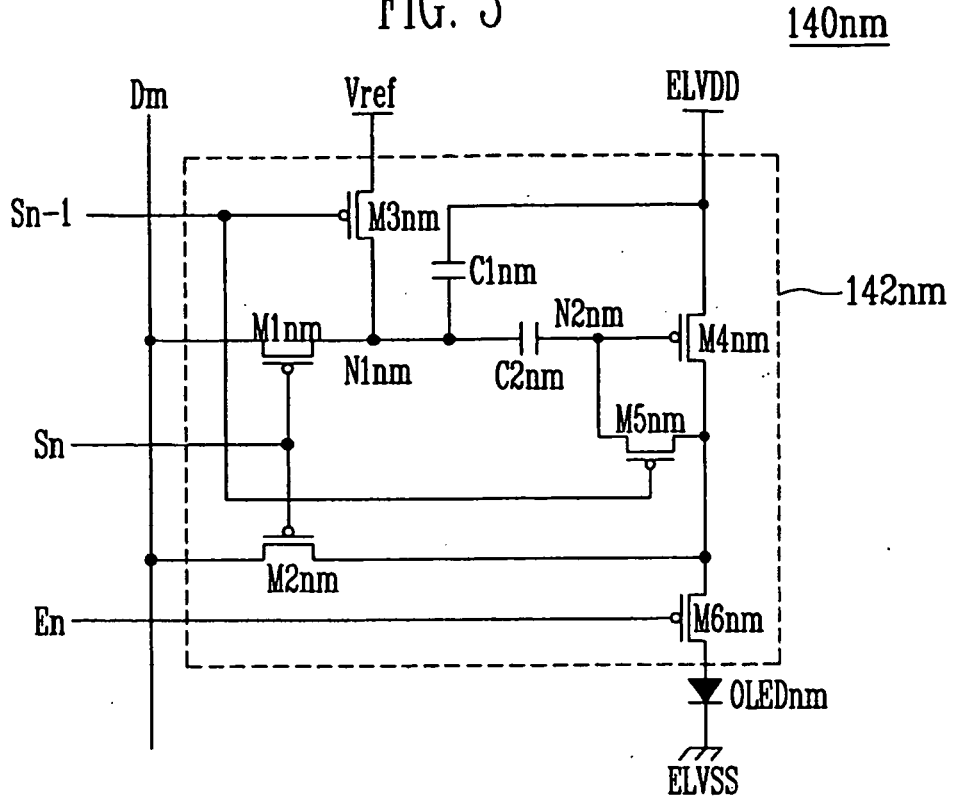


FIG. 4

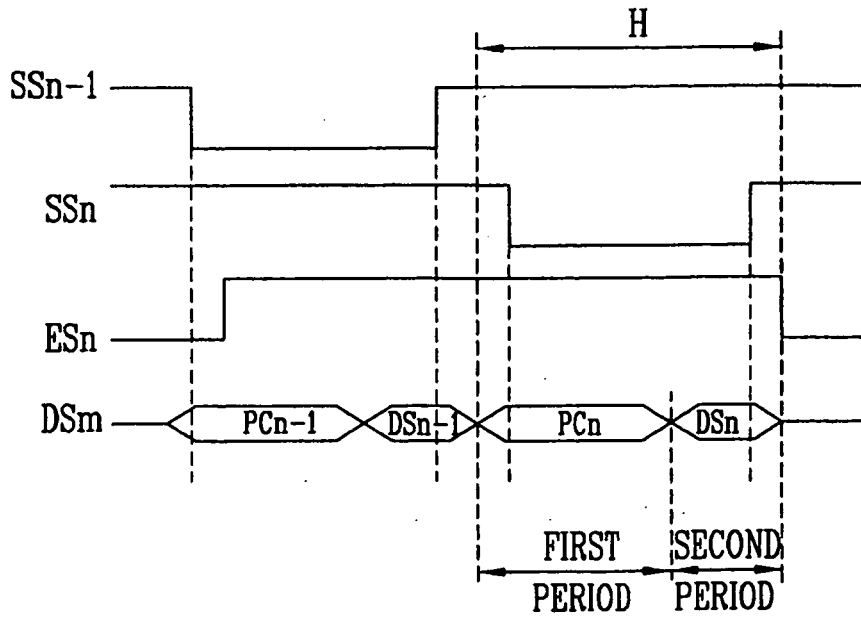


FIG. 5

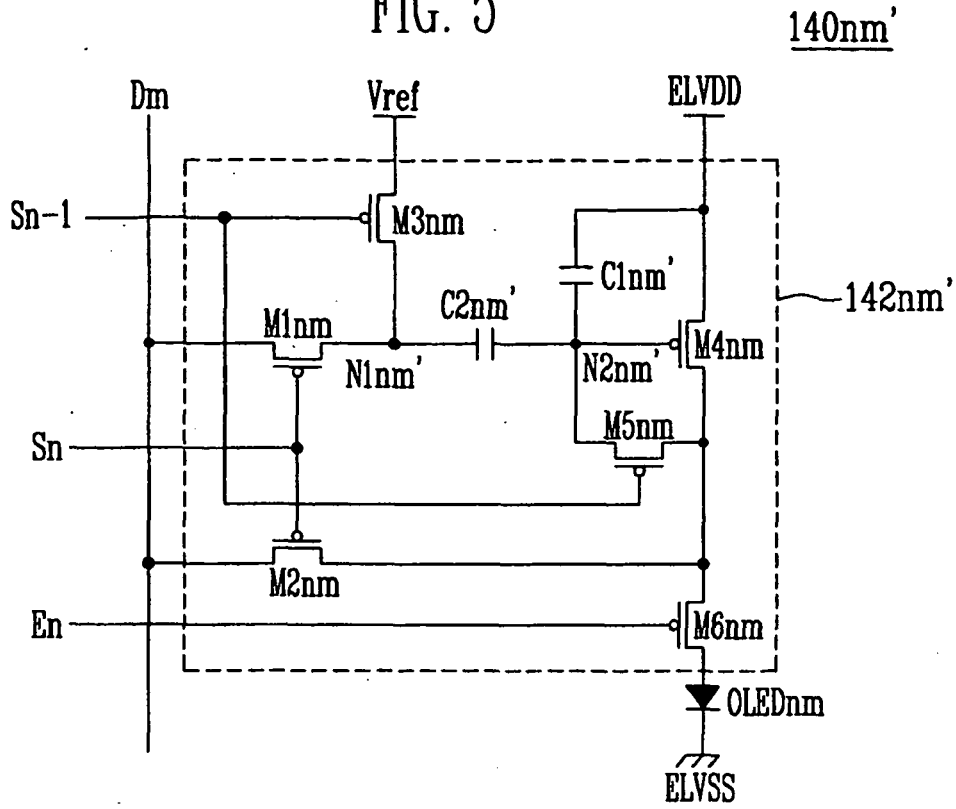


FIG. 6

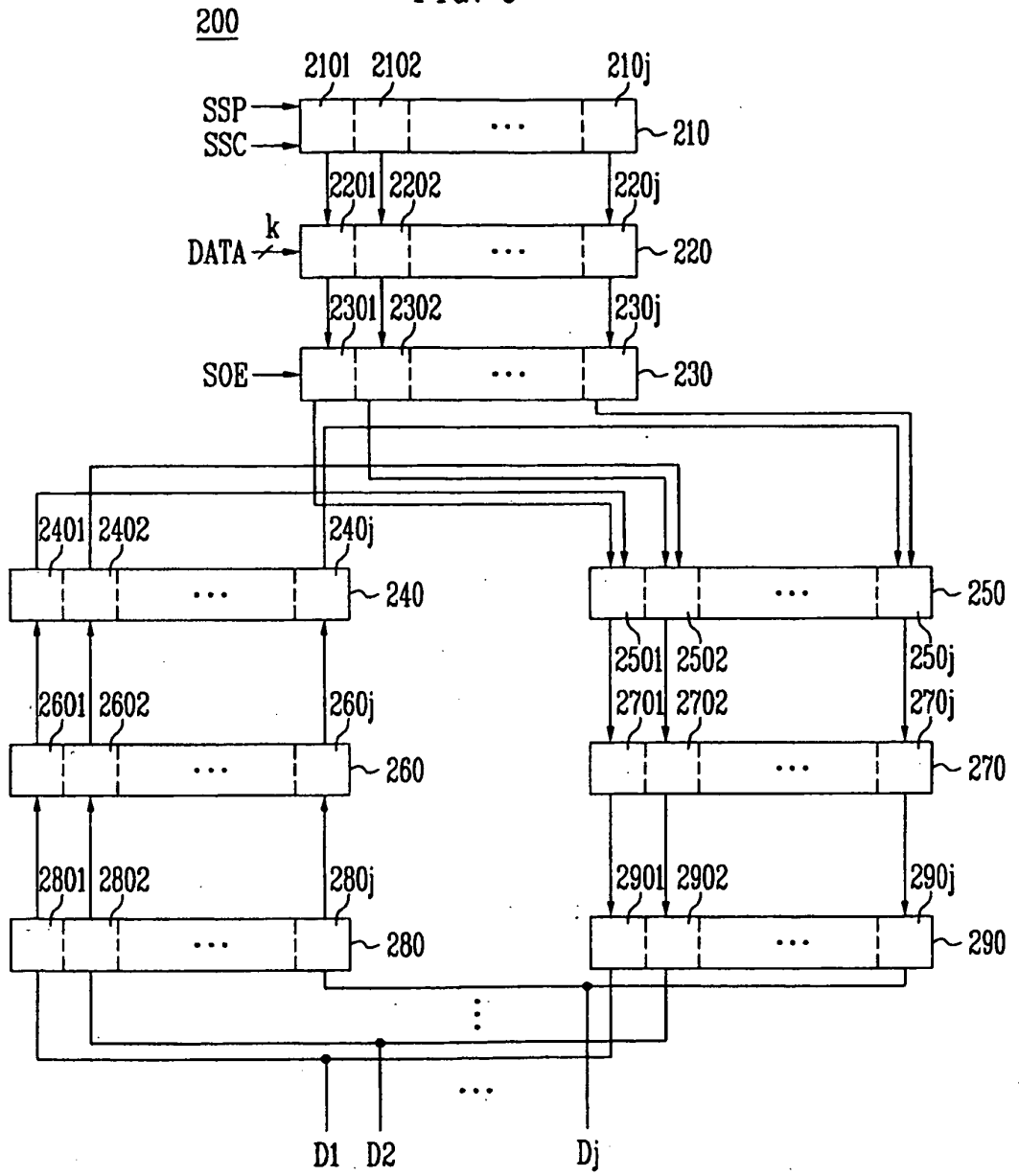


FIG. 7

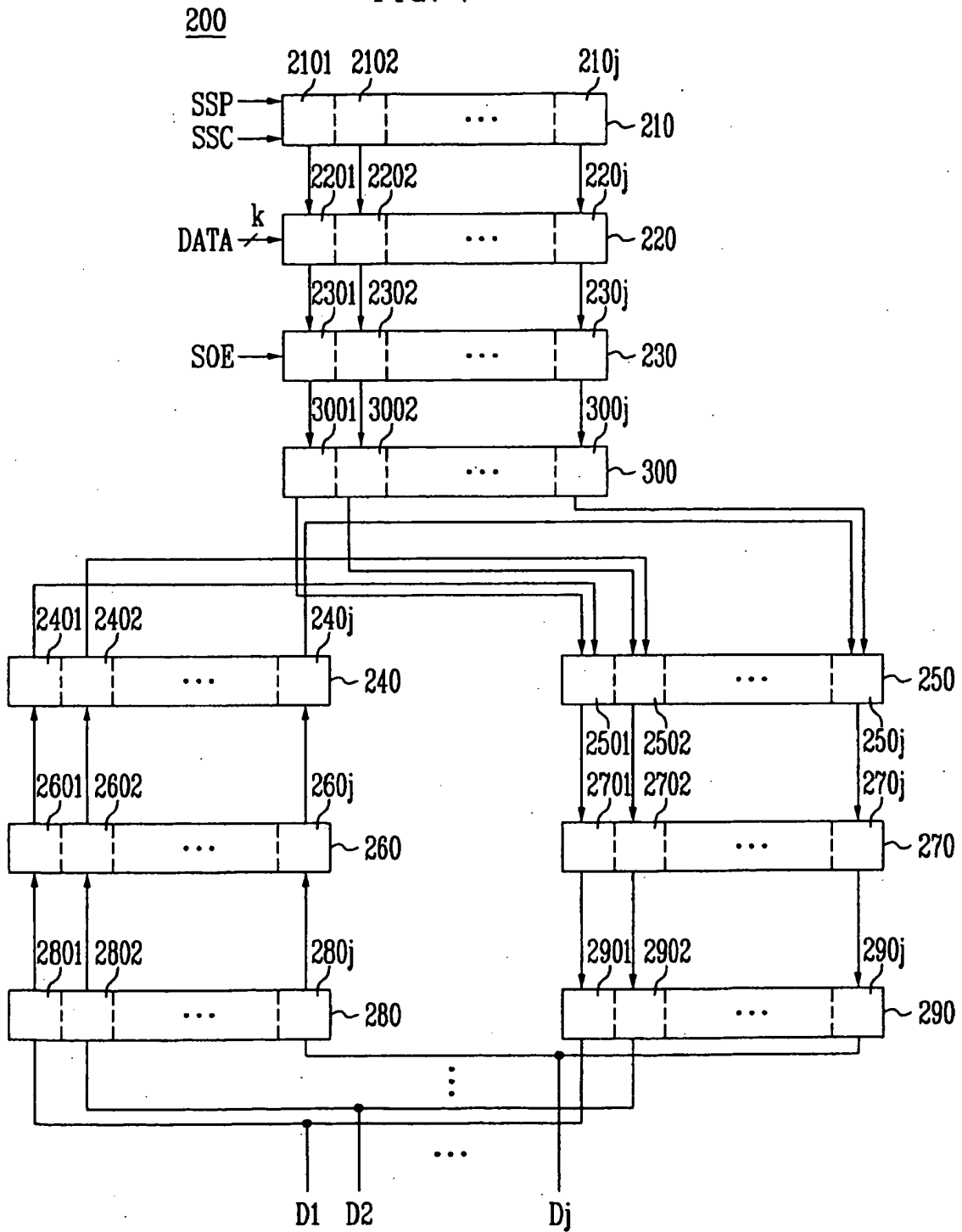


FIG. 8

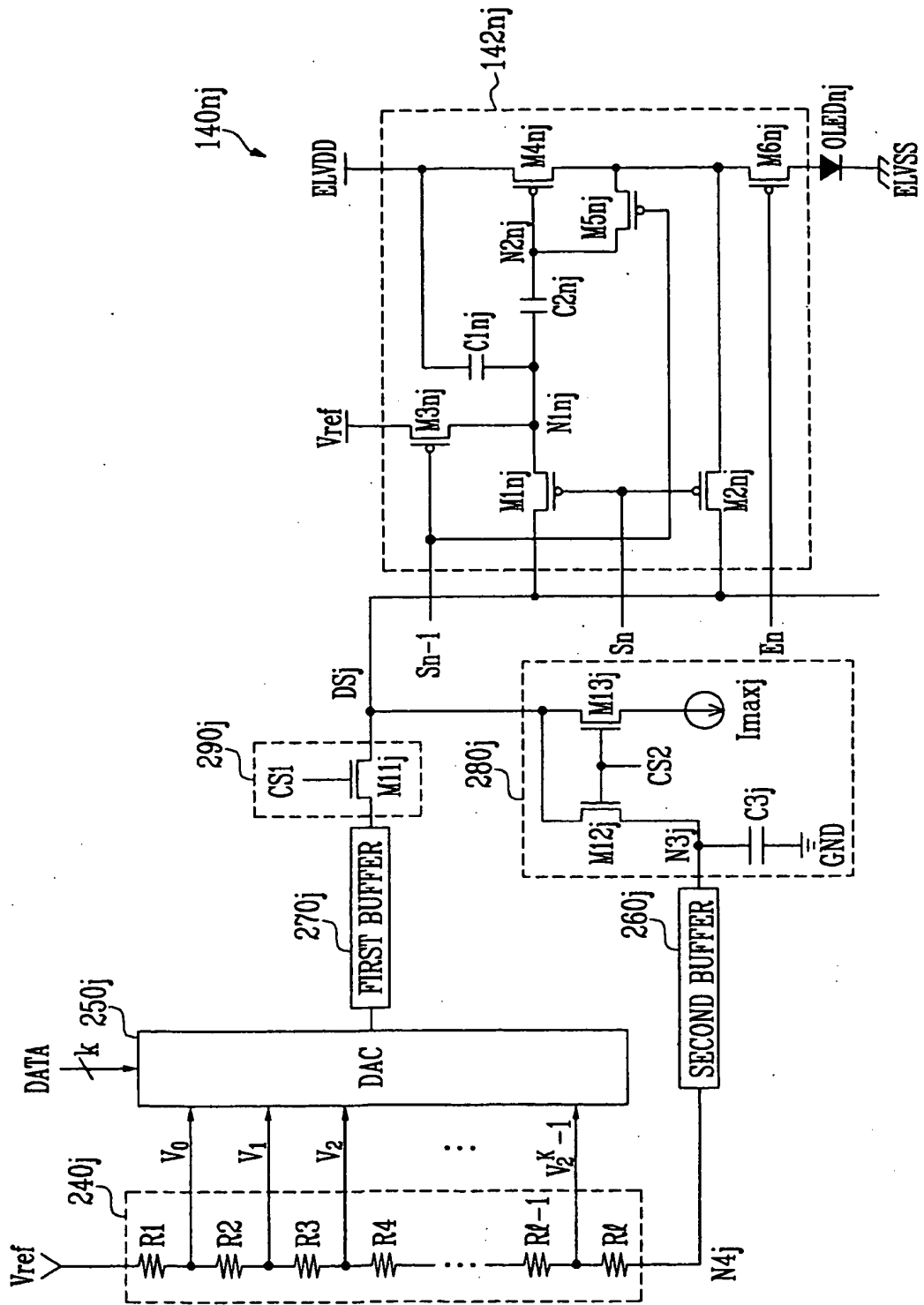


FIG. 9

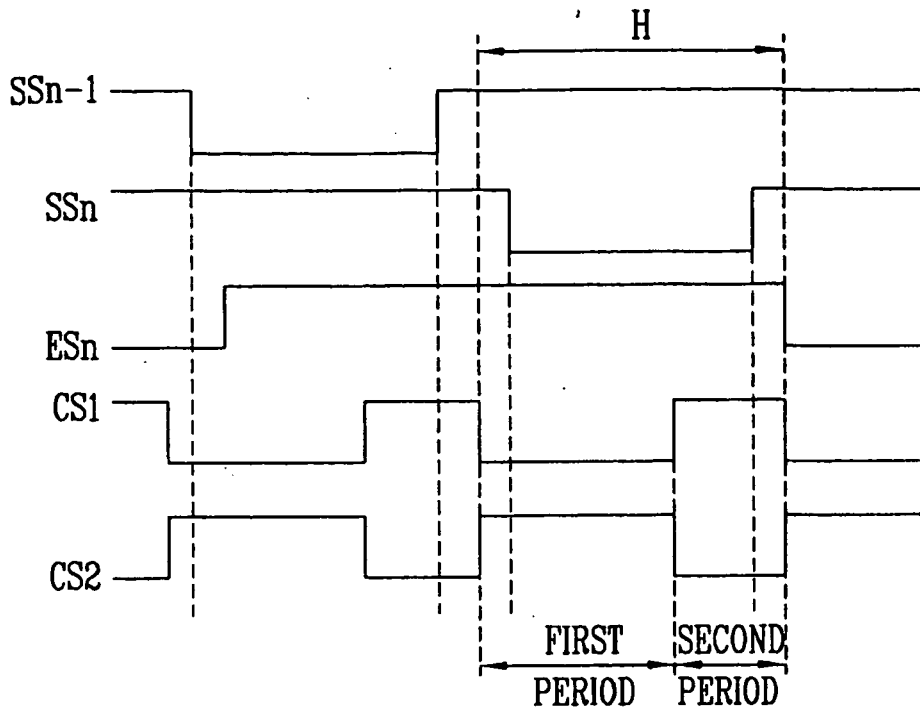




FIG. 11

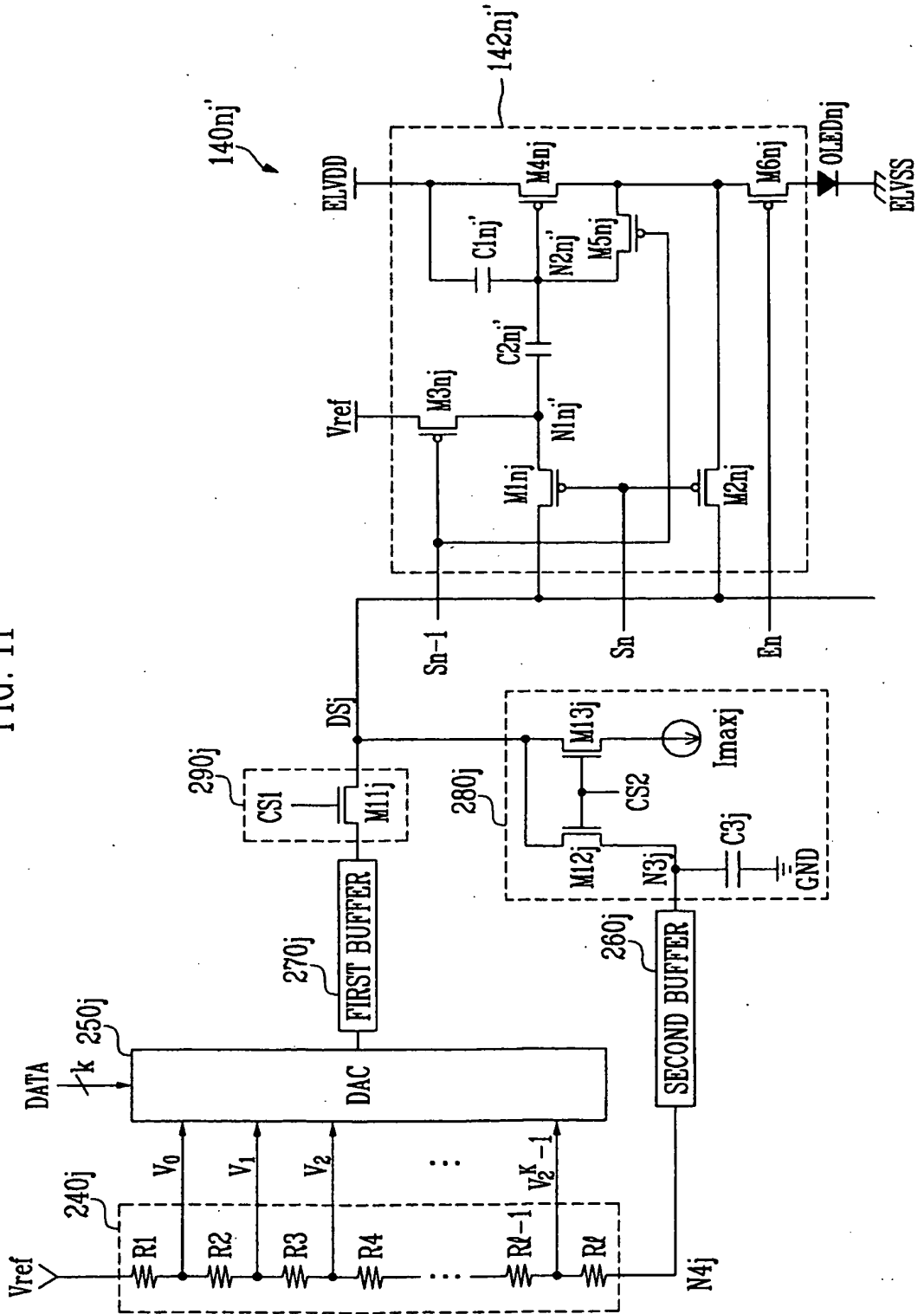
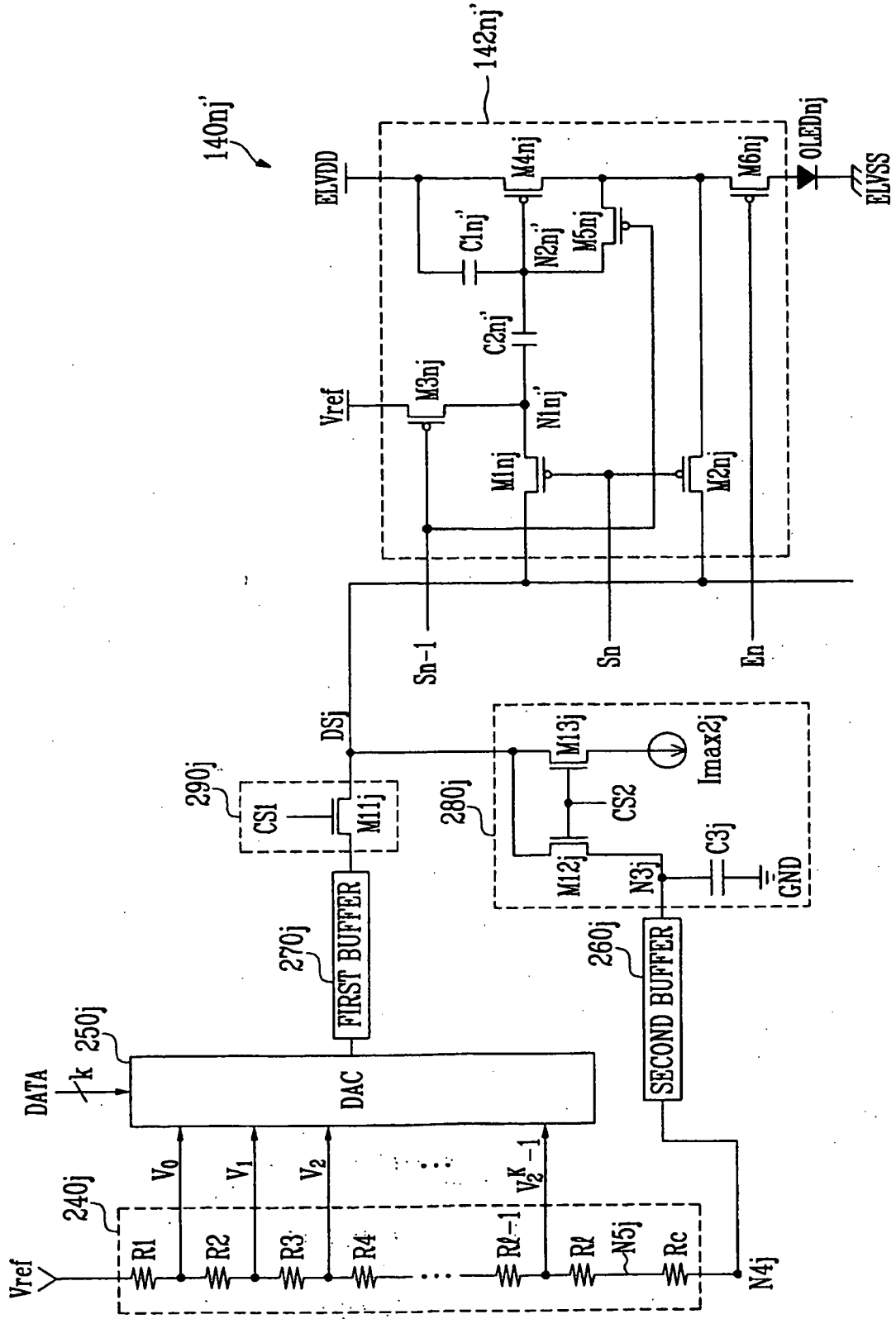




FIG. 13



**REFERENCES CITED IN THE DESCRIPTION**

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**Patent documents cited in the description**

- EP 1675093 A [0015]
- US 2005088103 A1 [0017]

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- **HAI-JUNG IN et al.** A Novel Voltage-Programming Pixel with Current-Correction Method for Large-Size and High-Resolution AMOLEDs on Poly-Si Backplane. *INTERNATIONAL MEETING ON INFORMATION DISPLAY*, 23 July 2005, vol. XX, XX (286), 901-904 [0016]

专利名称(译)	数据驱动电路，使用其的有机发光二极管显示器，以及驱动有机发光二极管显示器的方法		
公开(公告)号	<a href="#">EP1750246B1</a>	公开(公告)日	2015-06-24
申请号	EP2006254021	申请日	2006-08-01
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司 汉阳大学校产学协力团		
申请(专利权)人(译)	三星SDI CO. , LTD. IUCF-HYU ( 产学合作基金会汉阳大学 )		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
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IPC分类号	G09G3/32		
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优先权	1020050070440 2005-08-01 KR		
其他公开文献	EP1750246A2 EP1750246A3		
外部链接	<a href="#">Espacenet</a>		

摘要(译)

用于驱动发光显示器的像素以显示具有均匀亮度的图像的数据驱动电路可以包括电流吸收器，其能够经由数据线从像素接收预定电流以使数据驱动电路能够产生补偿像素的电压。补偿电压可以补偿显示器的像素之间的变化。像素之间的变化可能是由像素中包括的晶体管的不同电子迁移率和/或阈值电压引起的。预定电流的值可以等于或高于像素可用于发射最大亮度的光的最小电流的值。像素的最大亮度可以对应于当多个设置的灰度级电压中的最高者施加到像素时由像素发射的亮度。

[EQUATION 1]

$$V_{N1} = V_{ref}$$