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(54) **Data driving circuit, organic light emitting diode (OLED) display using the data driving circuit, and method of driving the OLED display**

Datentreiberschaltung, OLED (organische lichtemittierende Diode)-Anzeige mit der Datentreiberschaltung und Verfahren zur Ansteuerung der OLED-Anzeige

Circuit de commande de données, affichage à diodes électroluminescentes organiques utilisant le circuit de commande de données, et procédé de commande de l'affichage à diodes électroluminescentes organiques

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a data driving circuit, an Organic Light Emitting Diode (OLED) display using the data driving circuit, and a method of driving the OLED display, and more particularly, to a data driving circuit to display an image with a desired brightness, an OLED display using the data driving circuit, and a method of driving the OLED display.

2. Description of the Related Art

[0002] Various flat panel displays have recently been developed as alternatives to a relatively heavy and bulky Cathode Ray Tube (CRT) display. The flat panel display includes a Liquid Crystal Display (LCD), a Field Emission Display (FED), a Plasma Display Panel (PDP), an Organic Light Emitting Diode Display (OLED), etc.

[0003] Among the flat panel displays, the OLED display can emit light for itself by electron-hole recombination. Such an OLED display has advantages in that its response time is relatively fast and its power consumption is relatively low. Generally, the OLED display employs a transistor provided in each pixel for supplying a current corresponding to a data signal to a light emitting device, thereby allowing the light emitting device to emit light.

[0004] An OLED display comprises: a pixel portion including a plurality of pixels formed in a region defined by the intersection of scan lines and data lines; a scan driver to drive the scan lines; a data driver to drive the data lines; and a timing controller to control the scan driver and the data driver.

[0005] The timing controller generates a Data Control Signal (DCS) and a Scan Control Signal (SCS) corresponding to an external synchronization signal. The DCS and the SCS are supplied from the timing controller to the data driver and the scan driver, respectively. Furthermore, the timing controller supplies external data to the data driver.

[0006] The scan driver receives the SCS from the timing controller. The scan driver generates scan signals on the basis of the SCS and supplies the scan signals to the scan lines.

[0007] The data driver receives the DCS from the timing controller. The data driver generates data signals on the basis of the DCS and supplies the data signals to the data lines while synchronizing with the scan signals.

[0008] The display portion receives first and second voltages from an external power source, and supplies them to the respective pixels. When the first voltage and the second voltage are supplied to the pixels, each pixel controls a current corresponding to the data signal to flow from a first voltage line to a second voltage line via the light emitting device, thereby emitting light corresponding to the data signal.

[0009] That is, in this OLED display, each pixel emits light with a predetermined brightness corresponding to the data signal, but cannot emit light with the desired brightness because transistors provided in the respective pixels have different threshold voltages. Furthermore, in this OLED display, there is no method of measuring and controlling a real current flowing in each pixel in correspondence to the data signal.

[0010] Furthermore WO 03/107313 discloses a method of driving an organic light emitting display comprising the steps of: generating a first gradation voltage and a gradation current corresponding to data; supplying a first gradation voltage to the pixel; generating a pixel current corresponding to the first gradation voltage; supplying the pixel current to the data driver and comparing the gradation current with the pixel current.

[0011] Furthermore EP 0 378 249 A2 discloses a display circuit for a matrix display including a plurality of picture elements comprising display elements driven by drive circuits, wherein a data regenerative circuit determines whether an external video signal is to be displayed or whether the image being displayed by the picture elements is to be held.

[0012] Furthermore US 2003/0016201 A1 discloses an active matrix display device including a plurality of pixels arranged as rows and columns and column electrodes extending along corresponding columns of pixels, the pixels including a capacitance for storing image data and a read circuit for reading the charge stored on the capacitance and driving the column electrode with the read charge.

SUMMARY OF THE INVENTION

[0013] Accordingly, it is an object of the present invention to provide a data driving circuit to display an image with desired brightness, an Organic Light Emitting Diode (OLED) display using the data driving circuit, and a method of driving the OLED display.

[0014] The foregoing and/or other objects of the present invention are achieved by providing a data driving circuit for an organic light emitting diode display comprising a plurality of scan lines, a plurality of data lines, and a plurality of pixels at the intersections of the scan lines and the data lines, wherein each pixel comprises a driving transistor and an organic light emitting diode connected in series, the data driving circuit comprising: a voltage digital-analog converter adapted to generate a first gradation voltage corresponding to digital data supplied to the data driving circuit and to supply the first gradation voltage to a gate of the driving transistor via a data line in a first time period; a current digital-analog converter adapted to generate a gradation current corresponding to the digital data supplied to the data driving circuit; a voltage control unit adapted to receive in a second time period different from the first time period via the data line

a feedback pixel current flowing through the driving transistor of the pixel in response to the application of the first gradation voltage to the gate of the driving transistor in the first period, to compare the feedback pixel current with the gradation current, and to generate a second gradation voltage based on the result of the comparison of the feedback pixel current with the gradation current, a buffer unit adapted to selectively supply the first or second gradation voltage to the data line; and a selection unit adapted to selectively connect the data line to either the buffer unit or the voltage control unit.

[0015] The selection unit is adapted to preferably connect the data line to the buffer unit for a first period of one horizontal period, and is adapted to preferably alternately connect the data line to either the buffer unit or the voltage control unit for a second period of one horizontal period excluding the first period.

[0016] The selection unit comprises a plurality of selectors, each selector preferably comprising: a first transistor connected between the buffer unit and the data line; and a second transistor connected between the data line and the voltage control unit.

[0017] The first transistor is adapted to preferably be turned on for the first period, and the first and second transistors are adapted to preferably be alternately turned on and off for the second period.

[0018] The first gradation voltage is adapted to preferably be supplied to the pixel for the first period, and the second gradation voltage is adapted to preferably be supplied to the pixel upon the first transistor being turned on for the second period.

[0019] The pixel current is adapted to preferably be supplied from the data line to the voltage control unit upon the second transistor being turned on for the second period.

[0020] The voltage control unit comprises a plurality of voltage controllers, each voltage controller preferably comprising: a switching device connected between the voltage digital-analog converter and the buffer unit; a comparator adapted to preferably compare the gradation current with the pixel current; a capacitor having a first terminal connected to a common node between the switching device and the buffer unit; a voltage adjuster connected to a second terminal of the capacitor and adapted to preferably be controlled by the comparator to increase and decrease the voltage supplied to the second terminal of the capacitor; and a controller adapted to preferably control the switching device.

[0021] The controller is adapted to preferably turn on the switching device for the first period, and to preferably turn off the switching device for the second period.

[0022] The comparator is adapted to preferably generate a first control signal upon the gradation current being higher than the pixel current, and is adapted to preferably generate a second control signal upon the gradation current being lower than the pixel current.

[0023] The voltage adjuster is adapted to preferably selectively increase or decrease the voltage supplied to the capacitor on the basis of the first and second control signals to equalize the pixel current with the gradation current.

[0024] The controller is adapted to preferably output a counting signal, gradually increased for the second period, to the voltage adjuster.

[0025] An adjustable level of the voltage adjusted by the voltage adjuster is adapted to preferably correspond to the counting signal.

[0026] The adjustable level of the voltage adjusted by the voltage adjuster is adapted to preferably decrease in proportion as the counting signal increases.

[0027] The adjustable level of the voltage adjusted by the voltage adjuster is adapted to preferably decrease by half whenever the counting signal increases.

[0028] The controller is adapted to preferably receive a reset signal each horizontal period and to initialize the counting signal.

[0029] The reset signal preferably includes either a horizontal synchronous signal or a scan signal supplied to the pixel each horizontal period.

[0030] The data driving circuit preferably further comprises: a shift register adapted to preferably generate sampling signals in sequence; and a latch adapted to preferably store the data corresponding to the sampling signals, and to preferably supply the stored data to the voltage digital-analog converter and the current digital-analog converter.

[0031] The latch preferably comprises: a sampling latch adapted to preferably sequentially store the data corresponding to the sampling signal; a holding latch adapted to preferably store the data stored in the sampling latch and to preferably supply the stored data to the voltage digital-analog converter and the current digital-analog converter.

[0032] The data driving circuit preferably further comprises a level shifter adapted to preferably increase a voltage of the data stored in the holding latch and to supply the increased data to the voltage digital-analog converter and the current digital-analog converter.

[0033] The foregoing and/or other objects of the present invention are also achieved by providing an Organic Light Emitting Diode (OLED) display comprising: a plurality of first and second scan lines; a plurality of data lines intersecting the first and second scan lines; a pixel portion including a plurality of pixels connected to the first and second scan lines and the data lines; a scan driver adapted to respectively supply first and second scan signals to the first and second scan lines; and a data driver connected to the data lines and adapted to supply a first gradation voltage as a data signal to the data lines; wherein the data driver comprises at least one above-mentioned data driving circuit.

[0034] Preferably each pixel comprises: a light emitting device; a driver adapted to generate the pixel current corresponding to either the first or second voltage; a first transistor connected between the driver and the data line, and adapted to be controlled by a first scan signal sup-

plied via the first scan line; and a second transistor connected between the data line and a common node between the driver and the light emitting device, and adapted to be controlled by a second scan signal supplied via the second scan line. Preferably the first transistor is adapted to be turned on in correspondence with the first scan signal for a first period of one horizontal period, and is adapted to be turned on and off at least one time for a second period of the horizontal period excluding the first period. Preferably the second transistor is adapted to be turned off in correspondence with the second scan signal for the first period, and is adapted to be turned on and off alternately with the first transistor for the second period. Preferably the display further comprises a third transistor connected between the driver and the light emitting device, and adapted to be turned off for a predetermined period upon the first scan signal being supplied to the first transistor and adapted to be turned on for the other period in correspondence with an emission control signal supplied via an emission control line. Preferably the selection unit is adapted to connect the data line to the buffer unit for the first period, and is adapted to alternately connect the data line between the buffer unit and the voltage control unit for the second period. Preferably the first gradation voltage or the second gradation voltage is adapted to be supplied from the buffer unit to the pixel via the data line upon the third transistor being turned on, and the pixel current is adapted to be supplied to the voltage control unit via the data line upon the fourth transistor being turned on.

[0035] The foregoing and/or other objects of the present invention are further achieved by providing a method of driving an organic light emitting diode display comprising a plurality of scan lines, a plurality of data lines, and a plurality of pixels at the intersections of the scan lines and the data lines, wherein each pixel comprises a driving transistor and an organic light emitting diode connected in series, and a data driving circuit with a voltage digital-analog converter, a current digital-analog converter, and a voltage control unit, the method comprising the steps of: generating a first gradation voltage corresponding to digital data supplied to the data driving circuit with the voltage digital-analog converter, generating a gradation current corresponding to the digital data with the current digital-analog converter; supplying the first gradation voltage to the gate of the driving transistor of a pixel via a data line in a first time period; generating a pixel current with the driving transistor of the pixel corresponding to the first gradation voltage; supplying the pixel current to the data driving circuit via the data line in a second time period different from the first time period; and comparing the gradation current with the pixel current with the voltage control unit, and generating a second gradation voltage with the voltage control unit by increasing or decreasing a level of the first gradation voltage on the basis of the comparison of the gradation voltage with the pixel current.

[0036] The method preferably further comprises supplying the first gradation voltage to the pixel for a first period of one horizontal period.

[0037] The method preferably further comprises: generating the second gradation voltage by increasing or decreasing the level of the first gradation voltage on the basis of the compared result to cause the pixel current be equal to the gradation current; and supplying the second gradation voltage to the pixel via the data line.

[0038] The method preferably further comprises repeating supplying the pixel current to the data driver via the data line; and comparing the gradation current with the pixel current with the data driver, and generating a second gradation voltage by increasing or decreasing a level of the first gradation voltage on the basis of the compared result at least one time for a second period of one horizontal period excluding the first period.

[0039] The method preferably further comprises: generating a counting signal, gradually increased for the second period; and controlling an adjustable level of the first gradation voltage in accordance with the counting signal.

[0040] The method preferably further comprises decreasing the adjustable level of the first gradation voltage in proportion as the counting signal increases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0041] A more complete appreciation of the present invention, and many of the attendant advantages thereof, will be readily apparent as the present invention becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

FIG. 1 is a view of an Organic Light Emitting Diode (OLED) display;
FIG. 2 is a view of an OLED display according to an embodiment of the present invention;
FIG. 3 is a circuit diagram of a pixel of FIG. 2;
FIG. 4 is a view of waveforms of signals for driving the pixel of FIG. 3;
FIG. 5 is a block diagram of an embodiment of a data driving circuit of FIG. 2;
FIG. 6 is a block diagram of another embodiment of the data driving circuit of FIG. 2;
FIG. 7 is a circuit diagram including a voltage controller and a selector of FIG. 3 and 4;
FIG. 8 is a view of a waveform of a selection signal supplied to the selector of FIG. 7;
FIG. 9 is a graph to explain the operation of the voltage adjuster of FIG. 7; and
FIG. 10 is a detailed circuit diagram of the comparator of FIG. 7.

DETAILED DESCRIPTION OF INVENTION

[0042] FIG. 1 is a view of an OLED display. Referring to FIG. 1, an OLED display comprises: a pixel portion 30

including a plurality of pixels 40 formed in a region defined by the intersection of scan lines S1 through Sn and data lines D1 through Dm; a scan driver 10 to drive the scan lines S1 through Sn; a data driver 20 to drive the data lines D1 through Dm; and a timing controller 50 to control the scan driver 10 and the data driver 20.

[0043] The timing controller 50 generates a Data Control Signal (DCS) and a Scan Control Signal (SCS) corresponding to an external synchronization signal. The DCS and the SCS are supplied from the timing controller 50 to the data driver 20 and the scan driver 10, respectively. Furthermore, the timing controller 50 supplies external data to the data driver 20.

[0044] The scan driver 10 receives the SCS from the timing controller 50. The scan driver 10 generates scan signals on the basis of the SCS and supplies the scan signals to the scan lines S1 through Sn.

[0045] The data driver 20 receives the DCS from the timing controller 50. The data driver 20 generates data signals on the basis of the DCS and supplies the data signals to the data lines D1 through Dm while synchronizing with the scan signals.

[0046] The display portion 30 receives first and second voltages ELVDD and ELVSS from an external power source, and supplies them to the respective pixels 40. When the first voltage ELVDD and the second voltage ELVSS are supplied to the pixels 40, each pixel 40 controls a current corresponding to the data signal to flow from a first voltage line ELVDD to a second voltage line ELVSS via the light emitting device, thereby emitting light corresponding to the data signal.

[0047] That is, in this OLED display, each pixel 40 emits light with a predetermined brightness corresponding to the data signal, but cannot emit light with the desired brightness because transistors provided in the respective pixels 40 have different threshold voltages. Furthermore, in this OLED display, there is no method of measuring and controlling a real current flowing in each pixel 40 in correspondence to the data signal.

[0048] Hereinafter, exemplary embodiments according to the present invention will be described with reference to the accompanying drawings, wherein the exemplary embodiments of the present invention are provided to be readily understood by those skilled in the art.

[0049] FIG. 2 illustrates an OLED display according to an embodiment of the present invention.

[0050] Referring to FIG. 2, an OLED display according to an embodiment of the present invention comprises: a pixel portion including a plurality of pixels 140 formed in regions defined by first scan lines S11 through S1n, second scan lines S21 through S2n, emission control lines E1 through En, and data lines D1 through Dm; a scan driver 110 to drive the first scan lines S11 through S1n, the second scan lines S21 through S2n, and the emission control lines E1 through En; a data driver to drive the data lines D1 through Dm; and a timing controller 150 to control the scan driver 110 and the data driver 120.

[0051] The pixel portion 130 includes the plurality of pixels 140 formed in regions defined by the first scan lines S11 through S1n, the second scan lines S21 through S2n, the emission control lines E1 through En, and the data lines D1 through Dm. The pixels 140 receive external first and second voltages ELVDD and ELVSS. When the first voltage ELVDD and the second voltage ELVSS are supplied to the pixels 140, each pixel 140 controls a pixel current to flow from the first voltage line ELVDD to the second voltage line ELVSS via a light emitting device in correspondence with a data signal transmitted via the data line D. Furthermore, the pixel 140 supplies the pixel current to the data driver 120 via the data line D for a partial horizontal period. Thus, each pixel 140 is configured as shown in FIG. 3, which will be described later.

[0052] The timing controller 150 generates a DCS and an SCS in response to external synchronization signals. The timing controller 150 supplies the DCS and the SCS to the data driver 120 and the scan driver 110, respectively. Furthermore, the timing controller 150 supplies external data Data to the data driver 120.

[0053] The scan driver 110 receives the SCS from the timing controller 150. In response to the SCS, the scan driver 110 sequentially supplies first scan signals to the first scan lines S11 through S1n, and at the same time sequentially supplies second scan signals to the second scan lines S21 through S2n.

[0054] As shown in FIG. 4, the scan driver 110 supplies a first scan signal to turn on a first transistor M1 provided in the pixel 140 for a first period of one horizontal period, and to repeatedly turn on and off the first transistor M1 for a second period of one horizontal period. Furthermore, the scan driver 110 supplies a second scan signal to turn off a second transistor M2 provided in the pixel 140 for the first period of one horizontal period, and to repeatedly turn on and off the second transistor M2 alternately with the first transistor M1. The scan driver 110 also supplies an emission control signal to turn off a third transistor M3 provided in the pixel 140 for a predetermined horizontal period during which the first and second scan signals are supplied, and to turn on the third transistor M3 for the other period. According to an embodiment of the present invention, the emission control signal is supplied overlapping with the first and second scan signals, and has a width equal to or greater than that of the first scan signal.

[0055] The data driver 120 receives the DCS from the timing controller 150. Then, the data driver 120 generates the data signal in response to the DCS, and supplies the data signal to the data lines D1 through Dm. The data driver 120 supplies a predetermined gradation voltage as the data signal to the data lines D1 through Dm.

[0056] The data driver 120 receives a pixel current from the pixel 140 for a partial second period of one horizontal period, and checks whether the received pixel current has a level corresponding to the data Data. For example, when a pixel current flowing in the pixel 140 corresponding to a bit value (or gradation level) of the data

Data is 10μA, the data driver 120 checks whether the pixel current received from the pixel 140 is 10μA. When the data driver 120 receives an undesired current from each pixel 140, the data driver 120 adjusts the gradation voltage, thereby allowing a desired current to flow in each pixel 140. The data driver 120 comprises at least one data driving circuit 129 having j channels (where, j is a natural number). A detailed configuration of the data driving circuit 129 is described later.

[0057] FIG. 3 is a circuit diagram of a pixel of FIG. 2. For the sake of convenience, FIG. 3 exemplarily illustrates a pixel that is connected to the mth data line Dm, the nth first scan line S1n, the nth second scan line S2n, and the nth emission control line En.

[0058] Referring to FIG. 3, the pixel 140 according to an embodiment of the present invention comprises a first transistor M1, a second transistor M2, a third transistor M3 and a driver 142.

[0059] The first transistor M1 is connected between the data line Dm and a driver 142, and supplies the gradation voltage from the data line Dm to the driver 142. The first transistor M1 is controlled by the first scan signal transmitted to the nth first scan line S1n.

[0060] The second transistor M2 is connected between a data line Dm and the driver 142, and supplies the pixel current from the driver 142 to the data line Dm. The second transistor M2 is controlled by the second scan signal transmitted to the nth second scan line S2n.

[0061] The third transistor M3 is connected between the driver 142 and a light emitting device OLED. The third transistor M3 is controlled by the emission control signal transmitted to the nth emission control line En. The emission control signal is supplied overlapping with the first and second scan signals respectively supplied to the nth first and second scan lines S1n and S2n. The third transistor M3 is turned off while the emission control signal is being supplied, and is turned on while the emission control signal is not being supplied.

[0062] The driver 142 supplies the pixel current to the second transistor M2 and the third transistor M3 in correspondence with the data signal received from the first transistor M1. The driver 142 comprises a fourth transistor M4 connected between the first voltage line ELVDD and the third transistor M3, and a capacitor C connected between a gate electrode of the fourth transistor M4 and the first voltage line ELVDD. Alternatively, the driver 142 is not limited to the configuration shown in FIG. 3, and can comprise various well-known circuits. Also, the transistors M1 through M4 shown in FIG. 3 are illustrated as P-channel Metal Oxide Semiconductor (PMOS) transistors. However, the present invention is not limited thereto.

[0063] Referring to FIGS. 3 and 4, the pixel 140 operates as follows.

[0064] For a predetermined horizontal period of one frame, the first scan signal is supplied through the nth first scan line S1n, and at the same time, the second scan signal is supplied through the nth second scan line S2n.

[0065] The first transistor M1 receives the first scan signal and is turned on from the first period of one horizontal period. As the first transistor M1 is turned on, the data signal of the data line Dm is supplied to the capacitor C for the first period. The capacitor C is charged with a predetermined voltage corresponding to the data signal. The second transistor M2 receives the second scan signal and is maintained turned off for the first period.

[0066] Then, the first transistor M1 is turned off and the second transistor M2 is turned on for a part of a second period. As the second transistor M2 is turned on, the pixel current is supplied from the fourth transistor M4 to the data line Dm in correspondence with a predetermined voltage charged in the capacitor C. Thus, the pixel current is supplied from the data line Dm to the data driver 120, and the data driver 120 increases or decreases the level of the gradation voltage in accordance with the pixel current, thereby allowing a desired pixel current to flow in the pixel 140.

[0067] Then, the second transistor M2 is turned off, and the first transistor M1 is turned on. As the first transistor M1 is turned on, the gradation voltage increased or decreased by the data driver 120 is supplied to the capacitor C, thereby controlling the level of the voltage charged in the capacitor C. The first transistor M1 and the second transistor M2 are alternately turned on and off at least once in the second period, so that the voltage charged in the capacitor C is controlled to allow the desired pixel current to flow in the pixel 140.

[0068] The emission control signal is supplied to the nth emission control line En for the predetermined horizontal period, so that the third transistor M3 is turned off. Therefore, the pixel current is not supplied to the light emitting device OLED. Then, the emission control signal is not supplied to the nth emission control line En after the passage of the predetermined horizontal period, so that the third transistor M3 is turned on and the pixel current is supplied to the light emitting device OLED. The pixel current is adjusted to a desired value for the predetermined horizontal period, so that the light emitting device OLED can emit light with a desired brightness.

[0069] FIG. 5 is a block diagram of an embodiment of a data driving circuit of FIG. 2. For the sake of convenience, FIG. 5 exemplarily illustrates a pixel integrated circuit 129 having j channels.

[0070] Referring to FIG. 5, the data driving circuit 129 comprises a shift register 200 to generate sampling signals in sequence; a sampling latch 210 to store the data Data in sequence in response to the sampling signals; a holding latch 220 to temporarily store the data Data of the sampling latch 210 and supply the stored data Data to a voltage digital-analog converter (VDAC) 230 and a current digital-analog converter (IDAC) 240, the VDAC 230 to generate the gradation voltage Vdata corresponding to a gradation level of the data Data and the IDAC 240 to generate the gradation current Idata corresponding to the gradation level of the data Data; a voltage control unit 250 to control a gradation voltage Vdata in correspondence with the pixel current Ipixel supplied via the

data lines D1 through Dj; a buffer unit 260 to supply the gradation voltage Vdata from the voltage control unit 250 to the data lines D1 through Dj; and a selection unit 280 to selectively connect the data lines D1 through Dj to either of the buffer unit 260 or the voltage control unit 250.

[0071] The shift register part 200 receives a source shift clock SSC and a source start pulse SSP from the timing controller 150 and shifts the source start pulse SSP per period of the source shift clock SSC, thereby generating j sampling signals in sequence. The shift register 200 comprises j shift registers 2001 through 200j.

[0072] The sampling latch 210 stores the data Data therein in sequence in response to the sampling signals sequentially supplied from the shift register 200. The sampling latch 210 comprises j sampling latches 2101 through 210j to store j data Data therein. Furthermore, the size of each sampling latches 2101 through 210j corresponds to a bit value of the data Data. For example, when the data Data is of k bits, each of the sampling latches 2101 through 210j has a size corresponding to k bits.

[0073] The holding latch 220 receives the data Data from the sampling latch 210 and stores it therein in response to a source output enable signal SOE. Furthermore, the holding latch 220 supplies the data Data stored therein to the VDAC 230 and the IDAC 240 in response to the source output enable signal SOE. The holding latch 220 comprises j holding latches 2201 through 220j each corresponding to k bits.

[0074] The VDAC 230 generates the gradation voltage Vdata corresponding to the bit value (i.e., gradation level) of the data Data, and supplies the gradation voltage Vdata to the voltage control unit 250. The VDAC 230 generates j gradation voltages Vdata corresponding to j data Data supplied from the holding latch 220. The VDAC 230 comprises j voltage generators 2301 through 230j. For the sake of convenience, the gradation voltage Vdata generated by the VDAC 230 will be called a first gradation voltage Vdata.

[0075] The IDAC 240 generates the gradation current Idata corresponding to the bit value of the data Data, and supplies the gradation current to the voltage control unit 250. The IDAC 240 generates j gradation currents Idata corresponding to j data Data supplied from the holding latch 220. The IDAC 240 comprises j current generators 2401 through 240j.

[0076] The current control unit 250 receives the first gradation voltage Vdata, the gradation current Idata and the pixel current Ipixel, and compares the gradation current Idata with the pixel current Ipixel, thereby controlling the level of the first gradation voltage Vdata on the basis of difference between the gradation current Idata and the pixel current Ipixel. Hereinafter, for the sake of convenience, the first gradation voltage Vdata controlled by the voltage control unit 250 will be called a second gradation voltage. Preferably, the voltage control unit 250 controls the level of the second gradation voltage to make the gradation current Idata equal to the pixel current Ipixel. The voltage control unit 250 comprises j voltage controllers 2501 through 250j.

[0077] The buffer unit 260 supplies the first gradation voltage Vdata or the second gradation voltage from the voltage control unit 250 to j data lines D1 through Dj. The buffer unit 260 comprises j buffers 2601 through 260j.

[0078] The selection unit 280 selectively connects the data lines D1 through Dj to either of the buffer unit 260 or the voltage control unit 250. The selection unit 260 comprises j selectors 2801 through 280j.

[0079] According to another embodiment of the present invention, the data driving circuit 129 further comprises a level shifter 270 between the holding latch part 220 and both the VDAC 230 and IDAC 240 as shown in FIG. 6. The level shifter part 270 increases the voltage level of the data Data supplied from the holding latch 220, and supplies it to the VDAC 230 and the IDAC 240. When the data Data having a high voltage level is supplied from an external system to the data driving circuit 129, circuit elements are needed for the high voltage level, so that production costs are increased. However, according to this embodiment of the present invention, even though the external system supplies the data Data having a low voltage level to the data driving circuit 129, the level shifter 270 increases the voltage level of the data Data into the high level, so that the circuit elements for the high voltage level are not additionally needed, thereby reducing the corresponding production costs. The level shifter 270 comprises j level shifters 2701 through 270j.

[0080] FIG. 7 is a circuit diagram including a voltage controller and a selector of FIG. 5. For the sake of convenience, FIG. 7 exemplarily illustrates the jth voltage controller 250j and the jth selector 280j.

[0081] Referring to FIG. 7, the selector 280j comprises a fifth transistor M5 connected between the buffer 260j and the data line Dj, and a sixth transistor M6 connected between the voltage controller 250j and the data line Dj. The fifth transistor M5 and the sixth transistor M6 are alternately turned on, and connect the data line Dj with either of the buffer 260j or the voltage controller 250j. For this, the fifth transistor M5 and the sixth transistor M6 are different conductive types. The fifth transistor M5 and the sixth transistor M6 are controlled by a selection signal supplied via a control line CL.

[0082] As shown in FIG. 8, the selection signal is supplied for the first period of one horizontal period to turn on the fifth transistor M5. Furthermore, the selection signal is supplied to alternately turn on and off the fifth and sixth transistors M5 and M6 for the second period. For the second period, the selection signal is supplied to turn on and off the fifth transistor M5 in accordance with the first transistor M2, and to turn on and off the sixth transistor M6 in accordance with the second transistor M2.

[0083] The current controller 250j comprises a comparator 252, a voltage adjuster 254, a controller 256, a first capacitor C1, and a switching device SW1. The switching device SW1 is connected between the VDAC 230 and the buffer unit 260j. Furthermore, the switching

device SW1 is controlled by the controller 256 to be turned on for the first period and tuned off for the second period.

[0084] The first capacitor C1 is connected between the voltage adjuster 254 and a first node N1 formed as a common node between the switching device SW1 and the buffer unit 260j. The first capacitor C1 connected between the first node N1 and the voltage adjuster 254 increases or decreases the level of voltage supplied to the first node N1 in correspondence with the voltage supplied from the voltage adjuster 254. For instance, when the voltage adjuster 254 supplies a high level voltage, the voltage supplied to the first node N1 is increased by the first capacitor C1. On the other hand, when the voltage adjuster 254 supplies a low level voltage, the voltage supplied to the first node N1 is decreased by the first capacitor C1.

[0085] The comparator 252 receives the gradation current Idata from the IDAC 240 and receives the pixel current Ipixel from the pixel 140 via the data line Dj and the selector 280j. The pixel current Ipixel is supplied from the pixel 140 that currently receives the first and second scan signals. Then, the comparator 242 receives the gradation current Idata and the pixel current Ipixel, and compares the gradation current Idata with the pixel current Ipixel, thereby supplying first and second control signals corresponding to the compared results to the voltage adjuster 254. For example, the comparator 252 generates the first control signal when the gradation current Idata is higher than the pixel current Ipixel. Furthermore, the comparator 242 generates a second control signal when the gradation current Idata is lower than the pixel current Ipixel.

[0086] The voltage adjuster 254 controls a predetermined voltage to the first capacitor C1 on the basis of the first and second control signal supplied from the comparator 252. The voltage adjuster 254 supplies the predetermined voltage to the first capacitor C1 so that the pixel current Ipixel is approximately equal to the gradation current Idata. Then, the voltage supplied to the first node N1 is increased or decreased corresponding to the voltage supplied to the first capacitor C1. The increased or decreased voltage of the first node N1 is used as the second gradation voltage.

[0087] The controller 256 turns on the switching device SW1 for the first period of one horizontal period 1H, and turns off the switching device SW1 for the second period. Furthermore, the controller 256 supplies a counting signal to the voltage adjuster 254, wherein the counting signal is gradually increased for the second period. For example, the controller 256 supplies the counting signal to the voltage adjuster 254, wherein the counting signal increases from "1" to "1" (where, "1" is a natural number). The controller 256 comprises a counter (not shown). The counting signal of the controller 256 is initialized in response to a reset signal. The reset signal is set to be supplied each horizontal period. For example, a horizontal synchronous signal H or a scan signal can be employed as the reset signal.

[0088] The voltage controller according to this embodiment of the present invention operates as follows. First, the switching device SW1, the fifth transistor M5, and the first transistor ml are turned on for the first period of one horizontal period. When the switching device SW1 is turned on, the first gradation voltage Vdata is supplied from the VDAC 230 to the data line Dj via the buffer 260j and the fifth transistor M5. Then, the first gradation voltage Vdata is supplied from the data line Dj to the pixel 140 selected by the scan signal. That is, the first gradation voltage Vdata is supplied from the data line Dj to the driver 142 via the first transistor M1 turned on by the first scan signal. Then, the capacitor C of the driver 142 is charged with a voltage corresponding to the first gradation voltage Vdata. The first period is set to allow the capacitor C of the pixel 140 to be charged to a predetermined voltage corresponding to the first gradation voltage Vdata.

[0089] After the capacitor C of the pixel 140 is charged to the voltage corresponding to the first gradation voltage Vdata, at the beginning of the second period, the sixth and second transistors M6 and M2 are turned on, and the switching device SW1 and the fifth and first transistors M5 and M1 are turned off.

[0090] As the switching device SW1 is turned off, the first node is in a floating state. At this time, the voltage supplied to the first node is maintained as the first gradation voltage Vdata by a parasitic capacitor (not shown) or the like. Furthermore, the second transistor M2 is turned on, the pixel current Ipixel generated by the driver 142 of the pixel 140 is supplied to the comparator 252 via the second transistor M2, the data line Dj and the sixth transistor M6.

[0091] The comparator 252 receives the pixel current Ipixel and compares the pixel current Ipixel with the gradation current Idata supplied from the IDAC 240, thereby outputting the first and second control signals to the voltage adjuster 254 on the basis of the compared results. The gradation current Idata is an ideal current that should flow in the pixel 140 corresponding to the data Data, and the pixel current Ipixel is a real current that flows in the pixel 140.

[0092] For the second period, the controller 256 supplies the counting signal, which increases from "1" to "1", to the voltage adjuster 254. Then, the voltage adjuster 254 receives the counting signal and supplies a predetermined voltage corresponding to the first or second control signal of the comparator 252 to the first capacitor C1. The voltage adjuster 254 adjusts the voltage supplied to the first capacitor C1 on the basis of the first or second control signal so that the gradation current Idata and the pixel current Ipixel are approximately equal to each other. Then, the voltage supplied to the first node N1 varies corresponding to the voltage supplied to the first capacitor C1, thereby generating the second gradation voltage.

[0093] After the second gradation voltage has been generated, the sixth and second transistors M6 and M2 are turned off, and the fifth and first transistors M5 and

M1 are turned on. When the fifth transistor M5 and the first transistor M1 are turned on, the second gradation voltage supplied to the first node N1 is supplied to the pixel 140. Then, the pixel 140 generates the pixel current Ipixel corresponding to the second gradation voltage. According to this embodiment of the present invention, the sixth and second transistors M2 and M6 are turned on and off alternately with the fifth and first transistors M1 and M5 at least one time for the second period, so that the gradation current Idata is similar or equal to the pixel current Ipixel.

[0094] An adjustable level of the voltage adjusted by the voltage adjuster 254 is determined by the counting signal. For example, when the voltage adjuster 254 receives the first counting signal (e.g., "1"), the voltage adjuster 254 adjusts the voltage to a first voltage (V1) as shown in FIG. 9. That is, when the first counting signal is supplied, the voltage is increased or decreased corresponding to a voltage of V1/2. Furthermore, when the voltage adjuster 254 receives the second counting signal (e.g., "2"), the voltage adjuster 254 adjusts the voltage to a second voltage V2 lower than the first voltage V1. That is, when the second counting signal is supplied, the voltage is increased or decreased corresponding to a voltage of V2/2. The second voltage V2 is set to about one half of the first voltage V1. Also, when the voltage adjuster 254 receives the third counting signal (e.g., "3"), the voltage adjuster 254 adjusts the voltage to a third voltage V3 lower than the second voltage V2. Thus, the more the counting signal increases, the more the adjustable level of the voltage adjusted by the voltage adjuster 254 decreases. The decreased voltage can be set to one half of the previous voltage. Likewise, the voltage adjuster 254 adjusts the voltage supplied to the first capacitor C1 so that the gradation current Idata and the gradation voltage Idata are similar or equal to each other.

[0095] FIG. 10 is a detailed circuit diagram of the comparator of FIG. 7. The comparator of FIG. 10 was disclosed by the Institute of Electrical and Electronics Engineers (IEEE) in 1992. However, the comparator according to an embodiment of the present invention is not limited to that proposed by the IEEE. Alternatively, various well-known comparators can be used in the present invention as long as it can compare the currents.

[0096] Referring to FIG. 10, a current corresponding to difference between the pixel current Ipixel and the gradation current Idata is supplied to a second node N2. The current supplied to the second node N2 is supplied to gate terminals of third and fourth transistors M13 and M14 formed as an inverter. Then, either of the third transistor M13 or the fourth transistor M14 is turned on, thereby supplying a high voltage VDD or a low voltage GND to an output terminal. The voltage supplied to the output terminal is supplied to the gate terminals of first and second transistors M11 and M12, thereby stably maintaining the voltage supplied to the output terminal.

[0097] As described above, the present invention provides a data driving circuit to display an image with a desired brightness, an OELD display using the data driving circuit, and a method of driving the OELD display, in which a gradation current corresponding to data is compared with a pixel current flowing in a pixel, and a gradation voltage is controlled on the basis of the compared result so that the pixel current is approximately equal to the gradation current. According to an embodiment of the present invention, the pixel current is supplied from the pixel to the data driving circuit via a data line, and the gradation voltage is supplied from the data driving circuit to the pixel via the data line. Thus, the data line is shared in driving the OELD display according to an embodiment of the present invention, so that an additional line on a pixel portion is not needed, thereby improving an aperture ratio and simplifying the fabrication process.

[0098] Although exemplary embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that modifications can be made to these embodiment without departing from the principles of the present invention, the scope of which is defined by the following claims.

Claims

1. A data driving circuit (129) for an organic light emitting diode display comprising a plurality of scan lines (S11, S21, S12, S22, S1n, S2n), a plurality of data lines (D1, D2, Dm, Dj), and a plurality of pixels (140) at the intersections of the scan lines (S11, S21, S12, S22, S1n, S2n) and the data lines (D1, D2, Dm, Dj), wherein each pixel (140) comprises a driving transistor (M4) and an organic light emitting diode (OLED) connected in series, the data driving circuit (129) comprising:

   a voltage digital-analog converter (230) adapted to generate a first gradation voltage corresponding to digital data supplied to the data driving circuit (129) and to supply the first gradation voltage to a gate of the driving transistor (M4) via a data line (Dj) in a first time period;
   a current digital-analog converter (240) adapted to generate a gradation current corresponding to the digital data supplied to the data driving circuit (129);
   a voltage control unit (250, 250j) adapted to receive in a second time period different from the first time period via the data line (Dj) a feedback pixel current flowing through the driving transistor (M4) of the pixel (140) in response to the application of the first gradation voltage to the gate of the driving transistor (M4) in the first period, to compare the feedback pixel current with the gradation current, and to generate a second gradation voltage based on the result of the comparison of the feedback pixel current with the gradation current,

a buffer unit (260, 260j) adapted to selectively supply the first or second gradation voltage to the data line (Dj); and
a selection unit (280, 280j) adapted to selectively connect the data line (Dj) to either the buffer unit (260, 260j) or the voltage control unit (250, 250j).

2. The data driving circuit according to claim 1, wherein the selection unit (250, 250j) is adapted to connect the data line (Dj) to the buffer unit (260, 260j) for a first period of one horizontal period, and is adapted to alternately connect the data line (Dj) to either the buffer unit (260, 260j) or the voltage control unit (250, 250j) for a second period of one horizontal period excluding the first period.

3. The data driving circuit according to claim 2, wherein the selection unit comprises a plurality of selectors, each selector comprising:

a first transistor connected between the buffer unit and the data line; and
a second transistor connected between the data line and the voltage control unit.

4. The data driving circuit according to claim 3, wherein the first transistor is adapted to be turned on for the first period, and the first and second transistors are adapted to be alternately turned on and off for the second period.

5. The data driving circuit according to claim 4, wherein the first gradation voltage is adapted to be supplied to the pixel for the first period, and the second gradation voltage is adapted to be supplied to the pixel upon the first transistor being turned on for the second period.

6. The data driving circuit according to claim 4, wherein the pixel current is adapted to be supplied from the data line to the voltage control unit upon the second transistor being turned on for the second period.

7. The data driving circuit according to claim 2, wherein the voltage control unit comprises a plurality of voltage controllers, each voltage controller comprising:

a switching device connected between the voltage digital-analog converter and the buffer unit;
a comparator adapted to compare the gradation current with the pixel current;
a capacitor having a first terminal connected to a common node between the switching device and the buffer unit;
a voltage adjuster connected to a second terminal of the capacitor and adapted to be controlled by the comparator to increase and decrease the voltage supplied to the second terminal of the capacitor; and
a controller adapted to control the switching device.

8. The data driving circuit according to claim 7, wherein the controller is adapted to turn on the switching device for the first period, and to turn off the switching device for the second period.

9. The data driving circuit according to claim 7, wherein the comparator is adapted to generate a first control signal upon the gradation current being higher than the pixel current, and is adapted to generate a second control signal upon the gradation current being lower than the pixel current.

10. The data driving circuit according to claim 9, wherein the voltage adjuster is adapted to selectively increase or decrease the voltage supplied to the capacitor on the basis of the first and second control signals to equalize the pixel current with the gradation current.

11. The data driving circuit according to claim 10, wherein the controller is adapted to output a counting signal, gradually increased for the second period, to the voltage adjuster.

12. The data driving circuit according to claim 11, wherein an adjustable level of the voltage adjusted by the voltage adjuster is adapted to correspond to the counting signal.

13. The data driving circuit according to claim 12, wherein the adjustable level of the voltage adjusted by the voltage adjuster is adapted to decrease in proportion as the counting signal increases.

14. The data driving circuit according to claim 13, wherein the adjustable level of the voltage adjusted by the voltage adjuster is adapted to decrease by half whenever the counting signal increases.

15. The data driving circuit according to claim 11, wherein the controller is adapted to receive a reset signal each horizontal period and to initialize the counting signal.

16. The data driving circuit according to claim 15, wherein the reset signal includes either a horizontal synchronous signal or a scan signal supplied to the pixel each horizontal period.

17. The data driving circuit according to claim 1, further comprising:

a shift register adapted to generate sampling signals in sequence; and

a latch adapted to store the data corresponding to the sampling signals, and to supply the stored data to the voltage digital-analog converter and the current digital-analog converter.

18. The data driving circuit according to claim 17, wherein the latch comprises:

a sampling latch adapted to sequentially store the data corresponding to the sampling signal;
a holding latch adapted to store the data stored in the sampling latch and to supply the stored data to the voltage digital-analog converter and the current digital-analog converter.

19. The data driving circuit according to claim 18, further comprising a level shifter adapted to increase a voltage of the data stored in the holding latch and to supply the increased data to the voltage digital-analog converter and the current digital-analog converter.

20. An organic light emitting diode display, comprising:

a plurality of first and second scan lines (S11, S21, S12, S22, S1n, S2n);
a plurality of data lines (D1, D2, Dm, Dj) intersecting the first and second scan lines (S11, S21, S12, S22, S1n, S2n);
a pixel portion (130) including a plurality of pixels (140) connected to the first and second scan lines (S11, S21, S12, S22, S1n, S2n) and the data lines (D1, D2, Dm, Dj);
a scan driver (110) adapted to respectively supply first and second scan signals to the first and second scan lines (S11, S21, S12, S22, S1n, S2n); and
a data driver (120) connected to the data lines (D1, D2, Dm, Dj) and adapted to supply a first gradation voltage as a data signal to the data lines (D1, D2, Dm, Dj);
wherein the data driver (120) comprises at least one data driving circuit (129) according to one of the claims 1-19.

21. The display according to claim 20, wherein each pixel comprises:

a light emitting device;
a driver adapted to generate the pixel current corresponding to either the first or second voltage;
a first transistor connected between the driver and the data line, and adapted to be controlled by a first scan signal supplied via the first scan line; and
a second transistor connected between the data line and a common node between the driver and the light emitting device, and adapted to be controlled by a second scan signal supplied via the second scan line.

22. The display according to claim 21, wherein the first transistor is adapted to be turned on in correspondence with the first scan signal for a first period of one horizontal period, and is adapted to be turned on and off at least one time for a second period of the horizontal period excluding the first period.

23. The display according to claim 22, wherein the second transistor is adapted to be turned off in correspondence with the second scan signal for the first period, and is adapted to be turned on and off alternately with the first transistor for the second period.

24. The display according to claim 21, further comprising a third transistor connected between the driver and the light emitting device, and adapted to be turned off for a predetermined period upon the first scan signal being supplied to the first transistor and adapted to be turned on for the other period in correspondence with an emission control signal supplied via an emission control line.

25. The display according to claim 20, wherein the selection unit is adapted to connect the data line to the buffer unit for the first period, and is adapted to alternately connect the data line between the buffer unit and the voltage control unit for the second period.

26. The display according to claim 25, wherein the first gradation voltage or the second gradation voltage is adapted to be supplied from the buffer unit to the pixel via the data line upon the third transistor being turned on, and the pixel current is adapted to be supplied to the voltage control unit via the data line upon the fourth transistor being turned on.

27. A method of driving an organic light emitting diode display comprising a plurality of scan lines (S11, S21, S12, S22, S1n, S2n), a plurality of data lines (D1, D2, Dm, Dj), and a plurality of pixels (140) at the intersections of the scan lines (S11, S21, S12, S22, S1n, S2n) and the data lines (D1, D2, Dm, Dj), wherein each pixel (140) comprises a driving transistor (M4) and an organic light emitting diode (OLED) connected in series, and a data driving circuit (129) with a voltage digital-analog converter (230), a current digital-analog converter (240), and a voltage control unit (250), the method comprising the steps of:

generating a first gradation voltage corresponding to digital data supplied to the data driving circuit (129) with the voltage digital-analog converter (230),

generating a gradation current corresponding to the digital data with the current digital-analog converter (240);
supplying the first gradation voltage to the gate of the driving transistor (M4) of a pixel (140) via a data line (Dj) in a first time period;
generating a pixel current with the driving transistor (M4) of the pixel (140) corresponding to the first gradation voltage;
supplying the pixel current to the data driving circuit (129) via the data line (Dj) in a second time period different from the first time period; and
comparing the gradation current with the pixel current with the voltage control unit (250), and
generating a second gradation voltage with the voltage control unit (250) by increasing or decreasing a level of the first gradation voltage on the basis of the comparison of the gradation voltage with the pixel current.

28. The method according to claim 27, further comprising supplying the first gradation voltage to the driving transistor (M4) of the pixel (140) for a first period of one horizontal period.

29. The method according to claim 28, further comprising:

generating the second gradation voltage by increasing or decreasing the level of the first gradation voltage on the basis of the compared result to cause the pixel (140) current be equal to the gradation current; and
supplying the second gradation voltage to the pixel via the data line.

30. The method according to claim 29, further comprising repeating supplying the pixel current to the data driver via the data line; and comparing the gradation current with the pixel current with the data driver, and generating a second gradation voltage by increasing or decreasing a level of the first gradation voltage on the basis of the compared result at least one time for a second period of one horizontal period excluding the first period.

31. The method according to claim 30, further comprising:

generating a counting signal, gradually increased for the second period; and
controlling an adjustable level of the first gradation voltage in accordance with the counting signal.

32. The method according to claim 31, further comprising decreasing the adjustable level of the first gradation voltage in proportion as the counting signal increases.

Patentansprüche

1. Datentreiberschaltung (129) für eine OLED (organische lichtemittierende Diode)-Anzeige, wobei die OLED-Anzeige eine Vielzahl von Ansteuerleitungen (S11, S21, S12, S22, S1n, S2n), eine Vielzahl von Datenleitungen (D1, D2, Dm, Dj) und eine Vielzahl von Pixeln (140), welche sich an den Schnittpunkten der Ansteuerleitungen (S11, S21, S12, S22, S1n, S2n) und der Datenleitungen (D1, D2, Dm, Dj) befinden, aufweist, wobei jeder Pixel (140) einen Ansteuertransistor (M4) und eine organische lichtemittierende Diode (OLED), welche in Reihe geschaltet sind, aufweist, und wobei die Datentreiberschaltung (129) aufweist:

einen Spannungs-Digital-Analog-Wandler (230), welcher dazu ausgebildet ist, eine erste Gradationsspannung entsprechend digitalen Daten, welche an der Datentreiberschaltung (129) anliegen, zu erzeugen und in einem ersten Zeitintervall das Gate des Ansteuertransistors (M4) über eine Datenleitung (Dj) mit der ersten Gradationsspannung zu versorgen;
einen Strom-Digital-Analog-Wandler (240), welcher dazu ausgebildet ist, einen Gradationsstrom entsprechend den digitalen Daten, welche an der Datentreiberschaltung (129) anliegen, zu erzeugen;
eine Spannungssteuereinheit (250, 250j), welche dazu ausgebildet ist, in Reaktion auf das Anlegen der ersten Gradationsspannung an das Gate des Ansteuertransistors (M4) während des ersten Zeitintervalls in einem zweiten, vom ersten Zeitintervall abweichenden Zeitintervall über die Datenleitung (Dj) einen Rückkopplungspixelstrom, der durch den Ansteuertransistor (M4) des Pixels fließt, zu erhalten, wobei die Spannungssteuereinheit (250, 250j) weiterhin dazu ausgebildet ist, den Rückkopplungspixelstrom mit dem Gradationsstrom zu vergleichen und auf der Basis des Ergebnisses des Vergleiches des Rückkopplungspixelstroms mit dem Gradationsstrom eine zweite Gradationsspannung zu erzeugen;
eine Puffereinheit (260, 260j), welche dazu ausgebildet ist, die Datenleitung (Dj) wahlweise mit der ersten oder der zweiten Gradationsspannung zu versorgen; und
eine Auswahleinheit (280, 280j), welche dazu ausgebildet ist, die Datenleitung (Dj) wahlweise entweder mit der Puffereinheit (260, 260j) oder mit der Spannungssteuereinheit (250, 250j) zu verbinden.

2. Datentreiberschaltung nach Anspruch 1, wobei die Auswahleinheit (250, 250j) dazu ausgebildet ist, die Datenleitung (Dj) während eines ersten Zeitintervalls einer Horizontalperiode mit der Puffereinheit (260, 260j) zu verbinden und die Datenleitung (Dj) während eines zweiten Zeitintervalls einer Horizontalperiode, von dem das erste Zeitintervall ausgenommen ist, wechselweise entweder mit der Puffereinheit (260, 260j) oder mit der Spannungssteuereinheit (250, 250j) zu verbinden.

3. Datentreiberschaltung nach Anspruch 2, wobei die Auswahleinheit eine Vielzahl von Auswahlvorrichtungen aufweist, wobei jede Auswahlvorrichtung aufweist:

einen ersten Transistor, welcher zwischen der Puffereinheit und der Datenleitung angeschlossen ist; und
einen zweiten Transistor, welcher zwischen der Datenleitung und der Spannungssteuereinheit angeschlossen ist.

4. Datentreiberschaltung nach Anspruch 3, wobei der erste Transistor dazu ausgebildet ist, während des ersten Zeitintervalls eingeschaltet zu sein, und wobei der erste und der zweite Transistor dazu ausgebildet sind, während des zweiten Zeitintervalls wechselweise ein- und ausgeschaltet zu sein.

5. Datentreiberschaltung nach Anspruch 4, wobei die erste Gradationsspannung dazu geeignet ist, den Pixel während des ersten Zeitintervalls zu versorgen, und wobei die zweite Gradationsspannung dazu geeignet ist, den Pixel zu versorgen, während der erste Transistor im zweiten Zeitintervall eingeschaltet ist.

6. Datentreiberschaltung nach Anspruch 4, wobei der Pixelstrom dazu geeignet ist, die Spannungssteuereinheit über die Datenleitung zu versorgen, während der zweite Transistor im zweiten Zeitintervall eingeschaltet ist.

7. Datentreiberschaltung nach Anspruch 2, wobei die Spannungssteuereinheit eine Vielzahl von Spannungssteuervorrichtungen aufweist, wobei jede Spannungssteuervorrichtung aufweist:

eine Schaltvorrichtung, welche zwischen dem Spannungs-Digital-Analog-Wandler und der Puffereinheit angeschlossen ist;
einen Komparator, der dazu ausgebildet ist, den Gradationsstrom mit dem Pixelstrom zu vergleichen;
einen Kondensator, welcher einen ersten Anschluss aufweist, der mit einem zwischen der Schaltvorrichtung und der Puffereinheit befindlichen gemeinsamen Knotenpunkt verbunden ist;
einen Spannungsregler, welcher mit einem zweiten Anschluss des Kondensators verbunden ist und dazu ausgebildet ist, vom Komparator derart gesteuert zu werden, dass er die am zweiten Anschluss des Kondensators anliegende Spannung erhöht und senkt; und
eine Steuervorrichtung, welche dazu ausgebildet ist, die Schaltvorrichtung zu steuern.

8. Datentreiberschaltung nach Anspruch 7, wobei die Steuervorrichtung dazu ausgebildet ist, die Schaltvorrichtung während des ersten Zeitintervalls einzuschalten und während des zweiten Zeitintervalls auszuschalten.

9. Datentreiberschaltung nach Anspruch 7, wobei der Komparator dazu ausgebildet ist, ein erstes Steuersignal zu erzeugen, wenn der Gradationsstrom höher als der Pixelstrom ist, und ein zweites Steuersignal zu erzeugen, wenn der Gradationsstrom niedriger als der Pixelstrom ist.

10. Datentreiberschaltung nach Anspruch 9, wobei der Spannungsregler dazu ausgebildet ist, auf der Basis des ersten und des zweiten Steuersignals die am Kondensator anliegende Spannung wahlweise zu erhöhen oder zu senken, so dass der Pixelstrom und der Gradationsstrom aneinander angeglichen werden.

11. Datentreiberschaltung nach Anspruch 10, wobei die Steuervorrichtung dazu ausgebildet ist, ein während des zweiten Zeitintervalls graduell ansteigendes Zählsignal an den Spannungsregler auszugeben.

12. Datentreiberschaltung nach Anspruch 11, wobei ein regulierbarer Pegel der vom Spannungsregler regulierten Spannung dazu geeignet ist, dem Zählsignal zu entsprechen.

13. Datentreiberschaltung nach Anspruch 12, wobei der regulierbare Pegel der vom Spannungsregler regulierten Spannung dazu geeignet ist, in dem Verhältnis, in dem das Zählsignal sinkt, anzusteigen.

14. Datentreiberschaltung nach Anspruch 13, wobei der regulierbare Pegel der vom Spannungsregler regulierten Spannung dazu geeignet ist, immer wenn das Zählsignal erhöht wird, um die Hälfte zu sinken.

15. Datentreiberschaltung nach Anspruch 11, wobei die Steuervorrichtung dazu ausgebildet ist, in jeder Horizontalperiode ein Rücksetzsignal zu erhalten und das Zählsignal zu initialisieren.

16. Datentreiberschaltung nach Anspruch 15, wobei das Rücksetzsignal entweder ein horizontales Syn-

chronsignal oder ein Ansteuersignal, welches in jeder Horizontalperiode am Pixel anliegt, aufweist.

17. Datentreiberschaltung nach Anspruch 1, weiterhin aufweisend:

ein Schieberegister, welches dazu ausgebildet ist, aufeinander folgende Abtastsignale zu erzeugen; und
einen Speicher, welcher dazu ausgebildet ist, die Abtastsignalen entsprechenden Daten zu speichern und den Spannungs-Digital-Analog-Wandler und den Strom-Digital-Analog-Wandler mit den gespeicherten Daten zu versorgen.

18. Datentreiberschaltung nach Anspruch 17, wobei der Speicher aufweist:

einen Abtastspeicher, welcher dazu ausgebildet ist, die dem Abtastsignal entsprechenden Daten sequentiell zu speichern;
einen Haltespeicher, welcher dazu ausgebildet ist, die im Abtastspeicher gespeicherten Daten zu speichern und den Spannungs-Digital-Analog-Wandler und den Strom-Digital-Analog-Wandler mit den gespeicherten Daten zu versorgen.

19. Datentreiberschaltung nach Anspruch 18, weiterhin einen Pegelschieber aufweisend, wobei der Pegelschieber dazu ausgebildet ist, eine Spannung der im Haltespeicher gespeicherten Daten zu erhöhen und den Spannungs-Digital-Analog-Wandler und den Strom-Digital-Analog-Wandler mit den gespeicherten Daten zu versorgen.

20. OLED (Organische lichtemittierende Diode)-Anzeige, aufweisend:

eine Vielzahl erster und zweiter Ansteuerleitungen (S11,S21,S12, S22, S1n, S2n);
eine Vielzahl von Datenleitungen (D1, D2, Dm, Dj), welche die ersten und zweiten Ansteuerleitungen (S11, S21, S12, S22, S1n, S2n) kreuzen;
einen Pixelbereich (130), welcher eine Vielzahl von Pixeln (140), die mit den ersten und zweiten Ansteuerleitungen (S11, S21, S12, S22, S1n, S2n) und den Datenleitungen (D1, D2, Dm, Dj) verbunden sind, aufweist;
einen Ansteuerungstreiber (110), welcher dazu ausgebildet ist, jeweils erste und zweite Ansteuersignale an die ersten und zweiten Ansteuerleitungen (S11, S21, S12, S22, S1n, S2n) anzulegen; und
einen Datentreiber (120), welcher mit den Datenleitungen (D1, D2, Dm, Dj) verbunden ist und dazu ausgebildet ist, die Datenleitungen (D1, D2, Dm, Dj) mit einer ersten Gradationsspannung als Datensignal zu versorgen;
wobei der Datentreiber (120) zumindest eine Datentreiberschaltung (129) nach einem der Ansprüche 1-19 aufweist.

21. Anzeige nach Anspruch 20, wobei jeder Pixel aufweist:

eine lichtemittierende Vorrichtung;
einen Treiber, welcher dazu ausgebildet ist, den Pixelstrom entsprechend entweder der ersten oder der zweiten Spannung zu erzeugen;
einen ersten Transistor, welcher zwischen dem Treiber und der Datenleitung angeschlossen ist, wobei der erste Transistor dazu ausgebildet ist, durch ein an der ersten Ansteuerleitung anliegendes erstes Ansteuersignal gesteuert zu werden; und
einen zweiten Transistor, welcher zwischen der Datenleitung und einem zwischen dem Treiber und der lichtemittierenden Vorrichtung befindlichen gemeinsamen Knotenpunkt angeschlossen ist, wobei der zweite Transistor dazu ausgebildet ist, durch ein an der zweiten Ansteuerleitung anliegendes zweites Ansteuersignal gesteuert zu werden.

22. Anzeige nach Anspruch 21, wobei der erste Transistor dazu ausgebildet ist, während eines ersten Zeitintervalls einer Horizontalperiode entsprechend dem ersten Ansteuersignal eingeschaltet zu sein und zumindest einmal während des zweiten Zeitintervalls der Horizontalperiode, von dem das erste Zeitintervall ausgenommen ist, ein- und ausgeschaltet zu sein.

23. Anzeige nach Anspruch 22, wobei der zweite Transistor dazu ausgebildet ist, während des ersten Zeitintervalls entsprechend dem zweiten Ansteuersignal eingeschaltet zu sein und während des zweiten Zeitintervalls wechselweise mit dem ersten Transistor ein- und ausgeschaltet zu sein.

24. Anzeige nach Anspruch 21, weiterhin einen dritten Transistor aufweisend, wobei der dritte Transistor zwischen dem Treiber und der lichtemittierenden Vorrichtung angeschlossen ist, und wobei der dritte Transistor dazu ausgebildet ist, während eines vorbestimmten Zeitintervalls, in dem das erste Ansteuersignal am ersten Transistor anliegt, ausgeschaltet zu sein und während des anderen Zeitintervalls entsprechend einem an der Emissionskontrollleitung anliegenden Emissionskontrollsignal eingeschaltet zu sein.

25. Anzeige nach Anspruch 20, wobei die Auswahleinheit dazu ausgebildet ist, während des ersten Zeitintervalls die Datenleitung mit der Puffereinheit zu

verbinden und während des zweiten Zeitintervalls die Datenleitung wechselweise zwischen der Pufferschicht und der Spannungssteuereinheit anzuschließen.

26. Anzeige nach Anspruch 25, wobei die erste Gradationsspannung oder die zweite Gradationsspannung dazu geeignet ist, den Pixel von der Puffereinheit aus über die Datenleitung zu versorgen, während der dritte Transistor eingeschaltet ist, und wobei der Pixelstrom dazu geeignet ist, die Spannungssteuereinheit über die Datenleitung zu versorgen, während der vierte Transistor eingeschaltet ist.

27. Verfahren zur Ansteuerung einer OLED (Organische lichtemittierende Diode)-Anzeige, wobei die OLED-Anzeige aufweist: eine Vielzahl von Ansteuerleitungen (S11, S21, S12, S22, S1n, S2n), eine Vielzahl von Datenleitungen (D1, D2, Dm, Dj) und eine Vielzahl von Pixeln (140), welche sich an den Schnittpunkten der Ansteuerleitungen (S11, S21, S12, S22, S1n, S2n) und der Datenleitungen (D1, D2, Dm, Dj) befinden, wobei jeder Pixel (140) einen Ansteuertransistor (M4) und eine organische lichtemittierende Diode (OLED), welche in Reihe geschaltet sind, sowie eine einen Spannungs-Digital-Analog-Wandler (230), einen Strom-Digital-Analog-Wandler (240) und eine Spannungssteuereinheit (250) aufweisende Datentreiberschaltung (129) aufweist, und wobei das Verfahren die folgenden Schritte aufweist:

Erzeugen einer ersten Gradationsspannung entsprechend digitalen Daten, welche an der Datentreiberschaltung (129) anliegen, mit dem Spannungs-Digital-Analog-Wandler (230),
Erzeugen eines Gradationsstroms entsprechend den digitalen Daten mit dem Strom-Digital-Analog-Wandler;
Versorgen des Gates des Ansteuertransistors (M4) eines Pixels (140) über eine Datenleitung (Dj) mit der ersten Gradationsspannung während eines ersten Zeitintervalls;
Erzeugen eines Pixelstroms mit dem Ansteuertransistor (M4) des Pixels (140) entsprechend der ersten Gradationsspannung;
Versorgen der Datentreiberschaltung (129) über die Datenleitung (Dj) mit dem Pixelstrom während eines zweiten, vom ersten Zeitintervall abweichenden Zeitintervalls; und
Vergleichen des Gradationsstroms mit dem Pixelstrom mittels der Spannungssteuereinheit (250); und
Erzeugen einer zweiten Gradationsspannung mittels der Spannungssteuereinheit (250), indem die erste Gradationsspannung auf der Basis des Vergleichs der Gradationsspannung mit dem Pixelstrom erhöht oder gesenkt wird.

28. Verfahren nach Anspruch 27, weiterhin das Versorgen des Ansteuertransistors (M4) des Pixels (140) mit einer ersten Gradationsspannung während eines ersten Zeitintervalls einer Horizontalperiode aufweisend.

29. Verfahren nach Anspruch 28, weiterhin aufweisend:

Erzeugen der zweiten Gradationsspannung, indem die erste Gradationsspannung auf der Basis des Vergleichsergebnisses erhöht oder gesenkt wird, so dass eine Angleichung des Pixelstroms (140) an den Gradationsstrom erfolgt; und
Versorgen des Pixels über die Datenleitung mit der zweiten Gradationsspannung.

30. Verfahren nach Anspruch 29, weiterhin aufweisend:

Wiederholung des Versorgens des Datentreibers über die Datenleitung mit dem Pixelstrom; und Vergleichen des Gradationsstroms mit dem Pixelstrom mittels des Datentreibers, und Erzeugen einer zweiten Gradationsspannung, indem die erste Gradationsspannung auf dem Basis des Vergleichsergebnisses zumindest einmal während eines zweiten Zeitintervalls einer Horizontalperiode, von dem das erste Zeitintervall ausgenommen ist, erhöht oder gesenkt wird.

31. Verfahren nach Anspruch 30, weiterhin aufweisend:

Erzeugen eines während des zweiten Zeitintervalls graduell ansteigenden Zählsignals; und
Steuern eines regulierbaren Pegels der ersten Gradationsspannung entsprechend dem Zählsignal.

32. Verfahren nach Anspruch 31, weiterhin das Senken des regulierbaren Pegels der ersten Gradationsspannung in dem Verhältnis, in dem das Zählsignal ansteigt, aufweisend.

Revendications

1. Circuit d'attaque de données (129) pour un écran d'affichage à diodes électroluminescentes organiques comprenant une pluralité de lignes de balayage (S11, S21, S12, S22, S1n, S2n), une pluralité de lignes de données (D1, D2, Dm, Dj) et une pluralité de pixels (140) aux intersections entre les lignes de balayage (S11, S21, S12, S22, S1n, S2n) et les lignes de données (D1, D2, Dm, Dj), chaque pixel (140) comprenant un transistor d'attaque (M4) et une diode électroluminescente organique (OLED, pour « *Organic Light-Emitting Diode* ») connectés en sé-

rie, le circuit d'attaque de données (129) comprenant :

un convertisseur numérique-analogique de tension (230) conçu pour produire une première tension de gradation correspondant aux données numériques fournies au circuit d'attaque de données (129) et pour fournir la première tension de gradation à une grille du transistor d'attaque (M4) via une ligne de données (Dj) au cours d'une première période de temps ;
un convertisseur numérique-analogique de courant (240) conçu pour produire un courant de gradation correspondant aux données numériques fournies au circuit d'attaque de données (129) ;
une unité de commande de tension (250, 250j) conçue pour recevoir au cours d'une deuxième période de temps, différente de la première période de temps, via la ligne de données (Dj), un courant de pixel de contre-réaction circulant entre le transistor d'attaque (M4) du pixel (140) en réponse à l'application de la première tension de gradation sur la grille du transistor d'attaque (M4) au cours de la première période, pour comparer le courant de pixel de contre-réaction avec le courant de gradation et pour produire une deuxième tension de gradation basée sur le résultat de la comparaison entre le courant de pixel de contre-réaction et le courant de gradation ;
une unité tampon (260, 260j) conçue pour fournir sélectivement la première ou la deuxième tension de gradation sur la ligne de données (Dj) ; et
une unité de sélection (280, 280j) conçue pour connecter sélectivement la ligne de données (Dj) soit à l'unité tampon (260, 260j), soit à l'unité de commande de tension (250, 250j).

2. Circuit d'attaque de données selon la revendication 1, dans lequel l'unité de sélection (250, 250j) est conçue pour connecter la ligne de données (Dj) à l'unité tampon (260, 260j) pendant une première période d'une période horizontale et est conçue pour connecter alternativement la ligne de données (Dj) soit à l'unité tampon (260, 260j), soit à l'unité de commande de tension (250, 250j) pendant une deuxième période d'une période horizontale qui n'inclut pas la première période.

3. Circuit d'attaque de données selon la revendication 2, dans lequel l'unité de sélection comprend une pluralité de sélecteurs, chaque sélecteur comprenant :

un premier transistor connecté entre l'unité tampon et la ligne de données ; et
un deuxième transistor connecté entre la ligne de données et l'unité de commande de tension.

4. Circuit d'attaque de données selon la revendication 3, dans lequel le premier transistor est conçu pour être passant pendant la première période et les premier et deuxième transistors sont conçus pour être alternativement passants et bloqués pendant la deuxième période.

5. Circuit d'attaque de données selon la revendication 4, dans lequel la première tension de gradation est conçue pour être fournie au pixel pendant la première période et la deuxième tension de gradation est conçue pour être fournie au pixel lorsque le premier transistor devient passant pendant la deuxième période.

6. Circuit d'attaque de données selon la revendication 4, dans lequel le courant de pixel est conçu pour être fourni par la ligne de données à l'unité de commande de tension lorsque le deuxième transistor devient passant pendant la deuxième période.

7. Circuit d'attaque de données selon la revendication 2, dans lequel l'unité de commande de tension comprend une pluralité de contrôleurs de tension, chaque contrôleur de tension comprenant :

un dispositif de commutation connecté entre le convertisseur numérique-analogique de tension et l'unité tampon ;
un comparateur conçu pour comparer le courant de gradation avec le courant de pixel ;
un condensateur ayant une première borne connectée à un noeud commun entre le dispositif de commutation et l'unité tampon ;
un ajusteur de tension connecté à une deuxième borne du condensateur et conçu pour être commandé par le comparateur, afin d'augmenter ou de réduire la tension fournie à la deuxième borne du condensateur ; et
un contrôleur conçu pour commander le dispositif de commutation.

8. Circuit d'attaque de données selon la revendication 7, dans lequel le contrôleur est conçu pour rendre le dispositif de commutation passant pendant la première période et pour rendre le dispositif de commutation bloqué pendant la deuxième période.

9. Circuit d'attaque de données selon la revendication 7, dans lequel le comparateur est conçu pour produire un premier signal de commande lorsque le courant de gradation est supérieur au courant de pixel et est conçu pour produire un deuxième signal de commande lorsque le courant de gradation est inférieur au courant de pixel.

10. Circuit d'attaque de données selon la revendication 9, dans lequel l'ajusteur de tension est conçu pour augmenter ou réduire sélectivement la tension fournie au condensateur sur la base du premier et du deuxième signal de commande, afin de rendre égaux le courant de pixel et le courant de gradation.

11. Circuit d'attaque de données selon la revendication 10, dans lequel le contrôleur est conçu pour produire un signal de comptage, augmenté graduellement pendant la deuxième période, à l'ajusteur de tension.

12. Circuit d'attaque de données selon la revendication 11, dans lequel un niveau ajustable de la tension ajustée par l'ajusteur de tension est conçu pour correspondre au signal de comptage.

13. Circuit d'attaque de données selon la revendication 12, dans lequel le niveau ajustable de la tension ajustée par l'ajusteur de tension est conçu pour diminuer proportionnellement à l'augmentation du signal de comptage.

14. Circuit d'attaque de données selon la revendication 13, dans lequel le niveau ajustable de la tension ajustée par l'ajusteur de tension est conçu pour diminuer de moitié lorsque le signal de comptage augmente.

15. Circuit d'attaque de données selon la revendication 11, dans lequel le contrôleur est conçu pour recevoir un signal de réinitialisation à chaque période horizontale et pour initialiser le signal de comptage.

16. Circuit d'attaque de données selon la revendication 15, dans lequel le signal de réinitialisation comprend soit un signal synchrone horizontal, soit un signal de balayage fourni au pixel à chaque période horizontale.

17. Circuit d'attaque de données selon la revendication 1, comprenant en outre :

un registre à décalage conçu pour produire des signaux d'échantillonnage en séquence ; et
un échantillonneur-bloqueur conçu pour stocker les données correspondant aux signaux d'échantillonnage et pour fournir les données stockées au convertisseur numérique-analogique de tension et au convertisseur numérique-analogique de courant.

18. Circuit d'attaque de données selon la revendication 17, dans lequel l'échantillonneur-bloqueur comprend :

un échantillonneur-bloqueur d'échantillonnage, conçu pour stocker séquentiellement les données correspondant au signal d'échantillonnage ;
un échantillonneur-bloqueur de maintien, conçu pour stocker les données stockées dans l'échantillonneur-bloqueur d'échantillonnage et pour fournir les données stockées au convertisseur numérique-analogique de tension et au convertisseur numérique-analogique de courant.

19. Circuit d'attaque de données selon la revendication 18, comprenant en outre un décaleur de niveau, conçu pour augmenter une tension des données stockées dans l'échantillonneur-bloqueur de maintien et pour fournir les données augmentées au convertisseur numérique-analogique de tension et au convertisseur numérique-analogique de courant.

20. Écran d'affichage à diodes électroluminescentes organiques, comprenant :

une pluralité de premières et de deuxièmes lignes de balayage (S11, S21, S12, S22, S1n, S2n) ;
une pluralité de lignes de données (D1, D2, Dm, Dj) coupant les premières et deuxièmes lignes de balayage (S11, S21, S12, S22, S1n, S2n) ;
une portion de pixels (130) comprenant une pluralité de pixels (140) connectés aux premières et deuxièmes lignes de balayage (S11, S21, S12, S22, S1n, S2n) et aux lignes de données (D1, D2, Dm, Dj) ;
un circuit d'attaque de balayage (110) conçu pour fournir respectivement des premiers et deuxièmes signaux de balayage aux premières et deuxièmes lignes de balayage (S11, S21, S12, S22, S1n, S2n) ; et
un amplificateur d'attaque de données (120) connecté aux lignes de données (D1, D2, Dm, Dj) et conçu pour fournir une première tension de gradation comme signal de données aux lignes de données (D1, D2, Dm, Dj) ;
l'amplificateur d'attaque de données (120) comprenant au moins un circuit d'attaque de données (129) selon l'une des revendications 1 à 19.

21. Écran d'affichage selon la revendication 20, dans lequel chaque pixel comprend :

un dispositif électroluminescent ;
un amplificateur d'attaque conçu pour produire le courant de pixel correspondant soit à une première, soit à une deuxième tension ;
un premier transistor connecté entre l'amplificateur d'attaque et la ligne de données et conçu pour être commandé par un premier signal de balayage fourni sur la première ligne de balayage ; et

un deuxième transistor connecté entre la ligne de données et un noeud commun placé entre l'amplificateur d'attaque et le dispositif électroluminescent et conçu pour être commandé par un deuxième signal de balayage fourni sur la deuxième ligne de balayage.

22. Écran d'affichage selon la revendication 21, dans lequel le premier transistor est conçu pour devenir passant en correspondance avec le premier signal de balayage pendant une première période d'une période horizontale et est conçu pour devenir passant et bloqué au moins une fois pendant une deuxième période de la période horizontale qui n'inclut pas la première période.

23. Écran d'affichage selon la revendication 22, dans lequel le deuxième transistor est conçu pour devenir bloqué en correspondance avec le deuxième signal de balayage pendant la première période et est conçu pour devenir alternativement passant et bloqué avec le premier transistor pendant la deuxième période.

24. Écran d'affichage selon la revendication 21, comprenant en outre un troisième transistor connecté entre l'amplificateur d'attaque et le dispositif électroluminescent et conçu pour devenir bloqué pendant une période prédéterminée lorsque le premier signal de balayage est fourni au premier transistor et conçu pour devenir passant pendant l'autre période en correspondance avec un signal de commande de l'émission fourni sur une ligne de commande de l'émission.

25. Écran d'affichage selon la revendication 20, dans lequel l'unité de sélection est conçue pour connecter la ligne de données à l'unité tampon pendant la première période et est conçue pour connecter alternativement la ligne de données entre l'unité tampon et l'unité de commande de tension pendant la deuxième période.

26. Écran d'affichage selon la revendication 25, dans lequel la première tension de gradation ou la deuxième tension de gradation est conçue pour être fournie par l'unité tampon au pixel via la ligne de données lorsque le troisième transistor devient passant et le courant de pixel est conçu pour être fourni à l'unité de commande de tension via la ligne de données lorsque le quatrième transistor devient passant.

27. Procédé d'attaque d'un écran d'affichage à diodes électroluminescentes organiques comprenant une pluralité de lignes de balayage (S11, S21, S12, S22, S1n, S2n), une pluralité de lignes de données (D1, D2, Dm, Dj) et une pluralité de pixels (140) aux intersections entre les lignes de balayage (511, S21, S12, S22, S1n, S2n) et les lignes de données (D1, D2, Dm, Dj), chaque pixel (140) comprenant un transistor d'attaque (M4) et une diode électroluminescente organique (OLED) connectés en série, ainsi qu'un circuit d'attaque de données (129) avec un convertisseur numérique-analogique de tension (230), un convertisseur numérique-analogique de courant (240) et une unité de commande de tension (250), le procédé comprenant les étapes consistant à :

produire une première tension de gradation correspondant aux données numériques fournies au circuit d'attaque de données (129) à l'aide du convertisseur numérique-analogique de tension (230) ;
produire un courant de gradation correspondant aux données numériques, à l'aide du convertisseur numérique-analogique de courant (240) ;
fournir la première tension de gradation à la grille du transistor d'attaque (M4) d'un pixel (140) via une ligne de données (Dj) sur une première période de temps ;
produire un courant de pixel à l'aide du transistor d'attaque (M4) du pixel (140), correspondant à la première tension de gradation ;
fournir le courant de pixel au circuit d'attaque de données (129), via la ligne de données (Dj) pendant une deuxième période de temps différente de la première période de temps ;
comparer le courant de gradation avec le courant de pixel à l'aide de l'unité de commande de tension (250) ; et
produire une deuxième tension de gradation à l'aide de l'unité de commande de tension (250) en augmentant ou en diminuant un niveau de la première tension de gradation sur la base de la comparaison entre la tension de gradation et le courant de pixel.

28. Procédé selon la revendication 27, comprenant en outre l'étape consistant à fournir la première tension de gradation au transistor d'attaque (M4) du pixel (140) pendant une première période d'une période horizontale.

29. Procédé selon la revendication 28, comprenant en outre les étapes consistant à :

produire la deuxième tension de gradation en augmentant ou en diminuant le niveau de la première tension de gradation en fonction du résultat de la comparaison, afin que le courant de pixel (140) soit égal au courant de gradation ; et
fournir la deuxième tension de gradation au pixel via la ligne de données.

30. Procédé selon la revendication 29, comprenant en

outre les étapes consistant à :

répéter la fourniture du courant de pixel à l'amplificateur d'attaque de données via la ligne de données ;
comparer le courant de gradation avec le courant de pixel à l'aide de l'amplificateur d'attaque de données; et
produire une deuxième tension de gradation en augmentant ou en diminuant un niveau de la première tension de gradation sur la base du résultat de la comparaison au moins une fois pendant une deuxième période d'une période horizontale qui n'inclut pas la première période.

31. Procédé selon la revendication 30, comprenant en outre les étapes consistant à :

produire un signal de comptage, augmenté graduellement, pendant la deuxième période ; et
commander un niveau ajustable de la première tension de gradation en fonction du signal de comptage.

32. Procédé selon la revendication 31, comprenant en outre l'étape consistant à diminuer le niveau ajustable de la première tension de gradation en proportion de l'augmentation du signal de comptage.

FIG. 1

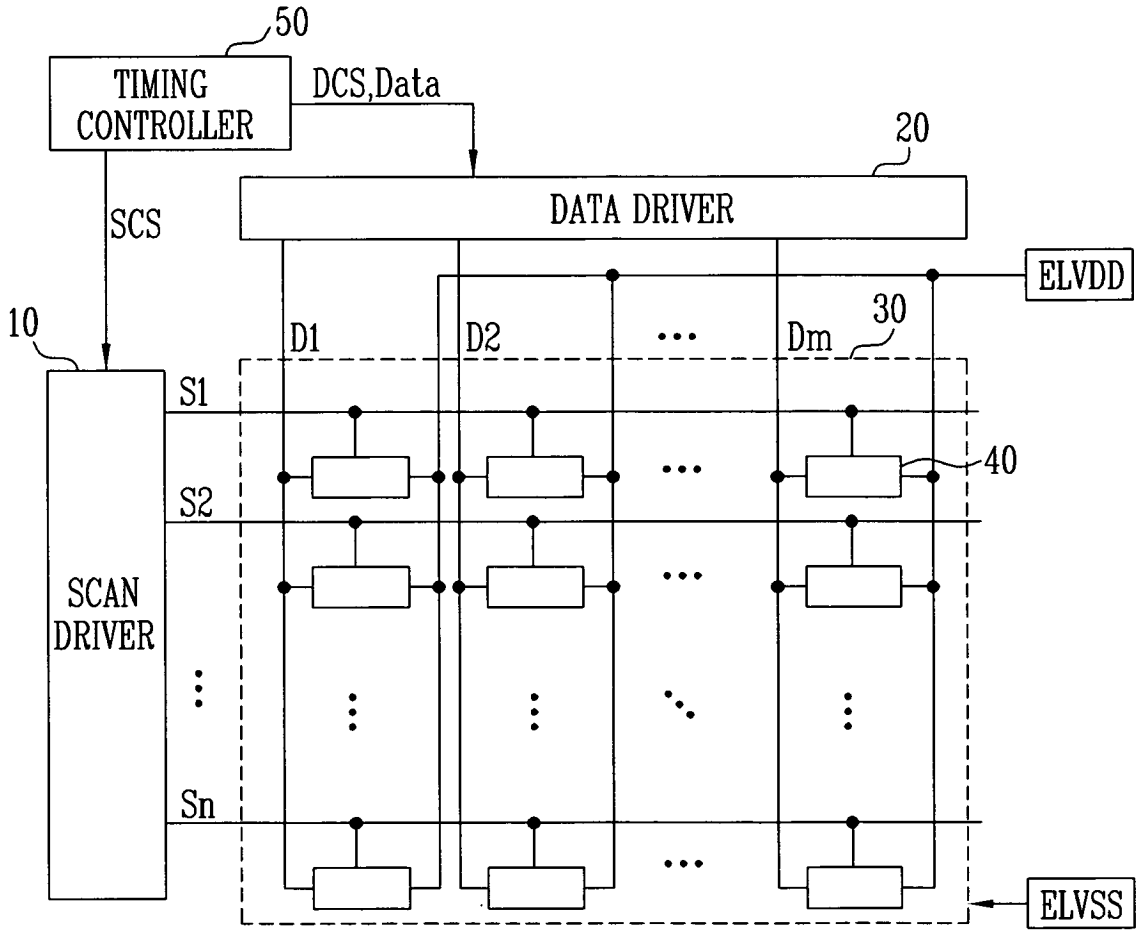

50
TIMING CONTROLLER
DCS,Data
20
DATA DRIVER
SCS
ELVDD
10
D1
D2
Dm
30
S1
S2
40
SCAN DRIVER
Sn
ELVSS

FIG. 2

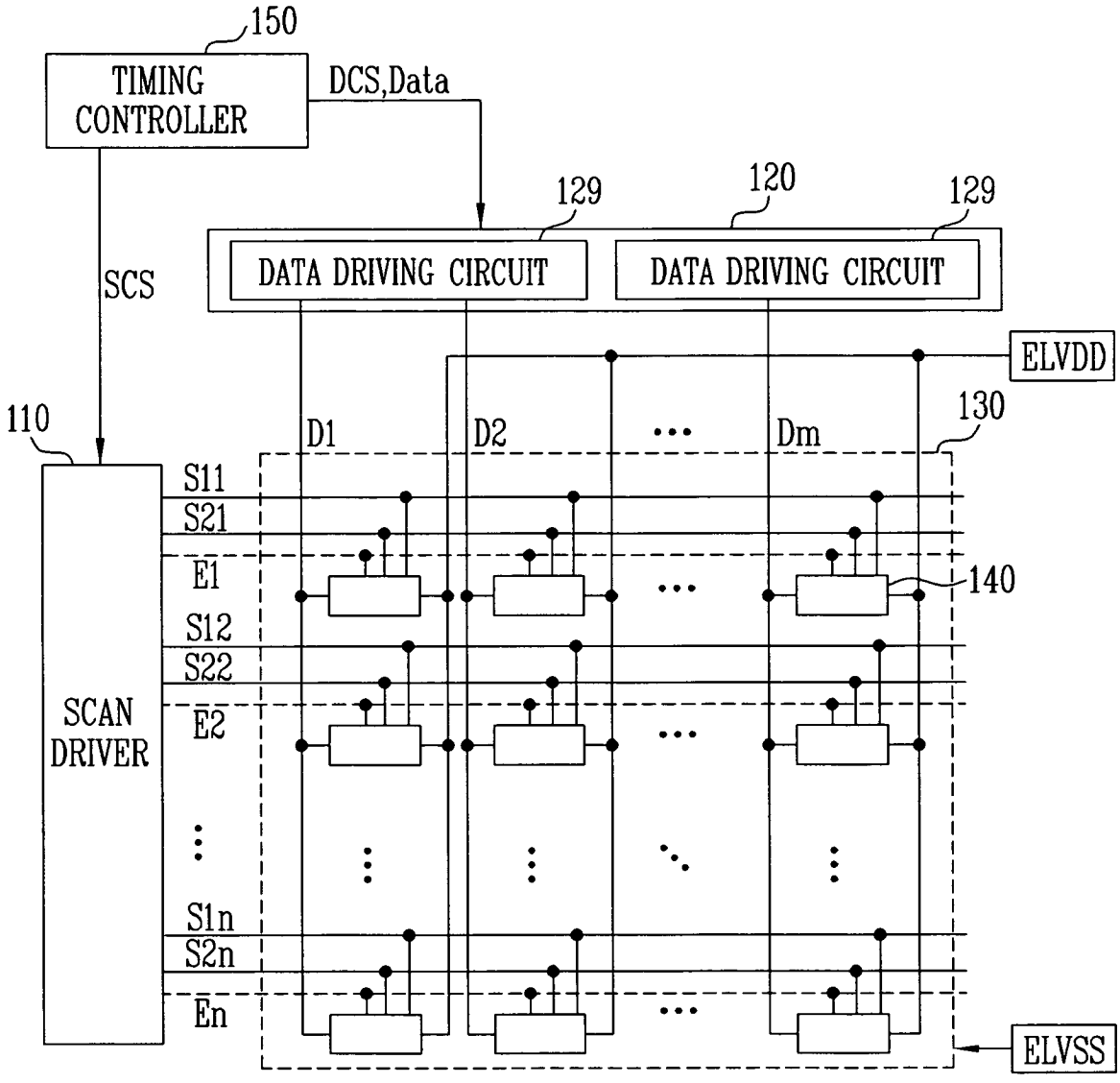

150
TIMING CONTROLLER
DCS,Data
129
120
129
DATA DRIVING CIRCUIT
DATA DRIVING CIRCUIT
SCS
ELVDD
110
D1
D2
Dm
130
S11
S21
E1
140
S12
S22
SCAN DRIVER
E2
S1n
S2n
En
ELVSS

FIG. 3

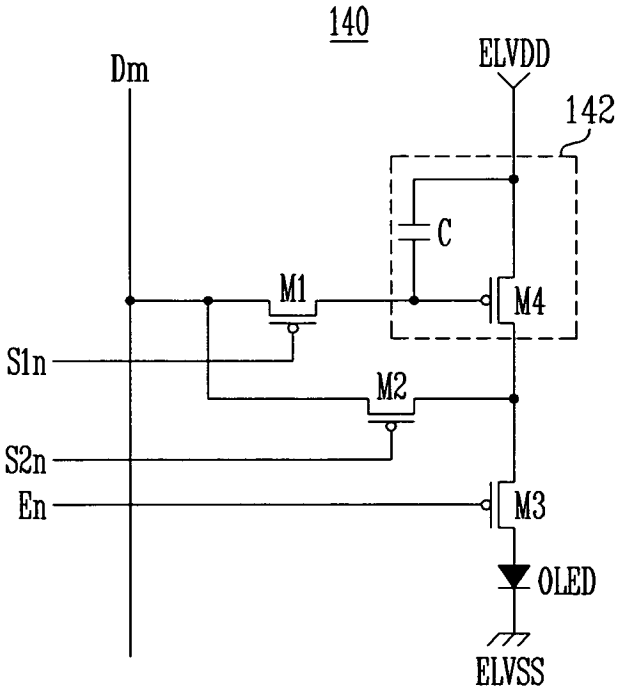

140
Dm
ELVDD
142
C
M1
M4
S1n
M2
S2n
En
M3
OLED
ELVSS

FIG. 4

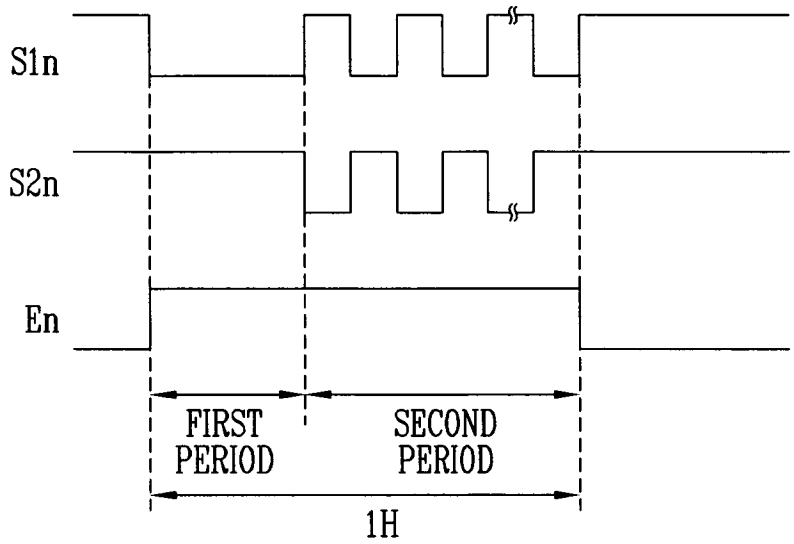

S1n
S2n
En
FIRST PERIOD
SECOND PERIOD
1H

FIG. 5

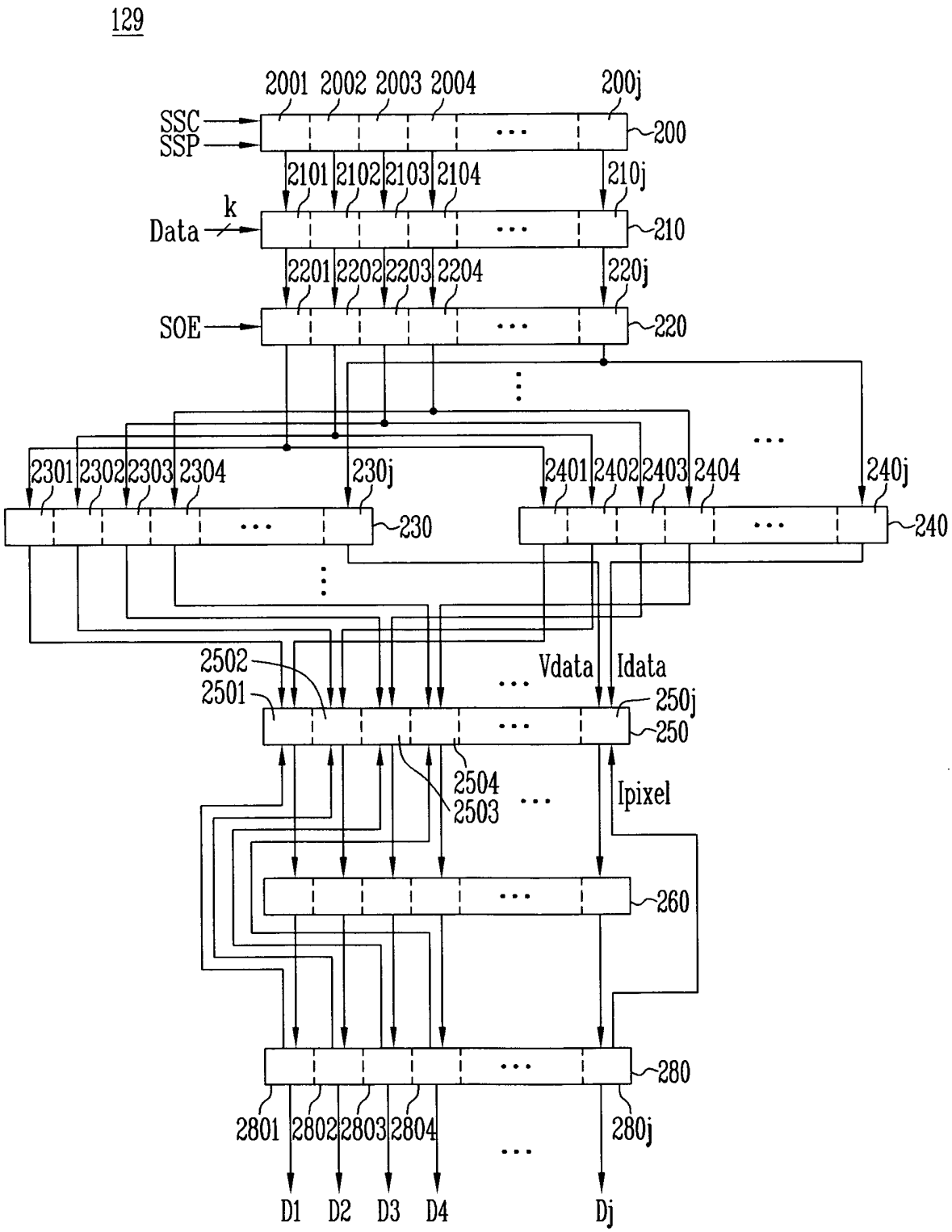

129
2001 2002 2003 2004 200j
SSC
SSP
200
2101 2102 2103 2104 210j
k
Data
210
2201 2202 2203 2204 220j
SOE
220
2301 2302 2303 2304 230j
230
2401 2402 2403 2404 240j
240
2502
2501
Vdata
Idata
250j
250
2504
2503
Ipixel
260
280
2801 2802 2803 2804 280j
D1 D2 D3 D4 Dj

FIG. 6

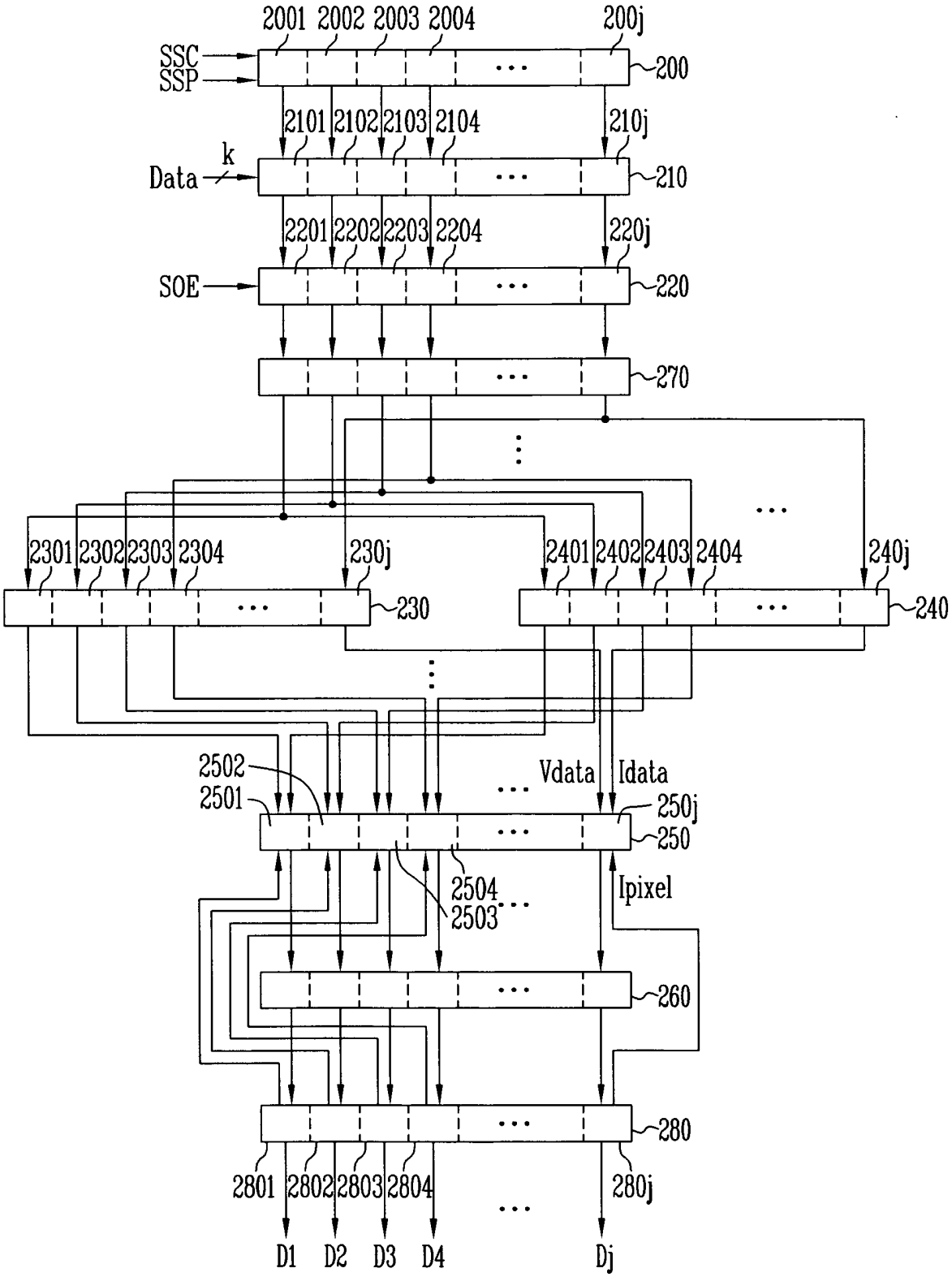

2001 2002 2003 2004
200j
SSC
SSP
200
2101 2102 2103 2104
210j
k
Data
210
2201 2202 2203 2204
220j
SOE
220
270
2301 2302 2303 2304
230j
230
2401 2402 2403 2404
240j
240
2502
2501
Vdata
Idata
250j
250
2504
2503
Ipixel
260
280
2801 2802 2803 2804
280j
D1 D2 D3 D4
Dj

FIG. 7

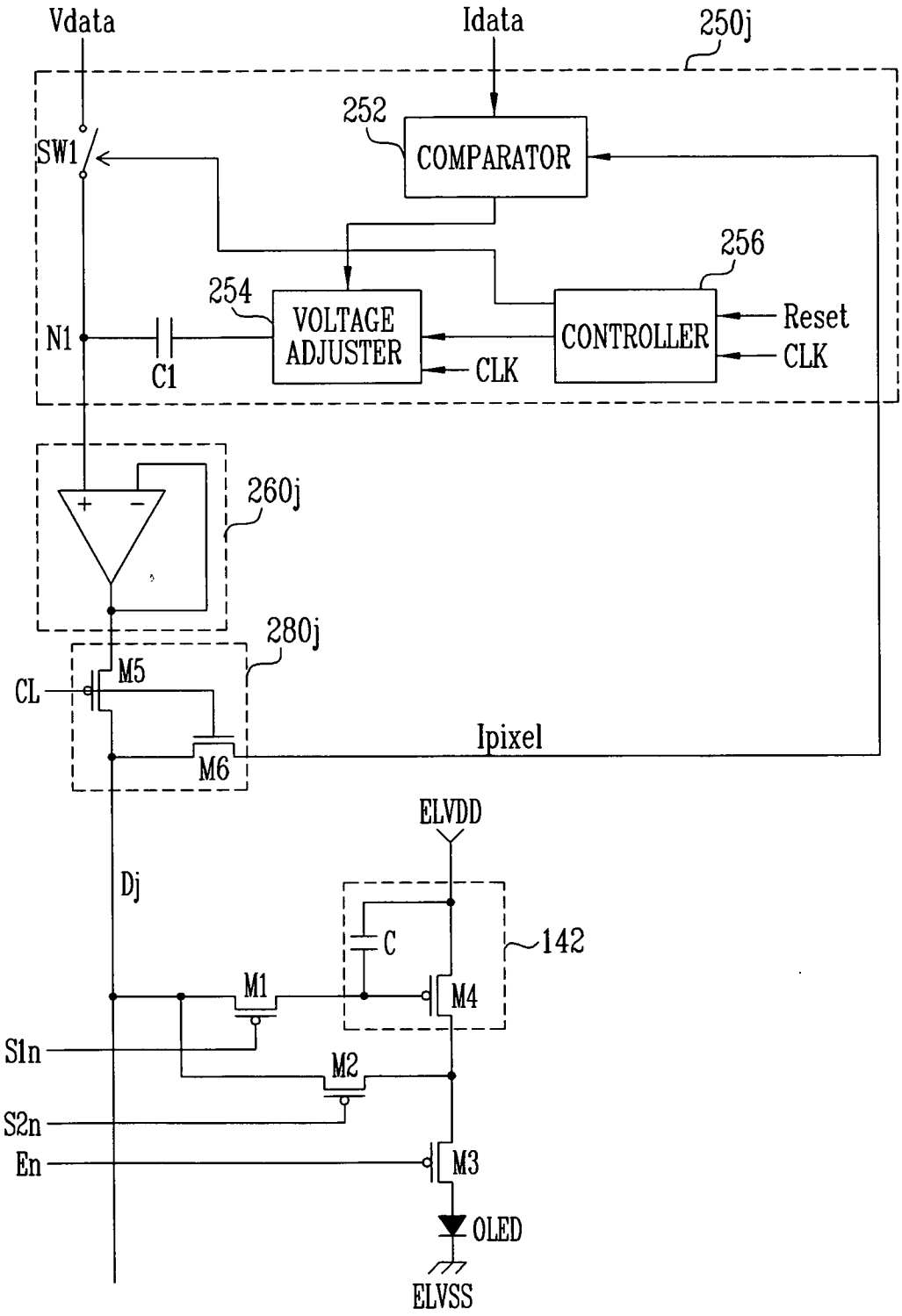

Vdata
Idata
250j
252
COMPARATOR
SW1
256
254
VOLTAGE ADJUSTER
CONTROLLER
Reset
CLK
N1
C1
CLK
260j
280j
CL
M5
M6
Ipixel
ELVDD
Dj
C
142
M1
M4
S1n
M2
S2n
En
M3
OLED
ELVSS

FIG. 8

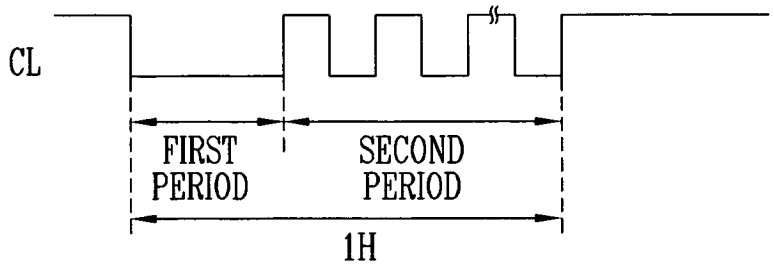

CL
FIRST PERIOD
SECOND PERIOD
1H

FIG. 9

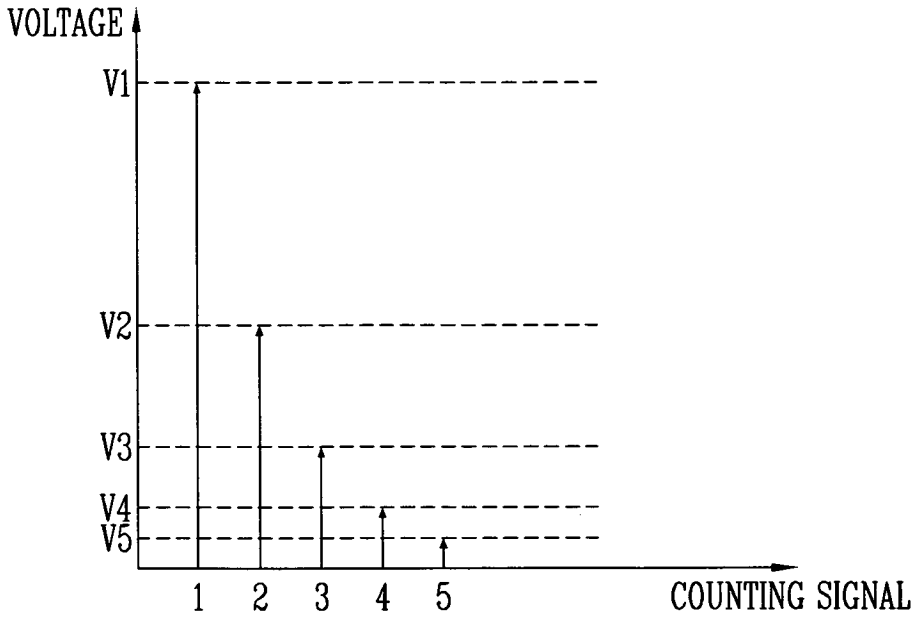
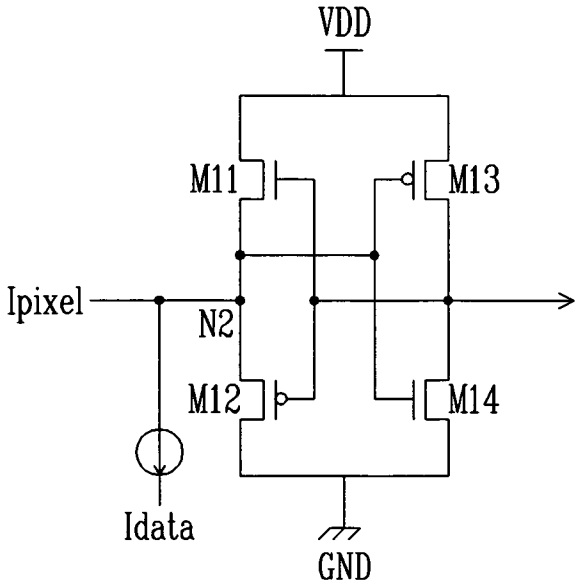

VOLTAGE
V1
V2
V3
V4
V5
1
2
3
4
5
COUNTING SIGNAL

FIG. 10



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- WO 03107313 A **[0010]**
- EP 0378249 A2 **[0011]**
- US 20030016201 A1 **[0012]**

专利名称(译)	数据驱动电路，使用数据驱动电路的有机发光二极管（OLED）显示器，以及驱动OLED显示器的方法		
公开(公告)号	EP1675093B1	公开(公告)日	2008-02-20
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代理机构(译)	hengelhaupt，Jürgen		
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外部链接	Espacenet		

摘要(译)

一种数据驱动电路（129），包括：电压数模转换器（230），适于产生对应于外部数据的第一灰度电压;电流数模转换器（240），适于产生对应于外部数据的灰度电流;电压控制单元（250），适于通过数据线（D1，..... Dj）从像素接收反馈像素电流，并通过根据第一灰度电压的电平增大或减小来产生第二灰度电压。反馈像素电流;缓冲单元（260），适于选择性地将第一或第二灰度电压提供给数据线;选择单元（280），适于将数据线（D1，..... Dj）选择性地连接到缓冲单元（260）或电压控制单元（250）。利用这种配置，以期望的亮度显示图像。

FIG. 1