(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 646 032 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
21.11.2007 Bulletin 2007/47

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **05109164.3**

(22) Date of filing: **04.10.2005**

(54) **Pixel circuit for OLED display with self-compensation of the threshold voltage**

Pixelschaltung für ein OLED Display mit automatischer Kompensation der Schwellenspannung

Circuit de pixel d'un dispositif organique luminescent avec autocompensation de la tension de seuil

(84) Designated Contracting States:
DE FR GB

(30) Priority: **08.10.2004 KR 2004080621**

(43) Date of publication of application:
12.04.2006 Bulletin 2006/15

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EP 1 646 032 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND

1. FIELD OF THE INVENTION

[0001] The present invention relates to a pixel circuit and a light emitting display comprising the same, and more particularly, to a pixel circuit and a light emitting display comprising the same, in which a threshold voltage is compensated, thereby improving the uniformity of brightness.

2. Related Art

[0002] Recently, various flat panel displays have been developed, to substitute cathode ray tube (CRT) displays because the CRT displays are relatively heavy and bulky. Among the flat panel displays, a light emitting display (LED) is notable because it has high emission efficiency, high brightness, wide view angle, and fast response time.

[0003] The light emitting display comprises a plurality of light emitting devices, wherein each light emitting device has a structure in which an emission layer is placed between a cathode electrode and an anode electrode. Here, an electron and a hole are injected into the emission layer and recombined to create an exciton. Light is emitted when the exciton falls to a lower energy level.

[0004] Such a light emitting display is classified into an inorganic light emitting display comprising an inorganic emission layer, and an organic light emitting display comprising an organic emission layer.

[0005] FIG. 1 is a circuit diagram of a pixel provided in a conventional light emitting display. Referring to FIG. 1, the pixel comprises an organic light emitting device OLED, a driving transistor M2, a capacitor Cst, a switching transistor M1. Further, the pixel is connected to a scan line Sn, a data line Dm, a pixel power line Vdd, and a second power supply line Vss. The second power supply line Vss is a voltage lower that the first voltage supply, for example, a ground voltage. Here, the scan line Sn is arranged in a row direction, and the data line Dm and the pixel power line Vdd are arranged in a column direction. For reference, n is an arbitrary integer between 1 and N, and m is an arbitrary integer between 1 and M.

[0006] The switching transistor M1 comprises a source electrode connected to the data line Dm, a drain electrode connected to a first node A, and a gate electrode connected to the scan line Sn.

[0007] The driving transistor M2 comprises a source electrode connected to the pixel power line Vdd, a drain electrode connected to the organic light emitting device OLED, and a gate electrode connected to the first node A. Here, the driving transistor M2 supplies current to the organic light emitting device OLED in response to a signal inputted to its gate electrode, thereby allowing the organic light emitting device to emit light. Further, the intensity of the current flowing in the driving transistor M2 is controlled by a data signal transmitted through the data line Dm and switching transistor M1.

[0008] The capacitor Cst comprises a first electrode connected to the source electrode of the driving transistor M2, and a second electrode connected to the first node A. Here, the capacitor Cst maintains voltage applied between the source and gate electrodes of the driving transistor M2 in response to the data signal, for a predetermined period.

[0009] With this configuration, when the switching transistor M1 is turned on in response to the scan signal transmitted to the gate electrode of the switching transistor M1, the capacitor Cst is charged with a voltage corresponding to the data signal, and then the voltage charged in the capacitor Cst is applied to the gate electrode of the driving transistor M2. Hence, the current flows in the driving transistor M2, thereby allowing the organic light emitting device OLED to emit light.

[0010] At this time, the current supplied from the driving transistor M2 to the organic light emitting device OLED is calculated by the following equation.

$$I_{OLED} = \frac{\beta}{2}(Vgs - Vth)^2 = \frac{\beta}{2}(Vdd - Vdata - Vth)^2 \qquad \text{[Equation 1]}$$

where I_{OLED} is a current flowing in the organic light emitting device OLED; *Vgs* is a voltage applied between the source and gate electrodes of the driving transistor M2; *Vth* is a threshold voltage of the driving transistor M2, *Vdata* is a voltage corresponding to the data signal; and β is a gain factor of the driving transistor M2.

[0011] Referring to the equation 1, the current I_{OLED} flowing in the organic light emitting device OLED varies depending on the threshold voltage of the driving transistor M2.

[0012] However, when the conventional light emitting display is fabricated, deviation arises in the threshold voltage of the driving transistor M2. Thus, the deviation in the threshold voltage of the driving transistor M2 causes in consistencies

in the current flowing in the organic light emitting device OLED to be not uniform, thereby deteriorating the uniformity of the brightness of the display device.

[0013] Further, the pixel power line Vdd connected to each pixel and supplying pixel power is connected to a first power line (not shown) and supplies the pixel power. In this case, voltage drop arises in the first power supplied from the pixel power line Vdd to the first power line. As the length of the first power line increases, the pixel power line Vdd connected thereto increases in number, thereby causing the voltage drop to get larger.

[0014] Several other conventional pixel circuits are disclosed in US 2004/174354 A1, US 2003/227262 A1 and US 6 680 580 B1. US 2003 / 0 227 262 A1 discloses pixel circuits for a current programmed OLED display, wherein the current used for programming is higher than the resulting OLED driving current and the higher programming current accelerates charging of the data lines. US 6 680 580 B1 discloses a pixel circuit for a voltage programmed OLED display with a bypass transistor turning off the light emitting device temporarily using frame or line inversion, thereby reducing deviations in the threshold voltage of the driving transistors. US 2004 / 0 174 354 A1 discloses pixel circuits for a voltage programmed OLED display with threshold voltage compensation. The claims have been characterised with respect to this document. However, these pixel circuits cannot solve the above-mentioned problems.

[0015] Particularly, for a large screen of the flat panel display, the voltage drop in the first power line increases further.

SUMMARY OF THE INVENTION

[0016] Accordingly, it is an aspect of the present invention to provide a pixel circuit and a light emitting display comprising the same, in which current flows in a driving transistor regardless of a threshold voltage of the driving transistor and pixel power. This way, the variations of the threshold voltage is compensated, so that the amount of current flowing in the light emitting device does not vary with voltage drop in first voltage used for the pixel power and the decrease in the pixel power, thereby improving the uniformity of brightness.

[0017] According to the present invention a pixel circuit is disclosed as defined in the appended claims.

[0018] According to another aspect of the present invention a light emitting display is disclosed as defined in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] These and/or other aspects and advantages of the invention will become apparent and more readily appreciated from the following description of some embodiments of the invention, taken in conjunction with the accompanying drawings of which:

[0020] FIG. 1 is a circuit diagram of a pixel provided in a conventional light emitting display;

[0021] FIG. 2 illustrates configuration of a light emitting display according to an embodiment of the present invention;

[0022] FIG. 3 is a circuit diagram of a pixel according to a first embodiment of the present invention;

[0023] FIG. 4 is a circuit diagram of a pixel according to a second embodiment of the present invention;

[0024] FIG. 5 shows timing between signals for driving the pixels shown in FIGs. 3 and 4;

[0025] FIG. 6 is a circuit diagram for compensating for variations in the threshold voltage of the pixels shown in FIGs. 3 and 4;

[0026] FIG. 7 is a circuit diagram formed when a driving voltage is applied to the pixels shown in FIGs. 3 and 4;

[0027] FIG. 8 is a circuit diagram of a pixel comprising NMOS transistors according to an embodiment of the present invention; and

[0028] FIG. 9 shows timing of signals for driving the pixel shown in FIG. 8.

DETAILED DESCRIPTION

[0029] FIG. 2 illustrates a configuration of a light emitting display according to an embodiment of the present invention. Referring to FIG. 2, the light emitting display comprises a pixel portion 100, a data driver 200, and a scan driver 300. The pixel portion 100 comprises a plurality of pixels 110 including N×M organic light emitting devices; N first scan lines S1.1, S1.2, ..., S1.N-1, S1.N arranged in a row direction; N second scan lines S2.1, S2.2, ..., S2.N-1, S2.N arranged in the row direction; N third scan lines S3.1, S3.2, ..., S3.N-1, S3.N arranged in the row direction; M data lines D1, D2, ...DM-1, DM arranged in a column direction; M pixel power lines Vdd to supply pixel power; and M compensation power lines Vinit to supply compensation power. Here, each pixel power line Vdd and each compensation power line Vinit are connected to a first power line 130 and a second power line 120.

[0030] Further, a data signal is transmitted from any of the data lines D1, D2, ...DM-1, DM to a pixel 110 in response to a first scan signal and a second scan signal transmitted through any of the first scan lines S1.1, S1.2, ..., S1.N-1, S1.N, and any of the second scan lines S2.1, S2.2, ..., S2.N-1, S2.N to generate a driving current corresponding to the data signal. Also, the driving current is supplied to a corresponding organic light emitting device OLED in response to

a third scan signal transmitted through one of the third scan lines S3.1, S3.2, ..., S3.N-1, S3.N, thereby displaying an image.

[0031] The data driver 200 is connected to the data lines D1, D2, ...DM-1, DM and supplies the data signal to the pixels 110. The scan driver 300 is provided on a side of the pixel portion 100, and connected to the first scan lines S1.1, S1.2, ..., S1.N-1, S1.N, the second scan lines S2.1, S2.2, ..., S2.N-1, S2.N, and the third scan lines S3.1, S3.2, ..., S3.N-1, S3.N. The scan driver 300 supplies the first, second and third scan signals to the pixel portion 100, and selects the rows of the pixel portion 100 in sequence. Then, the data driver 200 supplies the data signal to the selected row, thereby allowing a pixel 110 to emit light based on the data signal.

[0032] FIG. 3 is a circuit diagram of a pixel according to a first embodiment of the present invention. As shown in FIG. 3, the pixel comprises an emission part 111, a storage part 112, a driving device 113, a first switching part 114, a second switching part 115, and a third switching part 116.

[0033] The driving device 113 comprises source, gate and drain electrodes, and determines the intensity of current inputted to the emission part 111 on the basis of voltage stored in the storage part 112, thereby controlling the brightness of the emission part 111.

[0034] The first switching part 114 receives the data signal and selectively transmits it to the storage part 112. The second switching part 115 selectively transmits either the voltage stored in the storage part 112 or the compensation voltage applied through the compensation power line Vinit to a gate electrode of the driving device 113, based on scan signals S1.n and S2.n.

[0035] The storage part 112 stores a predetermined voltage and supplies the stored voltage to the gate electrode of the driving device 113. Further, the storage part 112 stores voltage obtained by subtracting the voltage applied to a source electrode of the driving device 113 from the voltage corresponding to the data signal received through the first switching part 114. Here, the voltage applied to the source electrode of the driving device 113 is higher than the compensation voltage by the absolute value of the threshold voltage of the driving device 113.

[0036] The third switching part 116 prevents the first power Vdd from being applied to the driving device 113 while the pixel power is selectively applied to the pixel through the pixel power line D_m and stored in the storage part 112. Further, the third switching part 116 supplies the first power Vdd to the driving device 113 when the pixel power is completely stored in the storage part 112.

[0037] In other words, the pixel 110 comprises the organic light emitting device OLED and its peripheral circuits including a first switching transistor M1, a second switching transistor M2, a third switching transistor M3, a driving transistor M4, a fourth switching device M5, and a capacitor Cst. Each of the first through third switching transistors M1, M2, M3, the driving transistor M4, and the switching device M5 comprises a gate electrode, a source electrode, and a drain electrode. Further, the capacitor Cst comprises a first electrode and a second electrode.

[0038] The gate electrode of the first switching transistor M1 is connected to the first scan line S1.n, the source electrode is connected to the data line Dm, and the drain electrode is connected to a first node A. Here, the first switching transistor M1 supplies the data signal to the first node A, in response to the first scan signal inputted through the first scan line S 1.n.

[0039] The gate electrode of the second switching transistor M2 is connected to the first scan line S1.n, the source electrode is connected to the compensation power line Vinit, and the drain electrode is connected to a second node B. Here, the second switching transistor M2 supplies the compensation power from the compensation power line Vinit to the second node B, in response to the first scan signal inputted through the first scan line S1.n. Further, the compensation power inputted through the compensation power line Vinit is maintained as a high signal.

[0040] The capacitor Cst is connected between the first node A and a third node C, and charged with the voltage difference between the voltage applied to the first node A and the voltage applied to the third node C, thereby supplying the charged voltage to the gate electrode of the driving transistor M4 for a period corresponding to one frame.

[0041] The gate electrode of the third switching transistor M3 is connected to the second scan line S2.n, the source electrode is connected to the first node A, and the drain electrode is connected to the second node B. Here, the third switching transistor M3 supplies the voltage charged in the capacitor Cst to the gate electrode of the driving transistor M4 in response to the second scan signal inputted through the second scan signal S2.n.

[0042] The gate electrode of the driving transistor M4 is connected to the second node B, the source electrode is connected to the third node C, and the drain electrode is connected to the anode electrode of the organic light emitting device OLED. Here, the driving transistor M4 controls the current corresponding to the voltage applied to its own gate electrode to flow via its own source and drain electrodes, thereby supplying the current to the organic light emitting device OLED.

[0043] The gate electrode of the fourth switching device M5 is connected to the third scan line S3.n, the source electrode is connected to the pixel power line Vdd to supply the pixel power, and the drain electrode is connected to the third node C. Here, the fourth switching device M5 is switched in response to the third scan signal inputted through the third scan line S3.n, and thus selectively supplies the pixel power to the organic light emitting device OLED, thereby controlling the current flowing in the organic light emitting device OLED.

[0044] FIG. 4 is a circuit diagram of a pixel according to a second embodiment of the present invention. Referring to FIG. 4, the pixel comprises an additional fifth switching transistor M6 connected in parallel to the organic light emitting device OLED, relative to the pixel circuit of the first embodiment.

[0045] The fifth switching transistor M6 comprises a gate electrode connected to a third scan line, a source electrode connected to a cathode electrode of the organic light emitting device OLED, and a drain electrode connected to an anode electrode of the organic light emitting device OLED. Further, the fifth switching transistor M6 has a reverse polarity relative to the fourth switching transistor M5. For example, when the fourth switching device M5 is of a p-type transistor as shown in FIG. 4, the fifth switching transistor M6 is of an n-type transistor. In this case, the fifth switching transistor M6 is turned off while the fourth switching device M5 is turned on. On the other hand, the fifth switching transistor M6 is turned on while the fourth switching device M5 is turned off.

[0046] Therefore, in a case that the organic light emitting device OLED emits light, the fifth switching transistor M6 is turned off, so that the current flows only in the organic light emitting device OLED. On the other hand, in a case that the organic light emitting device OLED does not emit light (particularly, while the threshold voltage is detected), the fifth switching transistor M6 is turned on, so that the current flows in the fifth switching transistor M6 and not in the organic light emitting device OLED, thereby preventing the organic light emitting device OLED from emitting light.

[0047] FIG. 5 shows timing of the signals for driving the pixels shown in FIGs. 3 and 4; FIG. 6 is a circuit diagram formed when threshold voltage is compensated in the pixels shown in FIGs. 3 and 4; and FIG. 7 is a circuit diagram formed when the driving voltage is applied to the pixels shown in FIGs. 3 and 4. Referring to FIGs. 5 through 7, operation of the pixel is divided according to a first operation period T1 and a second operation period T2. In the first operation period T1, the first scan signal s1.n is low, and the second scan signal s2.n and the third scan signal s3.n are high. In the second operation period T2, the first scan signal s1.n is high, and the second scan signal s2.n and the third scan signal s3.n are low.

[0048] In the first operation period T1, the first and second switching transistors M 1 and M2 are turned on by the first scan signal s1.n, and the third and fourth switching transistors M3 and M5 are turned off by the second scan signal s2.n and the third scan signal s3.n. Hence, the circuit is connected as shown in FIG. 6.

[0049] Referring to FIG. 6, the data signal is transmitted to the first node A through the first switching transistor M1, and the compensation power is supplied to the gate electrode of the driving transistor M4 through the second switching transistor M2. At this time, the first scan signal s1.n is changed from a high state to a low state after the second scan signal s2.n is changed from a low state to a high state, so that the first and second switching transistors M1 and M2 are turned on after the third switching transistor M3 is turned off. Therefore, the data signal is not distorted by other voltage and is correctly stored in the capacitor, thereby applying a uniform voltage to the gate of the driving transistor M4.

[0050] Because the applied compensation power is a high signal, the driving transistor M4 is maintained in the off state, and thus the voltage applied to the source electrode of the driving transistor M4 is higher than the voltage applied to the gate electrode thereof by the threshold voltage. Therefore, the voltage based on the following equation 2 is applied between the source and gate electrodes of the driving transistor M4 by the capacitor Cst.

$$Vcst = Vdata - (Vinit - Vth) \qquad [Equation\ 2];$$

; where *Vcst* is a voltage charged in the capacitor; *Vdata* is a voltage corresponding to the data signal; *Vinit* is the compensation voltage and *Vth* is the threshold voltage of the driving transistor M4.

[0051] In order to correctly operate the driving transistor M4, the pixel power voltage should be larger than or equal to the sum of the compensation voltage and the absolute value of the threshold voltage of the driving transistor M4.

[0052] In the second operation period T2, the first scan signal s1.n is maintained in the high state, and the second scan signal s2.n and the third scan signal s3.n are maintained in the low state. The second operation period T2 is maintained for a period corresponding to one frame. During this time, the first and second switching transistors M1 and M2 are turned off by the first scan signal s1.n, and the third and fourth switching transistors M3 and M5 are turned on by the second scan signal s2.n and the third scan signal s3.n. Hence, the circuit is connected as shown in FIG. 7.

[0053] Referring to FIG. 7, the voltage charged in the capacitor Cst is applied to the gate electrode of the driving transistor M4, so that the current corresponding to the voltage charged in the capacitor Cst flows in the organic light emitting device OLED through the driving transistor M4. At this time, the second scan signal s2.n is changed from a high state to a low state after the first scan signal s1.n is changed from a low state to a high state, so that the third switching transistor M3 applies only the voltage charged in the capacitor Cst to the gate electrode of the driving transistor M4, thereby applying a uniform voltage to the gate electrode of the driving transistor M4.

[0054] Therefore, a current based on the following equation 3 flows from the driving transistor M4 to the organic light emitting device OLED.

$$I_{OLED} = \frac{\beta}{2}(Vgs - Vth)^2 = \frac{\beta}{2}(Vdata - Vinit)^2 \qquad \text{[Equation 3]},$$

, where I_{OLED} is a current flowing in the organic light emitting device OLED; *Vgs* is a voltage applied between the source and gate electrodes of the driving transistor M4; *Vdata* is a voltage corresponding to the data signal; *Vinit* is a compensation voltage; and β is a gain factor of the driving transistor M4.

[0055] Therefore, as shown in the equation 3, the current flowing in the organic light emitting device OLED corresponds only to the data signal voltage and the compensation voltage, regardless of the threshold voltage of the driving transistor M4 and the pixel power.

[0056] At this time, the pixel power allows the current to flow in the light emitting device, so that a voltage drop occurs in the pixel power as the current flows. Due to the connection of the capacitor Cst to the gate and source electrodes of the driving transistor M4 the gate-source voltage Vgs of M4 and hence the OLED drive current are independent from a voltage drop in pixel power.

[0057] Thus, in the pixels shown in FIGs. 3 and 4, the deviation between the threshold voltages of the driving transistors M4 is compensated, and the voltage drop in the pixel power is compensated, so that the pixels are suitable for realizing a large sized light emitting display.

[0058] FIG. 8 is a circuit diagram of a pixel comprising NMOS transistors according to an embodiment of the present invention. Referring to FIG. 8, the pixel comprises an organic light emitting device OLED and its peripheral circuits including a first switching transistor M1, a second switching transistor M2, a third switching transistor M3, a driving transistor M4, a fourth switching device M5, and a capacitor Cst. Each of the first through third switching transistors M1, M2, M3, the driving transistors M4, and the switching device M5 is realized by an NMOS transistor comprising a gate electrode, a source electrode, and a drain electrode. Further, the capacitor Cst comprises a first electrode and a second electrode.

[0059] The organic light emitting device OLED is connected to the driving transistor M4, and the fourth switching device M5 is connected between the driving transistor M4 and a cathode electrode.

[0060] FIG. 9 shows timing between signals for driving the pixel shown in FIG. 8. Referring to FIG. 9, operation of the pixel is divided according to a first operation period T1 and a second operation period T2. In the first operation period T1, the first scan signal s1.n is high, and the second scan signal s2.n and the third scan signal s3.n are low. In the second operation period T2, the first scan signal s1.n is low, and the second scan signal s2.n and the third scan signal s3.n are high.

[0061] In the first operation period T1, the first and second switching transistors M1 and M2 are turned on by the first scan signal s1.n, and the third and fourth switching transistors M3 and M5 are turned off by the second scan signal s2.n and the third scan signal s3.n. Hence, the compensation voltage is supplied from the compensation power line Vinit to the gate electrode of the driving transistor M3, and the capacitor Cst is charged with a voltage based on the equation 2. During this time, the compensation power supplied through the compensation power line Vinit is kept low.

[0062] In the second operation period T2, the first scan signal s1.n is kept low, and the second scan signal s2.n and the third scan signal s3.n are kept high. The second operation period T2 is maintained for a period corresponding to one frame. During this time, the first and second switching transistors M1 and M2 are kept turned off by the first scan signal s1.n, and the third and fourth switching transistors M3 and M5 are kept turned on by the second scan signal s2.n and the third scan signal s3.n. The voltage stored in the capacitor Cst is applied to the organic light emitting device OLED, so that the driving current based on the equation 3 flows therein.

[0063] In the foregoing embodiment, the fourth switching device M5 for controlling the current to flow in the organic light emitting device OLED may be an NMOS transistor when other transistors provided in the pixel are PMOS transistors. Alternately, the fourth switching device M5 may be a PMOS transistor when other transistors provided in the pixel are NMOS transistors.

[0064] As described above, the present invention provides a pixel circuit and a light emitting display, in which current flows in a driving transistor regardless of threshold voltage of the driving transistor and pixel power. Thus, the difference between the threshold voltages is compensated, so that the intensity of current flowing in the light emitting device does not vary due to voltage drop in first power used for the pixel power and a decrease in the pixel power voltage, thereby improving the uniformity of brightness of the light emitting device.

[0065] Although a few embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes might be made in this embodiment without departing from the principles of the invention, the scope of which is defined in the claims.

Claims

1. A pixel circuit comprising:

a light emitting device (OLED) comprising a first and a second terminal, wherein the second terminal of the light emitting device (OLED) is connected to a second supply voltage (Vss);
a driving transistor (M4) comprising a source electrode connected to a third node (C), a drain electrode connected to the first terminal of the light emitting device (OLED), and a gate electrode connected to a second node (B), wherein the driving transistor (M4) is arranged to receive a first supply voltage (Vdd) and to supply a current to the light emitting device (OLED) corresponding to a voltage applied to a gate electrode thereof;
a first switching device (M1) comprising a first switching transistor comprising a source electrode connected to a data line (Dm), a drain electrode connected to a first node (A), and a gate electrode connected to a first scan line (S1.n), wherein the first switching device is arranged to transmit a data signal (Dm) selectively depending on a first scan signal (S1.n);
a second switching device (M2) comprising a second switching transistor comprising a source electrode connected to a compensation voltage line (Vinit) and a drain electrode connected to the second node (B);
a capacitor (Cst) comprising a first terminal connected to the first node (A);
a third switching device (M3) comprising a third switching transistor comprising a source electrode connected to the first node (A), a drain electrode connected to the second node (B), and a gate electrode connected to a second scan line (S2.n), wherein the third switching device (M3) is arranged to transmit a voltage corresponding to the voltage stored in the capacitor (Cst) to the gate electrode of the driving transistor (M4) selectively depending on a second scan signal (S2.n);
the pixel circuit **characterised in that**
the capacitor (Cst) furthermore comprises a second terminal connected to the third node (C), wherein the capacitor (Cst) is arranged to store a voltage corresponding to the data signal (Dm) and the compensation voltage (Vinit) according to operations of the first (M1) and second (M2) switching devices;
the second switching transistor furthermore comprises a gate electrode connected to the first scan line (S1.n), wherein the second switching device is arranged to transmit a compensation voltage (Vinit) to the gate electrode of the driving transistor (M4) selectively depending on the first scan signal (S1.n);
the pixel circuit furthermore comprises a fourth switching device (M5) comprising a fourth switching transistor comprising a source electrode connected to the first supply voltage (Vdd), a drain electrode connected to the third node (C), and a gate electrode connected to a third scan line (S3.n), wherein the fourth transistor is arranged to transmit the first supply voltage (Vdd) to the driving transistor (M4) selectively depending on a third scan signal (S3.n).

2. The pixel circuit according to claim 1, further comprising a fifth switching device (M6) controlled by the third scan signal (S3.n) to interrupt the current from flowing in the light emitting device (OLED), wherein the fifth switching device (M6) comprises a fifth switching transistor comprising a source electrode connected to the second supply voltage (Vss), a drain electrode connected to a connecting line between the drain electrode of the driving transistor (M4) and the first terminal of the light emitting device (OLED), and a gate electrode connected to the third scan line (S3.n).

3. The pixel circuit according to claim 1 or 2, wherein the voltage stored in the capacitor (Cst) is equal to a voltage obtained by subtracting a difference between the compensation voltage (Vinit) and a threshold voltage of the driving transistor (M4) from the voltage corresponding to the data signal (Dm).

4. The pixel circuit according to claim 1 or 2, wherein the first (S 1.n), second (S2.n) and third (S3.n) scan signals are periodic signals with a common period that is split into a first (T1) and second (T2) sub-period, wherein
the first scan signal (S1.n) is in on and off states for the first and second sub-periods, respectively;
the second scan signal (S2.n) is in off and on states for the first and second sub-periods, respectively; and
the third scan signal (S3.n) is in off and on states for the first and second sub-periods, respectively.

5. The pixel circuit according to claim 1 or 2, wherein the compensation voltage (Vinit) maintains the driving transistor (M4) in an off state.

6. The pixel circuit according to claim 1 or 2, wherein an absolute value of the difference between the first supply voltage (Vdd) and the compensation voltage (Vinit) is larger than or equal to an absolute value of a threshold voltage of the driving transistor (M4).

7. The pixel circuit according to claim 2, wherein the fourth switching device (M5) and the fifth switching device (M6) are driven by the third scan signal (S3.n) to be in different states.

8. A light emitting display comprising:

a data driver (200), and a scan driver (300), a plurality of first scan lines (S1.1 - S1.N); a plurality of second scan lines (S2.1 - S2.N), a plurality of third scan lines (S3.1 - S3.N), a plurality of data lines (D1-D_M); wherein the light emitting display furthermore comprises a plurality of pixel circuits (110) according to claim 1.

Patentansprüche

1. Eine Pixelschaltung, umfassend:

ein lichtemittierendes Bauelement (OLED), umfassend einen ersten und zweiten Anschluss, wobei der zweite Anschluss des lichtemittierenden Bauelements (OLED) an eine zweite Versorgungsspannung (Vss) angeschlossen ist;
einen Ansteuertransistor (M4), umfassend eine mit einem dritten Knoten (C) verbundene Source-Elektrode, eine mit dem ersten Anschluss des lichtemittierenden Bauelements (OLED) verbundene Drain-Elektrode sowie eine mit einem zweiten Knoten (B) verbundene Gate-Elektrode, wobei der Ansteuertransistor (M4) so ausgelegt ist, dass er eine erste Versorgungsspannung (Vdd) erhält und dem lichtemittierenden Bauelement (OLED) einen Strom liefert, der einer an eine Gate-Elektrode des Ansteuertransistors (M4) angelegten Spannung entspricht;
eine erste Schaltvorrichtung (M1), umfassend einen ersten Schalttransistor, umfassend eine mit einer Datenleitung (Dm) verbundene Source-Elektrode, eine mit einem ersten Knoten (A) verbundene Drain-Elektrode sowie eine mit einer ersten Abtastleitung (S1.n) verbundene Gate-Elektrode, wobei die erste Schaltvorrichtung so ausgelegt ist, dass sie selektiv in Abhängigkeit eines ersten Abtastsignals (S1.n) ein Datensignal (Dm) überträgt;
eine zweite Schaltvorrichtung (M2), umfassend einen zweiten Schalttransistor, umfassend eine mit einer Kompensationsspannungsleitung (Vinit) verbundene Source-Elektrode sowie eine mit dem zweiten Knoten (B) verbundene Drain-Elektrode;
einen Kondensator (Cst), umfassend einen mit dem ersten Knoten (A) verbundenen ersten Anschluss;
eine dritte Schaltvorrichtung (M3), umfassend einen dritten Schalttransistor, umfassend eine mit dem ersten Knoten (A) verbundene Source-Elektrode, eine mit dem zweiten Knoten (B) verbundene Drain-Elektrode sowie eine mit einer zweiten Abtastleitung (S2.n) verbundene Gate-Elektrode, wobei die dritte Schaltvorrichtung so ausgelegt ist, dass sie selektiv an die Gate-Elektrode des Ansteuertransistors (M4) eine der in dem Kondensator (Cst) gespeicherten Spannung entsprechende Spannung in Abhängigkeit eines zweiten Abtastsignals (S2.n) überträgt;
wobei die Pixelschaltung **dadurch gekennzeichnet ist, dass**
der Kondensator (Cst) ferner einen mit dem dritten Knoten (C) verbundenen zweiten Anschluss umfasst, wobei der Kondensator (Cst) so ausgelegt ist, dass er eine dem Datensignal (Dm) und der Kompensationsspannung (Vinit) entsprechende Spannung entsprechend den Operationen der ersten (M1) und zweiten (M2) Schaltvorrichtungen speichert;
der zweite Schalttransistor ferner eine mit der ersten Abtastleitung (S1.n) verbundene Gate-Elektrode umfasst, wobei die zweite Schaltvorrichtung so ausgelegt ist, dass sie selektiv in Abhängigkeit des ersten Abtastsignals (S1.n) an die Gate-Elektrode des Ansteuertransistors (M4) eine Kompensationsspannung (Vinit) überträgt;
die Pixelschaltung ferner eine vierte Schaltvorrichtung (M5) umfasst, umfassend einen vierten Schalttransistor, umfassend eine an die erste Versorgungsspannung (Vdd) angeschlossene Source-Elektrode, eine mit dem dritten Knoten (C) verbundene Drain-Elektrode sowie eine mit einer dritten Abtastleitung (S3.n) verbundene Gate-Elektrode, wobei der vierte Transistor so ausgelegt ist, dass er selektiv in Abhängigkeit eines dritten Abtastsignals (S3.n) an den Ansteuertransistor (M4) die erste Versorgungsspannung (Vdd) überträgt.

2. Die Pixelschaltung nach Anspruch 1, ferner umfassend eine fünfte Schaltvorrichtung (M6), die von dem dritten Abtastsignal (S3.n) gesteuert wird, um den Stromfluss in das lichtemittierende Bauelement (OLED) zu unterbrechen, wobei die fünfte Schaltvorrichtung (M6) einen fünften Schalttransistor umfasst, der eine an die zweite Versorgungsspannung (Vss) angeschlossene Source-Elektrode, eine mit einer Verbindungsleitung zwischen der Drain-Elektrode des Ansteuertransistors (M4) und dem ersten Anschluss des lichtemittierenden Bauelements (OLED) verbundene Drain-Elektrode sowie eine mit der dritten Abtastleitung (S3.n) verbundene Gate-Elektrode umfasst.

3. Die Pixelschaltung nach Anspruch 1 oder 2, wobei die in dem Kondensator (Cst) gespeicherte Spannung einer durch Subtrahieren einer Differenz zwischen der Kompensationsspannung (Vinit) und einer Schwellenspannung des Ansteuertransistors (M4) von der dem Datensignal (Dm) entsprechenden Spannung gewonnenen Spannung gleich ist.

4. Die Pixelschaltung nach Anspruch 1 oder 2, wobei die ersten (S1.n), zweiten (S2.n) und dritten (S3.n) Abtastsignale periodische Signale mit einer gemeinsamen Periode, die in eine erste (T1) und zweite (T2) Unterperiode unterteilt ist, sind, wobei
das erste Abtastsignal (S1.n) sich für die ersten und zweiten Unterperioden in An- beziehungsweise Aus-Zuständen befindet;
das zweite Abtastsignal (S2.n) sich für die ersten und zweiten Unterperioden in Aus- beziehungsweise An-Zuständen befindet; und
das dritte Abtastsignal (S3.n) sich für die ersten und zweiten Unterperioden in Aus- beziehungsweise An-Zuständen befindet.

5. Die Pixelschaltung nach Anspruch 1 oder 2, wobei die Kompensationsspannung (Vinit) den Ansteuertransistor (M4) in einem Aus-Zustand hält.

6. Die Pixelschaltung nach Anspruch 1 oder 2, wobei ein Absolutbetrag der Differenz zwischen der ersten Versorgungsspannung (Vdd) und der Kompensationsspannung (Vinit) größer oder gleich einem Absolutbetrag einer Schwellenspannung des Ansteuertransistors (M4) ist.

7. Die Pixelschaltung nach Anspruch 2, wobei die vierte Schaltvorrichtung (M5) und die fünfte Schaltvorrichtung (M6) von dem dritten Abtastsignal (S3.n) so angesteuert werden, dass sie sich in verschiedenen Zuständen befinden.

8. Eine lichtemittierende Anzeige, umfassend:

einen Datentreiber (200) und einen Abtasttreiber (300), eine Vielzahl von ersten Abtastleitungen (S1.1 - S1.N); eine Vielzahl von zweiten Abtastleitungen (S2.1 - S2.N), eine Vielzahl von dritten Abtastleitungen (S3.1 - S3.N), eine Vielzahl von Datenleitungen (D1-D_M), wobei die lichtemittierende Anzeige ferner eine Vielzahl von Pixelschaltungen (110) nach Anspruch 1 umfasst.

Revendications

1. Circuit de pixel comportant :

un dispositif émetteur de lumière (OLED) comportant des première et seconde bornes, dans lequel la seconde borne du dispositif émetteur de lumière (OLED) est connectée à une seconde tension d'alimentation (Vss) ;
un transistor d'attaque (M4) comportant une électrode de source connectée à un troisième noeud (C), une électrode de drain connectée à la première borne du dispositif émetteur de lumière (OLED) et une électrode de grille connectée à un deuxième noeud (B), le transistor d'attaque (M4) étant agencé de façon à recevoir une première tension d'alimentation (Vdd) et à fournir au dispositif émetteur de lumière (OLED) un courant correspondant à une tension appliquée à une électrode de grille de ce dispositif ;
un premier dispositif de commutation (M1) comportant un premier transistor de commutation comprenant une électrode de source connectée à une ligne de données (Dm), une électrode drain connectée à un premier noeud (A) et une électrode de grille connectée à une première ligne de balayage (S1.n), le premier dispositif de commutation étant agencé de façon à transmettre un signal de données (Dm) dépendant sélectivement d'un premier signal de balayage (S1.n) ;
un deuxième dispositif de commutation (M2) comportant un second transistor de commutation comprenant une électrode de source connectée à une ligne de tension de compensation (Vinit) et une électrode drain connectée au deuxième noeud (B) ;
un condensateur (Cst) comportant une première borne connectée au premier noeud (A) ;
un troisième dispositif de commutation (M3) comprenant un troisième transistor de commutation comportant une électrode de source connectée au premier noeud (A), une électrode de drain connectée au deuxième noeud (B) et une électrode de grille connectée à une deuxième ligne de balayage (S2.n), le troisième dispositif de commutation (M3) étant agencé de façon à transmettre une tension, correspondant à la tension stockée dans le condensateur (Cst), à l'électrode de grille du transistor d'attaque (M4) dépendant sélectivement d'un

second signal de balayage (S2.n) ;
le circuit de pixel étant **caractérisé en ce que** :

le condensateur (Cst) comporte en outre une seconde borne connectée au troisième noeud (C), le condensateur (Cst) étant agencé de façon à stocker une tension correspondant au signal de données (Dm) et à la tension de compensation (Vinit) conformément à des opérations effectuées par les premier (M1) et second (M2) dispositifs de commutation ;
le deuxième transistor de commutation comporte en outre une électrode de grille connectée à la première ligne de balayage (S1.n), le deuxième dispositif de commutation étant agencé de façon à transmettre une tension de compensation (Vinit) à l'électrode de grille du transistor d'attaque (M4) dépendant sélectivement du premier signal de balayage (S1.n) ;
le circuit de pixel comporte en outre un quatrième dispositif de commutation (M5) comprenant un quatrième transistor de commutation comportant une électrode de source connectée à la première tension d'alimentation (Vdd), une électrode de drain connectée au troisième noeud (C) et une électrode de grille connectée à une troisième ligne de balayage (S3.n), le quatrième transistor étant agencé de façon à transmettre la première tension d'alimentation (Vdd) au transistor d'attaque (M4) dépendant sélectivement d'un troisième signal de balayage (S3.n).

2. Circuit de pixel selon la revendication 1, comportant en outre un cinquième dispositif de commutation (M6) commandé par le troisième signal de balayage (S3.n) pour interrompre la circulation du courant dans le dispositif émetteur de lumière (OLED), dans lequel le cinquième dispositif de commutation (M6) comprend un cinquième transistor de commutation comportant une électrode de source connectée à la seconde tension d'alimentation (Vss), une électrode de drain connectée à une ligne de connexion entre l'électrode de drain du transistor d'attaque (M4) et la première borne du dispositif émetteur de lumière (OLED), et une électrode de grille connectée à la troisième ligne de balayage (S3.n).

3. Circuit de pixel selon la revendication 1 ou 2, dans lequel la tension stockée dans le condensateur (Cst) est égale à une tension de différence obtenue en soustrayant la tension de compensation (Vinit) et une tension de seuil du transistor d'attaque (M4) de la tension correspondant au signal de données (Dm).

4. Circuit de pixel selon la revendication 1 ou 2, dans lequel les premier (S1.n), deuxième (S2.n) et troisième (S3.n) signaux de balayage sont des signaux périodiques avec une période commune qui est divisée en première (T1) et seconde (T2) sous-périodes, dans lequel :

le premier signal de balayage (S1.n) est dans des états activé et désactivé pendant les première et seconde sous-périodes, respectivement ;
le deuxième signal de balayage (S2.n) est dans des états désactivé et activé pendant les première et seconde sous-périodes, respectivement ; et
le troisième signal de balayage (S3.n) est dans des états désactivé et activé pendant les première et seconde sous-périodes, respectivement.

5. Circuit de pixel selon la revendication 1 ou 2, dans lequel la tension de compensation (Vinit) maintient le transistor d'attaque (M4) dans un état désactivé.

6. Circuit de pixel selon la revendication 1 ou 2, dans lequel la valeur absolue de la différence entre la première tension d'alimentation (Vdd) et la tension de compensation (Vinit) est supérieure ou égale à la valeur absolue d'une tension de seuil du transistor d'attaque (M4).

7. Circuit de pixel selon la revendication 2, dans lequel le quatrième dispositif de commutation (M5) et le cinquième dispositif de commutation (M6) sont attaqués par le troisième signal de balayage (S3.n) de façon à être dans des états différents.

8. Appareil d'affichage émettant de la lumière, comportant :

un circuit d'attaque (200) de données, et un circuit d'attaque (300) de balayage, une pluralité de premières lignes de balayage (S1.1-S1.N) ; une pluralité de deuxièmes lignes de balayage (S2.1-S2.N), une pluralité de troisièmes lignes de balayage (S3.1-S3.N), une pluralité de lignes de données (D1-D_M) ; dans lequel l'appareil d'affichage émettant de la lumière comporte en outre une pluralité de circuits de pixels (110) selon la revendication 1.

FIG. 1
(PRIOR ART)

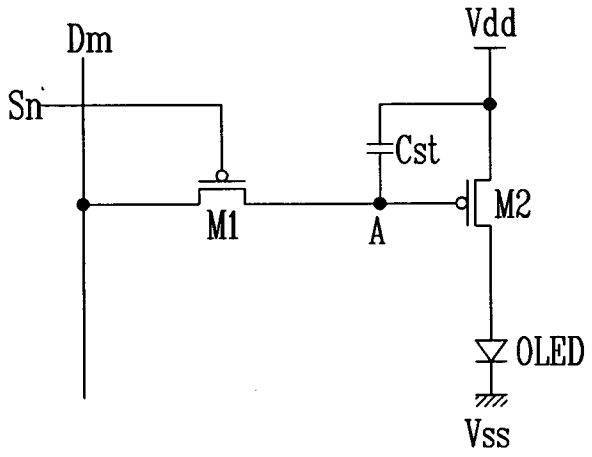


FIG. 2

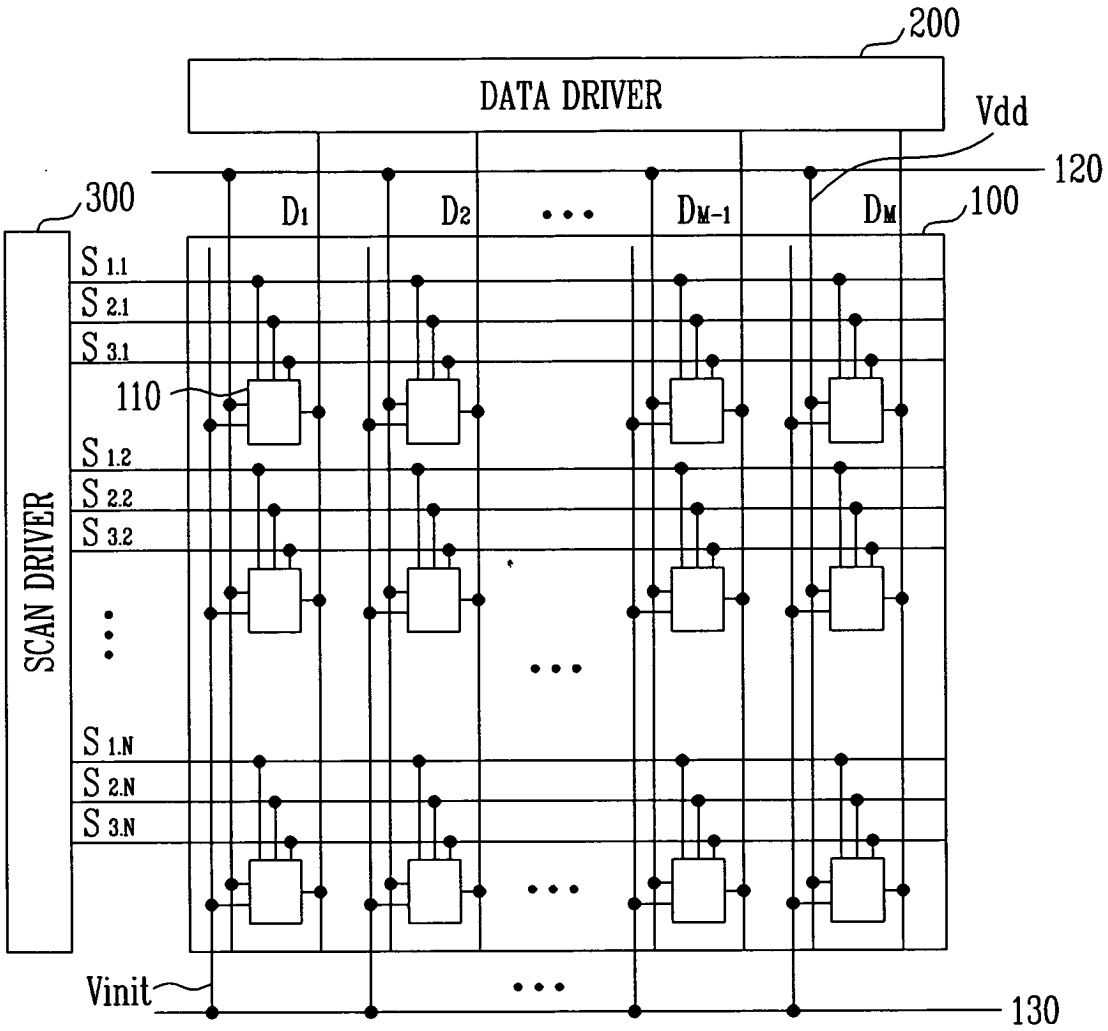

200
DATA DRIVER
Vdd
120
300
D1
D2
DM-1
DM
100
S 1.1
S 2.1
S 3.1
110
S 1.2
S 2.2
S 3.2
SCAN DRIVER
S 1.N
S 2.N
S 3.N
Vinit
130

FIG. 3

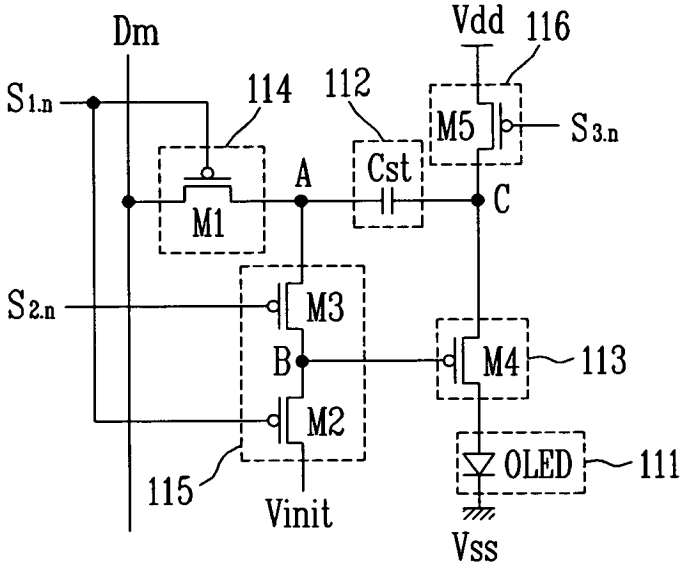

Dm
Vdd
116
S1.n
114
112
M5
S3.n
A
Cst
M1
C
S2.n
M3
B
M4
113
M2
OLED
111
115
Vinit
Vss

FIG. 4

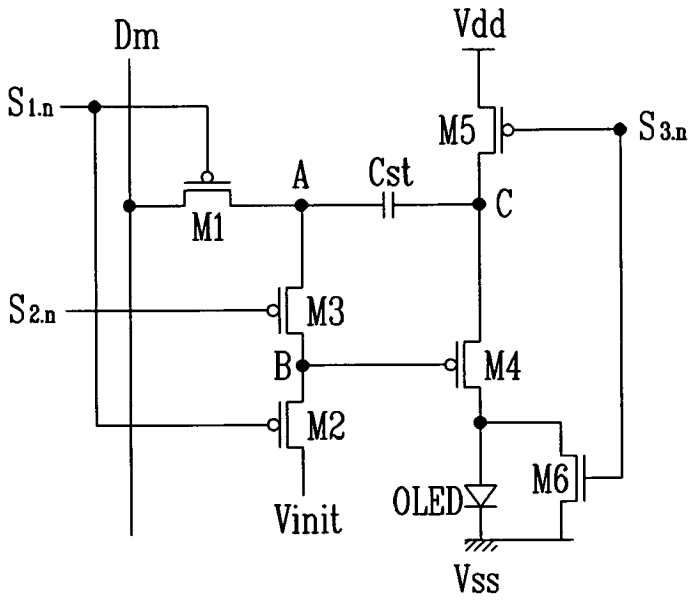


FIG. 5

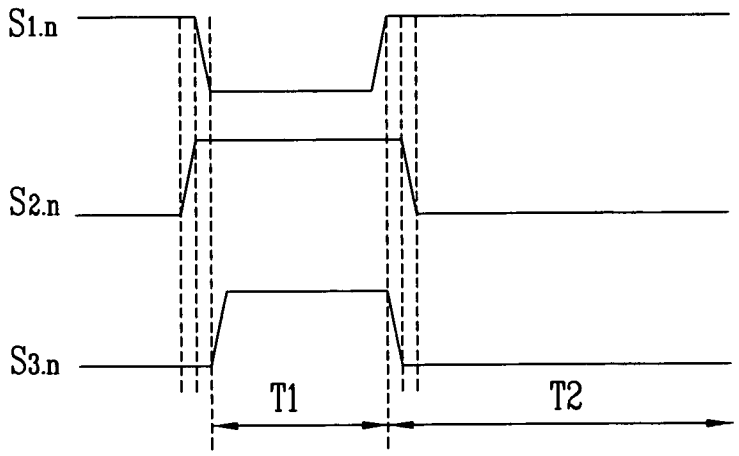


FIG. 6

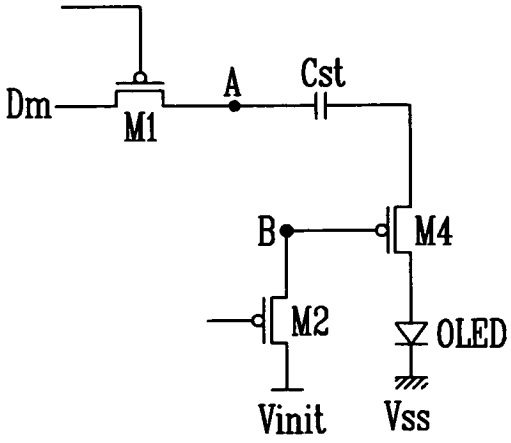


FIG. 7

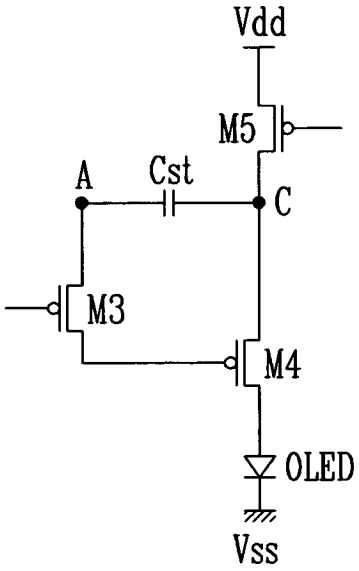


FIG. 8

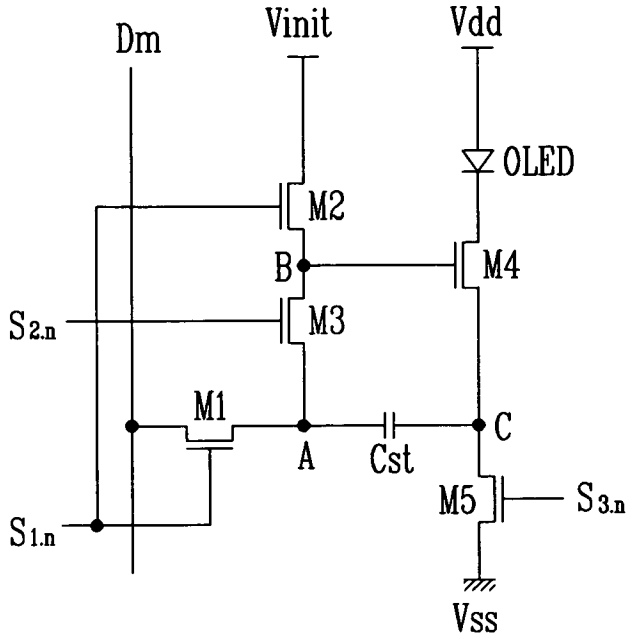
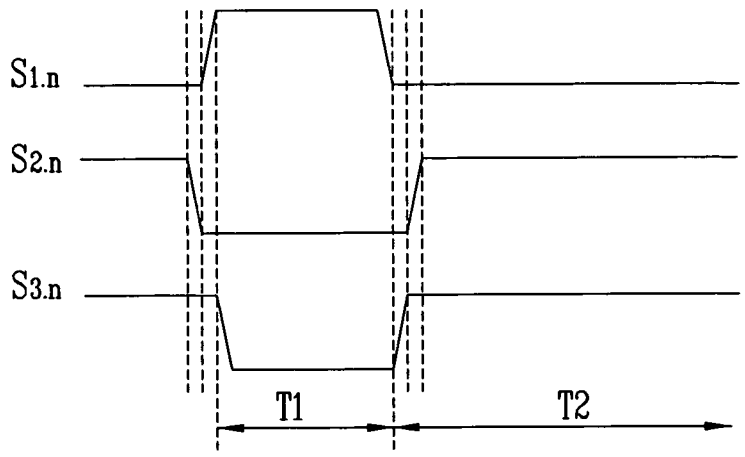


FIG. 9



REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	用于OLED显示器的像素电路具有阈值电压的自补偿		
公开(公告)号	EP1646032B1	公开(公告)日	2007-11-21
申请号	EP2005109164	申请日	2005-10-04
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申请(专利权)人(译)	三星SDI CO.，LTD.		
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IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2310/0251 G09G2320/043		
代理机构(译)	hengelhaupt，Jürgen		
优先权	1020040080621 2004-10-08 KR		
其他公开文献	EP1646032A1		
外部链接	Espacenet		

摘要(译)

像素电路包括发光器件（OLED）;驱动晶体管（M4），用于接收第一电源（Vdd），并将与施加到其栅电极的电压对应的电流提供给发光器件（OLED）;第一开关装置（M1），用于响应第一扫描信号（S1.n）提供数据信号（Dm）;第二开关器件（M2），响应于第一扫描信号（S1.n），向驱动晶体管（M4）的栅极提供第二功率（Vinit）;电容器（Cst），用于根据第一（M1）和第二（M2）开关器件的操作存储对应于数据信号（Dm）和第二电源（Vdd）的电压;第三开关器件（M3），用于响应于第二扫描信号（S2.n）将存储在电容器（Cst）中的电压施加到驱动晶体管（M4）的栅极;第四开关器件（M5）响应于第三扫描信号（S3.n）将第一电源（Vdd）传输到驱动晶体管（M4）。可选的第五开关装置（M6）响应于第三扫描信号（S3.n）绕过发光器件（OLED）。像素电路提供独立于电源线上的电压降和驱动晶体管的阈值电压的驱动电流，从而改善显示器的亮度均匀性。