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(12)

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(22) 2001 10 17

(71) 136 - 1

(72) 117 1403  
96 207 403  
408 806  
105 1003

(74)  
:

(54)

TFT - LCD

(jumper)

가

, EMI

4

1 XGA TFT - LCD

2

3

4 1

5 2

\*

\*

100, 110, 120 : 200, 210, 220 :

300, 310, 320 :

(masking)  
(jumper)

(test pattern)

가

1 XGA TFT - LCD (1),  
(2), DC/DC (3), (Gray scale) (VCOM) (4),  
(5), (6), (7) TFT - LCD (8) (DE, NCLK, Hsync, Vsync )

(2) (1) (RGB) (DE, NCLK,  
Hsync, Vsync ) (5) (6) .  
DC/DC (3) (VDD) (VG+, VG - )  
(5) VCOM (4) DC/DC (3) (VBS)  
(6) (VCOM) .  
(5) (2) (VCOM) (4)  
TFT - LCD (8)

(6) TFT - LCD (2) (VCOM) (4)

(8) (User Connector) (1) 가

XGA TFT - LCD (2)

8) 가 (5)(6) (7) (

(OFF)

(engineer)가 (tuning)

(jumper) 가 EMI

2

TFT - LCD (12) (Asic) IC

(DATA), (DE), (CLK)

IC가

(12) 2 (OE0 & OE1) 4가

ct test) EMI 4가 1 (black dot defe

(black dot defect test) EMI (write data output mode)

(normal operating mode) (don't care) (black data output mode)

[ 1 ]

|      |      |              |     |
|------|------|--------------|-----|
| OE 0 | OE 1 |              |     |
| 0    | 0    |              |     |
| 0    | 1    |              | EMI |
| 1    | 0    |              | EMI |
| 1    | 1    | (don't care) |     |

3  
 , (100), (200) (300)  
 (100) (jumper), (Asic) , (High)  
 (Low)

(200) (100)  
 (300) (200) (DATAin)  
 , (don't care) (DATAout)

4 1  
 (110), (210) (310)

(OE1) (R1) , (Nd1) (110) (Vcc) (OE0) (Nd1)  
 (R4) (Nd2) (R3) , (Nd2) (Vss) (Vcc)

Nd2) (210) (Nd1) (G1) , (G1) ( (Nd1) (OE1) 2 AND (G2) , (Nd2) (OE1) (G4) , (G4) 2 AND (G5) .  
 (310) AND (G2) (DATAout) (Nd3)  
 (Vcc) (G3) , AND (G5) (Nd3)  
 (Vss) (G6)

(110) (R1 - R4) 1 47† (00, 01, 10, 11)  
 (DATAout) 37†

5 2  
 (120), (220) (320)

(OE1) (R1) , (Nd1) (120) (Vcc) (OE0) (Nd1)  
 (R4) , (Nd2) (R3) , (Nd2) (Vss) (Vcc)  
 3) (Vss) (OE2) (Nd3) (R5) , (Nd

(220) (OE0)(OE1)(OE2) 3 AND (G1) , (OE0)  
 (G2) , (G2) (OE1)(OE2) 3 AND (G3)  
 (OE1) (G4) , (OE0)(OE2) (G4)  
 3 AND (G3) , (OE2) (G6) , (OE0)(OE1)  
 (G6) 3 AND (G7) , (OE2) (G8) ,  
 (OE0) (G9) , (OE1) (G8)(G9) 3  
 AND (10) .

(320) AND (G1) (A) (Nd4)  
 (D1) , AND (G1) (A) (Nd5) (D2) ,  
 AND (G1) (A) (Nd6) (D3) , AND (G3) (G  
 2) (B) (Nd8) (D4) , AND (G7) (D)  
 (B) (Nd7) (D5) , AND (G7) (D)  
 (Nd7) (D6) , (Nd8) (Nd7)  
 (D7) , (Nd8) (Nd9) (D8) , (Nd4)  
 (RDATAout) (Nd10) (Vcc) (G11) ,  
 (Nd5) (GDATAout) (Nd11) (Vcc)  
 (G12) , (Nd6) (BDATAout) (Nd12)  
 (Vcc) (G13) , (Nd7) (RDATAout)  
 (Nd10) (Vss) (G14) , (Nd7)  
 (GDATAout) (Nd11) (Vss) (Nd12)  
 (G15) , (Nd9) (RDATAout) (Nd12)  
 (Vss) (G16) .

3 6가  
 (OE0)(OE1)(OE2) ' , ' , ' , ' ' (Red) 가 ' , ' .  
 (defect) , EMI EMI

2 .

[ 2]

| OE0 | OE1 | OE2 |                     |
|-----|-----|-----|---------------------|
| 0   | 0   | 0   |                     |
| 1   | 1   | 1   |                     |
| 0   | 1   | 1   |                     |
| 1   | 0   | 1   | (Only Red Output)   |
| 1   | 1   | 0   | (Only Green Output) |
| 0   | 1   | 0   | (Only Blue Output)  |

(RGB)  
 , TFT (Module), HDTV, TV

가

36 (Issue)가 EMI (tuning) EMI  
 (fliter) (value) (jumper)  
 (on)/ (off) 2 3

(Asic) (DE), 가 가  
 (Test) 36 ( 8 : LVDS TMD )

(chamber) (setup) . TMDS LVDS  
 ( )  
 . LCD LVDS, TMDS, TTL(1ch & 2ch) 가

, , 가 가 ,

(57)

1.

TFT - LCD

2.

1

(Asic)

3.

1

4.

1 ,  
2 1 1 1 , 1  
2 , 2 1 2 1 3  
, 2 4

5.

4 , ,  
1 1 ,  
1 2 2 1 AND ,  
2 2 ,  
1 2 2 2 AND

6.

5 , ,  
1 AND 3 1  
,  
2 AND 3 2

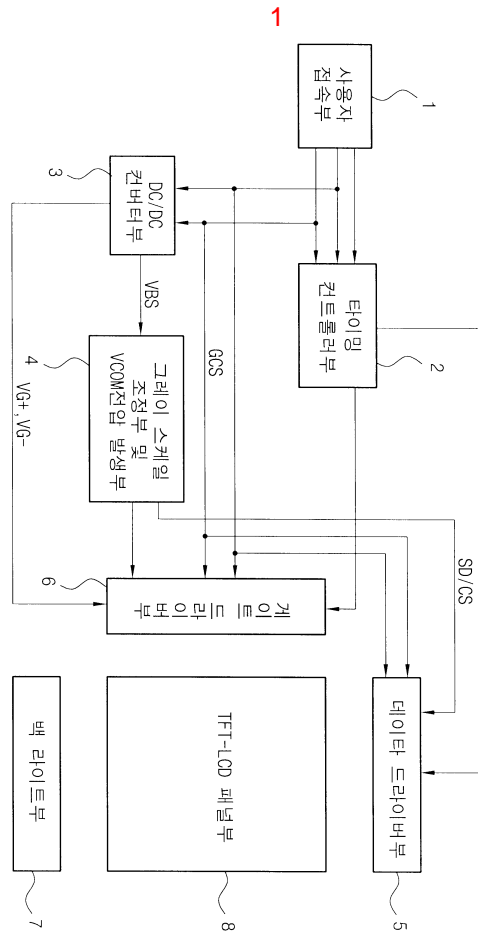
7.

1 , ,  
2 1 1 1 1 , 1  
2 , 2 2 3 , 2 5  
, 3 4 , 6 3 3

8.

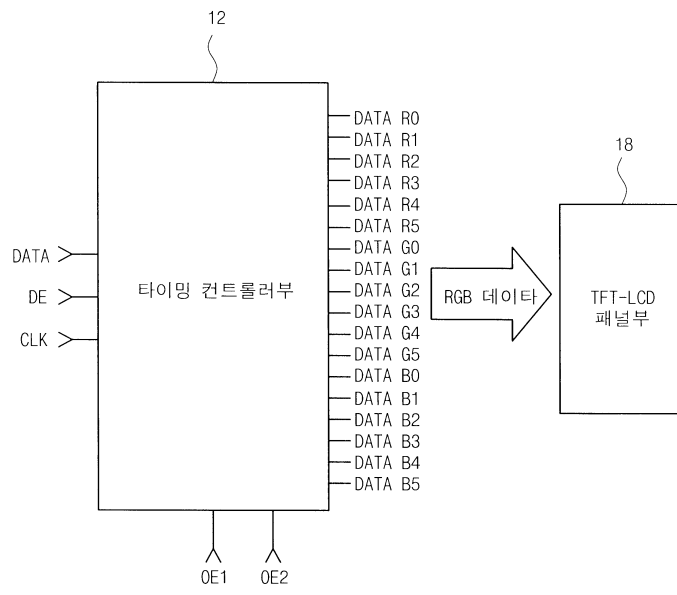
7 , ,  
1 3 3 1 AND , 1 1 ,

1 2 3 3 2 AND 2  
 , 2 , 1 3 3 2 3 3 AND  
 3 3 4 AND , 3 1 2 3 3  
 5 , 2 , 4 5 3 5 AND  
 .  
 9.  
 8 , ,  
 1 AND 4 1 , 1 AND  
 6 5 2 AND , 1 AND 8  
 4 3 2 AND 7 5  
 8 , 4 AND 7 7 6 ,  
 8 8 , 4 7 8 9 10  
 11 1 5 6 7 (RDATAout) (GDATAout) (BDATA  
 out) 12 3 7 4 , 7  
 5 , 9 10 (GDATAout) 11 (RDATAout) 12  
 6 .

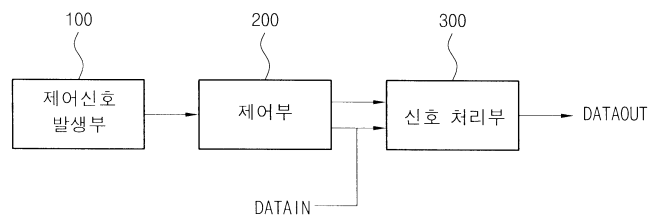


1

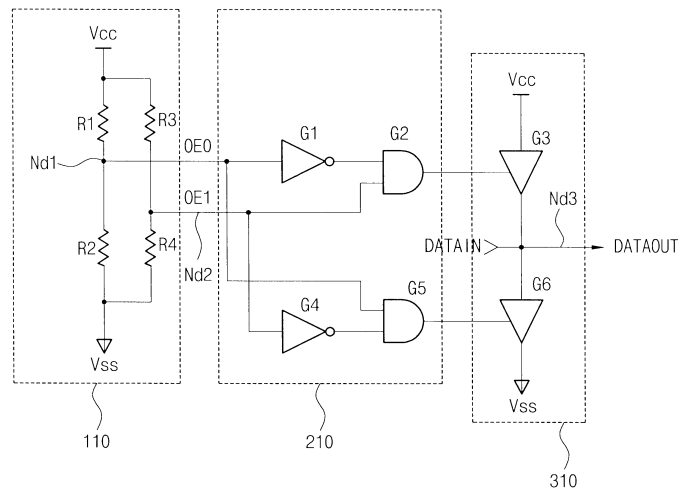
2



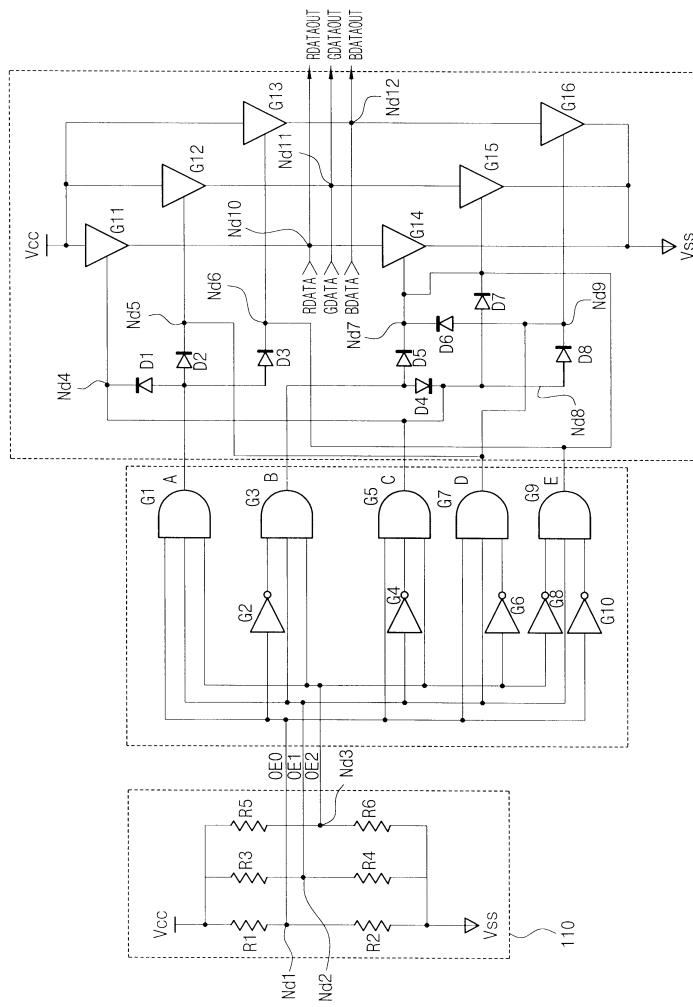
3



4



5



|                |  |         |            |
|----------------|--|---------|------------|
| 专利名称(译)        | 时序控制器的数据屏蔽和测试模式生成电路  |         |            |
| 公开(公告)号        | <a href="#">KR1020030032244A</a>   | 公开(公告)日 | 2003-04-26 |
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| IPC分类号         | G09G3/36   |         |            |
| 外部链接           | <a href="#">Espacenet</a>  |         |            |

摘要(译)

当引导到TFT-LCD产生电路，如EMI测试的定时控制器的数据屏蔽和测试模式本发明通过在各种模式控制输出信号到外部简单跳线（跳线）的操作，而不管所述输入数据信号的它可以方便地使用，并且可以通过在生产缺陷检查和腔室测试期间最小化设备变化来进行测试。和本发明的用于此的时序控制器的数据屏蔽和测试图案生成电路是用于产生单元，控制单元，用于选择以确定所述模式控制信号的模式控制信号生成的控制信号是控制数据的输出，其中模式并且通过从控制单元接收的信号中接收的数据信号，其特征在于，用于输出具有白色数据输出模式时，黑色数据，所述输出模式中，操作的正常模式中，钱护理的单一模式的信号处理器。

- 1 - 4

