

(19)
(12)(KR)
(A)(51) 。 Int. Cl. ⁷
G09G 3/36(11)
(43)2001 - 0100763
2001 11 14(21) 10 - 2001 - 0002343
(22) 2001 01 16(30) 2000 - 105317 2000 04 06 (JP)
2000 - 105308 2000 04 06 (JP)(71) 가 가
가 가 가 가 4 1 - 1(72) 가
가 가 가 4 - 1 - 1 가 가
가 가 가 4 - 1 - 1 가 가
가 가 가 4 - 1 - 1 가 가

(74)

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(54)

1 : .
 2 : .
 5 : .
 6 : .
 11 : .
 30, 40 : .
 101 : .
 102 : .
 103 : D/A .
 104 : .
 105 : .
 111 : NOT .
 112 : P MOS .
 113 : N MOS .
 121 : 1 .
 122, 124, 126 : .
 V1 V9 : .
 W1 W33 : .
 WA : .
 WB : .
 R1, R2, R : .
 Tr : .
 SEL : .
 NSEL : .
 PSEL : .

LN : .

NLN : .

PLN : .

LT : .

NLT : .

PLT : .

OP : .

SW : .

PNL : TFT .

, , (stress) ,

21 (PNL) (PNL) (40) (TFT)
 (LT), (SEL), (OP) (40)
 $\times m$ (LT1 LT4)가 (SW) (SEL) 2 $\times m$ (LT) 2
 SEL4)가 (SW) m (OP) 2 $\times m$ (OP1 OP4)가 (SEL1
 (SW) m (SW1, SW2)가

(40) , 384 , m 192 가 . 21
 가

(LT) , [()]
 (LT1 LT3) (LT2 LT4) 2 $\times m$ 가
 (LT1 LT3)
 n (64 6) (LT2 LT4) n

(SEL) , (SEL1 SEL3) (SEL2 SEL4) 2 × m
 가 (SEL1 SEL3) N MOS (SEL2 SEL4) (SEL2
 SEL4) P MOS . 64 , 64 × 2
 (LN) (SEL1 SEL4) (SEL1 SEL3) , 64
 (LN) (1) (SEL2 SEL4) , 64
 (LN) (1) .

(SEL1 SEL3) , (LN) 6V 0V
 (LT1 LT3) (SEL2 SEL4) (LN)
 6V 12V (LT2 LT4)

(OP) , (OP1 OP3) (OP2 OP4)
 2 × m 가 (OP1 OP3) (SEL1 SEL3)
 (OP2 OP4) (SEL2 SEL4)

(SW) , (SW1 SW2) m 가 (SW1)
 (OPL1)
 (OPL2) (PNL)
 (SW2) (OPL3)
 (PNL) (PNL) (OPL4) 가

(40) (LT), (SEL) (OP)가 , 2
 × m (, 384) (24) 15 mm , (24)
 (40) 가 , (40) 2 mm .
 (40)

(SEL1 SEL3) , (LN) (1)
 (SEL1 SEL3) , (LN) (2)
 () (SEL1 SEL3)
 , (SEL2 SEL4) (2)
 , N MOS (SEL1 SEL3) P MOS
 (SEL2 SEL4)가 (23)
 (40)가 (24)

22

(IC ; V1 V9), (R) (WW) (WW) (

WA) (WB)

(WW) 64 64

33 (W1 W33) (W1 W33)

(R) (V1) (W1) (V2) (W5)

(V3) (W9) (V4) (W13) (V5)

(W17) (V6) (W21) (V7) (W25)

(V8) (W29) (V9) (W33)

(W1 W33) (PNL) , (W1 W33)

(PNL) . 0V (V1) , 6V

(V9) , (V2 V8) 0V 6V (補間) 가

0V 6V (W1 W33) (R) ()

1 W33) (W1 W33) 가 (W

(PNL)

(W1 W33) (R)

가

(W1 W33)

가

(PNL)

가

가

가

가 , 12V (

V2 (V3) 가 (V1 V2) 가 , 12V (

(V3 V9) 가

가

가 , (PNL)
(V1) , 0V가 가 , (V9) 6V가 가 (V2 V8) 0
V 6V 가 . (W1 W33) .
, 가 12V (W1 W5) 가 ,
3V (=12V ÷ 4) (W1) (W2) 가 .
가 (V1 V2) 가 .
(V2 V3) 가 8 (V3 V9)
(PNL)
(PNL) n
n
가
(PNL)
1 , 1
1 , 2 1
2 가 1 가 1
가 , 2 가 2 가 .
(1)가 1 가 ,

(1
2
가
가 , 1
2
가
가 . , 1
2
가
가 .

가 , 가 .

(1)

1 (PNL) (PNL) 1 (30) TFT
(N ;NSEL), (LT), (P ;PSEL), (OP)
(SW) , 21 (SEL) (NSEL)
(PSEL) , TFT (PNL) 21 .

[1; ()
(LT1 LT3)가
(LT) , m (LT2 LT4)가
(LT1 LT3) , m (LT2 LT4)
(LT1 LT3) (64 6
) n

(NSEL) N MOS () , m
(SEL1 SEL3) , m/3 (, 64)
(NLN) (SE
L1 SEL3) , m/3 (NLN) (1)
(SEL1 SEL3) (NLN) , 6V 0V
(LT1 LT3) (3)
(OP) , (4)

2 (NSEL;N ;SEL1) (5)
(V-) (5) (V+) , 6V가 가 , (V-) , 0V가 가 (V+)
(V-) (6) (6) , 3/m(, 64)

(NLN) (6) , 6V 0V 64

64(6) , 6 N MOS (;Tr)가 (NLN)
 . N MOS (Tr) 6 × 64 2 .
 (LT1; 1) (3) (Tr) (3)
 64 (NLN) 가 (1) (4) (OP
 1) (NSEL;SEL3) (NSEL;SE
 L1)

1 , (PSEL) P MOS () . m
 (SEL2 SEL4) . (SEL2 SEL4) , m/3(, 64)
 (PLN) (PLN) . m/3
 (PLN) (SEL2 SEL4) (1)

(SEL2 SEL4) (LT2 LT4)
 . (V -) 6V가 가 , 2 (V+) 12V가 가 , (Tr) N (SEL2 SEL4)
 (5) 6V 12V

(OP) , m () (OP2 OP4)가 ,
 (OP2 OP4) m () (OP1 OP3)가
 (OP1 OP3) (SEL1 SEL3)
 (OP2 OP4) (SEL2 SEL4)

(SW) , m (SW1 SW2)가 (SW1)
 (OP1) (OP2) (PNL) (SW2)
 (OP2) (OP4)
 (PNL) (PNL) (P
 NL) , , 3 .

, (SEL2 SEL4) (LT2 LT4) ,
 (SEL1 SEL3) (LT1 LT3) (LT1 LT3)가 (PNL)
 (LT2 LT4) (NLN) 가 (PLN) (NLN)
 ,

, (30) (NSEL), (LT), (PSEL)
 (OP) m (, 192)
 , 21 (40) 2 × m (, 384)가
 (30) m (, 193)가
 (22) (30) 21
 (24) (30)

, 21 (40) (SEL) (LN) (SEL)
 (;2) (30)
 (PSEL) (NSEL)

, 21 (40) (23)가 (SEL)
 (SEL1 SEL3) (SEL1 SEL3) (21)
 N , (SEL2 SEL4) (SE
 L2 SEL4) P

(2)

3 2 TFT
 (PNL) (30) , 1 (1)
 (NSEL) (LT) 가 (PSEL)
 (LT) 가

(30) (NLT), (NSEL),
 (PSEL), (PLT), (OP) (SW)가
 (NLT) , m (LT1 LT3)가
 (PLT) , m (LT2 LT4)가

(PSEL) (PLT) (PSEL)
 NSEL) (NLT) (NLN PNL)
 (NSEL)가 가
 (PLN) (NLN) (1) 1
 , 1

(3)

4 3 TFT
 (PNL) (PNL) (30) , 2 (3)
 (PSEL) (PLT) 가

(PLT), (30) (PSEL), (OP) (NLT), (NSEL), (SW)가

(PSEL) (PLT) (NLT) (SEL1 SEL3) (LT2 LT4)가 (PLN) (NLN) (1) 1

(4)

5 (PNL) (PNL) (30) TFT (NSEL)가
1 (PSELa) 2 (PSELb) (NSELb) 2 (3) 1

(30) 1 (NSELa), (NLT), 2
(NSELb), 1 (PSELa), (PLT), 2 (PSELb),
(OP) (SW)가 1 (NSELa)
2 (PSELa) 2 (PSELb)가 (NLT) 1
(PLT)

(PLT) 1 2 (PSELa PSELb)
(NLT) 1 2 (NSELa NSELb)
가 . 가 .
(NLN) 1 (PSELa)가 (PLN) 2 (NSELb)
1 (1) 1

(5)

6 (PNL) (PNL) (30) TFT (L
T)가 1 (NLTa) 2 (NLTb) ,
(LT)가 1 (PLTa) 2 (PLTb) 1
(n) 가 (NLTa,

NLTb, PLTa, PLTb)

(30) , 1 (NLTa), (NSEL), 2
 (NLTb), 1 (PLTa), (PSEL), 2 (P
 LTb), (OP) (SW)가
 (NLTa) 2 (NLTb) (NSEL)가
 , 1 (PLTa) 2 (PLTb) (PSEL)가

, (PSEL)가 1 2 (PLTa PLTb)
 , (NSEL)가 1 2 (NLTa NLTb)

(PLN) (NLN)
 1 (PLTa)가 2 (NLTb)
 , 1 (1) 1

(6)

7 6 TFT
 (PNL) (PNL) (30) 1 (1)
 (LT1 LT3) (LT2 LT4)
 , (LT1 LT3) (LT2 LT4)

(OP) (30) (NSEL), (LT), (PSEL),
 T) , (SW)가 (LT2 LT4) (L
 (LT1 LT3)

, (LT1 LT3) (LT2 LT4)가 (PLN)
 (NLN) (1) 1
 , 1

(7)

8 7 TFT
 (PNL) (PNL) (30) 2 (LT1b LT3b)
 1 (LT2a LT4a) 5 (6)
 , 2 (LT1b LT3b) 1 (LT2a LT4a)

1 (30) (NPLT), 1 (NLT), 2 (NSEL), 2 (O
P) 1 (SW)가 (NPLT), 2 (PSEL), 2 (PLT), 1 (LT1b LT3b) 1 (LT2a LT4a)
(NPLT), 2 (LT1b LT3b) 1 (LT2a LT4a)
, 2 (PLN) (NLT1b NLT3b) 1 (PLT1a PLT3a) (NLN)
1) 1 , 1
(8)
9 8 TFT
(PNL) (PNL) (30) (30) (11) 1
7 가 (SW) (11)
(OP) (OP1 OP3) (OP2 OP4) (OP1 OP3)
(OP1 OP3) , (OP2 OP4)
1 8 , (OP1 OP3) (OP2 OP4) 1
(LN) (NLN)
(9)
10 9 TFT
(PNL) (PNL) (30) (OP1 OP3)
(OP2 OP4) 8 (9) ,
(OP1 OP3) (OP2 OP4)
, (OP2 OP4) (OP1 OP3) (PLN) (NLN) 1
(30; 11a 1 9 (PNL)
(30a) (30b) (30)
, (NSEL) (30a)
(30b)
11b (PNL) (30;) 10
(30a) 10 1

(31a) 2
(30b) 가 , 1

(31b)
(31a) 2 (31b)

(31a 31b)
1

(30b)

(30b) (30)

(30b) (30)

가 (SW) IC() (30) TAB(

;tape automated bonding)

1 10 (30) 가 21

(40) (30)

21 (40) (2;) (PSEL) (30)

(30) (NSEL)

21 (SEL) 가

(30) 가

(30)

(11)

12 11 (PNL;101)

(102) (102) (IN)

(OUT) D/A (103) D/A

(103) (104) (105)

(104) (105) 64 (IN)

(PNL;101) (104) 64 (105) (IN)

(105) , 64 (104) (OUT)

(PNL;101) (OUT) (

105) (102) (PNL;101)

(PNL;101) (PNL;101)

13 1 (NSEL) (PSEL)
 11 (104) (front half) (WA)
 104) 22 (WB)
 (rear half)
 (104) (IC ;V1 V9), (WA), (WB)
 (R1 R2) (WA) (WB)
 (WW)
 (WW) 64 64
 33 (W1 W33) 가
 (W1 W33) (W1)
 (W33)
 (WA) 2 (WB) 2
 16 (W1 W16) 16 (W17b W33)
 (WA) (W1 W16) 1 (R1) (WB)
 (W17b W33) 2 (R2) (V1) (W9)
 (W1) (V2) (W5) (V3)
 (V4) (W13) (V5) (W17a)
 W17b) (V6) (W21) (V7) (W25)
 (V8) (W29) (V9) (W33)
 (W1 W33) 12 (105) (PNL;101) (V1
 V9) 가 (PNL;101) , 0V (V
 1) 가 , 6V (V9) 가 , 0V 6V (V2 V8) 가 ,
 (W1 W33) 14 0V 6V
 (R1 R2) 14 , 가
 14 (V2 V8)
 가
 13 , 9 (V1 V9)가
 (W1 W4) (V1 V4) (WB) (WA) [W17a(
 W17b) W33] (V5 V9)
 (V1 V9) 가 , 1
 (W1) (W17a)
 W17a) (W17b) , 2 (R2)
 (W17b) (W33) 1 (R1)
 가 2 (R2) 가 , (W1 W33)
 (R1 R2) , 14

, (12) (102) (W1 W33) , (R1 R2) ()
 (102) , 가 ,
 3, V4) , 가 , 12V() 가 , 0V가 (V1, V2, V (V5, V6, V7, V8, V9) 가 .
 가 , (V1 V4) 0V 가 가 , (R1) , 0V (W1 W13) , 12V 가 (V5 V9) 가 , (R2) , 12V (W17b W33) , 0V가 (V1) 가 , 12V가 (V5) 가 , 12V (W1 W17b) 가 , (W2) 1 (R1) (V1 V2) 0V가 가 , 12V (W2 W1 7b) 가 . 12V 가 .
 , 22 , (104) , 12V 3V(=12 ÷ 4) (W1 W5) 12V 가 ,
 가 , 22 , (V3 V9) 가 , (V2 V3) 가 , (V1 V2) (104) 0V가 (V1 V4) 가 , 12V가 (V5 V9) 가 ,
 V 가 가 12V가 (V5) , 0 (V9) 가 가 . 12V ((V5 V9) 가 , 12V (V6 (R1) (W13) (W17a) 가 , (W13) 1 (W17a) 12V 가 , 0V (V1 V4) 가 , 12V (V5 V9) 가 , 0V (V1 V5) , 12V (V6 V9) 가 (104) 16
 가 , , , 0V가

(V1) 가 , 6V가 (V9) 가 , 0V 6V (V2 V8)
 . (W1 W33) .
 (102) 가 ,
 가 , .

(12)

15 (104) 12 13 11
 , (WB) (W17b)
 (W33) (W17b W33) .
 , (WB) (W18)
 (W33) (W18 W33) , (W17a W
 17b) (17) , (WA) 11
 (WA)

(WA) 17 (W1 W1
 7) . (WB) 16
 (W18 W33) .

(WA) (W1 W17) 1 (R1) (WB)
 (W18 W33) 2 (R2) (V1 V4) (WA)
 11 (V5) (W17) (V6) (W2
 1) . (V7) (W25) (V8) (W29) .
 (V9) (W33) .

PNL;101 , 11 (V1 V9) 가 가 ,
 (V2 V8) 0V 6V (V1) 0V가 가 , (V9) 6V가 가 ,
 1 (R1) (W1)
 (W17) 2 (R2) (W17) 1 (R1)
 , 2 (R2) ,
 (W17) (W33) , 1 (R1) 2 (R2)
 가 (W1 W33) , 1 2
 (R1 R2) , 14 가 1
 2 (R1 R2) .

, 11 , 12V
 가 , .

(13)

16 (104) 13 13 13
 11 (V5) (V5A V5B) ,
 11 .

(WB) , 가 (W17c) (W17c) 1 (R1) (W1 W17a) (W17c) 2 (V5A) (V5B)

(W17d W33) (W17d) (V5B)

가 , 0V (V1, V2, V3, V4, V5A) 가 , 12V() (V5B, V6, V7, V8, V9) (W13) (W17a) 가 , 0V (W13 W17a) (V4 V5) 가 , 12V (V5B V6) 가 , 12V (W13) (W17a) 12V 가 , 12V 가 , 13 11 (V5A V5B) 가 (14) 17 (104) 14 14 15 12 (V5) (V5A V5B) 12 (WA) , (W17a W17c) (W17c) (W17a) 1 (R1) (W1 W17a) 2 (R2) (W17c W33) (V5A) (W17a) (V5B) (W17c) (V5B) (V5A) (V5B) (V1, V2, V3, V4, V5A) 가 , 12V() (V5B, V6, V7, V8, V9) (W13 W17) 가 (W13 W17a) (V4 V5) A) 가 , 12V (V5B V6) 가 , 12V (W13) (W17) 12V 가 , 15 12 (V5A V5B) 가

(15)

18 (104) 14 16
13 (V5A V5B) (SW)가 , 13

(SW) (V5A V5B) 13 (16)
가 , (SW) (V5A V5B) ,
(SW) (V5A V5B) 1
4 (17) (V5A V5B)

19 (SW) (SW) P MOS (;112) N
MOS (;113) NOT (;111) (CTL) N
OT (111) N (113) . NOT (111) P
(112) (112 113) / (V5A V5B)

(CTL) , (V5A V5B) (
112 113) 가 , (CTL) 가 ,
(112 113) 가 , (V5A V5B) 가 .
(SW) P N MOS () ,
N MOS () P MOS ()

, 11 15 , 1 (,) 2
(,)
가 ,
가 , 가
가 ,

20a , (12) (102) . 1 (121) , (1)
(105) . 1 (121) (122) (122) 2 (
WA WB) . 2 (WA) , 2 (WB) . 2
(WA WB) . 2 (WA WB) (124)

20a (WA) (WB) ,
20b , (WA) (WB) 가 .
20b , (12) (102) . 1 (121) , (
1) (105) . 1 (121) (122) (122) 2
(WA;) . 2 (WA) (124) . (124) 3
(WB;) . 3 (WB) (126)

$$\begin{array}{ccccccc}
20c & (12) & & (102) & & 1 & (121) & (1) \\
2 &) & (105) & & 1 & (121) & (122) & & 2 \\
(WA; & &) & 2 & (WB; & &) & & \\
2 & (WA & WB) & & (124) & & (124) & 3 & (WA; &) \\
3 & (WB; & & & & & & 3 & (WA & WB) \\
& (126) & & & (WA & WB) & & & &
\end{array}$$

(WA) (WB) , (W1 W4) 1 ,
 가 , 22 , (W13 W16) 4 ,
 (W5 W8) 2 , (W9 W12) 3 ,
 . 1 2 , 3 4 ,
 2 , (,
 (WB) (WA) 4 . (

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3 1 2 1 2 , ,
1 2 1 2 ,
1 2 ,

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11 , 2 1 가

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3 , 1 2 ,

1 2 1 2 ,

14.

13 , 2 1 가

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2 2

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27.

26 1 2 가 1
2

28.

26 1 2 가 1
2

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31 , N P

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31 , N .

34.

31 , P .

35.

21 , 1 2

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36.

21 , 1 2

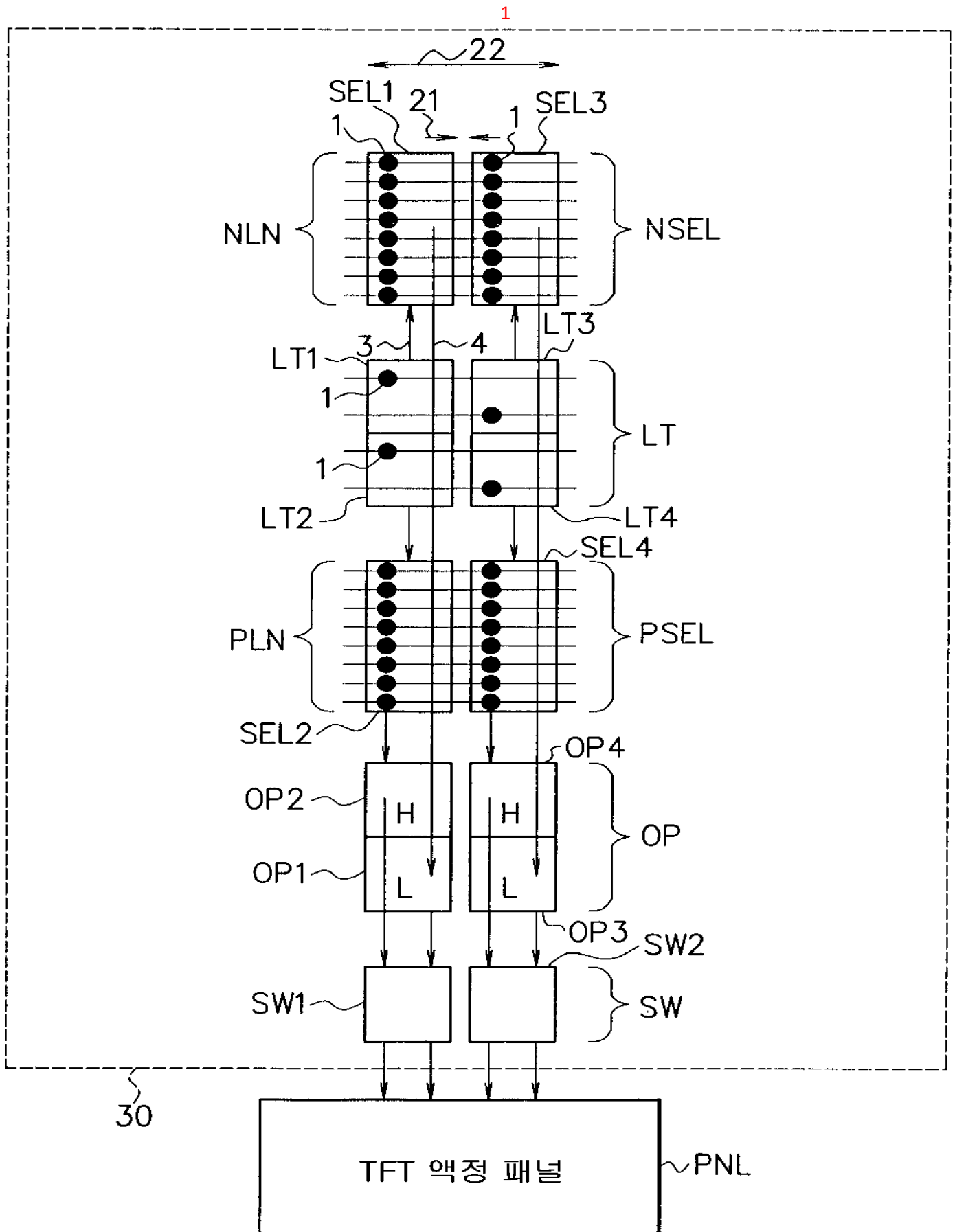
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37.

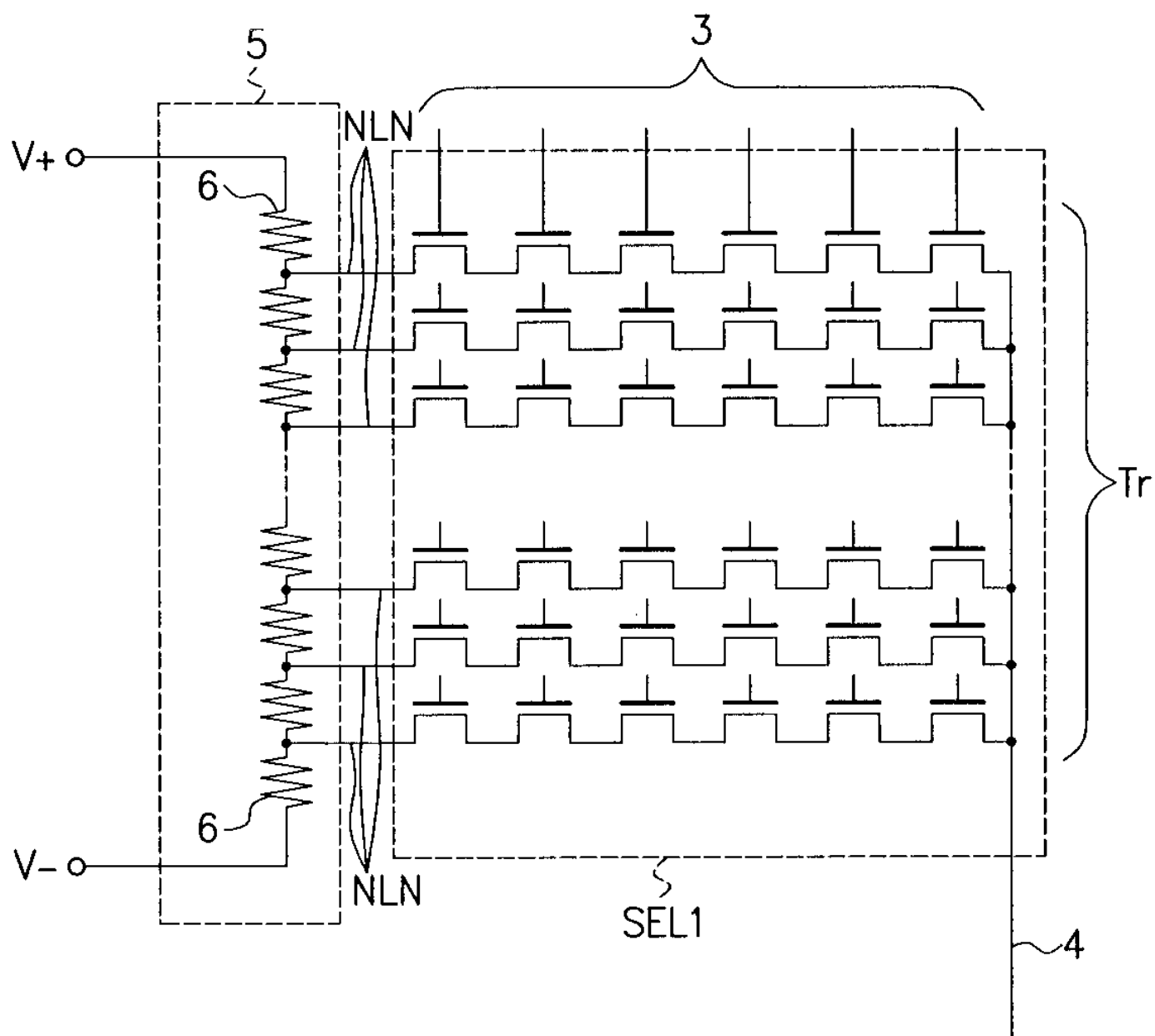
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1 1,
1 2, 1 2
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1 1,
2 2,
1 1,
2 2,
1 2
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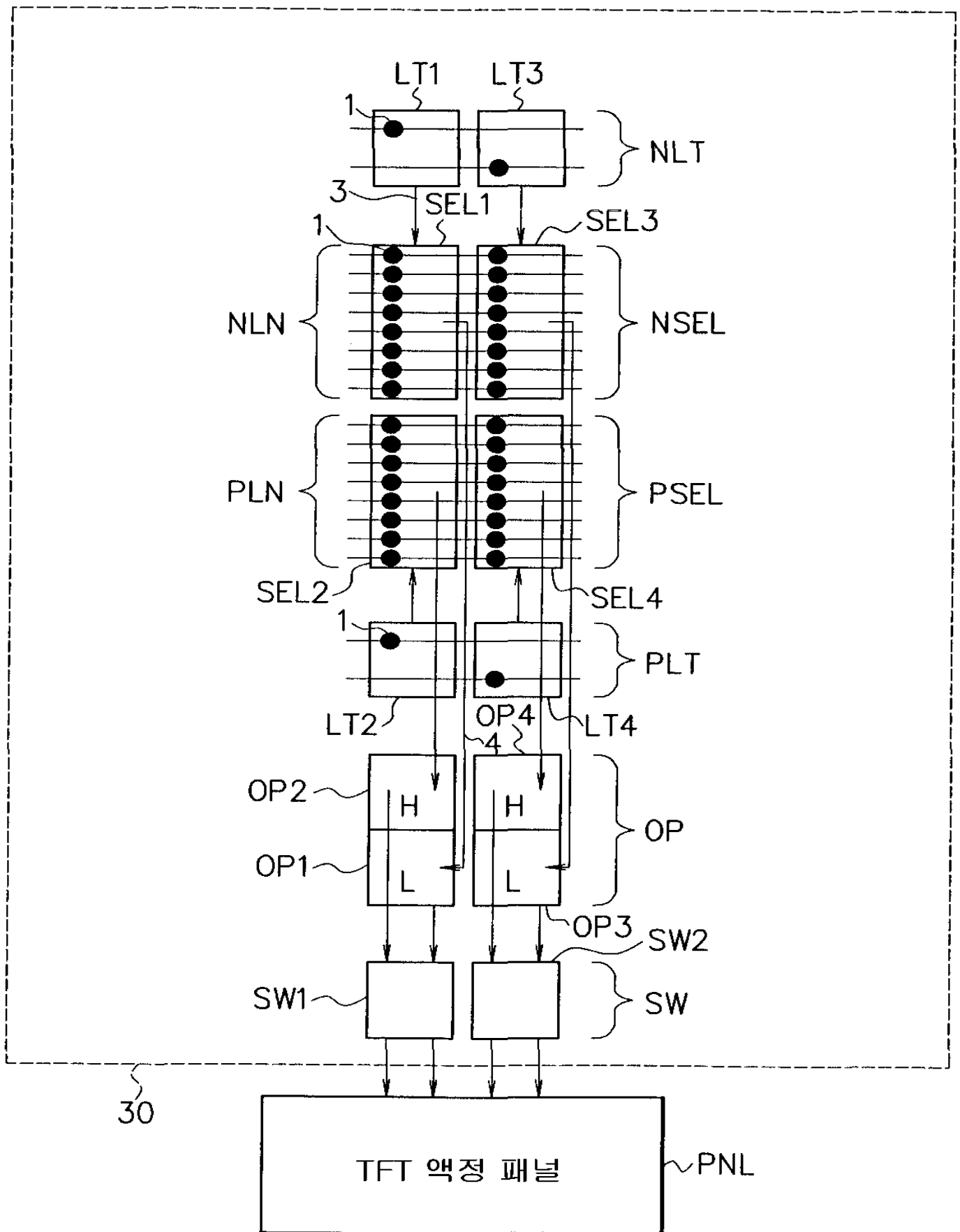
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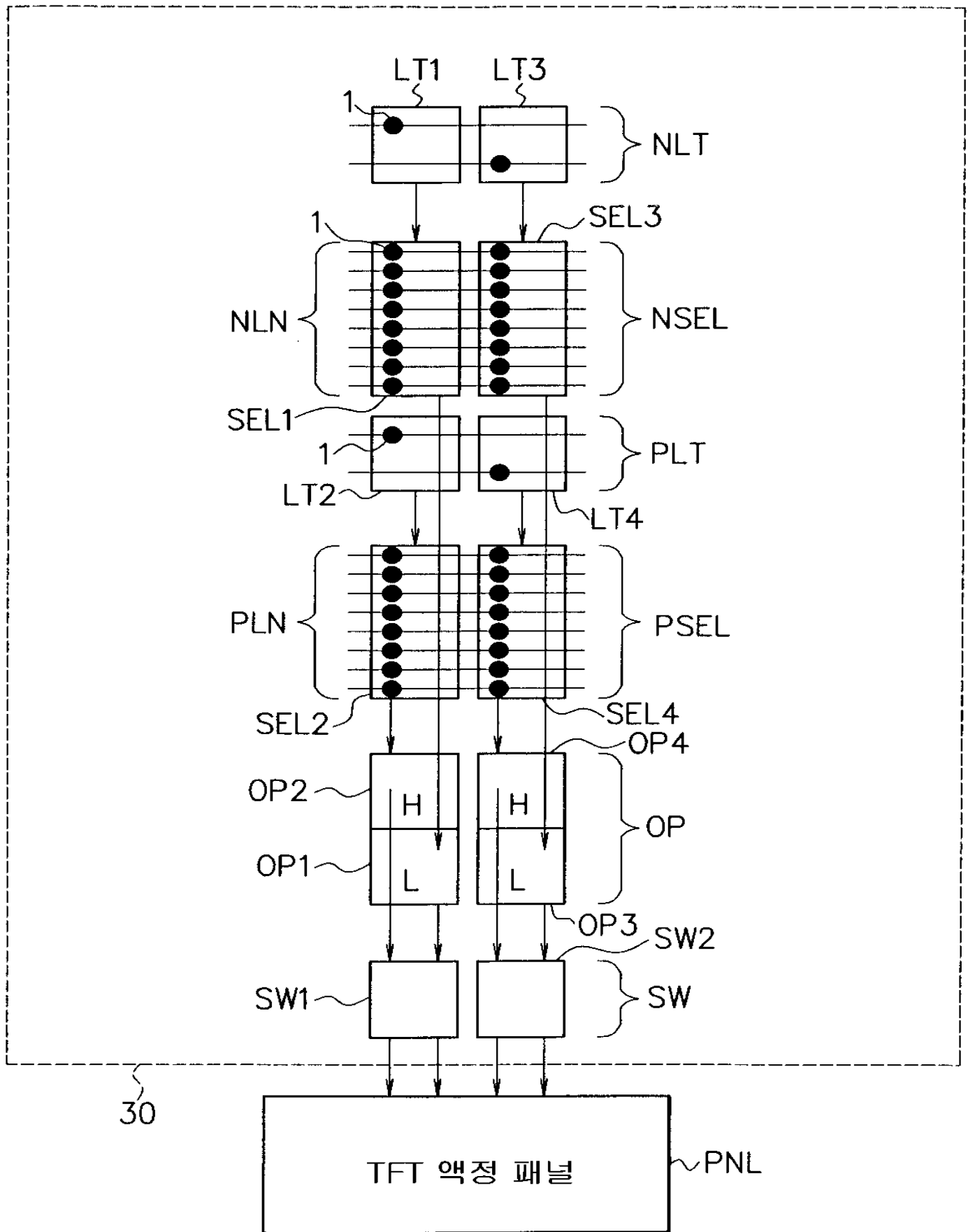
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1 1 가 , 2
2 가 ,
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1 2 가 ,
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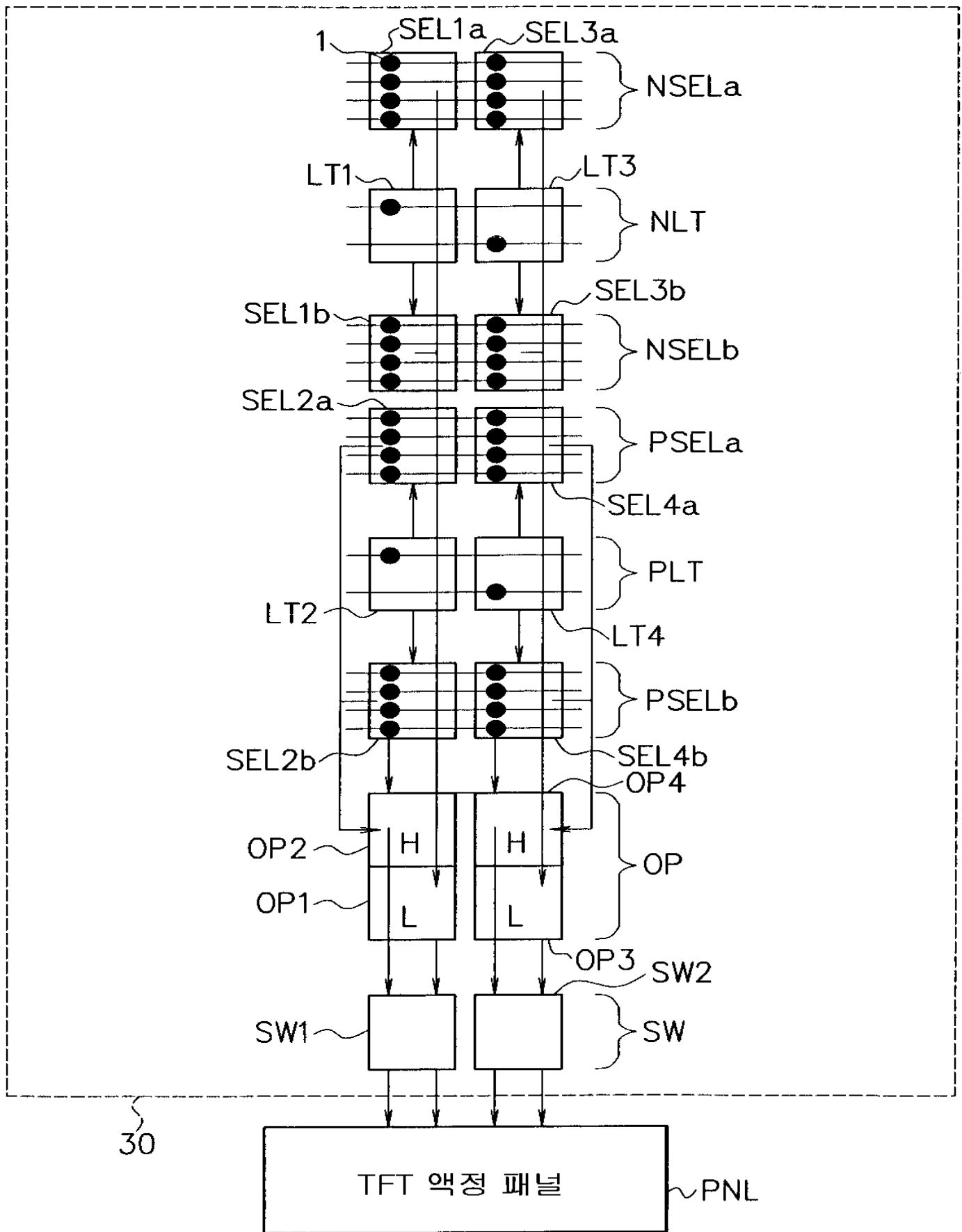


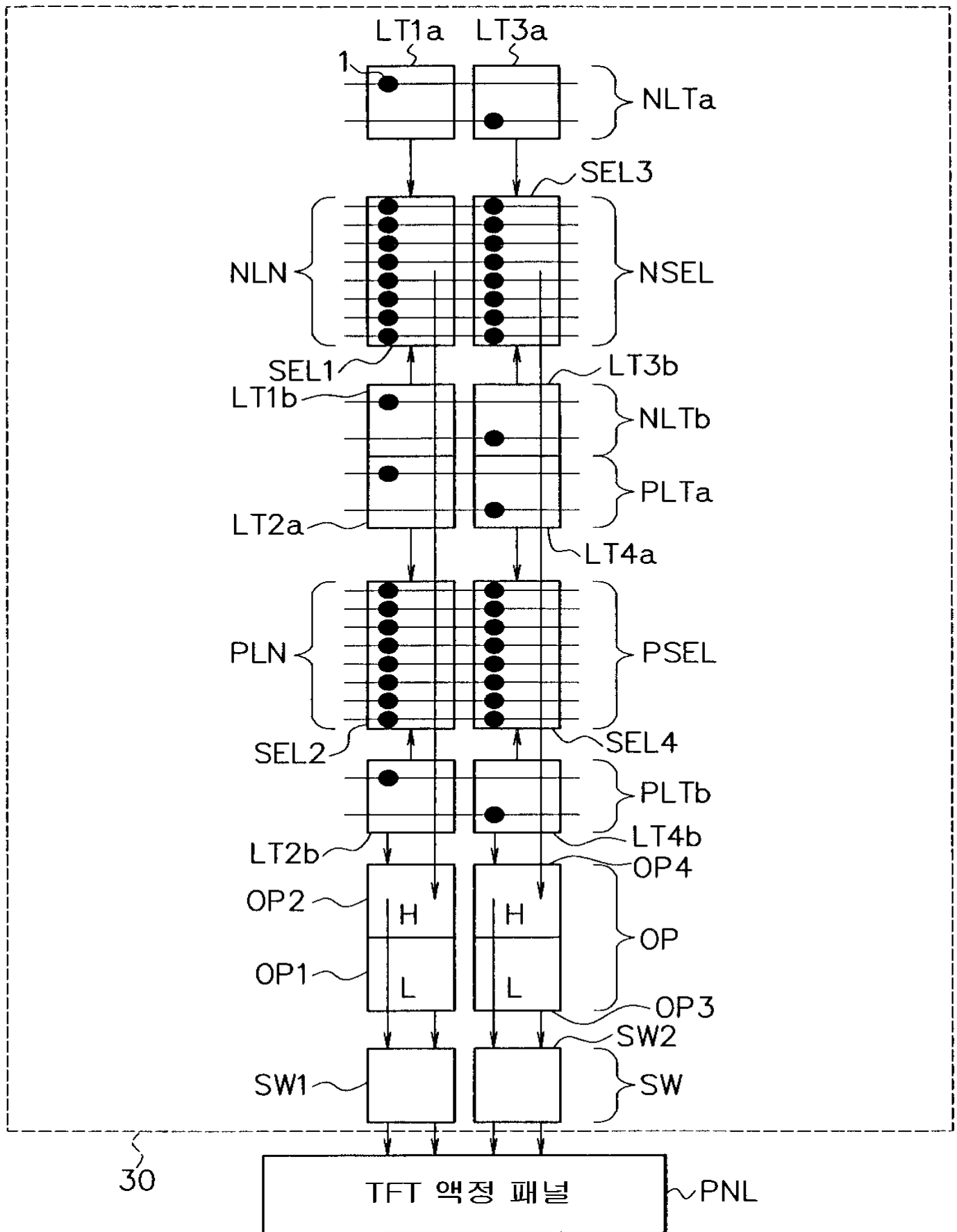
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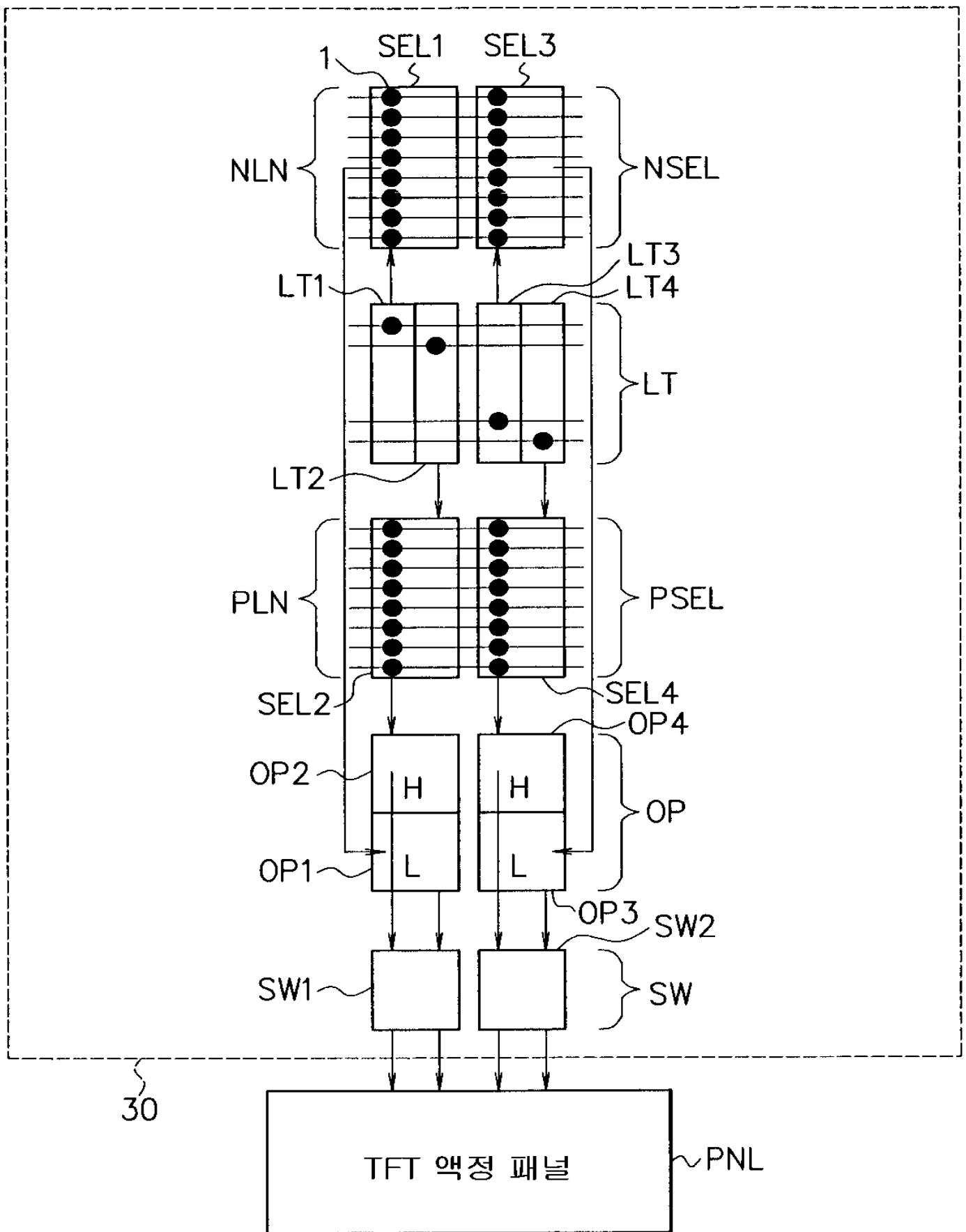


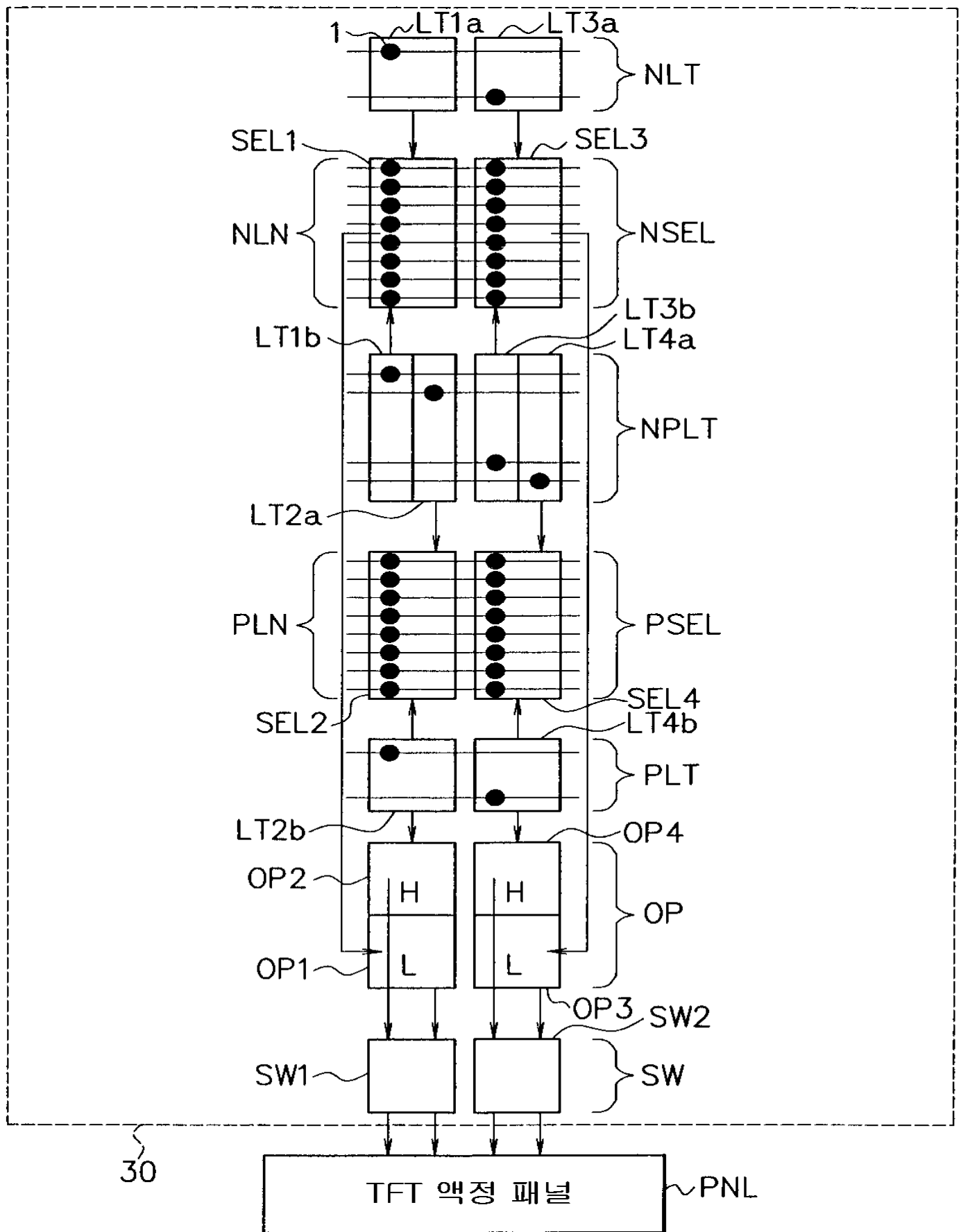


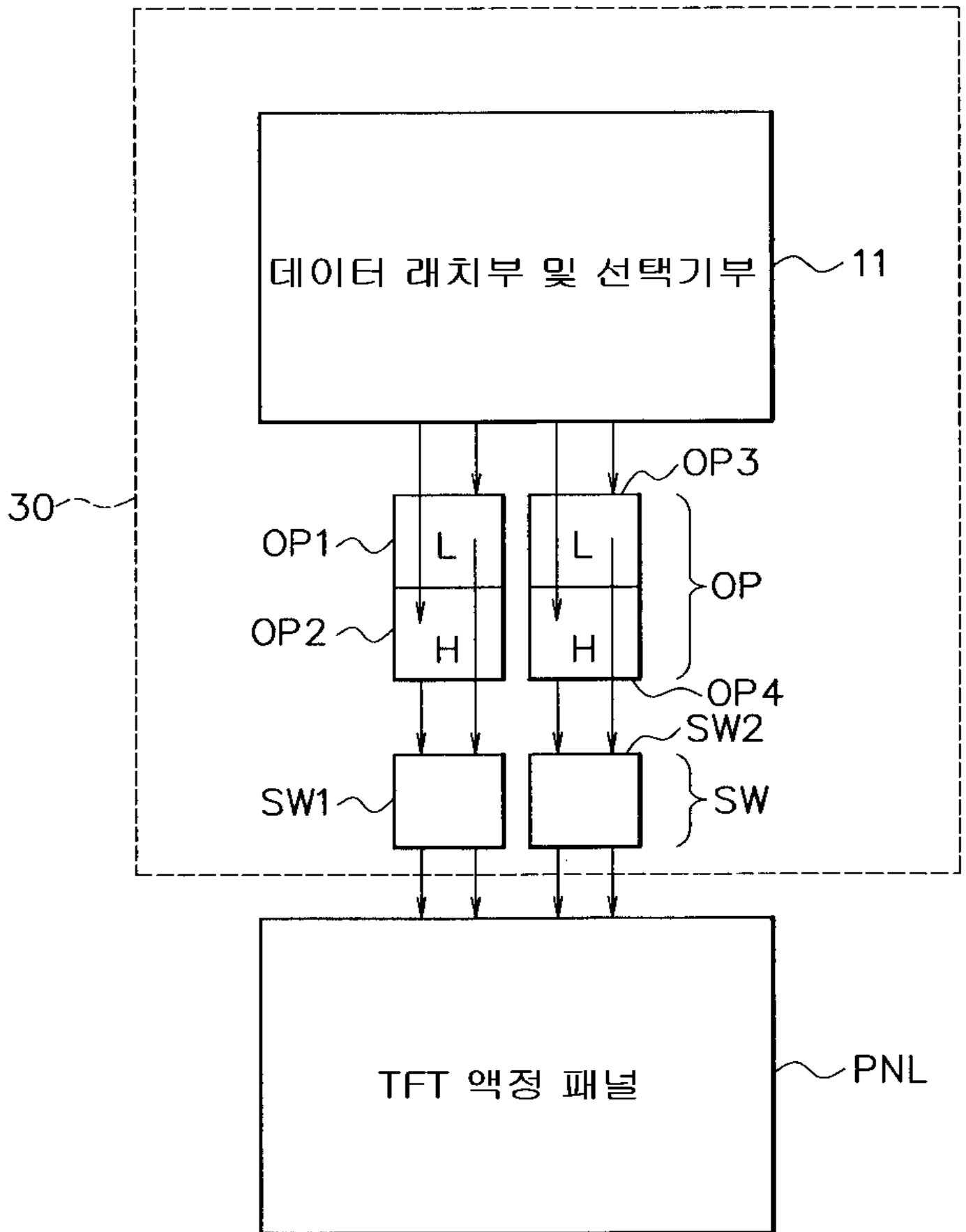




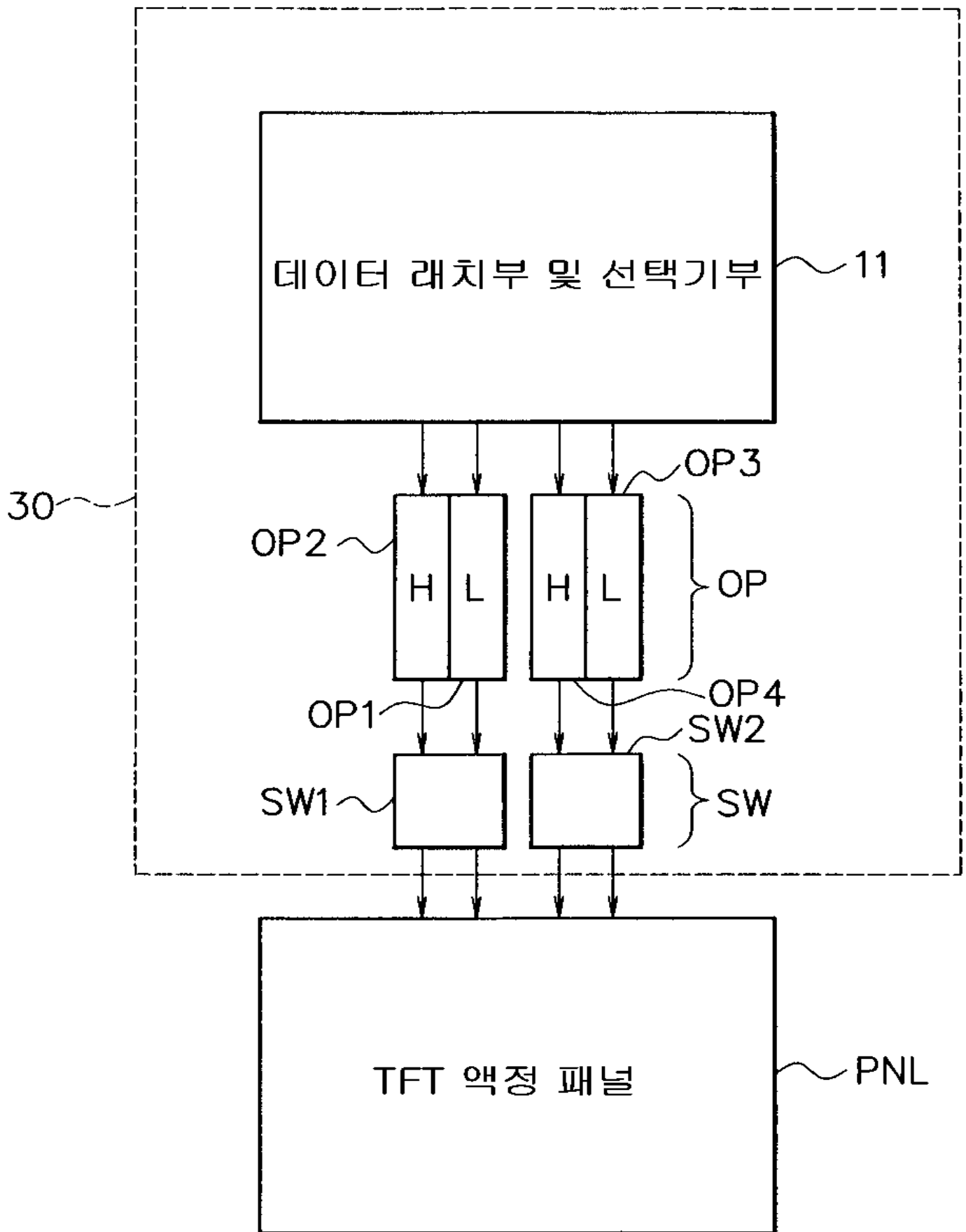


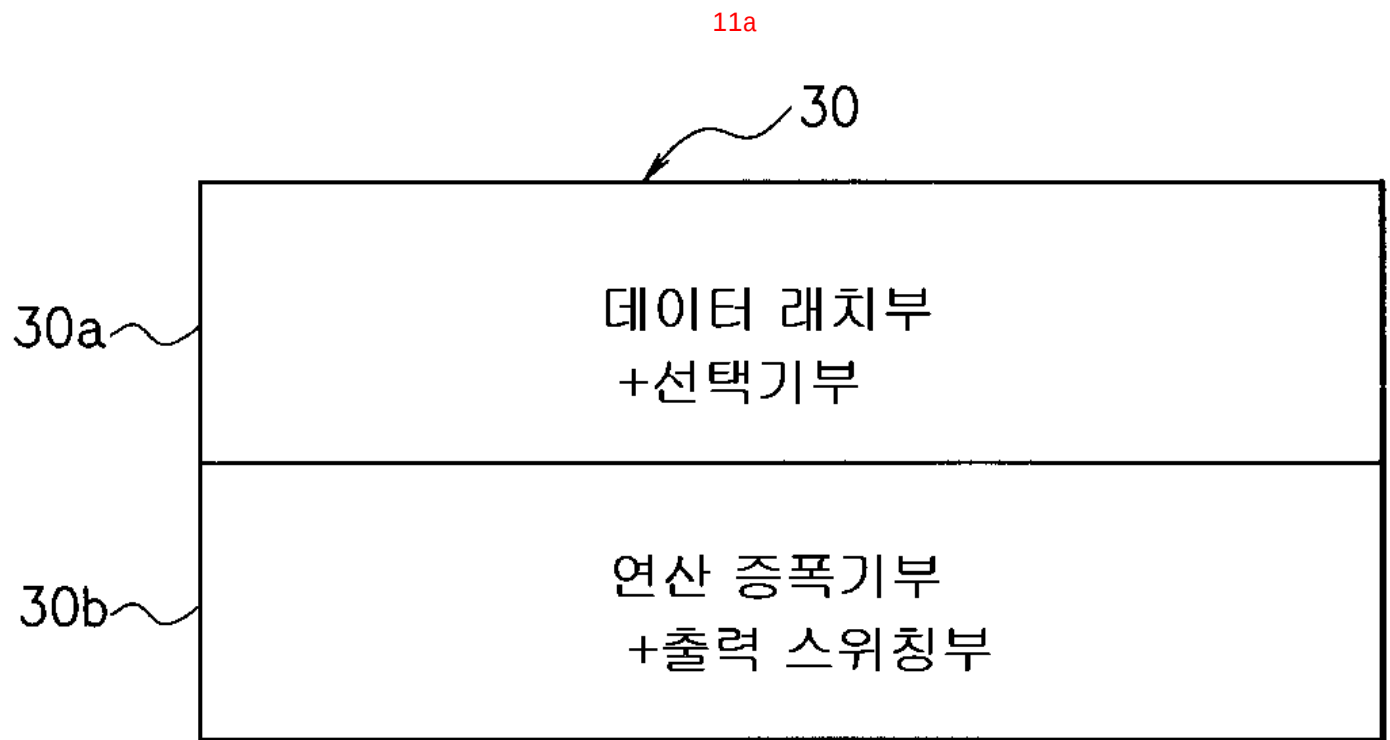




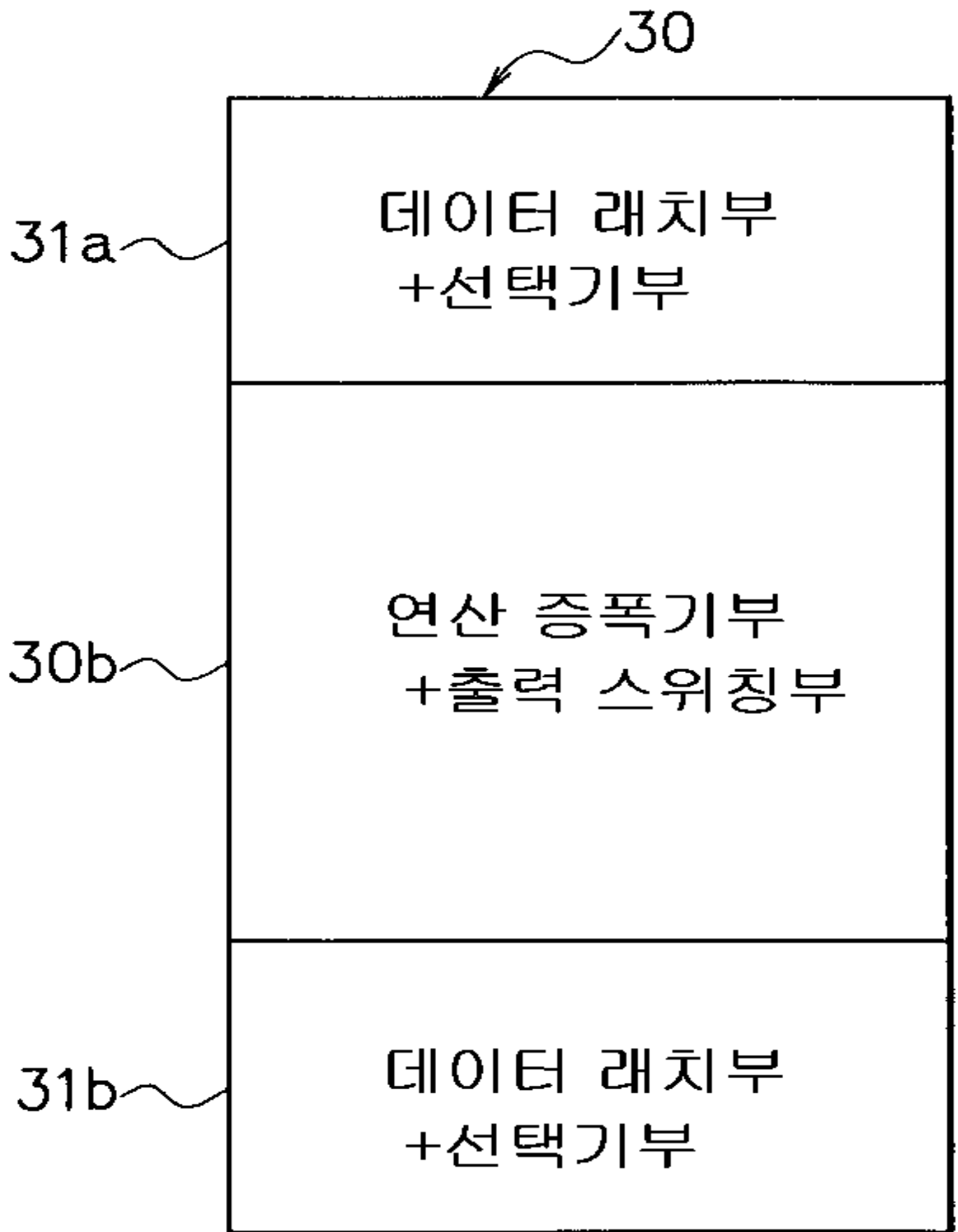


10

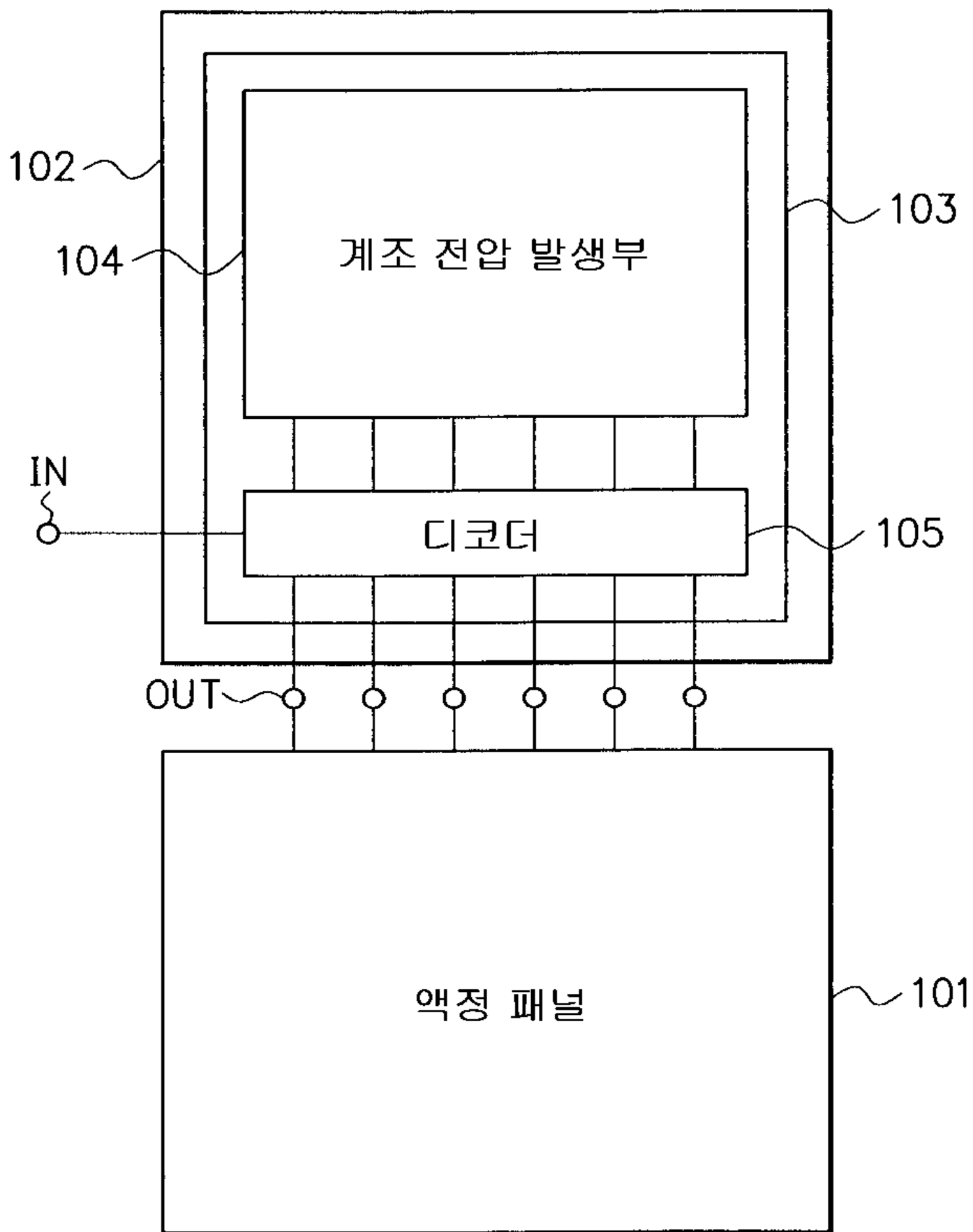




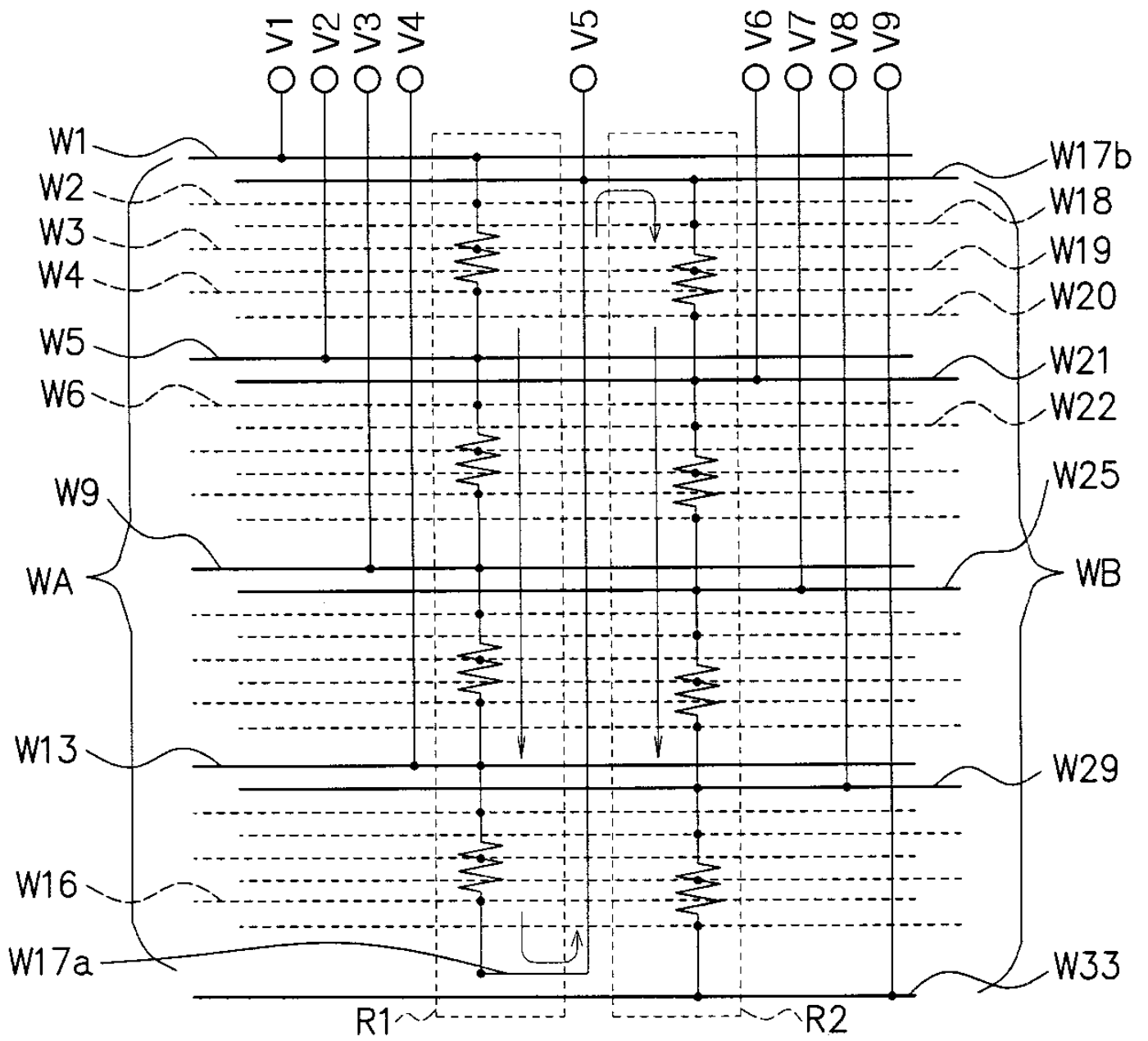
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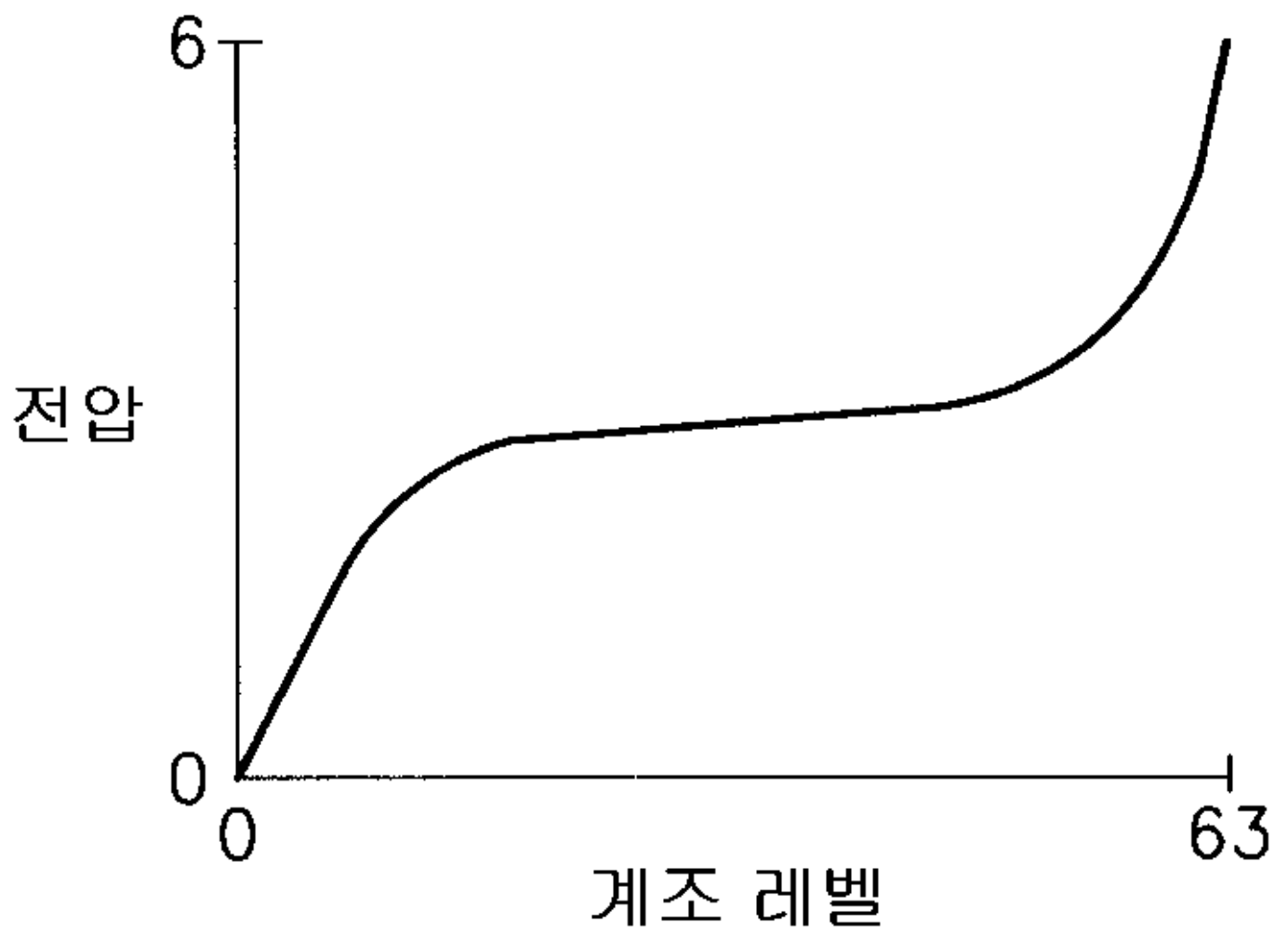
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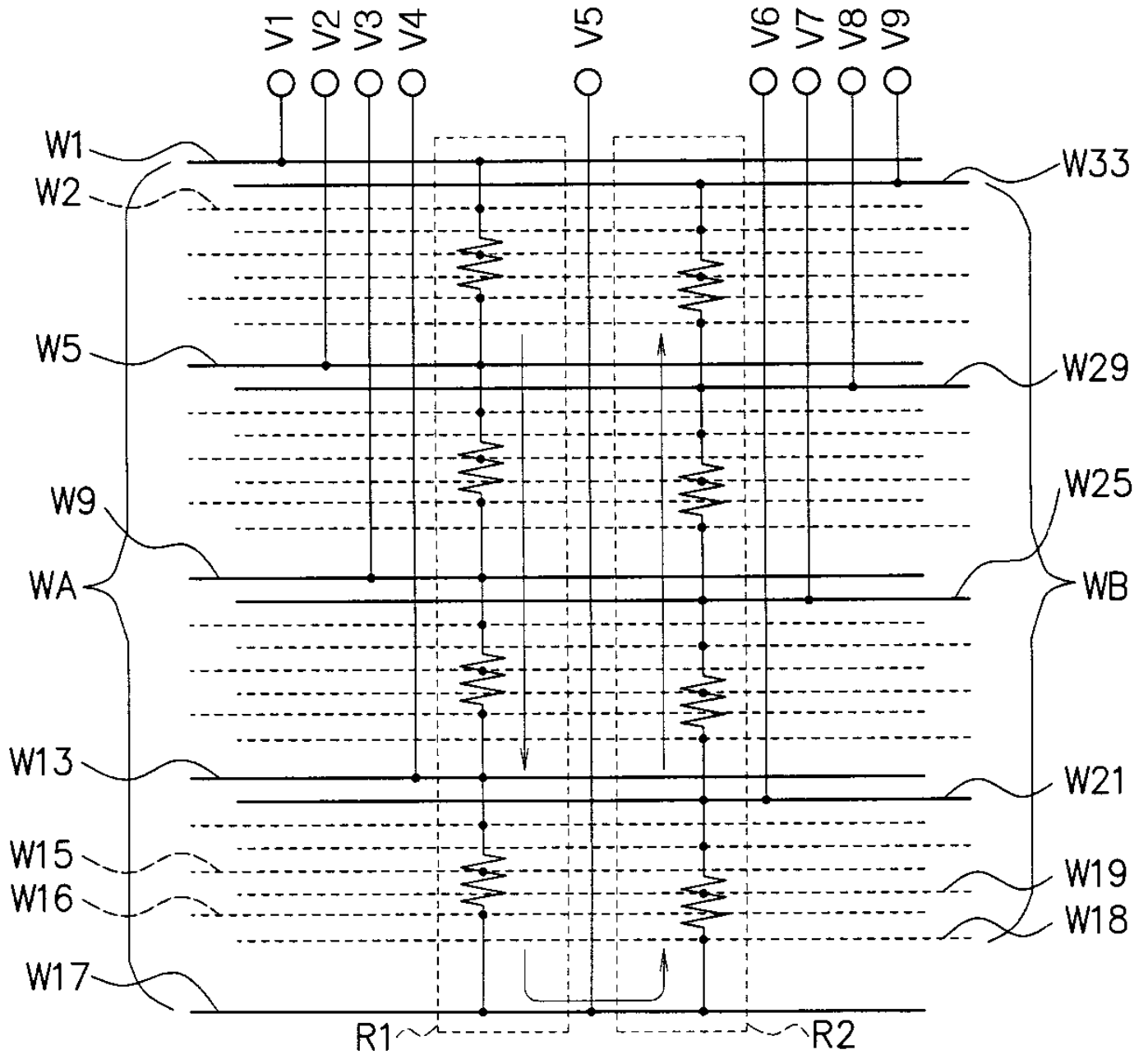
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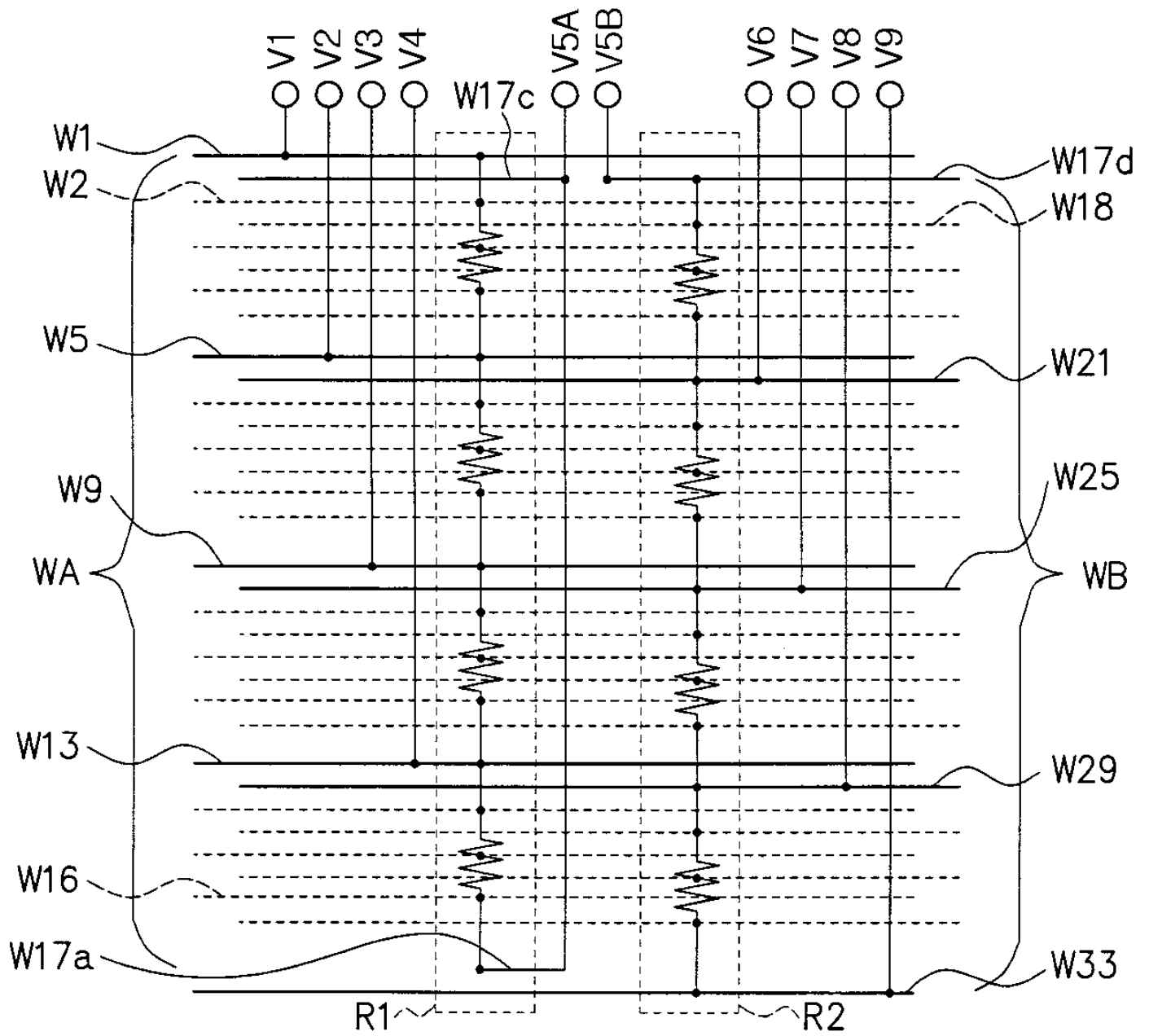
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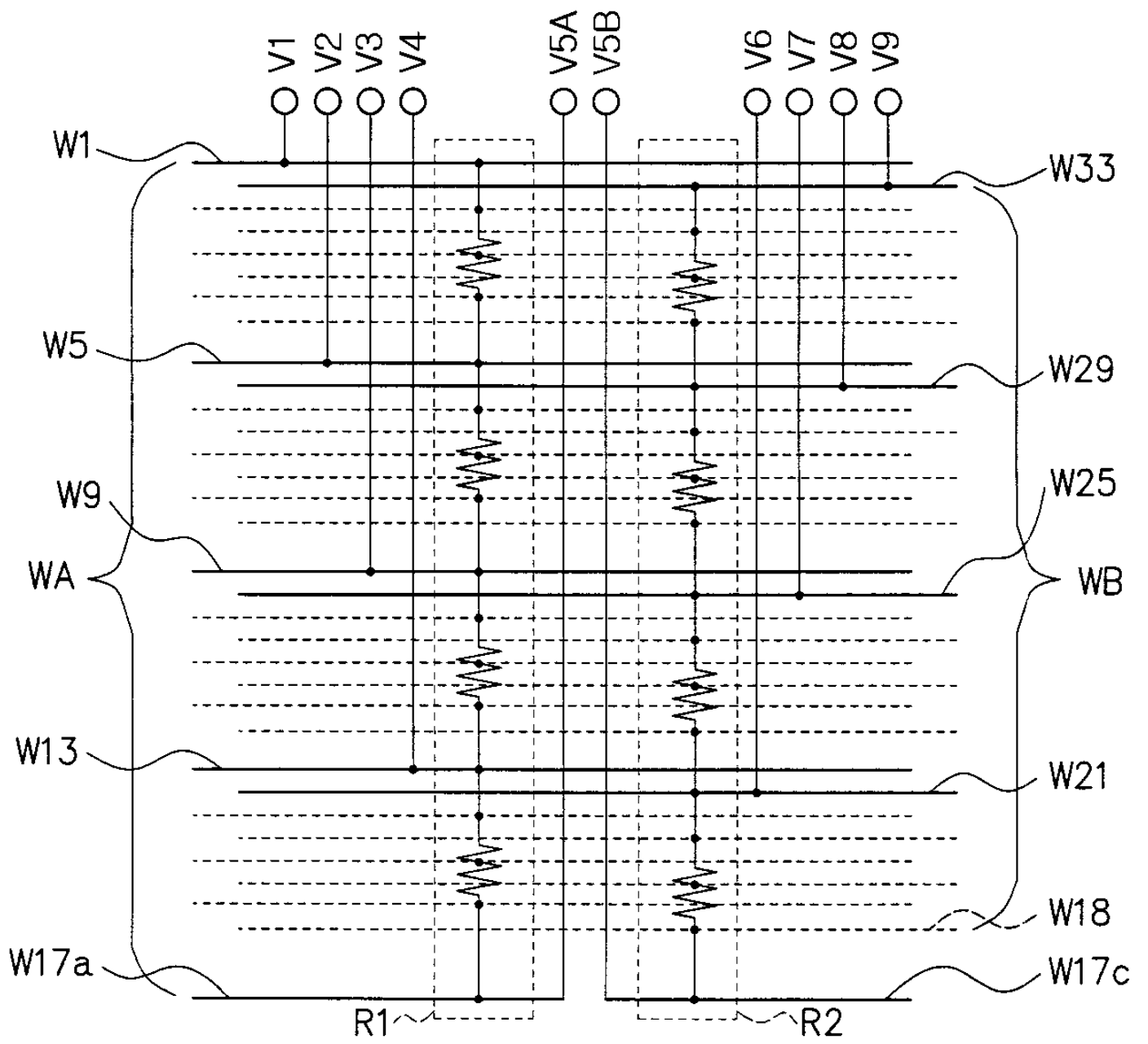
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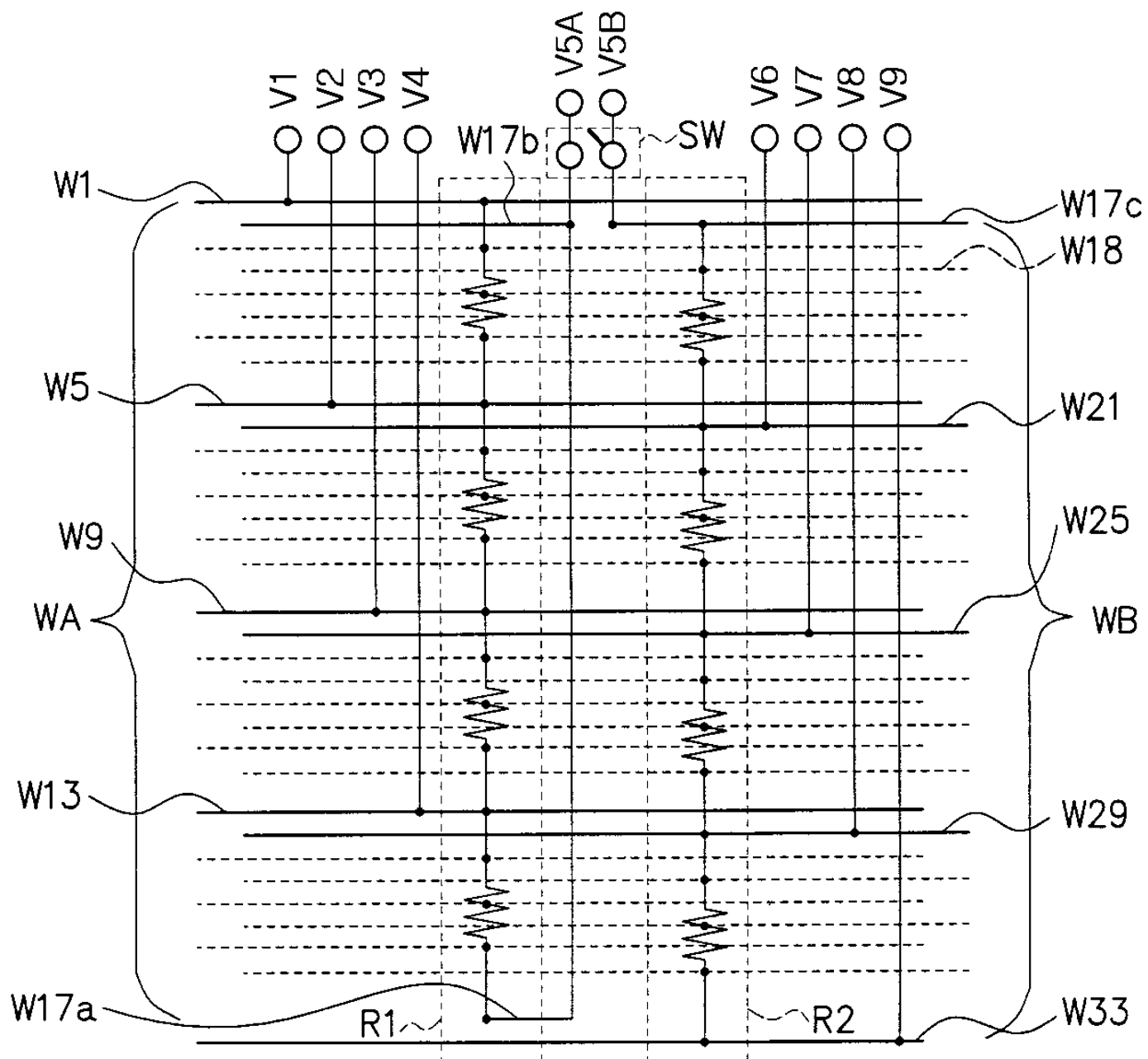
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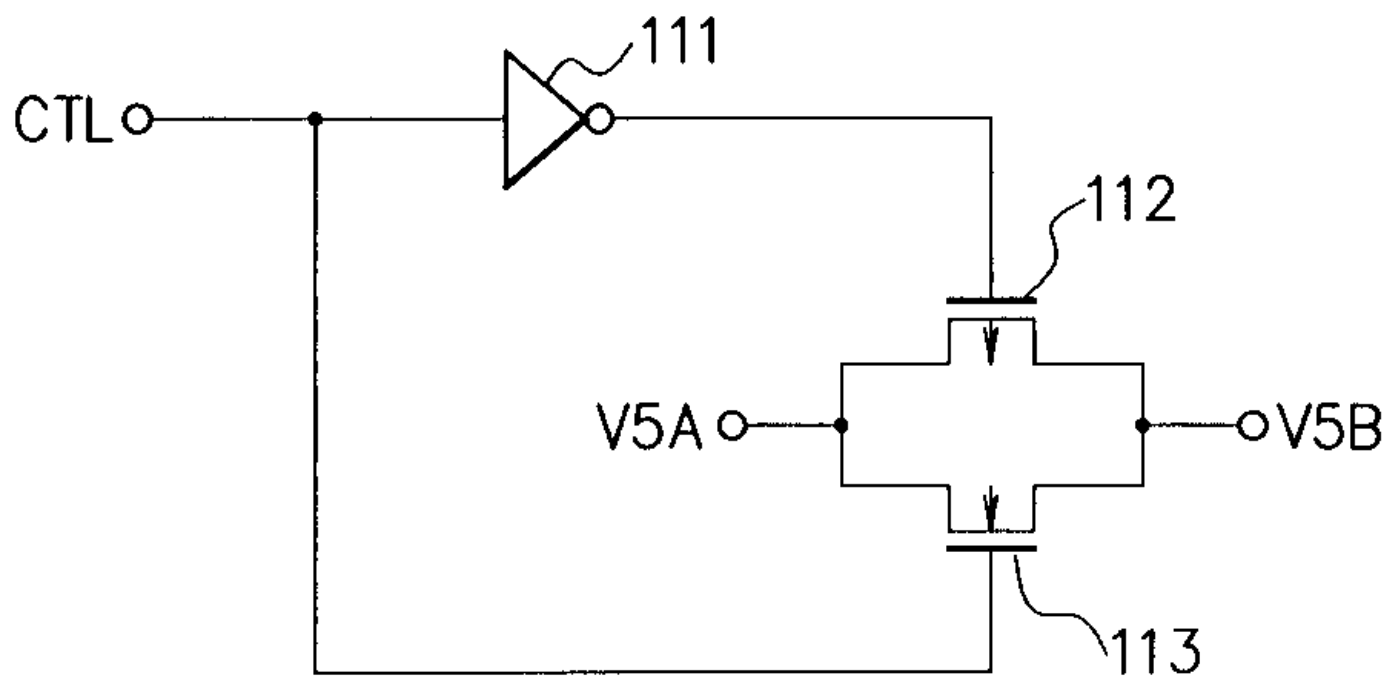
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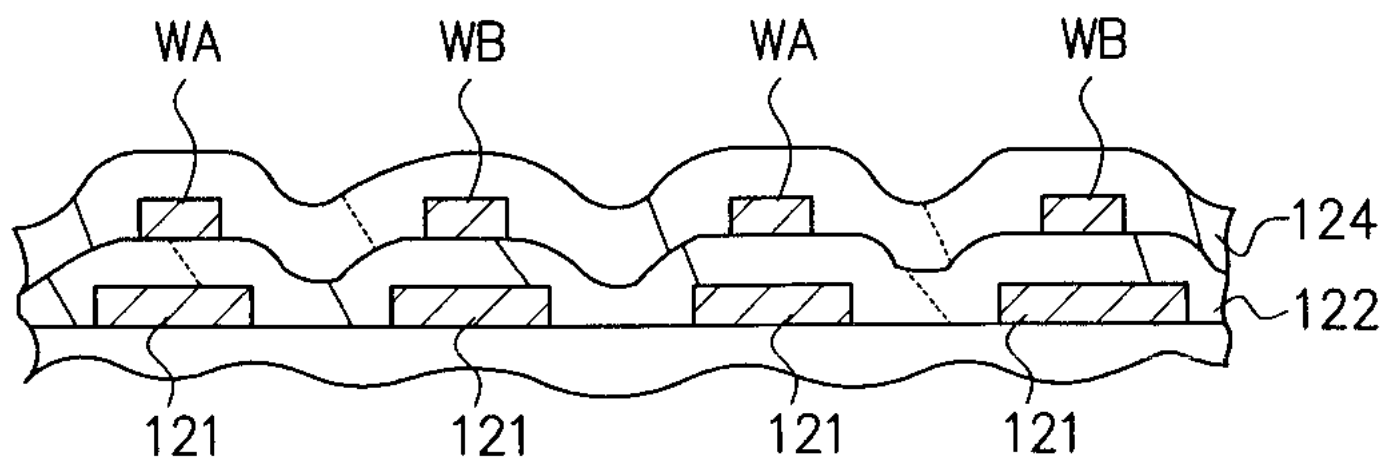
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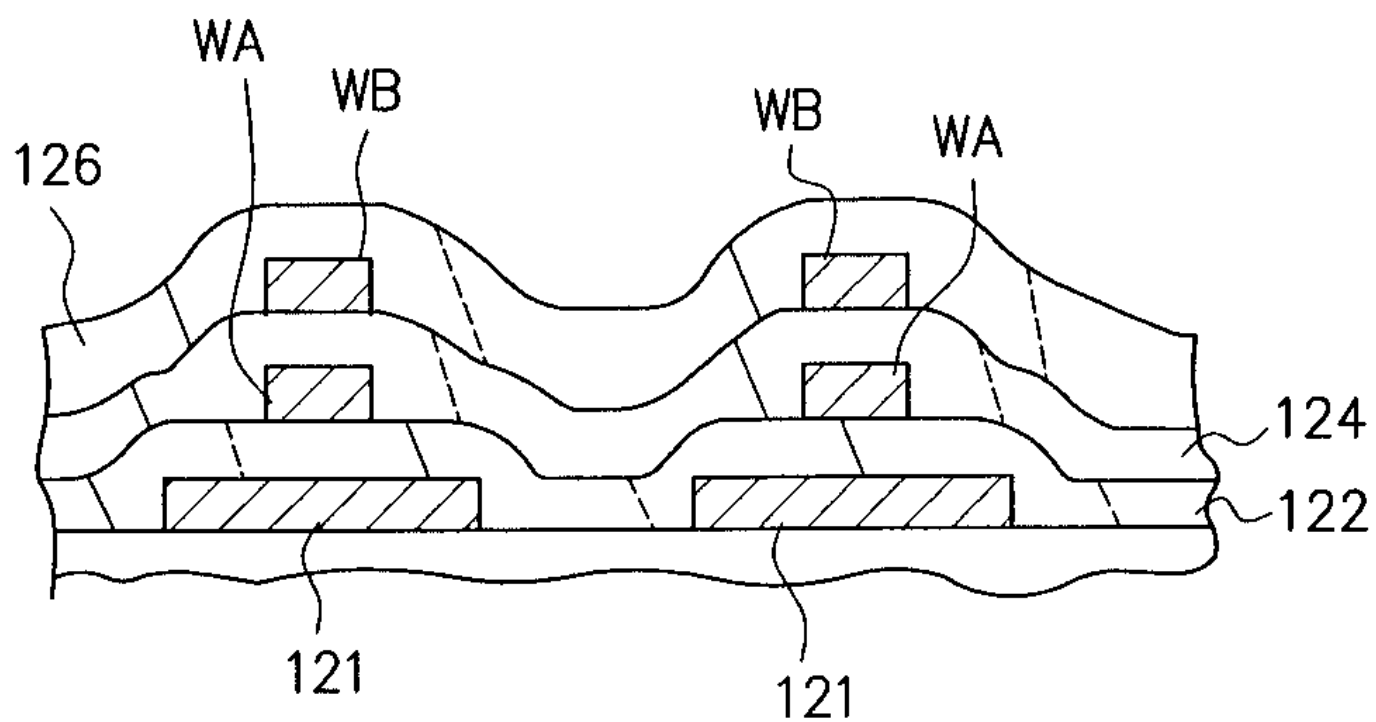
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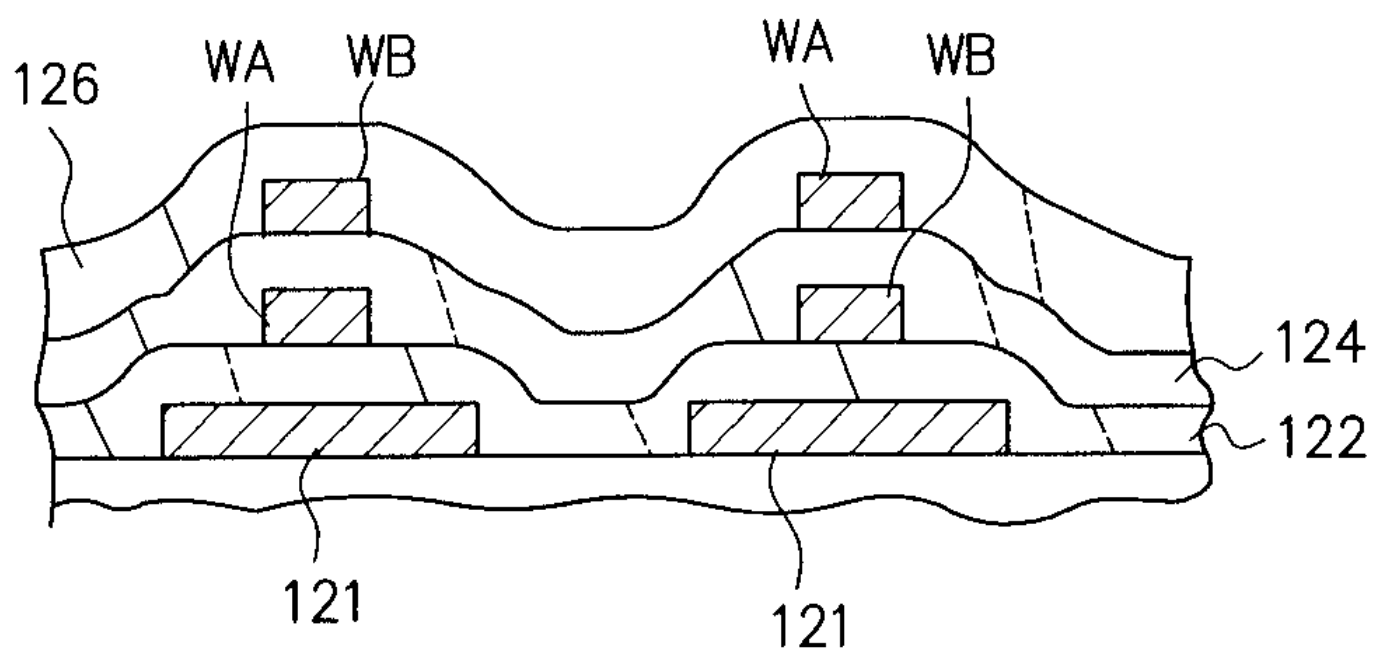
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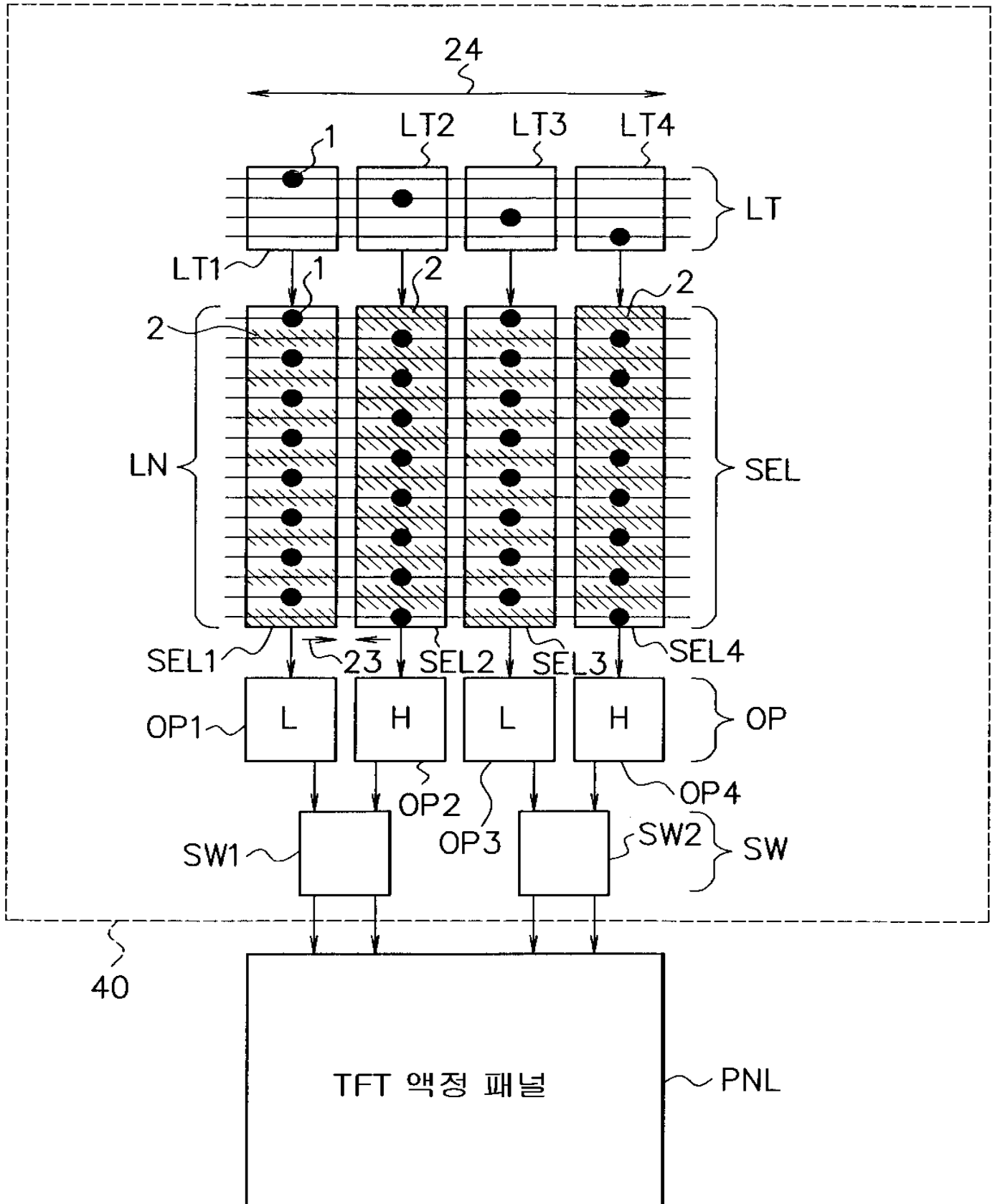
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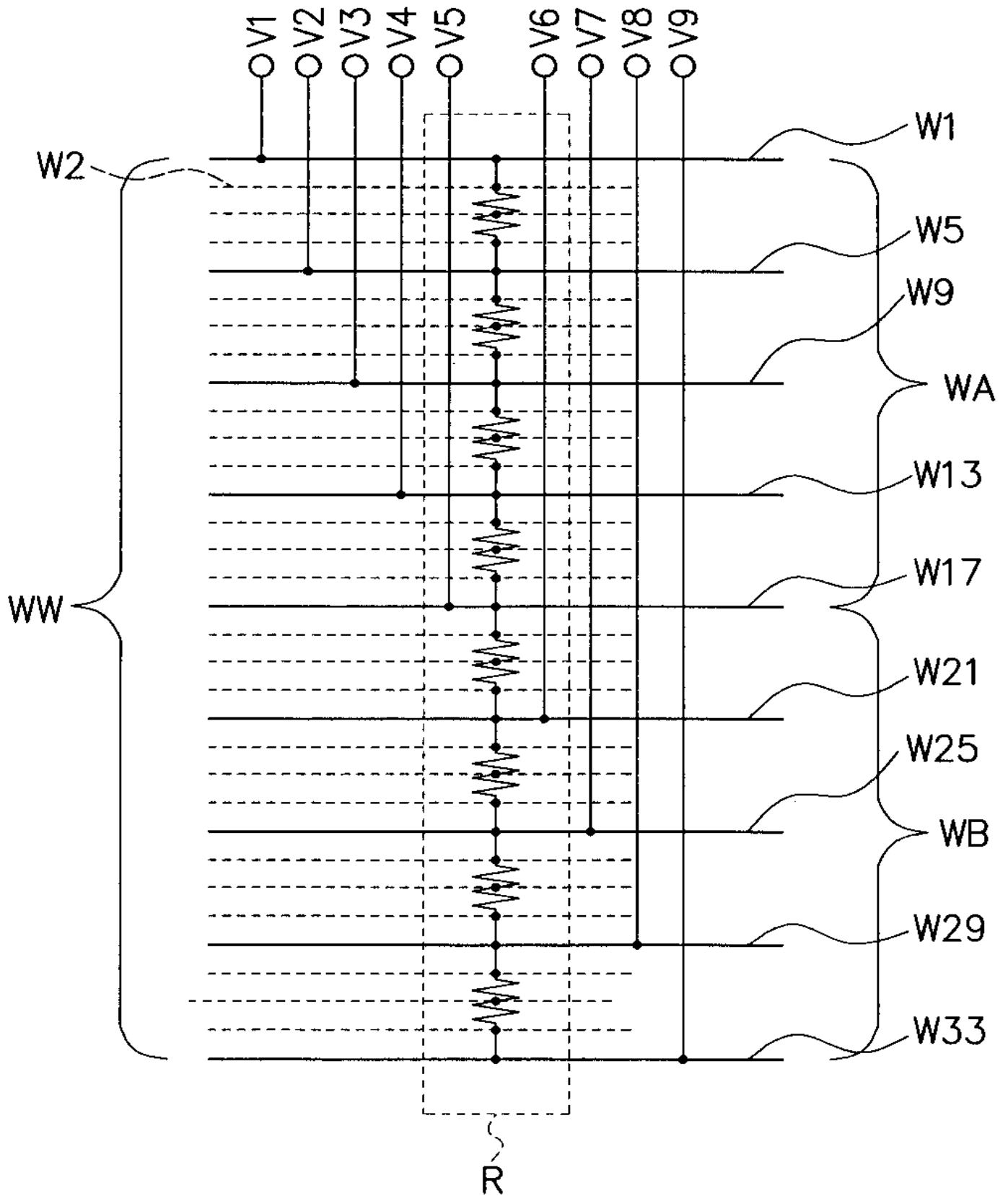
20c



(종래 기술)



(종래 기술)



专利名称(译)	用于驱动液晶面板的半导体集成电路		
公开(公告)号	KR1020010100763A	公开(公告)日	2001-11-14
申请号	KR1020010002343	申请日	2001-01-16
[标]申请(专利权)人(译)	富士通株式会社		
申请(专利权)人(译)	富士sikki有限公司		
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IPC分类号	G09G3/00 G09G3/20 G09G3/36 G09G5/00 G09G5/10		
CPC分类号	G09G3/006 G09G3/2011 G09G3/3614 G09G3/3688 G09G2300/0426 G09G2310/027 G09G2310/0297 Y10S345/904		
代理人(译)	金泰HONG		
优先权	2000105308 2000-04-06 JP 2000105317 2000-04-06 JP		
其他公开文献	KR100746933B1		
外部链接	Espacenet		

摘要(译)

根据本发明的实施例，为了选择双极灰度级的双极模拟灰度级电压，其中保持数字图像数据的数据锁存器的下端和双极灰度电压线的一组双极选择器设置在正上方，用于保持数字图像数据的数据锁存器的上端和设置在负极性灰度电压线正上方的负极性选择器被设置为一组。两组沿垂直方向排列。以这样的方式布置多组垂直布置的组，以缩短相对于灰度级电压线的水平长度。

1

