

(19) (KR)
(12) (A)

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(21) 10-2001-0071123
(22) 2001 11 15

(71) . 20

(72) 642-3

642-3

(74) :

(54)

가 . 가 n +

1 , , , 2
가 가 1 가
가 (strip)

5c

, , , ,

1 .

2 .

3 .

4

5

**

**

101,201 : 103,203 :

204 : 205 : LDD

206 : n⁺ 207 : p⁺

109,209 : 120,220 :

211 : / 213 :

215 :

가 가

(Active Matrix LDC device)
(Thin Film Transistor)

(gate bus line) (data bus line) (pixel) 가

2가 TFT TFT

가 (p-Si) TFT CMOS(Complimentary Metal Oxide Semiconductor) TFT CMOS

TFT TFT

1 TFT가 가 가 NMOS TFT가 A PMOS TFT가 B

A NMOS TFT LDD(Light Doped Drain) TFT ,
(1) (3) , (3) p-Si (, ;4
a,4b), n⁻ LDD (5a,5b) n⁺ (6a,6b) , (4a,4b), LDD (5a,5b) n⁺ (6a,6b)
(1) (9) , (9) (4a,4b)
(2a,2b) , (2a,2b) (1) (interlayer;13) ,
(13) (via hole) n⁺ (6a,6b) / (11a,11b) , T
FT가 (passivation;15) , (15)
가 (17) (contact hole) /
(11a)

PMOS TFT (1) (3) (3) (9) , (4c) p + (7) (4c) p + (7) (2c) (1) (2c) (11a,11b) , (1) PM OS TFT가 (13) , (15) .

TFT CMOS TFT TFT NMOS TFT LDD n + n + (P) n + 2 , .

가 MOS TFT MOS TFT NMOS TFT .

2(a) (1) LDD (3) A B (2b,2c) (9) (2b,2c) (4b,4c) , n - (2b,2c) LDD (5b,5c) (20) 2(b) LDD (5b) A LDD (5b) B (high dose) n + 가 (20) .

(20) 100 (soft baking) .

n + A LDD (5b) 가 n + (6b) , 2(c) LDD NMO S TFT가 , (/ B LDD (5c) p + PMOS TFT가 .

NMOS TFT NMOS TFT n + 가 , n + n + 가 (strip) 가 (A)가 TFT (20) .

가 n + 가 가 3 .

3(a) , LDD A B (4b,4c) LDD (5b,5c) (9) , 3(b) , (2b,2c) (9) .

(20) , LDD (5b) B A LDD (5b) n + B 가 n + (6b) LDD NMOS TFT가 .

(2b,2c) (9) 가 n + , n + .

(9) , n + 가
 , n + ()
 , (9) 가
 가 (9) (B) /

, 가
 (strip) 가

, 1
 , 1 , 2
 ,
 100 1 , 130 , 140 165 2
 가
 2
 ,
 ,
 , 1 , 2
 , /
 , 3 가 1 2
 ,
 LDD , LDD ,
 2 1 1 LDD 1
 , 1 2 LDD 1
 , 1 2 1
 2 LDD 2 2 2
 / , /

n + 가 가

가 . 가 .

(negative) (solvent), (sensitizer) . (cross-linki

ng) . 가 . , 가

가 . n +

4 4(a) 4(b)

(101) (104) (109) (120)

(109) (negative PR) (positive PR) 가

4(c) 100 (120)

(120) 2 2 1 1

50 155 140 165

(120) 4(d) 가 (104a)

4(e) (120) (106) (P) n +

B) p + 2 p + n +

가 n +

130 2 140 1

n + 가 n +

가 n +

p-Si TFT p-Si CMOS TFT

가 p-Si TFT p-Si CMOS TFT가

p-Si TFT p-Si CMOS TFT

5 NMOS TF

T가 CMOS TFT가 NMOS TFT가

A PMOS TFT가 B

5(a) (203) (203) (201) A SiO₂ B a-Si (204a,204b,204c) (204a,204b,204c) (Laser annealing) (p-Si layer) (Eximer Laser) (204a,204b,204c)

5(b) (209) (210) SiO₂ SiNx A B 1800 (209) (202a,202b,202c) (202a,202b,202c) (202a,202b,202c) AlNd/Mo (209) AlNd A Mo B 3000 500 (202a,202b,202c) LDD n⁻ (204a,204b,204c) LDD n⁻ (205a,205b,205c)

5(c) (201) (220) 1 (130) (220) (100) (220) A LDD (205a,205b) (220) B (220) 2 140 165 2 1 150 155 165 2 가 165 2 (220) 가 (220) 105 155 2 (220) 5(d) (220) n⁺ (206a,206b) A LDD n⁺ (205a,205b) (220) 5(e) (220) (130) PMOS TFT (220) 2 (220) p⁺ (207) p⁺ B LDD (205c) (220) p⁺ (207) 5(f) (209) (213) (via hole) (209) n⁺ (206a,206b) (213) SiNx 7000 (211a,211b,211c) AlNd/Mo (211a,211b,211c) 5(g) (211a) (201) ITO(Indium Tin Oxide) (215) (217)

(215) ,
SiNx
BCB(Benzocyclobutane)
(215) SiNx/BCB /

가 .
가 가
가 가
TFT TFT

150 155
가 가
가 가

가

(57)

1.

•
;

•
;

1 ;

2 ;

•
,

2.

3.

$$2 \quad , \quad n^+ \quad .$$

4.

1 ;

4 **5.** , 100 .

6. 1, 1 130.

7. $1^2 + 2^2 + 1^2 = 6$.

8. $7^2 = 49$, $2^2 = 4$, $140 = 14 \cdot 10$, $165 = 11 \cdot 15$.

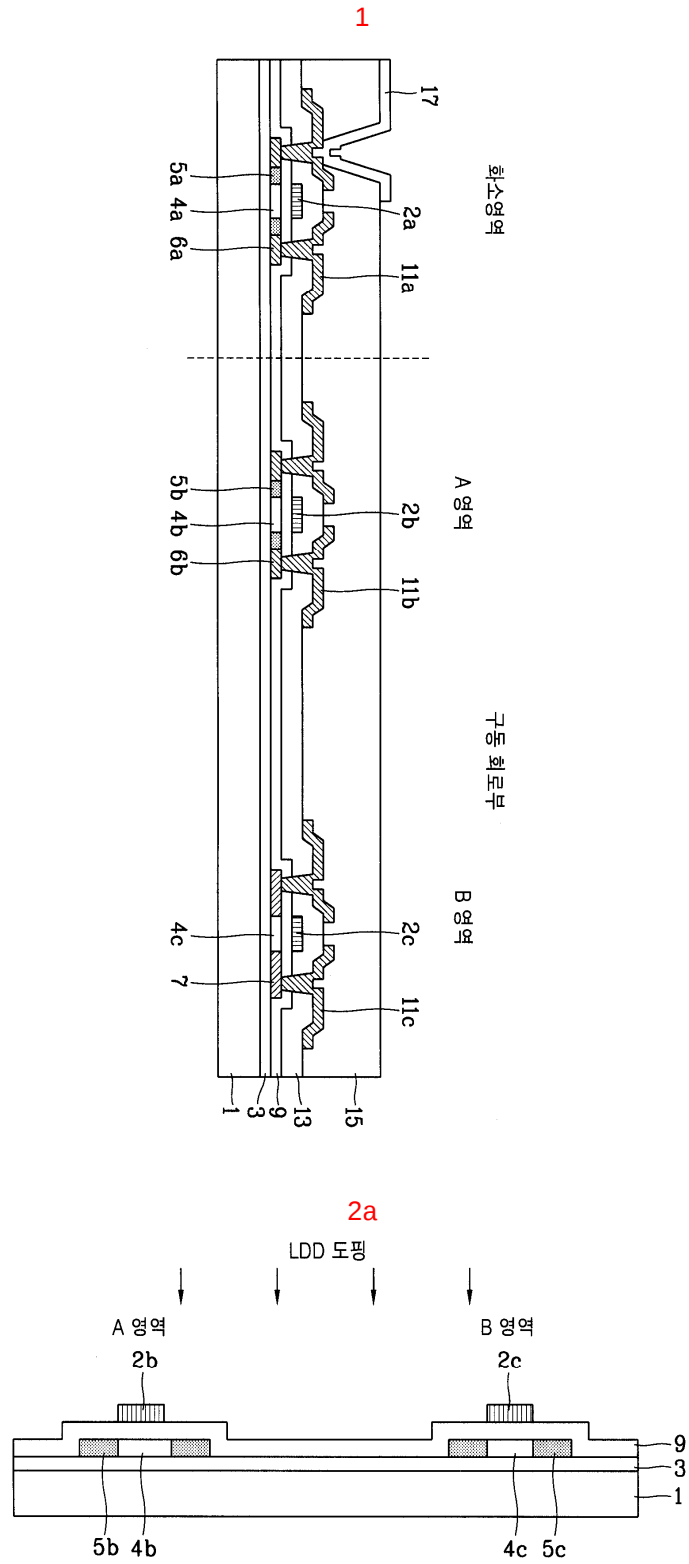
9. 8, 2 150 155 .

1 ;

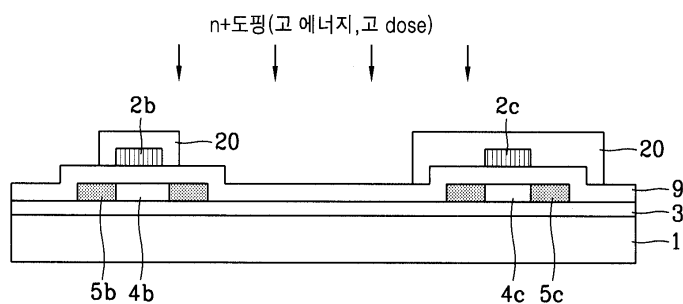
2 ;

[illegible]

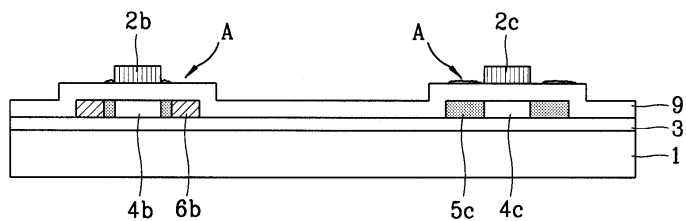
20. 19 , , .
21. 19 , 1 n+ .
22. 19 , 2 p+ .
23. 19 , 1 , ; ; ; ; .
24. 23 , 100 .
25. 19 , 1 130 .
26. 19 , 2 1 .
27. 26 , 2 140 165 .
28. 27 , 2 150 155 .
29. 19 , .
30. 19 , ; ; ; 가 .



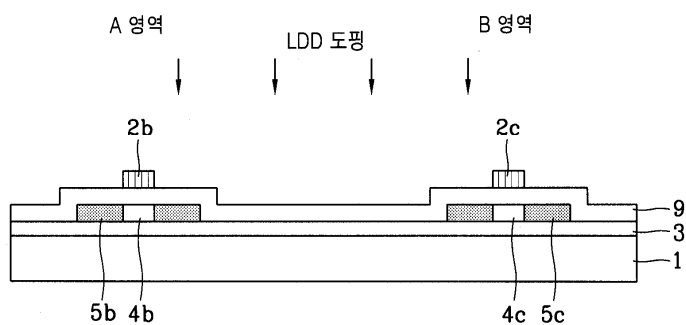
2b



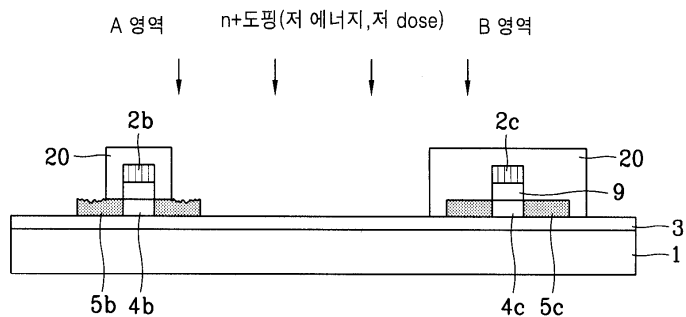
2c



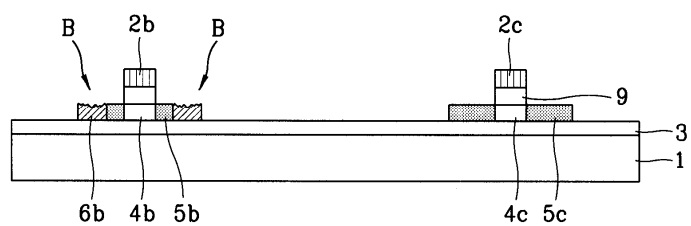
3a



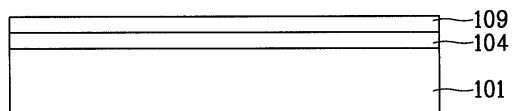
3b



3c

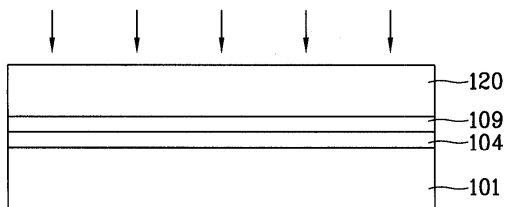


4a



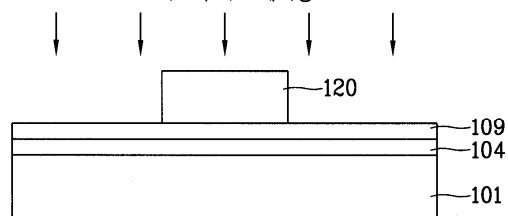
4b

소프트 베이킹 & UV노광



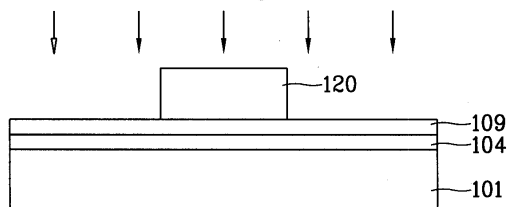
4c

제1 차 하드 베이킹
제2 차 하드 베이킹

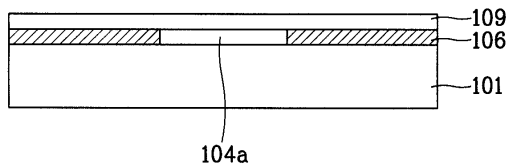


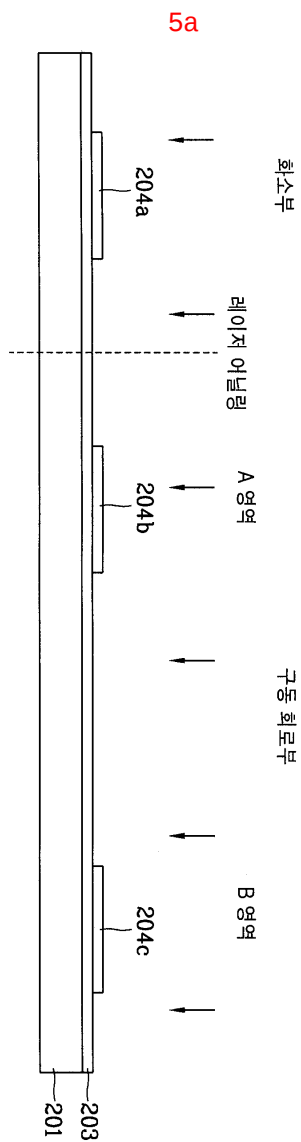
4d

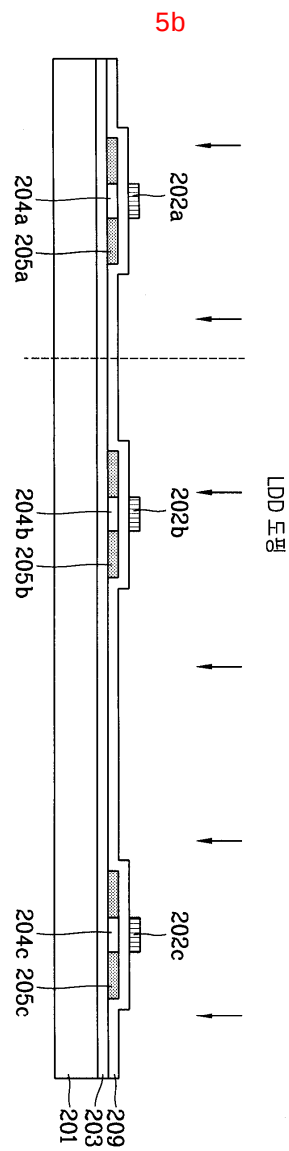
불순물 도핑

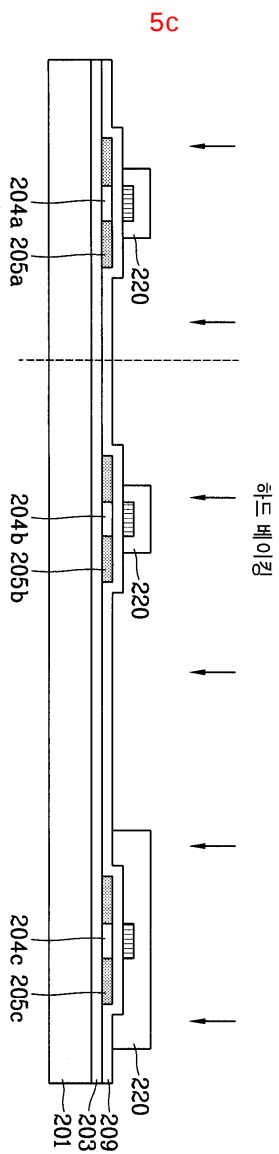


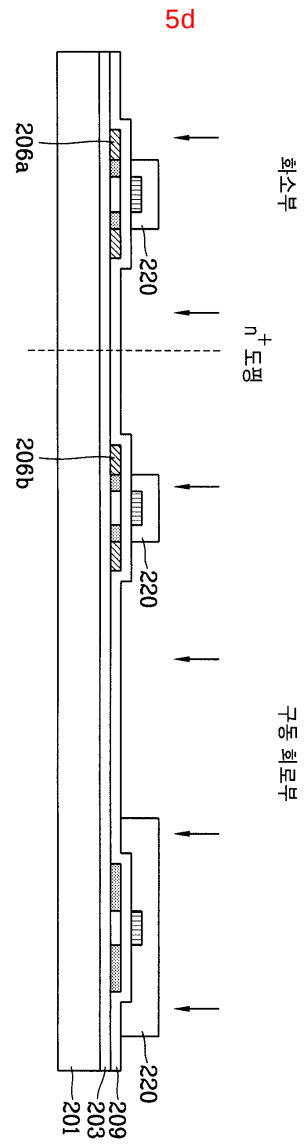
4e

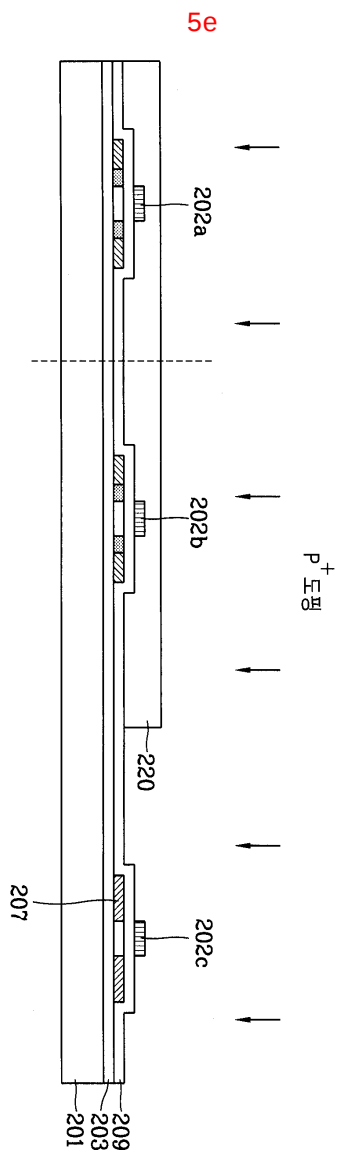


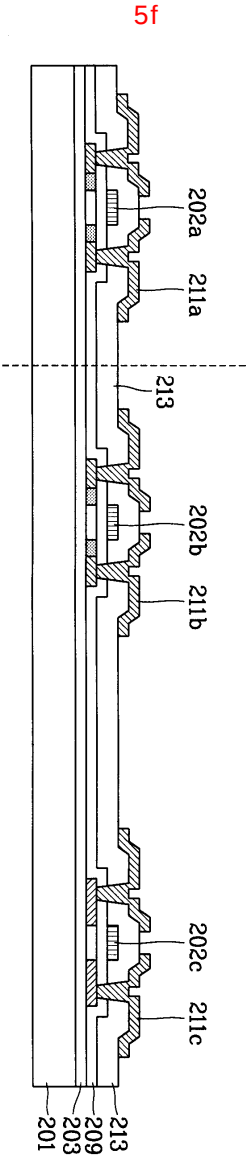


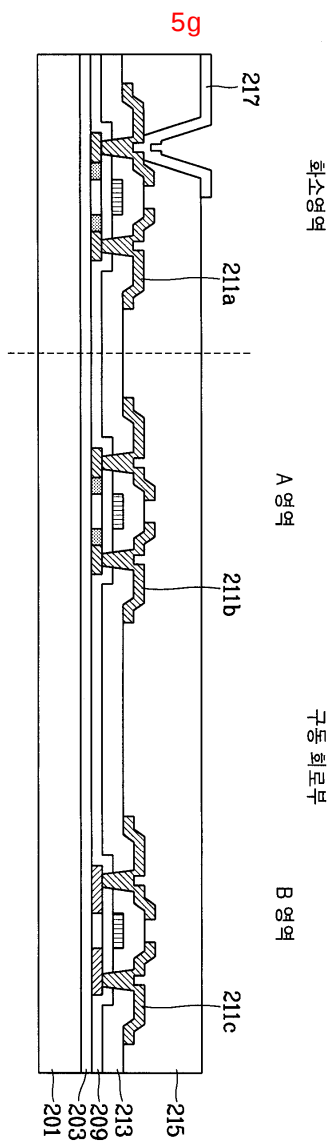












专利名称(译)	防止光致抗蚀剂残留缺陷的半导体掺杂方法和使用该方法制造液晶显示元件的方法		
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[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG显示器有限公司		
当前申请(专利权)人(译)	LG显示器有限公司		
[标]发明人	HWANG EUIHOON 황의훈 KIM KEEJONG 김기종		
发明人	황의훈 김기종		
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CPC分类号	H01L29/78621 H01L27/1288 H01L27/1214 H01L29/66757		
代理人(译)	PARK , JANG WON		
其他公开文献	KR100492727B1		
外部链接	Espacenet		

摘要(译)

本发明提供一种适用于多晶薄膜晶体管或液晶显示元件的半导体掺杂方法。当通过诸如光致抗蚀剂涂覆，软烘烤，曝光和显影的普通光致抗蚀剂工艺形成高速能量的n⁺掺杂时，光致抗蚀剂层阻挡未掺杂区域，然后进行第一次硬烘烤，在温度下的第二次硬烘烤再次增加了光致抗蚀剂的交联，以防止光致抗蚀剂的化学结构由于高速掺杂离子的渗透而改变。结果，可以在后续工艺中完全剥离光致抗蚀剂，从而防止有缺陷的光致抗蚀剂残留物被不完全地去除。图5c 指数方面 液晶显示元件，光刻胶，交联，硬烘烤，残留缺陷

