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10-2005-0006363
2005 01 17

(21) 10-2003-0046067
(22) 2003 07 08

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(72) 746 APT1007 311

1494-6 302

(74)
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(54) ,

4

1

2

3a 3b 2

4

5 4

6a	6b	5	.
7		2	.
8a	8b	7	.
9		3	.
10a	10b	9	.
11		4	.
12a	12b	11	.
13			가 .

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1, 110 : 2, 124 :

3, 126 : 4, 116 :

5 : 6 :

8, 15, 16, 17, 18, 41, 42 :

51, 55, 56, 71, 77, 78, 80, 81, 82, 83, 91, 97, 98, 99 :

9, 11, 13, 52, 72, 79, 92, 101 :

10, 12, 14, 53, 54, 73, 74, 89, 90, 93, 94 :

67, 68 : NMOS 40 :

43, 84, 100 : 34, 44, 70 :

36 : 38 :

57, 58, 75, 76, 95, 96 : PMOS

112 : 114 :

118 : 120 : Vcom

122 : DC-DC 128 :

130 : 132 : DAC +

134 : MUX

(GL1 GLn) 1 (4r) (2r) (2r) (DL1 DLm)
 (8r) (6r) (4r) (6r)
 (2r) (GL) (DL) (12r) (Clc) (Clc)
 (TFT) (TFT) (GL) (VGH) (TFT)
 (DL) (VGL) (Clc) (Clc)
 (GL) (Clc) 가 (TFT)
 (Clc) 가 (Clc) 가 (Clc) 가 (TFT)
 FT) (Clc) 가 가 가 (Clc) (TFT)
 (4r) (8r) (Gate Shift Pulse; GSP) (V
 (Gate Shift Clock; GSC) (GL1 GLm) (VGH)
 GH) 가 (4r) (VGL) (GL) (VGL)
 (6r) (8r) (Source Shift Pulse; SSP) (6r)
 (Source Shift Clock; SSC) (RGB) (SSC)
 Source Output Enable; SOE (6r) (RGB)
 (DL1 DLm) (POL) (6r)
 (8r) (4r) (GSP), (GSC)
 (SOE), (POL) (SSP), (SSC),
 (RGB) (Data Enable; DE) (8r) (Hsync), (Vsync),
 POL (Dot Clock; DCLK) (GSP, GSC, GOE, SSP, SSC, SOE,
 RC 가 (6r) RC (4r)
 RC 가 (OPAMP)가
 (Toshiba) 'AMLCD '02' PP21~24 2 3
 (3, 5, 7) 1 3 (3, 5, 7) 1 3 1 3 (2, 4, 6)

, 1 (2) 1 (1) , 1 3 (3, 5, 7) (11)
 . 3a 3b 2 4 (8, 9, 10) , 5
 , 1 3 (3, 5, 7) 2 4 (8, 9, 10) 3a (Short)
 1 (RESET) 3 (3, 5, 7) , 1 3 (3, 5, 7) (Vm)
 , (Vin) 1 (1)가 - 3a (Vm) (Vin)
 1 5 (2) (11)가 - (Vin) (3)가 (Vin) (Vout)
 7) (Vin) (OPAMP) 2 (Vm) 1 3 (3, 5, 3)
 (3, 5, 7) - (Stand-by) 가 3b 가 가 (Vin) 가
 (-80 μ W) 가 .
 ;
 ; 1 ;
 2 ;
 3
 - / - 가 .
 2 4 , 4 6 가 1 5
 , 2 4 6 가 .
 1, 2, 6 가 - , 3 5 -
 가 - 1, 2, 6 가 - , 3 5
 4 5 PMOS .

6 1 2 , 4

4 5 NMOS .

4 , 6
2 .

가 7 2 ; 2 1 2 8

1, 2, 6, 8 가 - , 3, 5, 7 -

5, 7 가 - 1, 2, 6, 8 가 - , 3

2

1 3 2 1 , 1

6 2 1 , 1

, 2 가 .

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2 가 ,

2 , 2 . 2

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4 13

4 5 4

4 (34) (Vin) (Vout) (36) (ISS)
 (40) (36) (40) - / -

(38)

(34) (42) (43) (41) - ,
 42 (36)

(40) - (Vout) (40) (42) - (41) - (36) (2)
 (Vout) (Vin) (38) (40) - (36) (36) (V

in)

(34) 5

5 (34) 4 (36) 1 (53) 1 (53)
 (52) (52) (51) 1 (53)
 (55) (34) (56)

1 5 (VDD) (34) 4 (38) 2 (54) (40)
 (57) (34) (41) 5 (57) (54) (34)
 (58) (57, 58) 5 PMOS

5 (42, 51, 55, 56, 58) (RESET) (42, 51, 55) (5
 6 58)

6, 58) - 6a (RESET) (42, 51, 55)가 - (5
 (Vm) (53) (Short) (53)
 (GND) (Vin) (V_L) (Vin) (V_L)
 (Vin) (Vin)
 (52) (Vin) (Vm) (51) (Vin)
 58) (57) (42) 2 (GND) V_L
)

(RESET) (42, 51, 55)가 - (56, 58) -
 (Vout) (53) (VDD) (57, 58) (36) (Vin) (Vin)
 (53) 6a (54) 1 (53) (Vn) 57 1
 (VDD) (53) 6a (Vout) (Vin)
 (Vn) 1 (53) (57) - (54) 1 (53)

PMOS 가 CMOS (96) (RESET)

(98)

12a (RESET) (91, 97, 99)가 (93)

96, 98) - 1 (93) (Short) 1 (93)

(Vm) 2 (GND) 2 (91)

(Vcom_in) (GND) (Vcom_in) (Vm)

(Vcom_in) (92) (95) (99)

2 (GND)

(RESET) (91, 97, 99)가 (96, 98)

(VDD) (95, 96)

(Vcom_out) (Vcom_in) 1 (93) 12a

D) 2 (94) 1 (93) (Vcom_out) (95)가 1 (VD

(Vcom_in)

1 (93) (94) 1 (93)

(95)

(Vcom_in) (Vcom_out)

(34)가 (Vin) (Vcom_out) 12b 5 0.

7 μ W

13 가 13

(110) (136)

13 (136) ,

(124, 126) (124) , (126) ,

(116) , (112)

(118) , (136) (114) , (126)

DC-DC (122) (120) ,

(126) (128) ,

(116) (130) , (130)

(118) (132) , DAC (132)

(, MUX)(134)

가 (126) DAC (132) , (Vcom) (120)

, 2 1 2

가,

가

(57)

1.

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2.

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1 ;

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3

3.

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가

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4.

3 ,

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5.

3 ,

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6.

4 ,

4

5

가

7.

6 ,

2 6 가

7 8.

1, 2, 6 가 - , 3 5 -

8 9.

가 - 1, 2, 6 가 - , 3 5

6 10.

4 5 PMOS

10 11.

6 1 2 , 4

6 12.

4 5 NMOS

12 13.

4 2 , 6

7 14.

2 ;
1 2 7 ;
2 2 8 가

14 15.

1, 2, 6, 8 가 - , 3, 5, 7 -

15 16.

5, 7 가 -

1, 2, 6, 8 가 - , 3

17.

16 ,
2

18.

9 ,
1 3

1 ,

1 2

19.

18 ,
6

1 ,

1 2

20.

4 ,
2 가

21.

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가 1 20

22.

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23.

22 ,

가

22 24.

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가

24 25.

가

24 26.

24 27.

2

가

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2

2

28.

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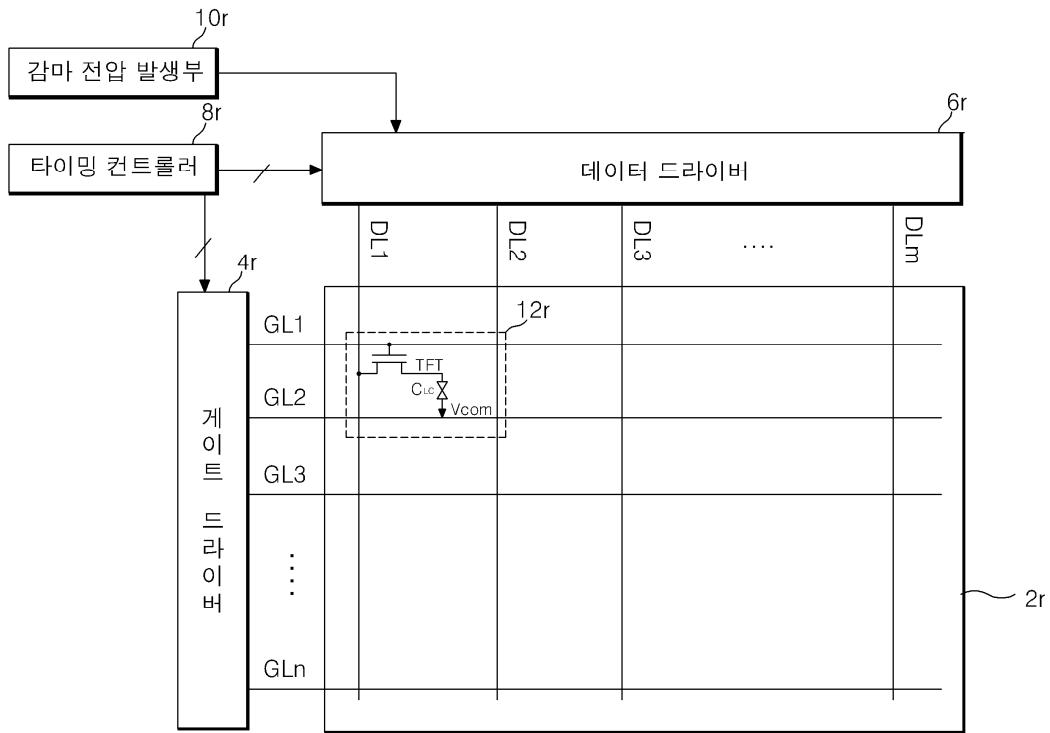
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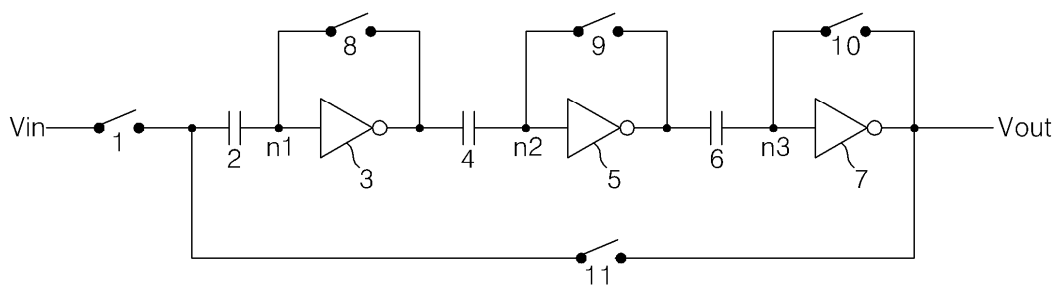
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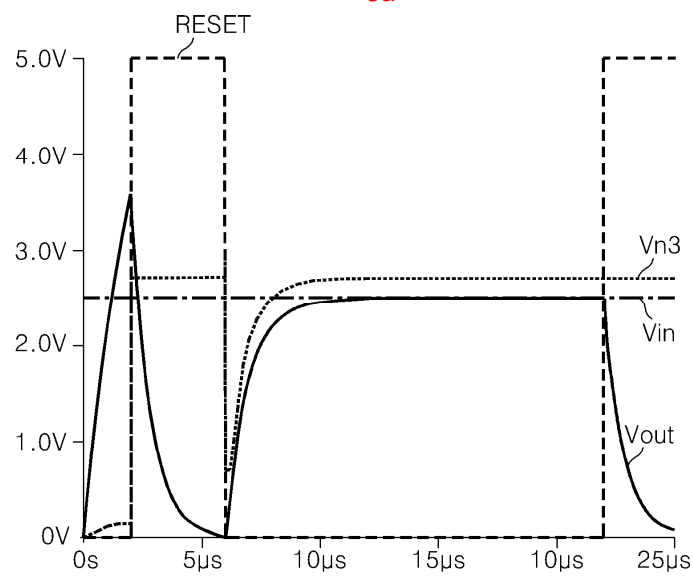
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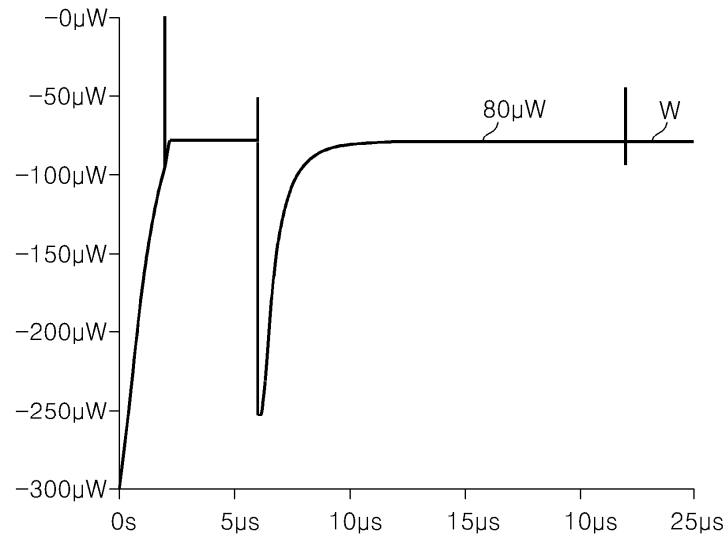
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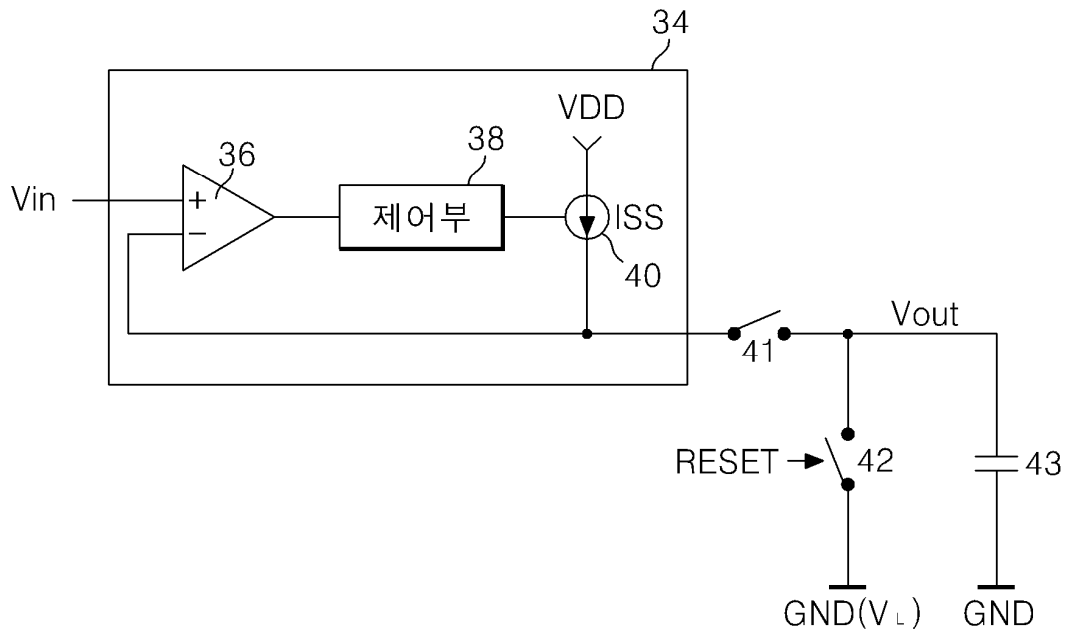
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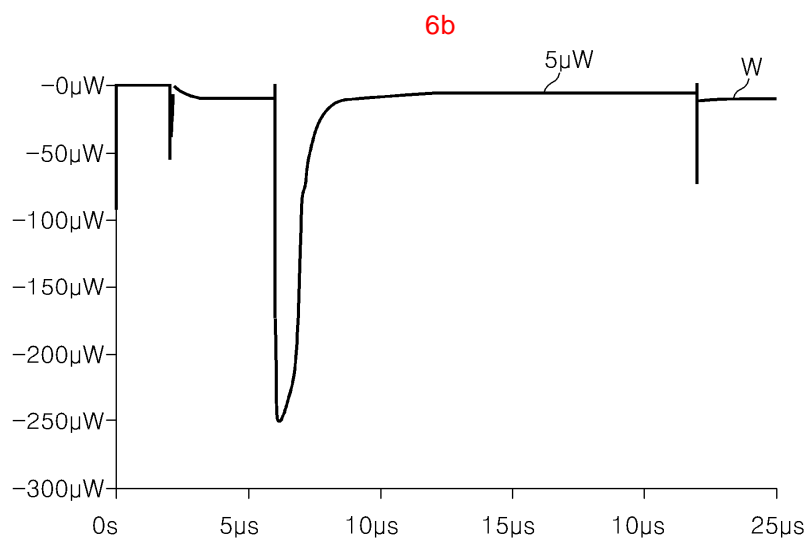
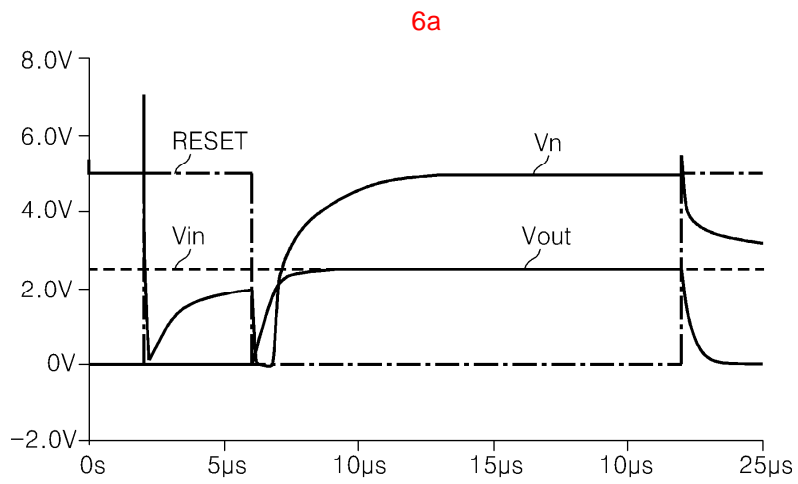
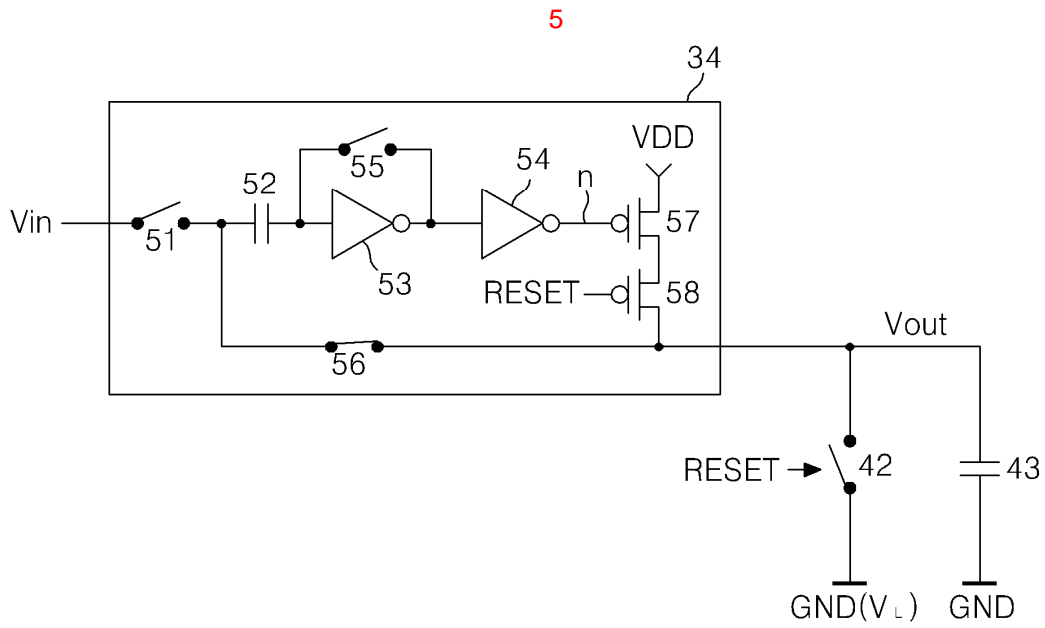


3b

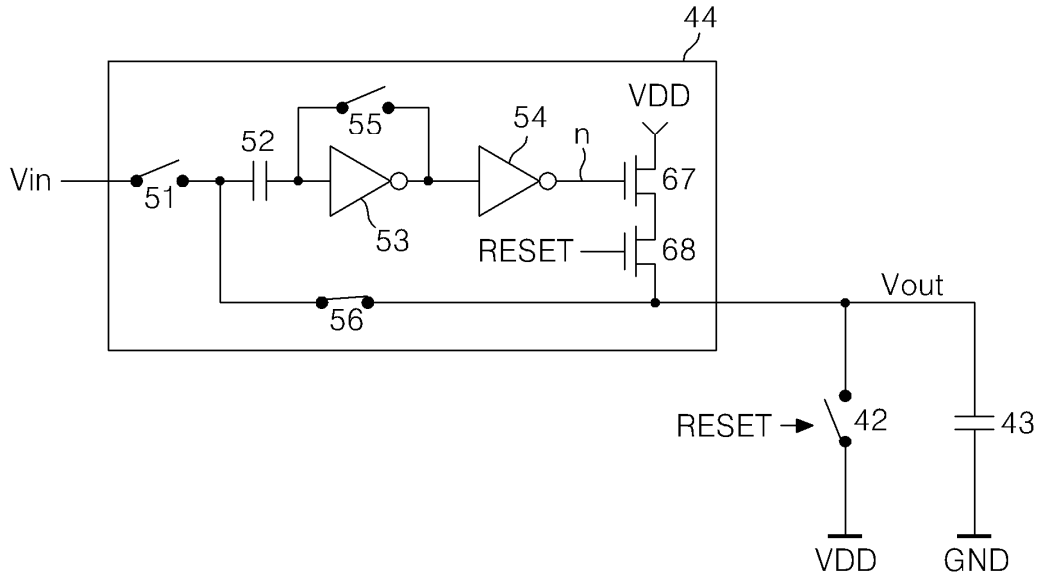


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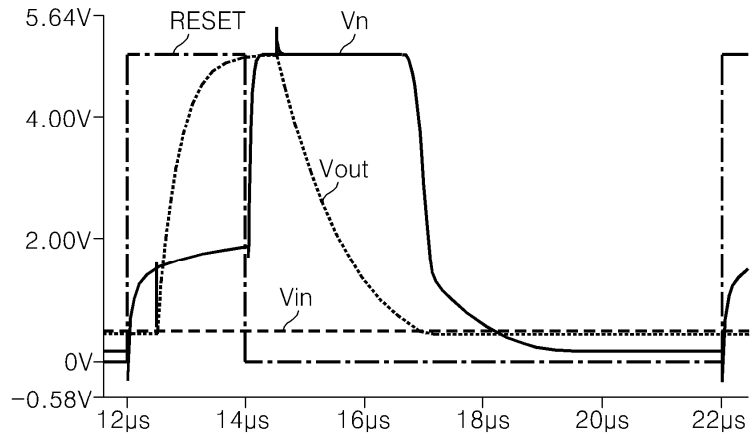




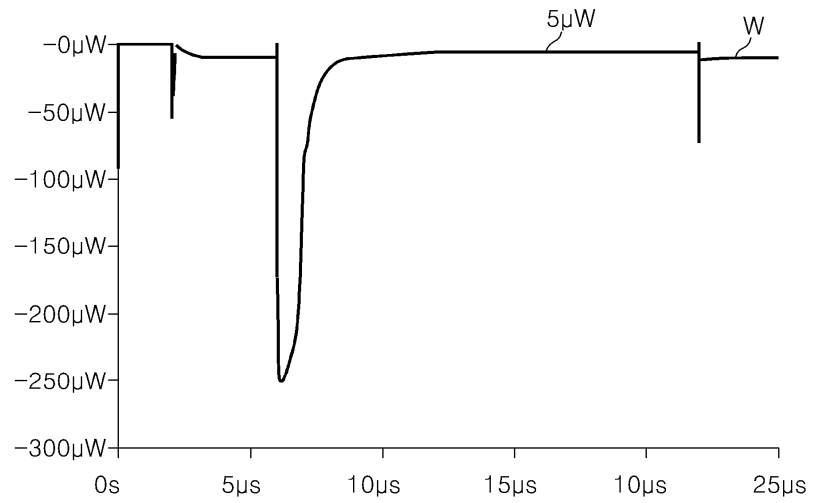
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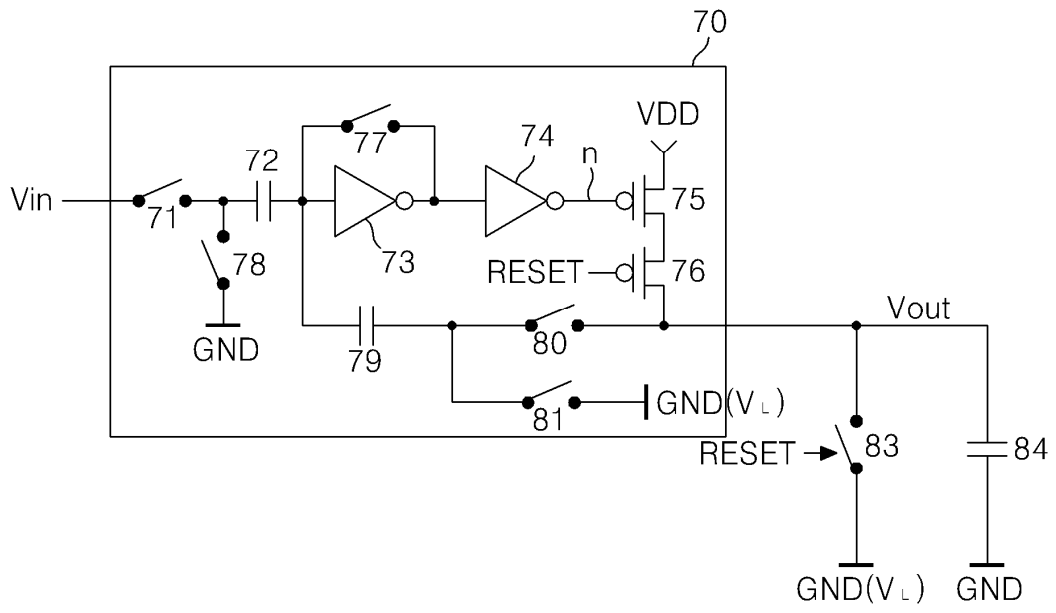
8a



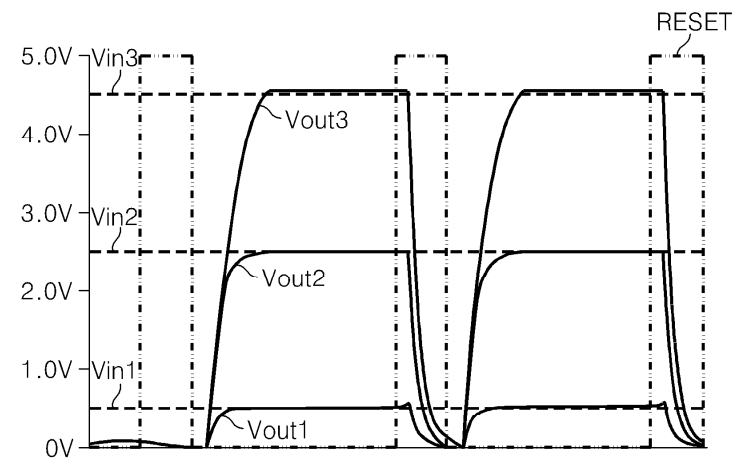
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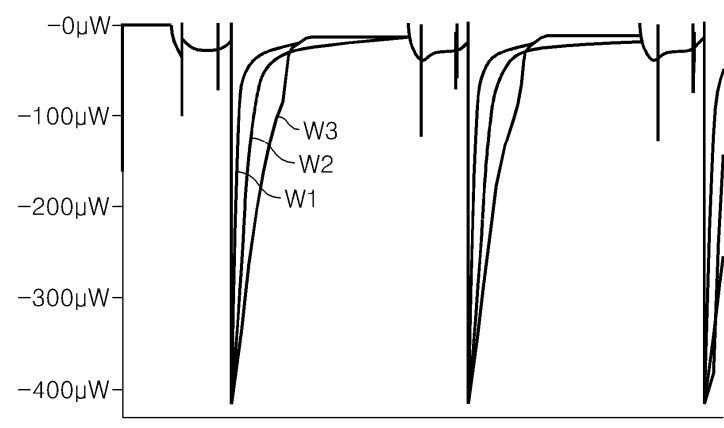
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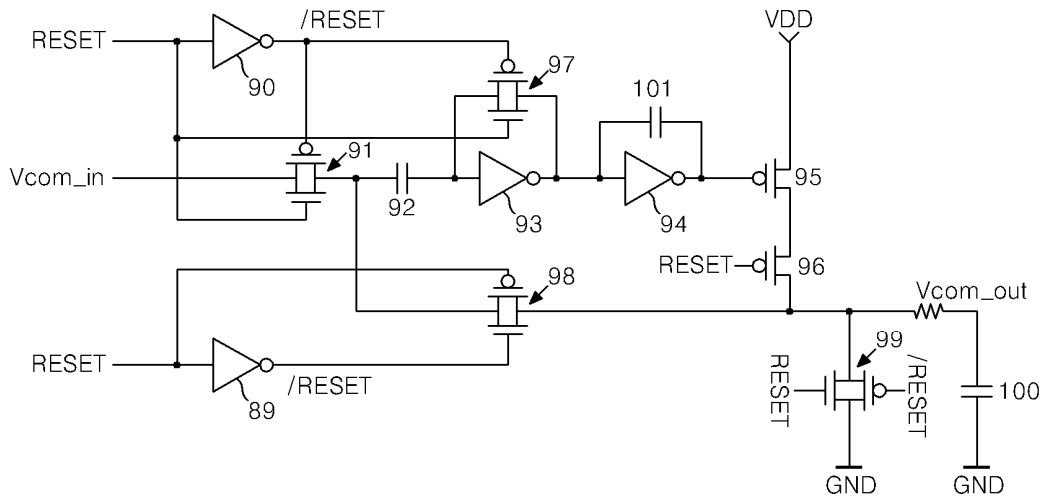
10a



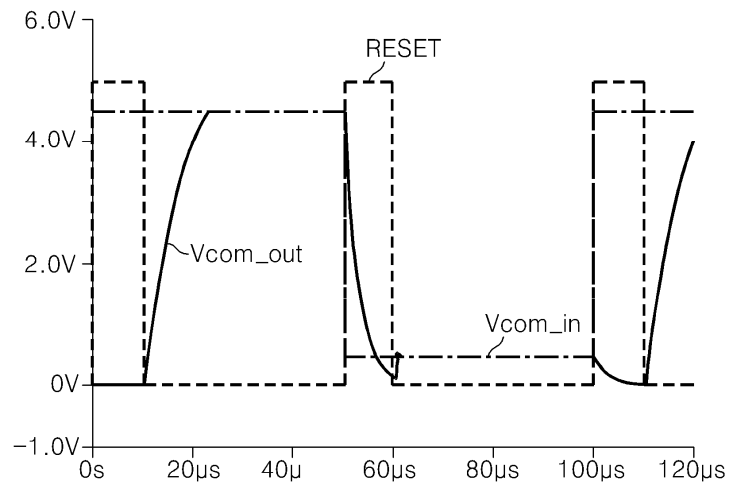
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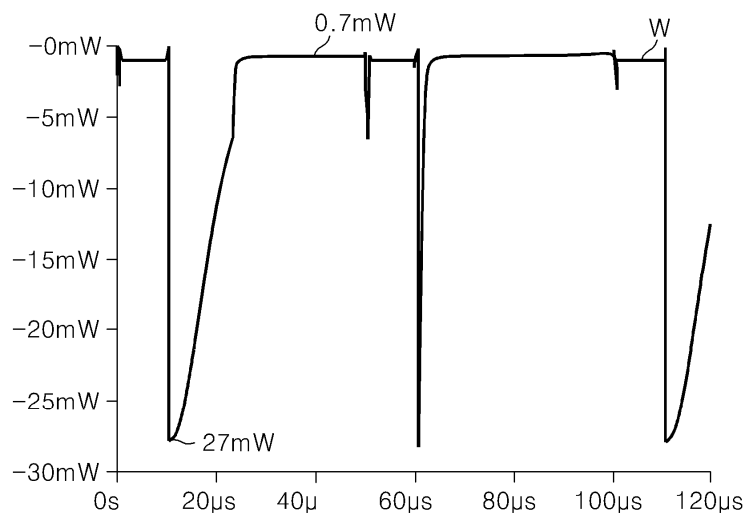
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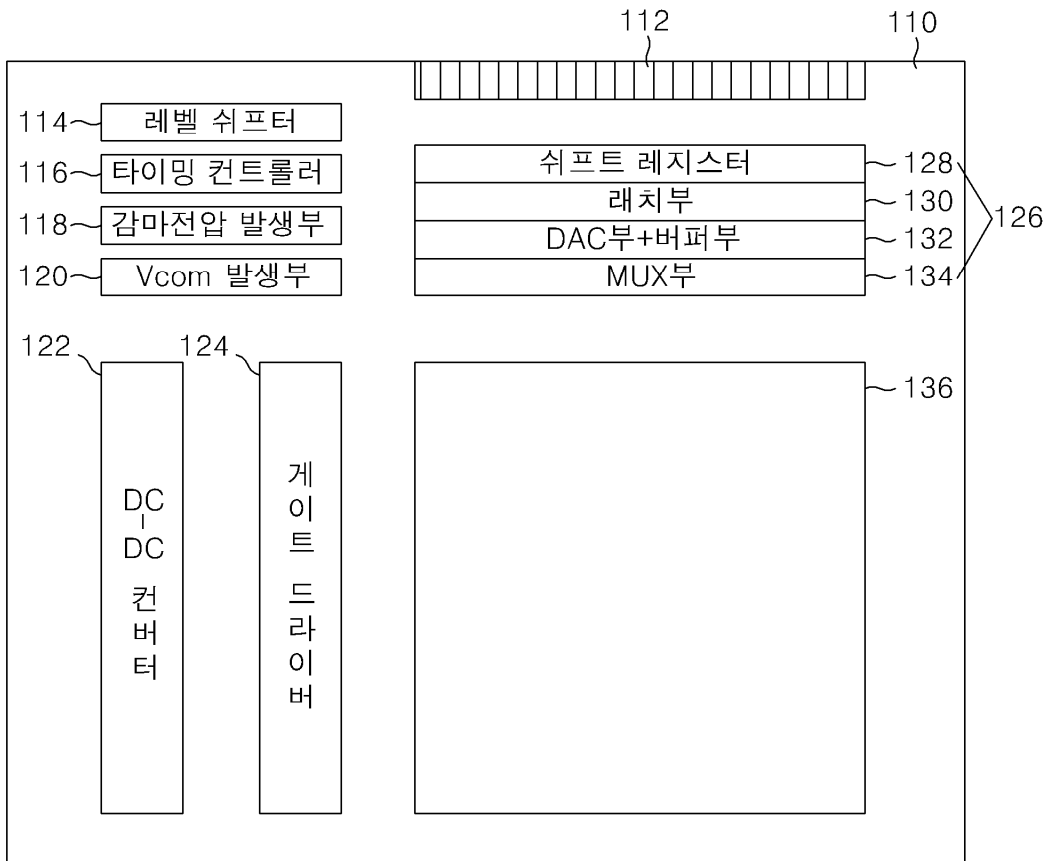
12a



12b



13



专利名称(译)	模拟缓冲器及其驱动方法，使用其的液晶显示器及其驱动方法		
公开(公告)号	KR1020050006363A	公开(公告)日	2005-01-17
申请号	KR1020030046067	申请日	2003-07-08
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG显示器有限公司		
当前申请(专利权)人(译)	LG显示器有限公司		
[标]发明人	KIM KIJONG 김기종 YOO JUHNSUK 유준석		
发明人	김기종 유준석		
IPC分类号	G09G3/36		
CPC分类号	G09G2310/027 G09G3/3655 G09G3/3688		
代理人(译)	KIM , YOUNG HO		
其他公开文献	KR100637060B1		
外部链接	Espacenet		

摘要(译)

模拟缓冲器，其驱动方法和液晶显示装置及其驱动方法技术领域本发明涉及一种模拟缓冲器，其驱动方法，以及液晶显示装置及其驱动方法，其可以在简化的同 根据本发明的模拟缓冲器将输入电压缓冲到输出线，包括：恒流源，用于利用恒定电流源对输出线充电;并且比较器用于将反馈的输出线上的电压与输入电压进行比较，并且当对应于输入电压的电压被缓冲在输出线上时关闭恒定电流源。 4

