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(43)2002 - 0013714
2002 02 21(21) 10 - 2001 - 0045113
(22) 2001 07 26

(30) JP - P - 2000 - 00231392 2000 07 27 (JP)

(71) 가 가
가
가 4 6

(72) 1 5 - 1 가 가

1 5 - 1 가 가

1 5 - 1 가 가

1 5 - 1 가 가

가 가 292 가

(74)

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(54)

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22, 24 :

23, 25 :

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27 :

28 :

29 - 1 29 - 8 :

, 11 - 337909
, 가 가

, 11 - 337909 (scene)
가

,
가 DVD , OA
가 ,

$$2^N(N)$$
 2^N 2^N

가

가

가

1

1

20

1
638400

(1)

(100)

$$, 1280 \times \text{RGB} \times 1024 \quad (100)$$

RGB 256 , 1

, (2) (3) (4)
 , (5) (6) (7-1 7-8) 256 ,
 480 (7-1 7-8) 8 (8)
 (17), (18) (9)
 (10) $1280 \times \text{RGB} \times 1024$.

(11) (12) (13)
 (14) (15) (13)
 13 (16)
 (15) 256 (19)
 (20) (22) (20)
 (21) (5) (24) (22)
 (23) (4) (26)
 (24) (25) (19) (16)
 (28) (26) (27)
 (29-1 29-8) $1280 \times \text{RGB} \times 1024$ (10)
 (30) .

2, 3 , 4
 , 5 , 6, 7, 8
 9 , 10 , 11
 , 12 , 13 1
 8 , 19, 20 .

2 가 ,
 3 .
 , 1 (1)
 (100) , (7-1 7-8),
 (9) (1) 2^N (N , RGB 256)
 , RGB N (8) 2
 (7-1 7-8) (2) RGB 2
 1, 4 (2) (5)
 가 (1)가 (3) , 1
 (7-1)가 (7-1) RGB 2
 , 80 480 (7-1) (自段)
 (7-2) (31-1)
 1 (7-2)가 (7-3 7-8)
 A22 .

A22 1 (4)
 B24 , (19) (16) (26)
 (28) (29-1 29-8) 1 .

3 , (9) (1) FLM CL
 1 CL3 1024 1024 2 , 3 FLM
 1 1024
 (7 - 1 7 - 8) (10) (29)
 - 1 29 - 8)

(16) (8) (17)
 V0 V8 9 , (18) V9 V17 9 (15)
 2^N (256) , 2^N (256) 5, 6, 7, 8 ((202 - 1,
 15) (201 - 1, 201 - 2) (17, 18) (202 - 1,
 202 - 2) VS0 VS255 256 (203 - 1, 203 - 2) (202 - 1, 202 - 2)
 (204 - 1, 204 - 2) (205 - 1, 20
 5 - 2) (204 - 1, 204 - 2) 256 (VG0 VG 255)
 (16)

(17), (18) (201 - 1, 201 - 2)
 VS0 VS31 32 , 6 V0 V1 32
 VS63 32 , V1 V2 가 32 VS32
 , VS0 VS255 256 . V2 V8 가
 V17) 가 (202 - 1) (18: V9
 (203 - 1, 203 - 2) (201 - 2) 256 (202 - 2)
 (205 - 1, 205 - 2)

6 (205) V1B V7B
 VG0 VG31 32 V0 (203) V1B 32
 VG32 VG63 32 (203) V1B V2B
 32 가 , V2B V7B VG64 VG223
 VG224 VG255 32 (203) V1B
 V8 32 (205 - 2) 가 VG0
 VG255 (203 - 1, 203 - 2) (14) (20
 4 - 1, 204 - 2)

6 (206) V1B V7B
 (205) , VS0, VS1 VG63 64
 1 , V2B VS0, VS2 VG126
 64 1 가 , V3B VS32, VS34
 VG158 64 1 , V4B VS64,
 VS66 VG190 64 1 , V5B
 VS98, VS100 VG224 64 1 V6B
 VS129, VS131 VG255 64 1 V
 7B VS192, VS193 VG255 64 1

, 6 (207, 208) , V0, V8 , 7, 8
 7 (205) VG8, VG16, VG24, VG40, VG48, VG56
 B1 B6 , (14) 가 V0
 8 가 (205) VG200, VG208, VG216, VG232, VG240, VG
 48 W6 W1 , (14) 가 V
 8 (207, 208) (205) V0 ,
 V8 .

36 (1) 9 (13) 48
 10 9 6 10
 , NO.1 NO.9 B1 B6, W1 W6 , V1B V7B NO.10
 10 RGB 8 2 RO[7:0], RE[7
 :0], GO[7:0], GE[7:0], BO[7:0], BE[7:0] 48 , RO [5:0], RE [5:0], GO[5:0], GE[5:0], BO[5:0], B
 E[5:0] 36 0 5 5 , 9
 0 4 , P0 P4
 , RS
 2 .

11
 , 12 ,
 (4)
 가 가 , 가 가 ,
 , 11 0 4 30 9
 , 5 P0 P4 RS

가 ,
 , 13 18 .
 13 . 32 0 255
 , 32 255 0 31 가 , 0 31
 , 14 32 0 255 224 255
 가 , 224 255 , 0 223
 , 가 .
 , 15 32 0 255 0 31 224
 255 가 , 0 31 224 255 , 32
 223 , 가 .

18 , 32 0 255
가 , 32 63 32 63
, 128 159 , 128 1
59 . ,
가
, 가 ,
, (1)
NO.3 NO.9 V1B V7B ,
, 19, 20 . 19
(301) , (100) (2),
(3), (4), (19) (302)
(100) (,),
(303) (303)
(304) (7 - 1 7 - 8)
(306) (306) (305) 12
(308) (307)
, 1
(16) (8) (17, 18) (13) 256
(13) (8) (17, 18)
20 ,
(401) , (100) 20
(3), (4), (19) (400) (2),
(,),
(402) (1) (1)
(403) (400) (402)
(404) (7 - 1 7 - 8)
406) (406) (405) 12 (408) (

(407)

, 256 5 가 , 9 , , 가
 V1B V7B 32 , , 16 가
 , 2 9 18, 21 29 .
 2 , 64 FRC 2^N (256)
 1 .
 21 , 1280 × RGB × 1024 FRC
 RGB 256 , 1638400 (100)
 , (101) (100)
 , (102) , (103) ,
 (104) (105) (106) ,
 (107 - 1 107 - 8) 64 , 480 , (107 - 1 107 - 8) 8
 (108) (131),
 (132), (141), (142) , (109)
 , (110) 1280 × RGB × 1024 , (111)
 , (112) (113) , (114)
 (115) (116) (15)
 64 (119) (133)
 (131), (132) (119) , (143)
 (141), (142) (119) , (120)
 , (122) (120) (121) (105)
 , (124) (122) (123)
 (104) , (126) (124)
 (125) (116) , (128)
 (126) (127)
 (129 - 1 129 - 8) 1280 × RGB × 1024 (110) , (130)

22, 23 , 24
 , 25 , 26, 27, 28
 . 29 .

22 , , 가
 , 23
 (Vcom) .

, 21 (101)
 RGB 8 256 , 1638400 (100) ,

(107 - 1 107 - 8) (109) (101)
 (7 - 1 7 - 8)가 64 , RGB 8 FRC 6
 256 . FRC 가 ,
 (101) 0 63 3 ,
 62 63 FRC FRC 6 , 256
 , (101) RGB 6 2 36
 , (107 - 1 107 - 8) (102) RGB 2
 .
 21, 24 (102)
 (105) 가 (101)가 (103)
 , 1 (107 - 1)가 . (107 - 1) RGB 2
 , 80 480 . (107 - 1)
 , (107 - 2)가 (107 - 2) (134 - 1)
 , 1 . (107 - 3 107 - 8)
 A122 .
 , A122 1 (104)
 B124 , (125) (116) (126)
 , (128) (129 - 1 129 - 8) 1 .
 , (109) (101) FLM
 CL3 1 , CL3 1024 1024 2 , 3 FLM
 . CL3 1024 1024 , 1024 (110)
 , 1 (107 - 1 107 - 8) (129 - 1 129 - 8)
 (129 - 1 129 - 8)
 , (116) (108) (131)
 (132) (133) (119) , (117) V0 V8
 9 (115) .
 , (143) 23 가
 가 , (119) (110) .
 (115) (117) V0 V8 9 64 (16) ,
 (117) , 가
 .
 25, 26, 27, 28 (115) , (501) ,
 (502) VS0 VS63 64 . (503)
 (502) , (504) , (505)

(504) 64 (VG0 VG63) (116)

, V0 V1 8 VS0 VS7 8 (501) 26
 가 8 VS8 VS15 8 (502) , V1 V2
 가 , VS0 VS63 64 . V2 V8
 (503) (505) (502) (502)

26 (505) V1B V7B
 VG0 VG7 8 V0 (503) V1B 8
 VG8 VG15 8 (503) V1B V2B
 8 가 , V2B V7B VG16 VG55
 VG56 VG63 8 (503) (503) V1B V8
 8 (503) (114) (504)
 V1B V7B 26 (506)
 VS0, VS1 VG31 32 1 (505) V1B
 V2B V3B VS0, VS1 VG31 32 1 가 ,
 V4B VS8, VS9 VG39 32 1
 V5B VS16, VS17 VG47 32 1
 V6B VS25, VS26 VG56 32 1
 V7B VS32, VS33 VG63 32 1
 VS32, VS33 VG63 32 1

, 26 (507, 508) , V0, V8 , 27, 28
 27 (505) VG2, VG4, VG6, VG10, VG12, V
 G14 B1 B6 (114) 가
 V0 28 가 (505) VG50, VG52, VG54, VG58, VG60, V
 G62 W6 W1 (114) 가
 V8 (507, 508) (505) V0
 V8

, 2
 9 12 (113) 36
 (101) 9
 10 , NO.1 NO.9 B1 B6, W1 W6 , V1B V7B 6 10
 O.10 N

10 RGB 8 2 RO[7:0], RE [7:0], GO[7:0], GE[7:0], BO[7:0]
], BE[7:0] 48 , RO[5:0], RE[5:0], GO [5:0], GE[5:0], BO[5:0], BE[5:0] 36 0
 5 , 2 NO.3 NO.9 V1B V7B 32
 가 , D4 D0 5 가 , D5 가 , 5 ,
 9 0 4 , P0 P4
 , RS .
 2 .
 , 2 11, 12 1
 .
 , 가 ,
 , 13 18 . 2
 1 가 .
 13, 14, 15 1 가 가 ,
 가 , 가 ,
 , (101) ,
 NO.1, NO.2 B1 B6, W1 W6 8
 V0(VG0), V8(VG63) .
 , 16, 17 (101) 가 1 가 DVD , OA
 , V1B V7B NO.3 NO.9
 .
 , 18 (101) 1 가 NO.3 NO.9
 V1B V7B ,
 .
 , 29 . 29
 , 29 (601)
 (100) (102), (103),
 (104), (119) , (601) RGB 8 FRC
 RGB 6 (602) , (100)
 (,), ,
 (603) 가 (600) 가 가
 가 (603) (602)

, (600) (609)
 , (604) (107 - 1 107 - 8)
 (606) (606) (605) 12 (60
 8) (607) , . , ,
 , .
 , 64 (FRC 256) 9 , ,
 , 5 가 , ,
 V1B V7B 32 , , 16
 가
 , 3 9 18, 30 36 . 3
 2 , 64 1,
 30 , $160 \times \text{RGB} \times 240$ RGB 64 , 262
 144 (701) CPU, (7
 02) , (703) , (704)
 , $160 \times \text{RGB} = 480$, 240 (705)
 (731), (732, 733) , (706)
 (707) (708, 709) (702) (706)
 704) (755) CPU(701) (744)
 (736) , (710)
 , (711) (710)
 (712), (714), (713)
 , (716) (717) , (718)
 , (719) (720) , (723)
 (721) (755) (725) (718)
 (715) (744) (726) (727)
 (728) (714) (729) , (73
 0) (706) (736)
 (738) (737) , (739)
 , (740) (744)
 (741) , (742) (744) /
 I/O , (745) (746)
 (747) (744) , (748) 1
 , (749) , (750) (739)
 (749) , (752)
 (750) (751) , (753) $160 \times$
 RGB $\times 240$ (707) .

31, 32 CPU, 33, 34, 35, 36

2 가 22, 23 (Vcom)

30 CPU(701) (704)

(744) CPU(701) (702) (708), (

709) D15 D0 31, 32 CS, WR, RD, 16

(704) (744) CPU(701)

(704)

(710)

(711)가 (740), (745)

(744) (744) (716) , 1

(717) (718) (720) (719)

(726) (715) (72)

6) (745) (744)

(747) (720) 480 (748)

(749) (739) (750) (752)

(753) 1

(706) (704) FLM

CL3 1 CL3 1024 CL3 1024 240 2, 3

FLM (704) (707) (753)

V4, V5 V9 10 (731) (739) (705) V0

(738) 33, 34, 35

(803) (801) (802)

(804) VS0 VS63 64

(805) (804) (806)

(807) (806) 64 (VG0

VG63) (739)

(801) (729)

(731) V0 V4 V5 V9 (738) (729)가

(739)

, 23 , 가가 , (734)
 , (729) 가 (732) (733) , 가 (707)
 ,
 (803) 35 V0S V1S 16 VS0 VS15 16
 (804) , V1S V2S 가 16 VS16 VS31 16
 . V2S V4S 가 , V
 S0 VS63 64 (804) (805) (807)
 (807) V1B V7B 35 VG0 VG7
 8 V0S (805) V1B 8
 VG8 VG15 8 (805) V1B V2B 8
 가 , V2B V7B VG16 VG55 VG56
 VG63 8 (805) (737) (806)
 , (805) , (808) , V
 1B V7B 35 (807) , V1B VS0,
 VS1 VG31 32 1 V1B , V2B
 V2B 가 , VS0, VS1 VG31 32 1
 V3B , VS8, VS9 VG39 32 1
 VG47 32 1 V4B , VS16, VS17
 VS25, VS26 VG56 32 1 V5B ,
 V6B VS32, VS33 VG63 32 1 VG63 32
 1 V7B
 , 35 (809, 810) , V0S, V4S , 2
 V0, V8 27, 28 27 가 (809) ,
 (807) VG2, VG4, VG6, VG10, VG12, VG14 B1 B6 ,
 (737) 가 V0S가 28 가
 (810) , (807) VG50, VG52, VG54, VG58, VG60, VG62
 W6 W1 (737) 가 V4S가
 , (809, 810) (807) V0S ,
 V4S
 , (736) 3 36
 9 , NO.1 NO.9 B1 B6, W1 W6 , V1B V7B
 (736) (736) (744) 가
 . CPU(701) (704)
 (736) . CPU(701) (702) (708), (709)
 , 31 CS, WR, RD, 16 D15 D0
 (704) , ,

(736) , CPU(701) (704)

(No.) (704)

가 (736)

가

13 18 3

1 가

13, 14, 15 1 가

가 가

가

CPU(701)

NO.1, NO.2 B1 B6, W1 W6 8

V0S (VG0), V4S(VG63)

16, 17 CPU(701) 가 DVD NO.3 NO.9 , OA

V1B V7B

18 CPU(701) 가 NO.3 NO.9

V1B V7B

CPU

가

64 9 가 5 V1B V7B

32 , 16 가

가

가

DVD , OA

가 가

(57)

1.

2.

1 ,

2^N

2^N

3.

2 ,

2^N

256

4.

2 ,

256

5.

2 ,

32 , 2^N

6.

2 ,

32 ,

7.

2 ,

가 가 2

N

8.

2 ,

가 가 2

N

9.

1 ,

10.

1 ,

1

11.

1 ,

1 1

12.

1 ,

1

13.

1 ,

14.

15.

14 ,

가 가

16.

14 ,

1 1

17.

18.

17 ,

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19.

18 ,

2^N

,

2^N

,

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20.

19 ,

2^N

256

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21.

19 ,

256

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22.

19 ,

32

,

2^N

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23.

19 ,

32

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24.

19 ,

가

가

2

N

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25.

19 ,

가 가 2
N .

26.

18 ,

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1 1 .

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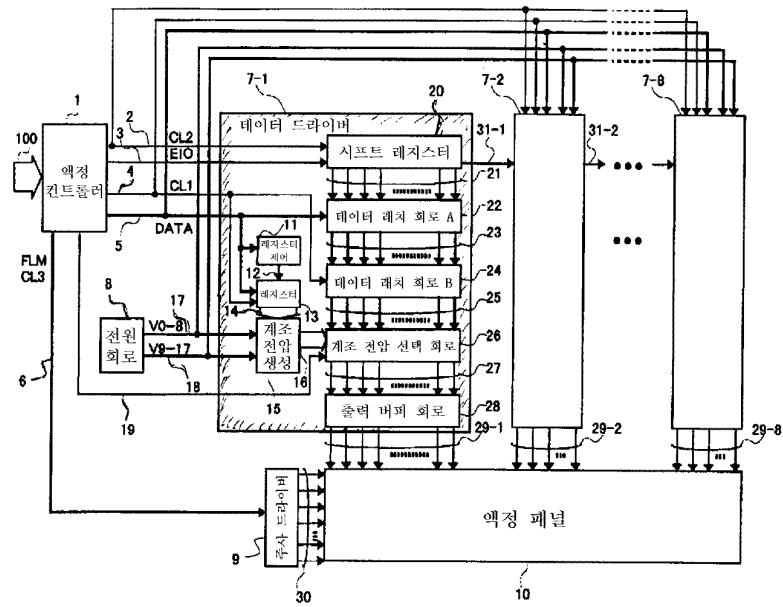
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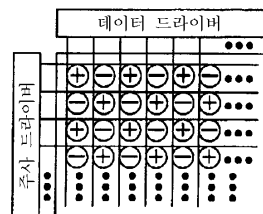
36.

31 ,

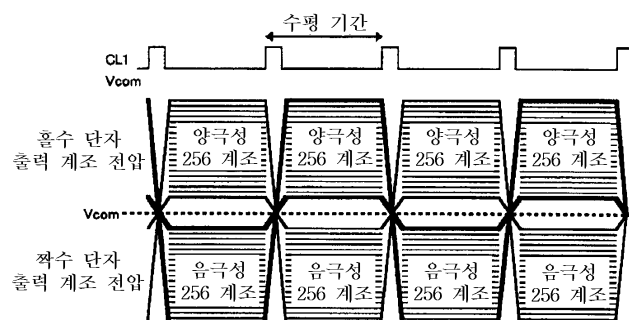
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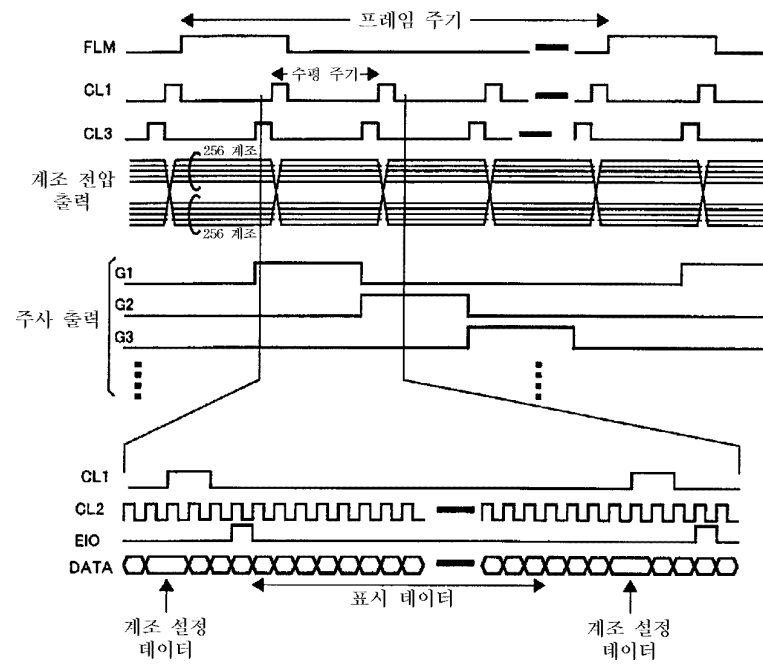
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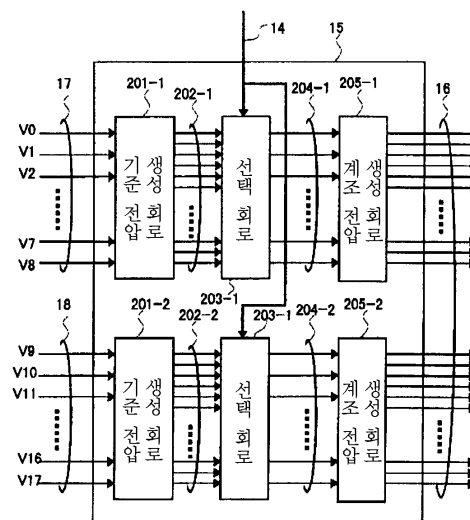
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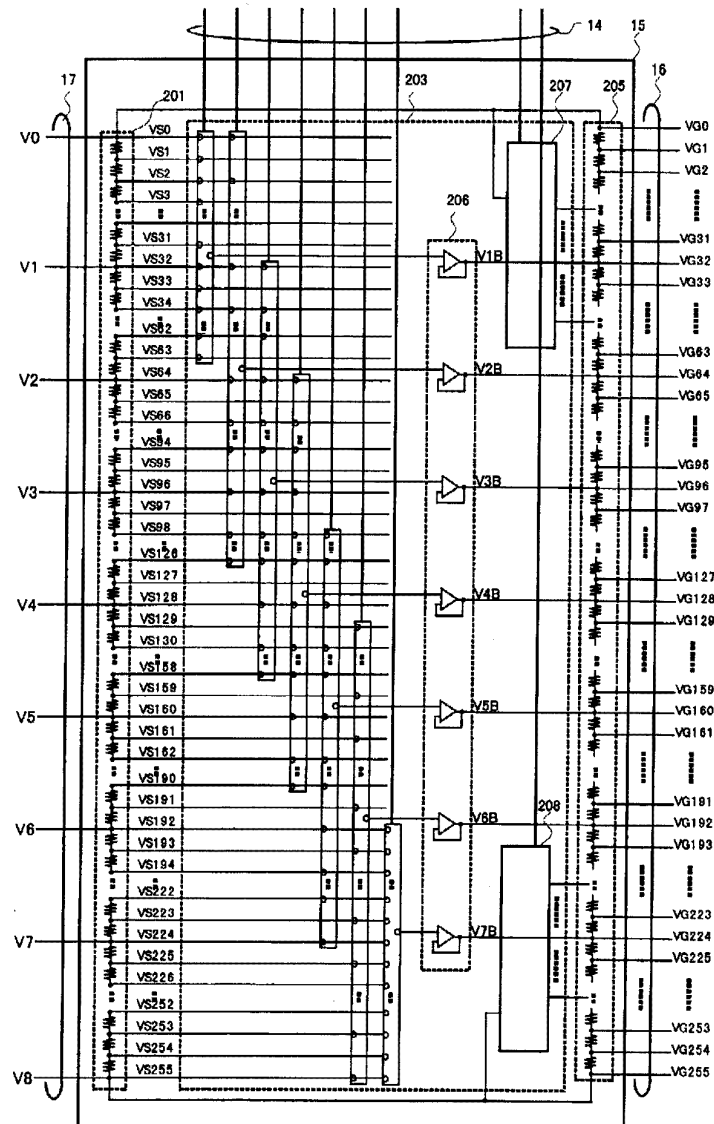
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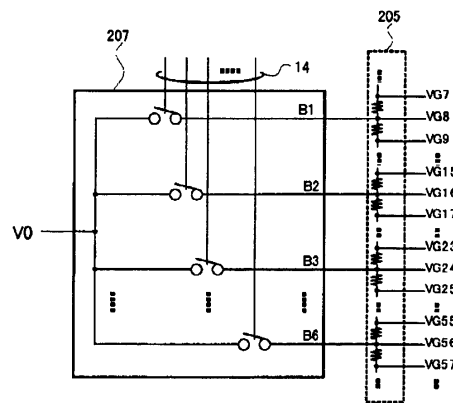
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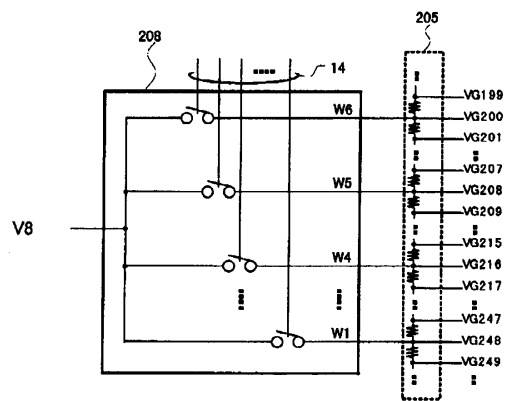
6



7



8

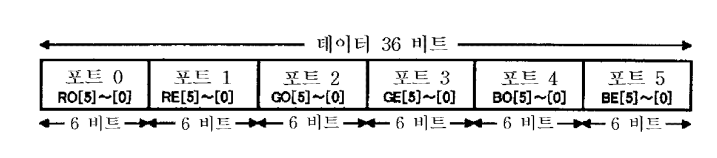


9

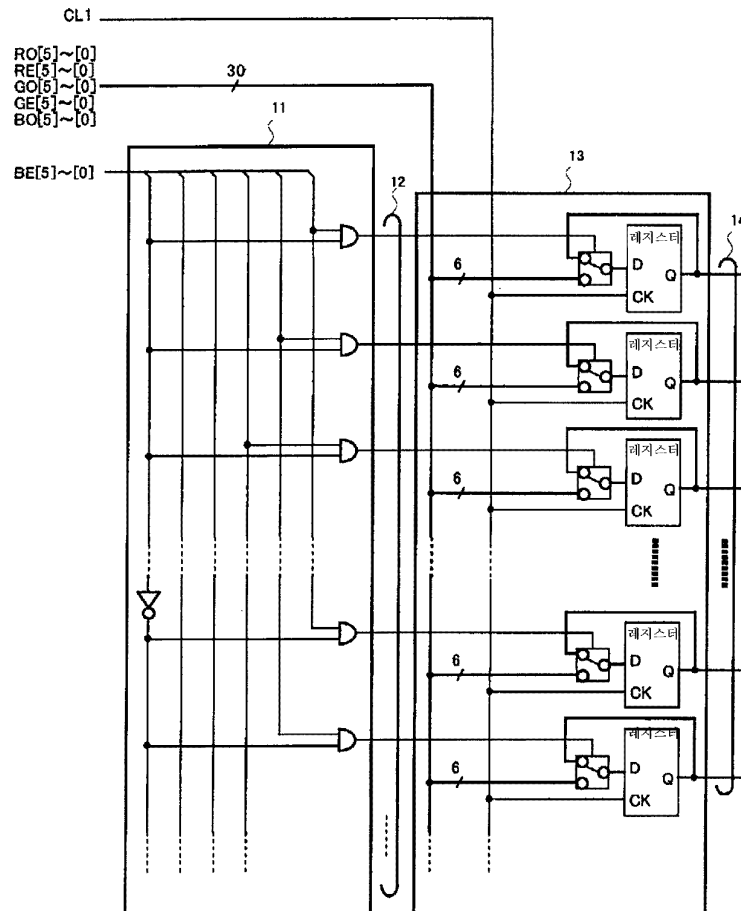
NO	포트	RS	P4~0	데이터 비트	내용
1	0	0	P0	B6 B5 B4 B3 B2 B1	B1~B6
2	1	0	P1	W6 W5 W4 W3 W2 W1	W1~W6
3	2	0	P2	D5 D4 D3 D2 D1 D0	V1B 설정
4	3	0	P3	D5 D4 D3 D2 D1 D0	V2B 설정
5	4	0	P4	D5 D4 D3 D2 D1 D0	V3B 설정
6	0	1	P0	D5 D4 D3 D2 D1 D0	V4B 설정
7	1	1	P1	D5 D4 D3 D2 D1 D0	V5B 설정
8	2	1	P2	D5 D4 D3 D2 D1 D0	V6B 설정
9	3	1	P3	D5 D4 D3 D2 D1 D0	V7B 설정
10	5	—	—	RS P4 P3 P2 P1 P0	제어 레지스터

P4~P0='1': 대응하는 계조 제어 레지스터에 대한 기입을 실시
 P4~P0='0': 대응하는 계조 제어 레지스터에 대한 기입을 행하지 않는다
 RS='0': B1~B6, W1~W6, V1B~V3B의 계조 제어 레지스터를 선택
 RS='1': V4B~V7B의 계조 제어 레지스터를 선택

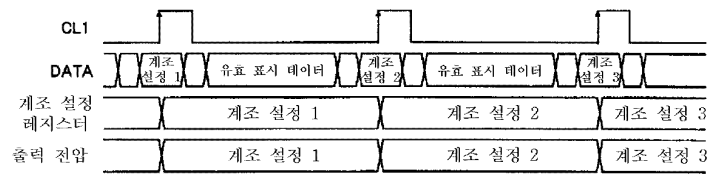
10



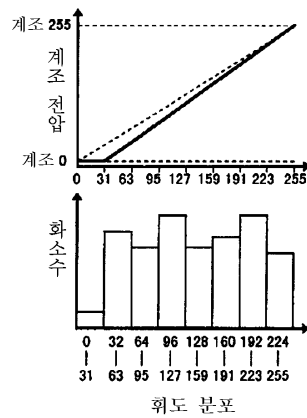
11



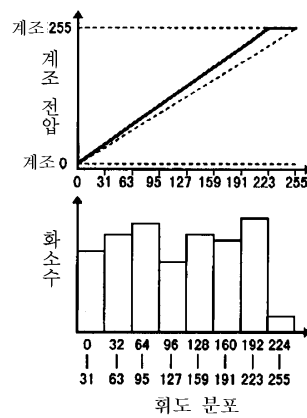
12



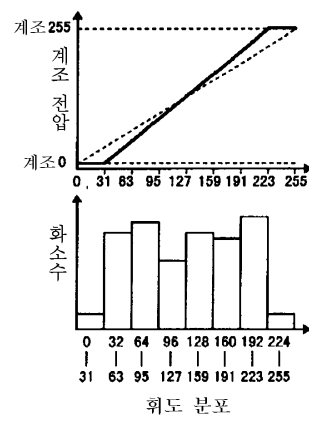
13



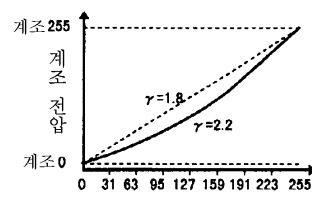
14



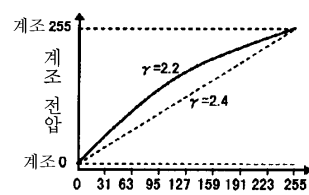
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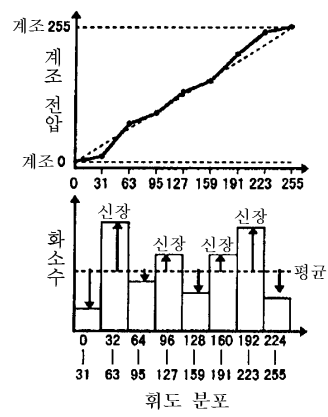
16



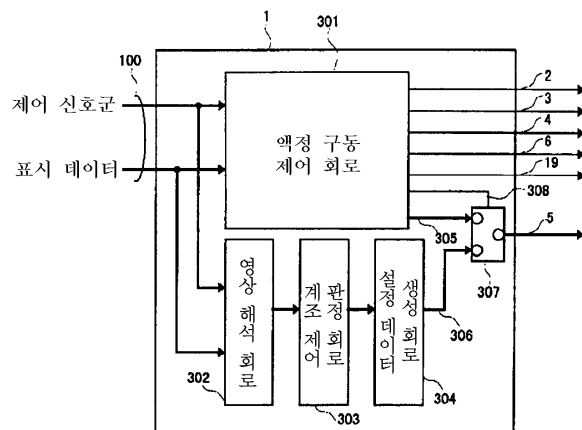
17



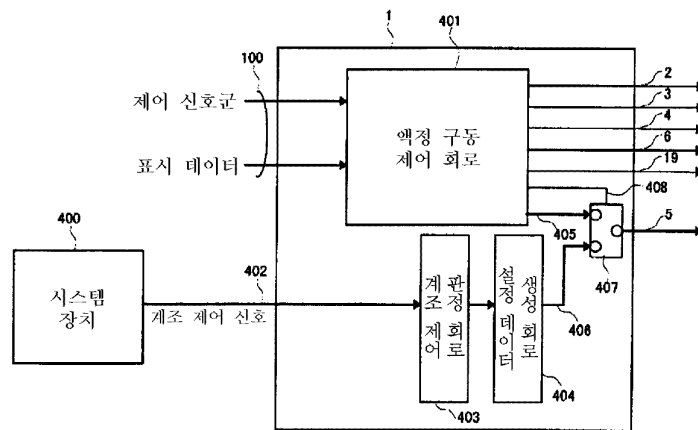
18



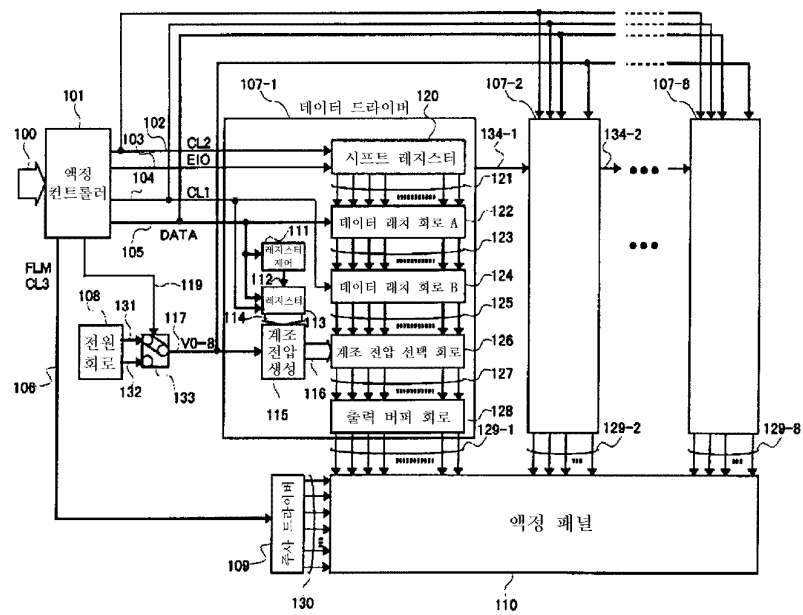
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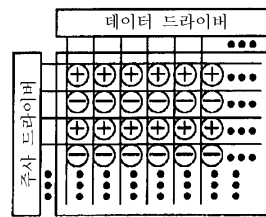
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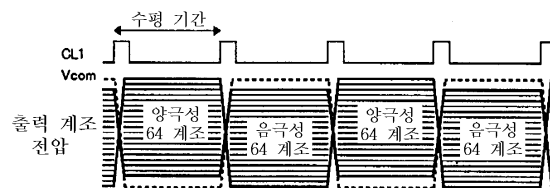
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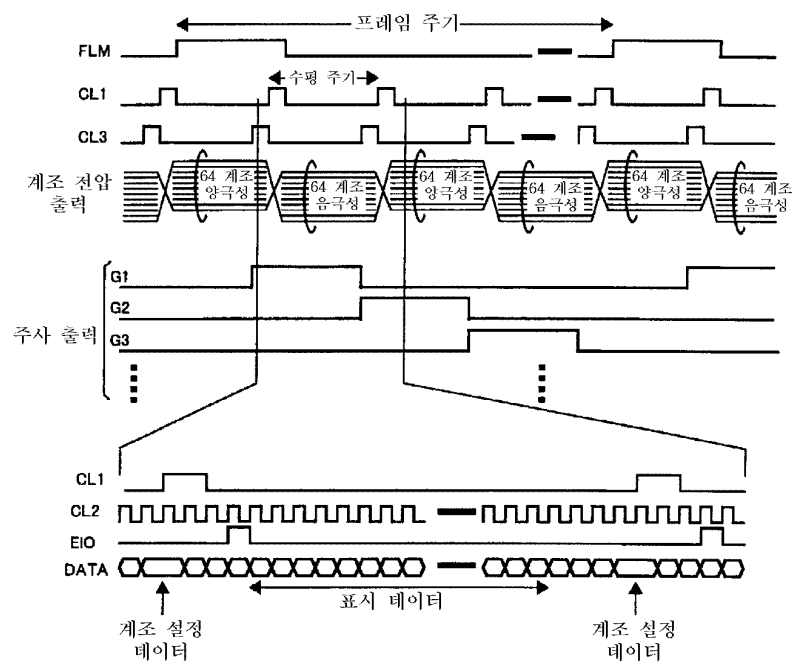
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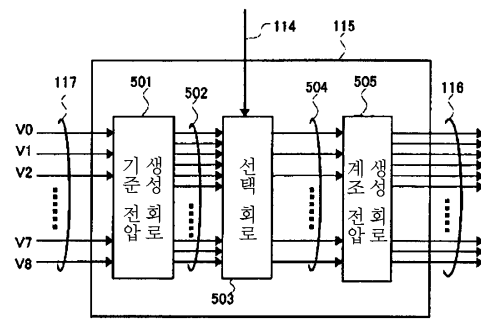
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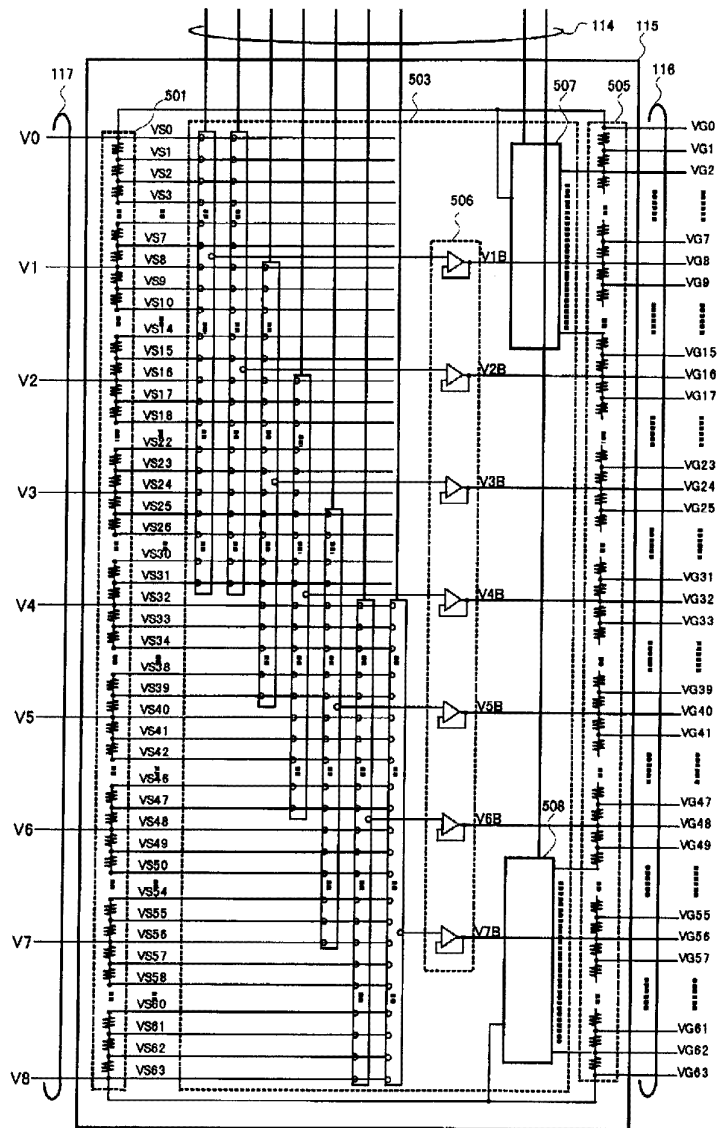


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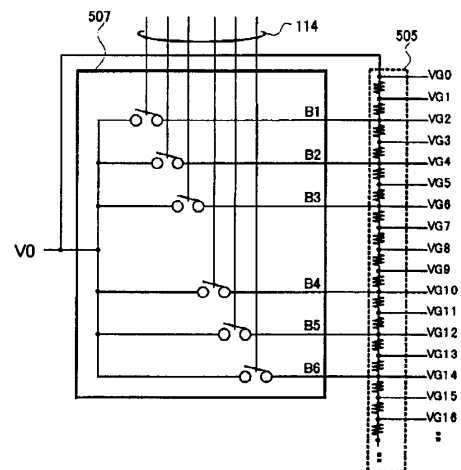


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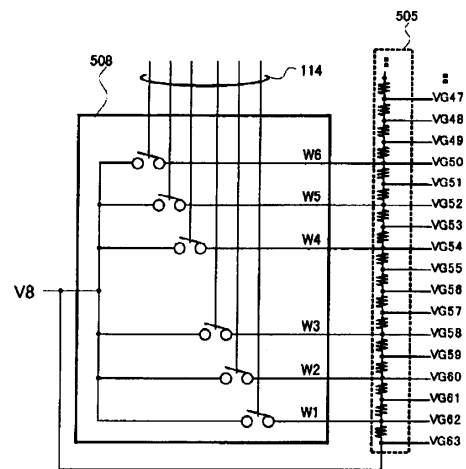




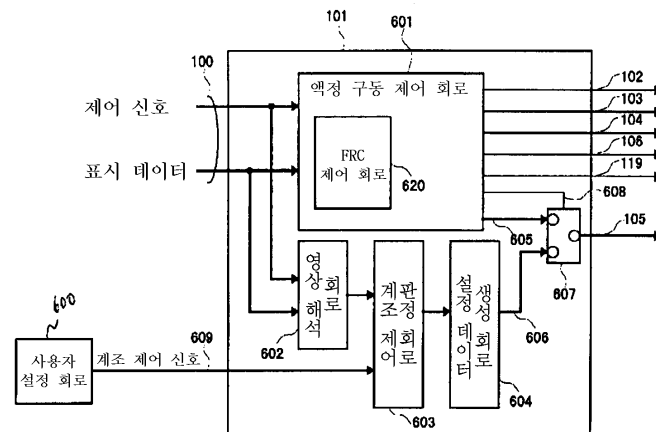
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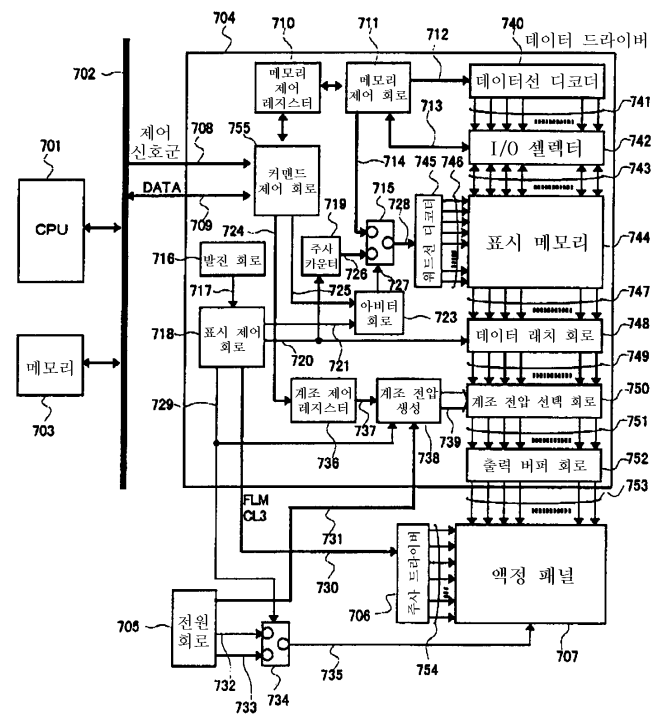
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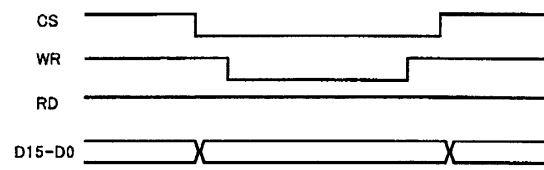
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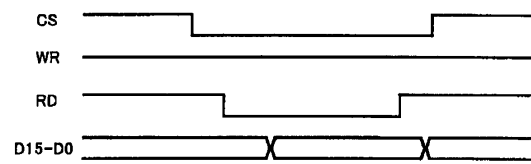
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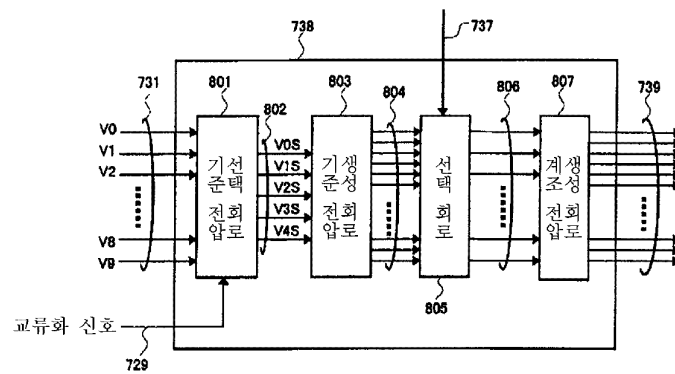
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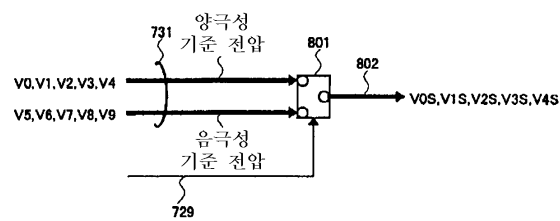
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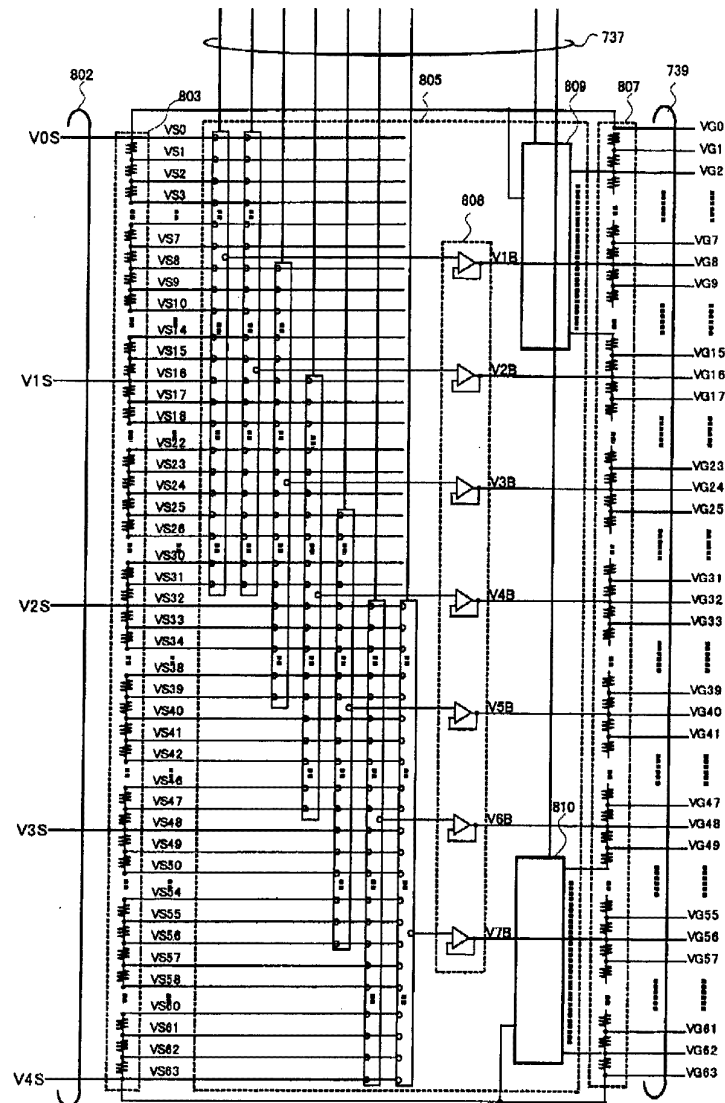
33



34



35



36

NO.	어드레스	내용						내용
1	0	B6	B5	B4	B3	B2	B1	B1 ~ B6 설정
2	1	W6	W5	W4	W3	W2	W1	W1 ~ W6 설정
3	2	—	S4	S3	S2	S1	S0	V1B 설정
4	3	—	S4	S3	S2	S1	S0	V2B 설정
5	4	—	S4	S3	S2	S1	S0	V3B 설정
6	5	—	S4	S3	S2	S1	S0	V4B 설정
7	6	—	S4	S3	S2	S1	S0	V5B 설정
8	7	—	S4	S3	S2	S1	S0	V6B 설정
9	8	—	S4	S3	S2	S1	S0	V7B 설정

专利名称(译)	显示驱动设备和显示设备		
公开(公告)号	KR1020020013714A	公开(公告)日	2002-02-21
申请号	KR1020010045113	申请日	2001-07-26
[标]申请(专利权)人(译)	日立HITACHI SEISAKUSHODBA		
申请(专利权)人(译)	株式会社日立制作所		
[标]发明人	NITTA HIROYUKI 닛타히로유키 FURUHASHI TSUTOMU 후루하시쯔토무 KIMURA MAKOTO 기무라마코토 KOSHI HIROBUMI 고시히로부미 MAEDA TAKESHI 마에다다케시		
发明人	닛타히로유키 후루하시쯔토무 기무라마코토 고시히로부미 마에다다케시		
IPC分类号	G02F1/133 G09G3/20 G09G3/36		
CPC分类号	G09G3/2011 G09G3/2018 G09G3/3614 G09G3/3688 G09G3/3696 G09G2310/027 G09G2320/02 G09G2320/0276		
代理人(译)	Jangsugil		
优先权	2000231392 2000-07-27 JP		
其他公开文献	KR100432290B1		
外部链接	Espacenet		

摘要(译)

目的：通过为数据驱动器提供灰度控制寄存器，提供一种具有图像数据的最佳灰度控制的液晶显示装置，其中可以使用数据总线设置液晶控制器，用于控制灰度电压产生电路。结构：数据驱动器具有灰度控制寄存器，并且从输入的参考电压在数据驱动器中产生参考电压。根据灰度控制寄存器的设置选择参考电压，以控制灰度电压。灰度控制寄存器由液晶控制器设置，使用数据总线传输显示数据，用于根据图像数据控制液晶控制器的灰度。©KIPO & JPO 2002

