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2004 02 21

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(22) 2002 08 16

(71) .

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(72) 1322-20

(74)

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(54)

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1 IPS .

2a 1, 2b 2a

3 2a .

5a 5b 4

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7 6
8 6
9a 9b 9
< >
DL1 DLm : GL0 GLn :
VCOML0 VCOMLn : TFT :
Clc : Cst1, Cst2, Cst3 :
Hi, Hi+1 : Vcom :
Vd : Vdo :
Vde : 10 :
12 : 14 :
16 :

가
(Thin Film Transistor)
가 1

가
가

가
1

가 가 IPS(In Plane Switch) 가 가 TN(Twisted Nematic)

TN 가 가 .

IPS 가 가 .

1 IPS 가 .

1 IPS (DL1 D_{Lm}) (GL1 GL_n) (TFT) , (VCOML1 VCOML_m) .

(VCOML1 GL_n) (GL0 GL_n) (GL0 (DL1 GL_{n-1} D_{Lm}) (G (GL0 (Cst2) (Cst1, Cst2) (C_{lc}) 2 (VCOML1 VCOML_n) (C_{lc}) .

L1 D_{Lm}) (TFT) (GL1 GL_n) (D (C_{lc}) (VCOML1 VCOML_n) 1 (Cst1) , (Cst2) 가 (TFT) 2 가 (Cst1, Cst2) (C_{lc}) 2 가 (TFT) .

m), (Line Inversion System), (Frame Inversion System) (Dot Inversion System)

()

가 , 2 가 .

2a , 2b 2a

2a (Strip) , , (R, G, B) (R, G, B) . , , (R, G, B)

가 (R, G, B) (, 127)

127 , i (H_i) (Vd) 2b (Vcom) (Vd_127) (H_{i+1}) (Vd) 2b (Vd_0)가 (Vcom) , i+1 127 (Vd_127) (H_{i+1}) (Vd) i (Vd_0) 가 (H_i) (Vd) , i+1 가 (H_{i+1}) (Vd) i (Vd_0) , i (H_i) (Vcom)

The diagram illustrates a multi-stage CMOS differential signal processing circuit with $N=4$ stages. The circuit is composed of four stages, each containing a PMOS transistor (P_1, P_2, P_3, P_4) and an NMOS transistor (N_1, N_2, N_3, N_4). The PMOS transistors are connected to a common source (V_{com}) and the NMOS transistors are connected to a common source (V_{de}). The output of each stage is taken from the drain of the PMOS transistor. The diagram also shows the input and output signals, including the differential input (V_i) and the differential output (V_o).

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(V_{com}) $(Cst3)$ (V_{com}) (V_{com}) 가 $\cdot$ 3
 (V_{com}) (V_{com}) (V_{com}) (V_{com}) (V_{com}) (V_{com})
 $(VCOML1$ $가$ $VCOMLn)$ (V_{com}) (V_{com})
 $\cdot$
 $\cdot$ 3 $(Cst3)$ $\cdot$ 3 $(Cst3)$
 (V_{com})
 $\cdot$
7 2a (V_{com}) $\cdot$
7 (H) (V_{com}) 가 3 $(Cst3)$ (V_{com})
 $\cdot$
8 6 (22) $\cdot$
8 6 (20) (24) $($
22) (22) (24) (V_{com}) 가 3
 $(Cst3)$ (22) (24) $\cdot$
 $\cdot$ (22) (24) i (H_i) (V_{com}) 3 (H_i)
 $(Cst3)$ 6a (V_{do}) 가 $\cdot$ (22) (V_{de}) 가 i
 $\cdot$
 $\cdot$ (22) (24) i+1 (H_{i+1}) (V_{com}) 3 $($
 $(Cst3)$ 6b (V_{do}) 가 $\cdot$ (22) (V_{de}) 가 i+1
 $H_{i+1})$
 $\cdot$
 (Cst) (V_{com}) 가 (V_{com}) 3 (V_{com})
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 $\cdot$ 3 (V_{com}) $(Cst3)$ (V_{com})
 $\cdot$ 가
가
가

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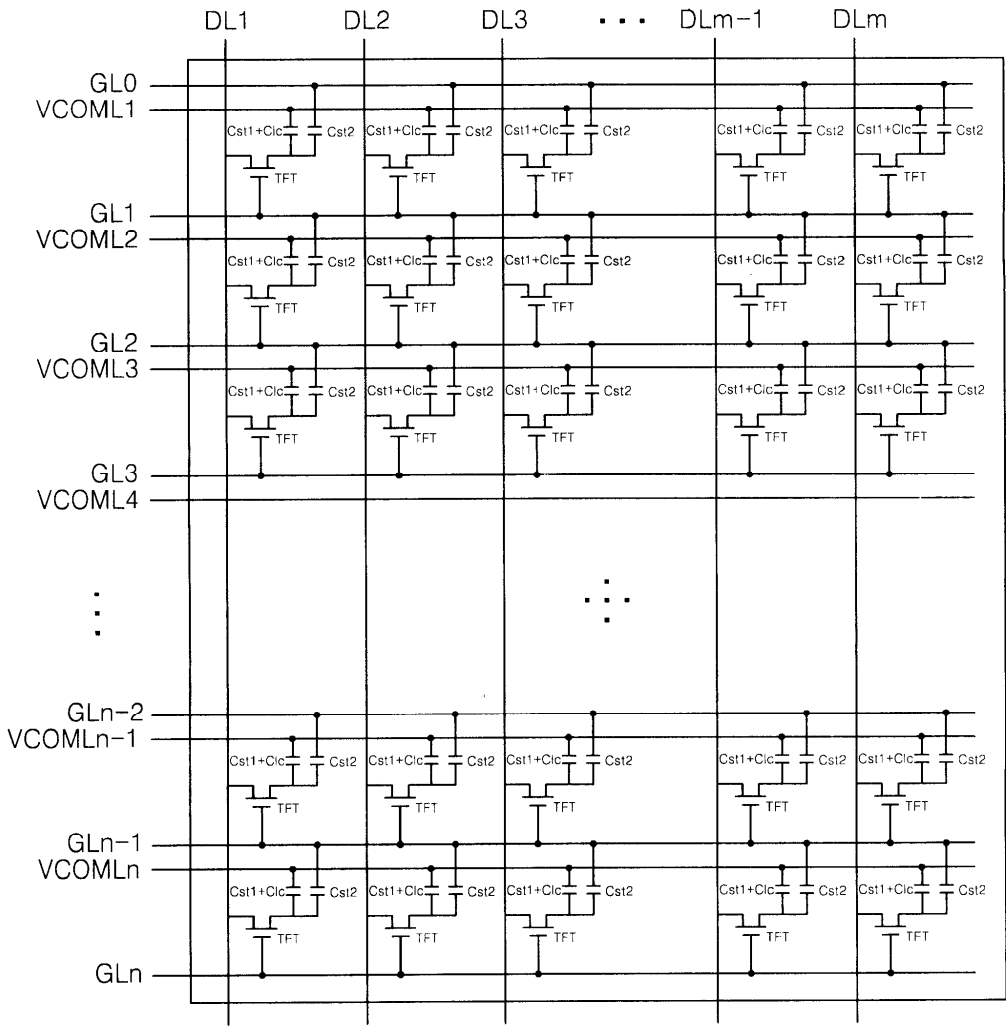
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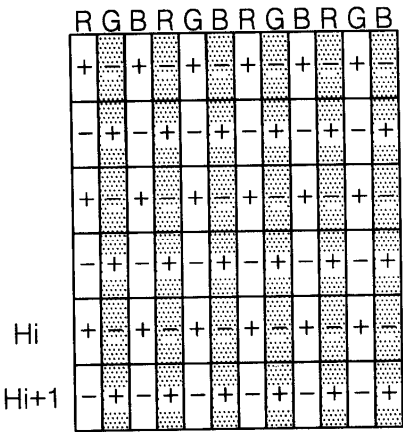
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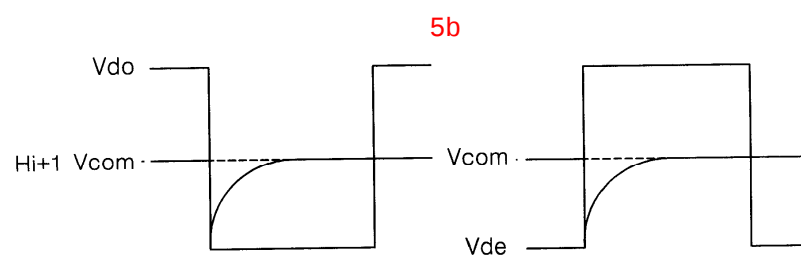
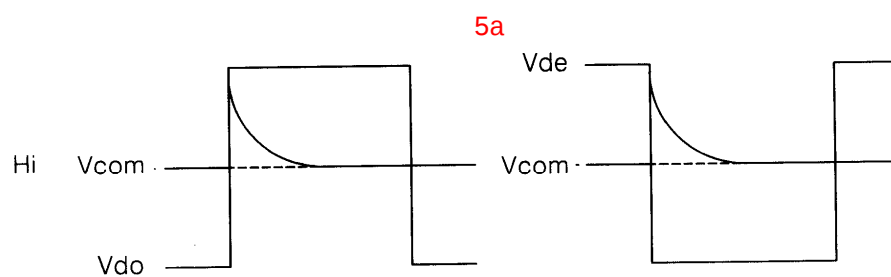
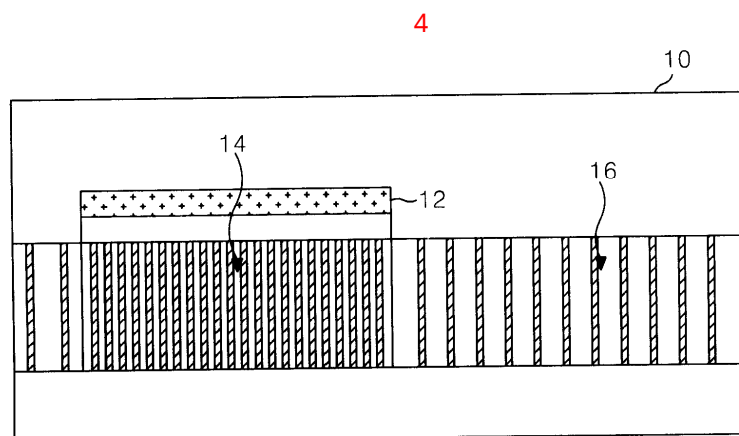
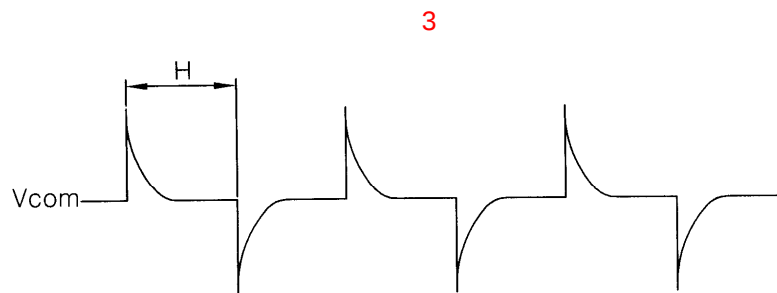
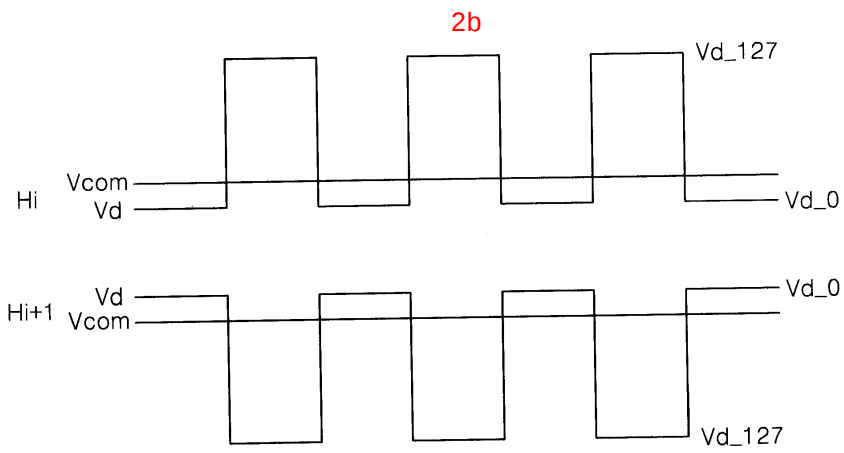
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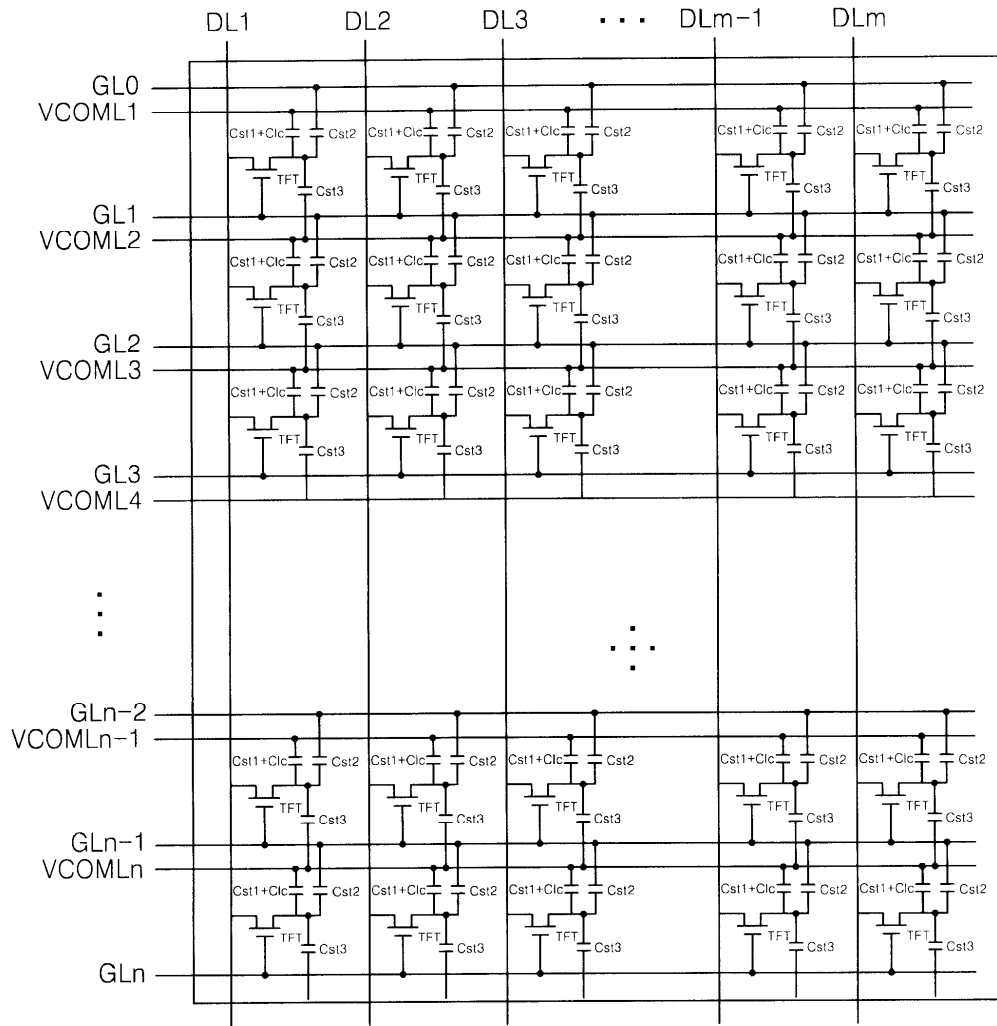


2a

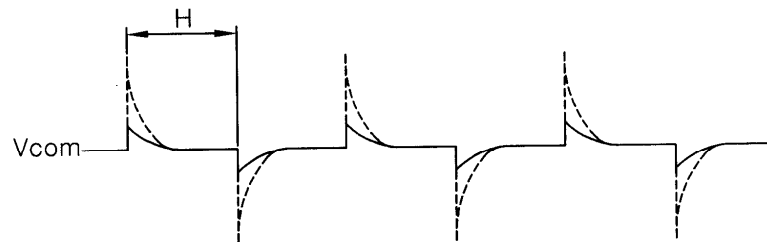




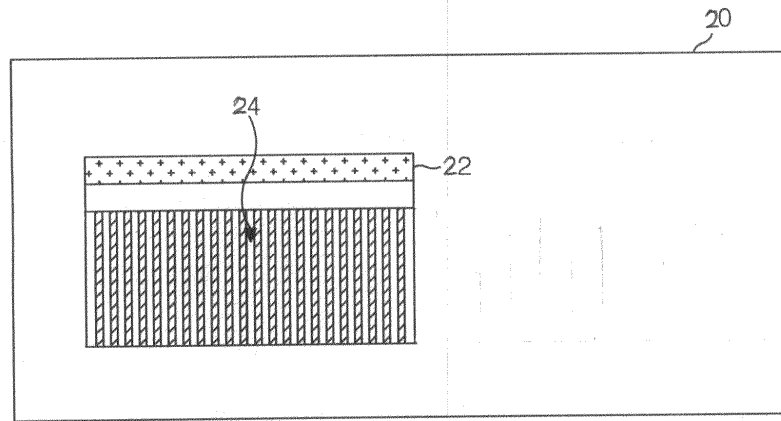
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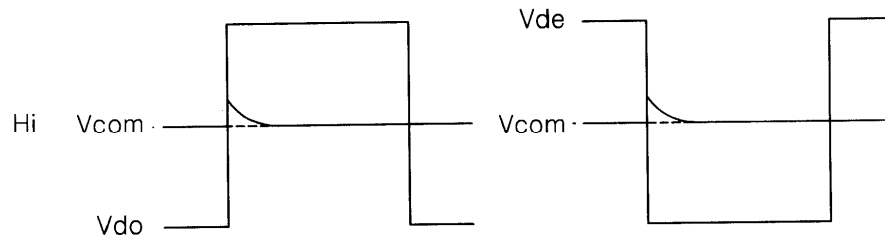
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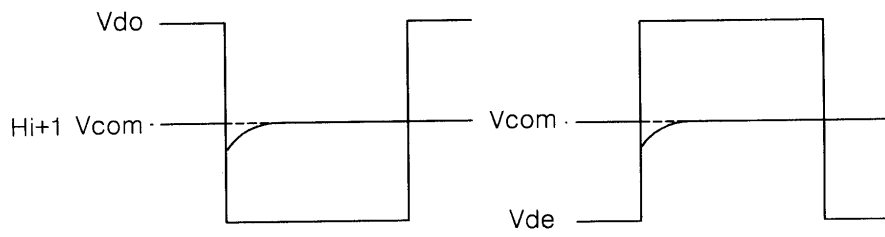
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9a



9b



专利名称(译)	液晶显示面板及其驱动方法		
公开(公告)号	KR1020040016185A	公开(公告)日	2004-02-21
申请号	KR1020020048441	申请日	2002-08-16
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG显示器有限公司		
当前申请(专利权)人(译)	LG显示器有限公司		
[标]发明人	LEE JINHA		
发明人	LEE,JINHA		
IPC分类号	G02F1/133		
CPC分类号	G02F1/1333 G02F1/136213 G02F1/136286 G02F2201/121 G02F2201/123 G09G3/3614 G09G3/3696		
代理人(译)	KIM , YOUNG HO		
其他公开文献	KR100531478B1		
外部链接	Espacenet		

摘要(译)

本发明的目的在于提供一种LCD面板及其驱动方法，在显示器的情况下，使特定图案的公共电压波动的尺寸最小化到点反转系统。本发明的LCD面板具有多条栅极线和数据线，在数据线的交叉区域形成有栅极线的液晶单元，由像素电极和公共电极构成的液晶电容器，以及第一存储电容器包括像素电极和先前的移位栅极线，在该间隔中放置绝缘层：关于当前驱动的点反转LCD面板，第二存储电容器包括在水平线中包括的公共电压线，即在像素电极附近，在该间隔中放置绝缘层，数据信号的极性以点为单位反转。由像素电极和公共电极组成的液晶电容器包括液晶单元并且在液晶单元的间隔中放置液晶，形成与栅极线成一直线的多条公共电压线。

