



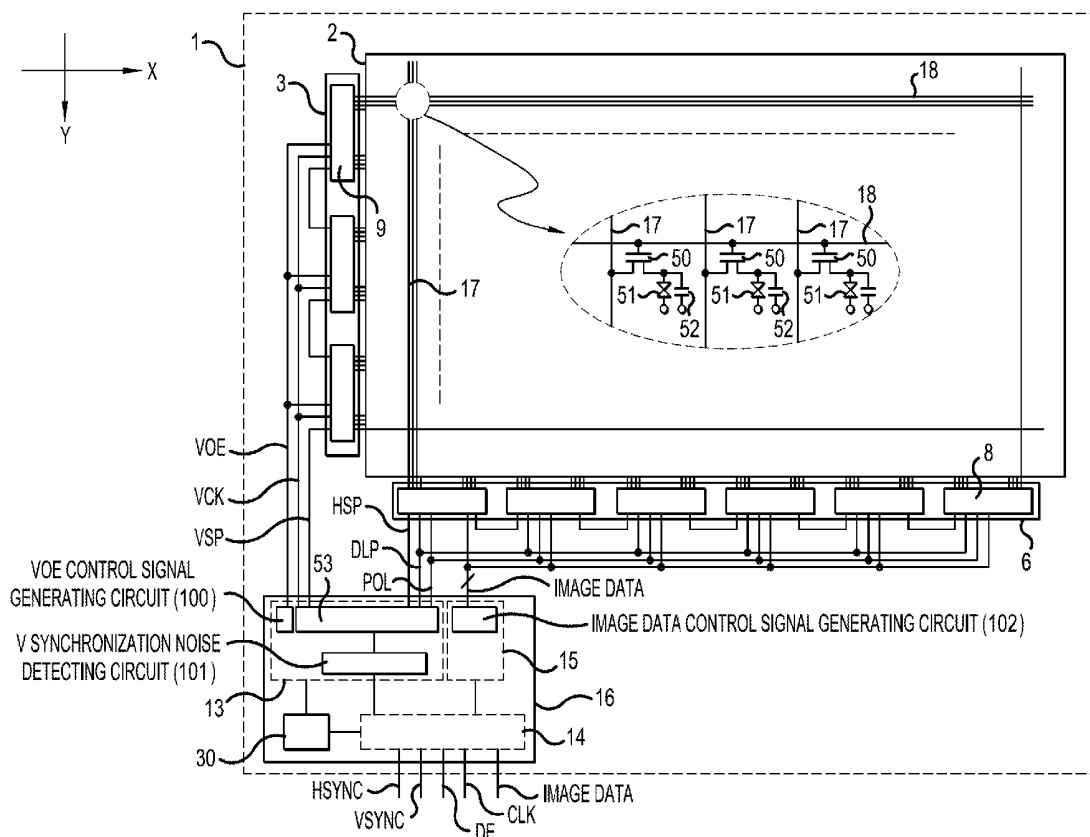
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(19) **United States**(12) **Patent Application Publication**
ISONO(10) **Pub. No.: US 2016/0019848 A1**(43) **Pub. Date: Jan. 21, 2016**(54) **TIMING CONTROLLER AND DISPLAY
DEVICE**(52) **U.S. CL.**CPC **G09G 3/36** (2013.01); **G09G 3/006**
(2013.01); **G09G 2320/04** (2013.01); **G09G**
2310/08 (2013.01)(71) Applicant: **NLT Technologies, Ltd.**, Kanagawa (JP)(72) Inventor: **Katsuji ISONO**, Kanagawa (JP)(21) Appl. No.: **14/755,195**(22) Filed: **Jun. 30, 2015**(30) **Foreign Application Priority Data**

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Publication Classification(51) **Int. Cl.****G09G 3/36** (2006.01)**G09G 3/00** (2006.01)(57) **ABSTRACT**

When applying exogenous noise with a synchronizing signal or a transmission clock period, influence by the applied noise is inhibited from appearing on a liquid crystal display, without increasing circuit size. There are included: a timing controller generating a control signal of a scanning line driving gate driver and a control signal of a signal line driving source driver based on an input signal to be a reference inputted from the outside; an enable signal generation unit including a noise detecting circuit for detecting various items of noise entering the input signal and outputs an enable signal for turning OFF or ON the output of a gate driver control signal for a predetermined period based on output from the noise detecting circuit; and an image data output control circuit when detecting noise synchronized in a vertical period. The gate driver control signal is controlled to have an idle period.



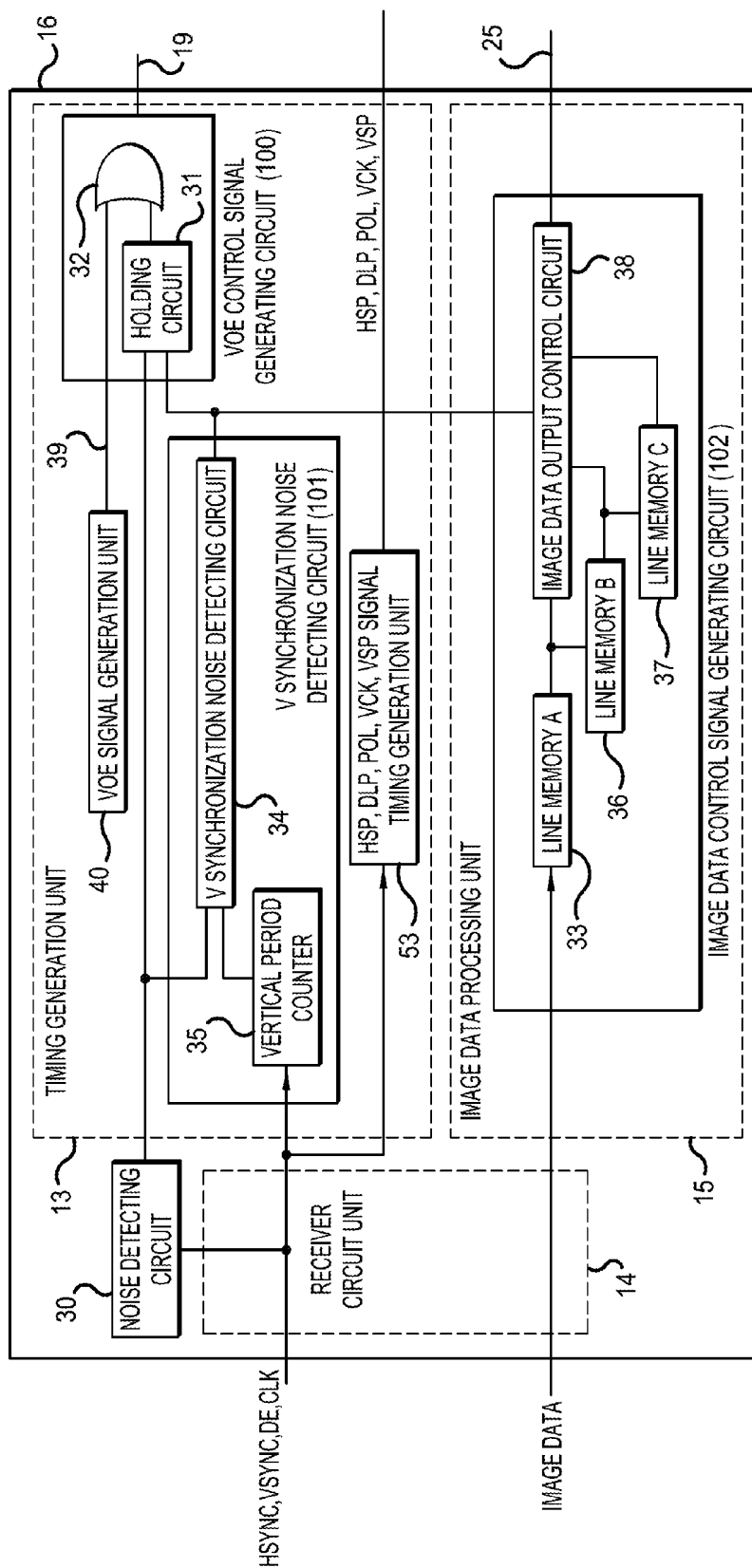
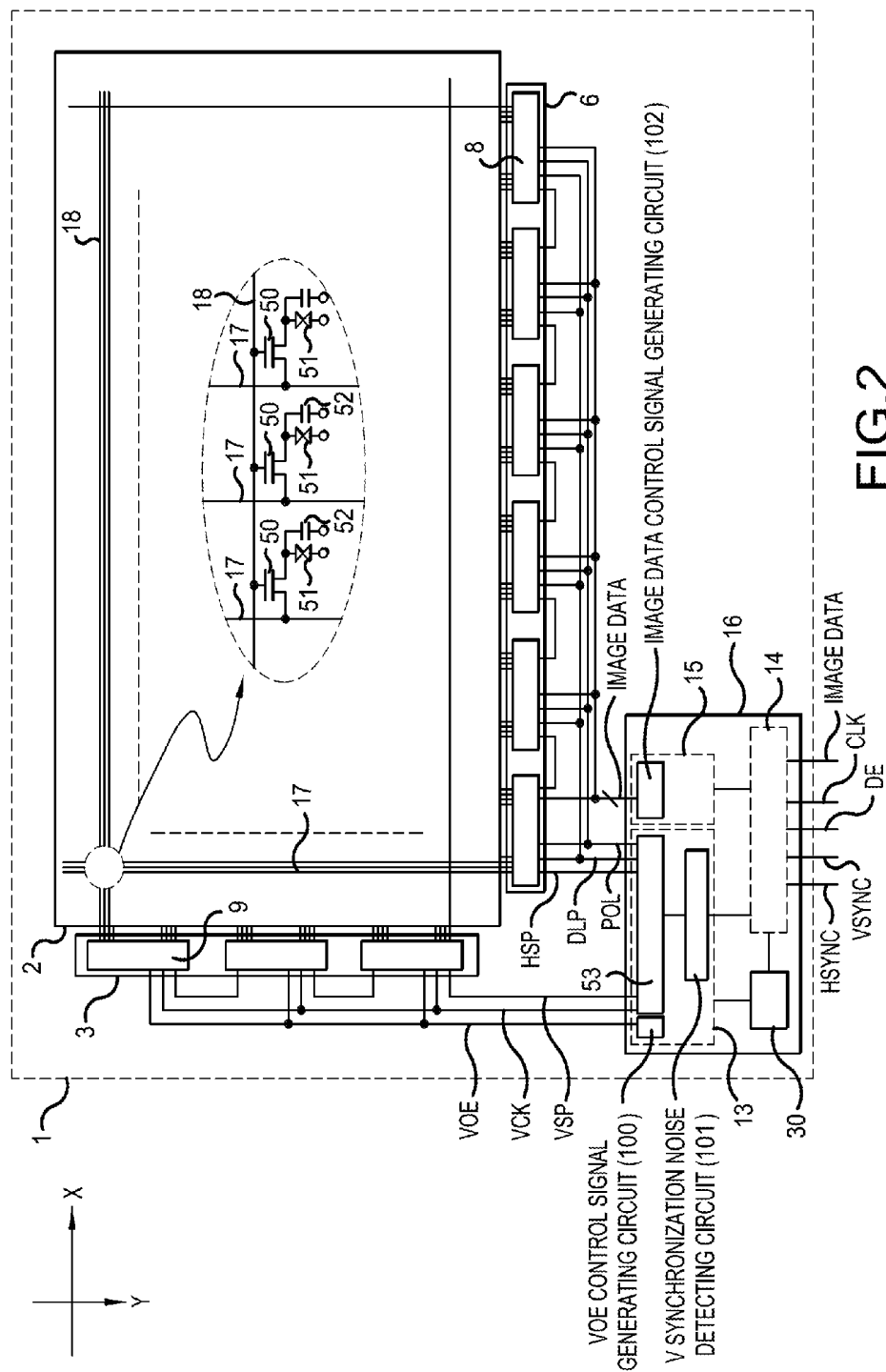


FIG.1



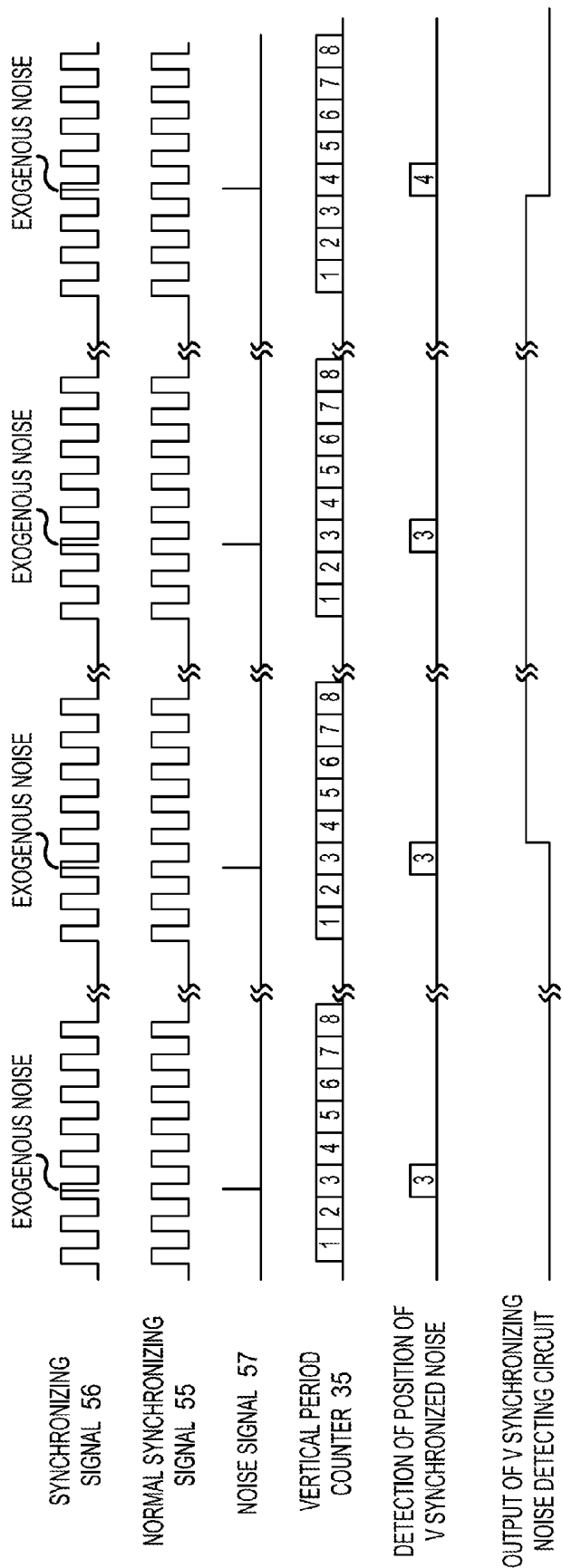


FIG.3

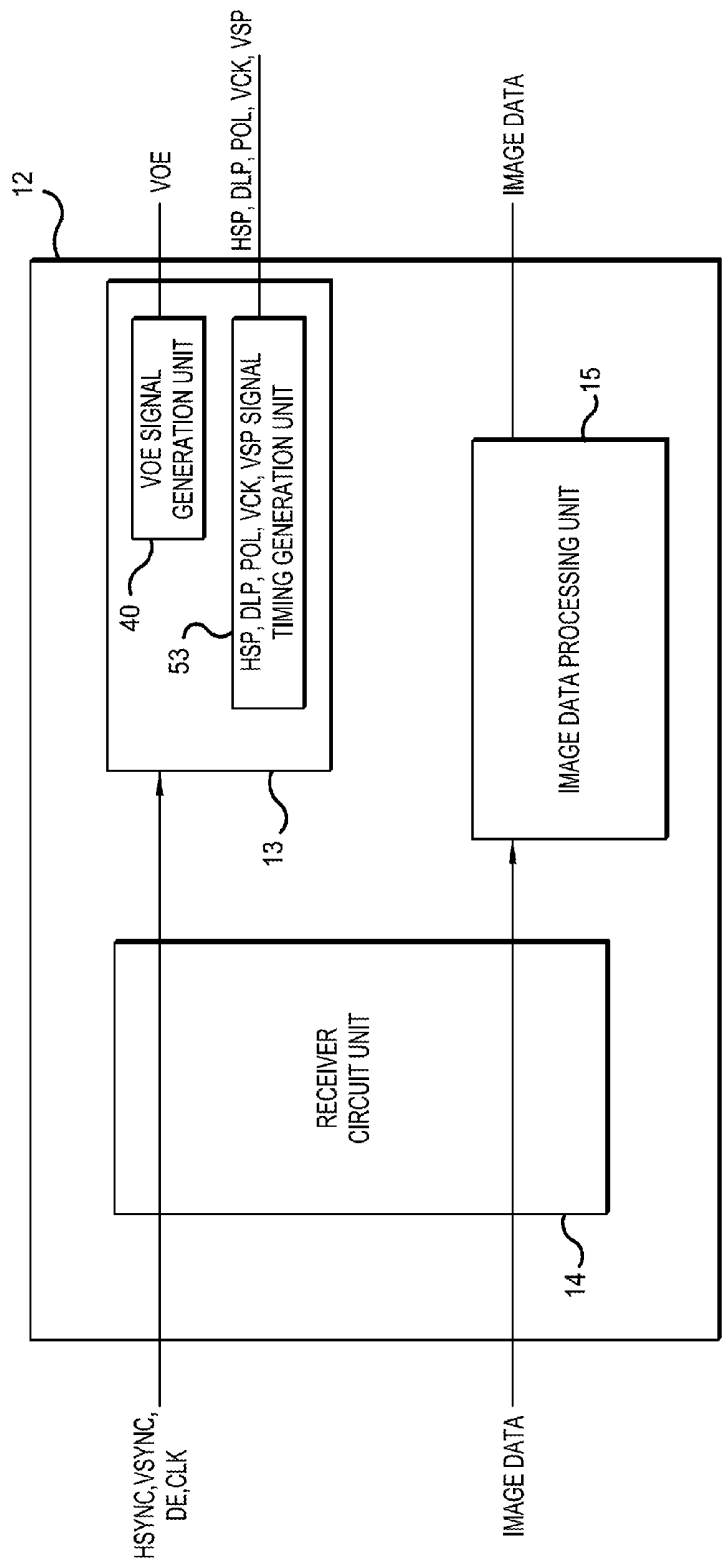
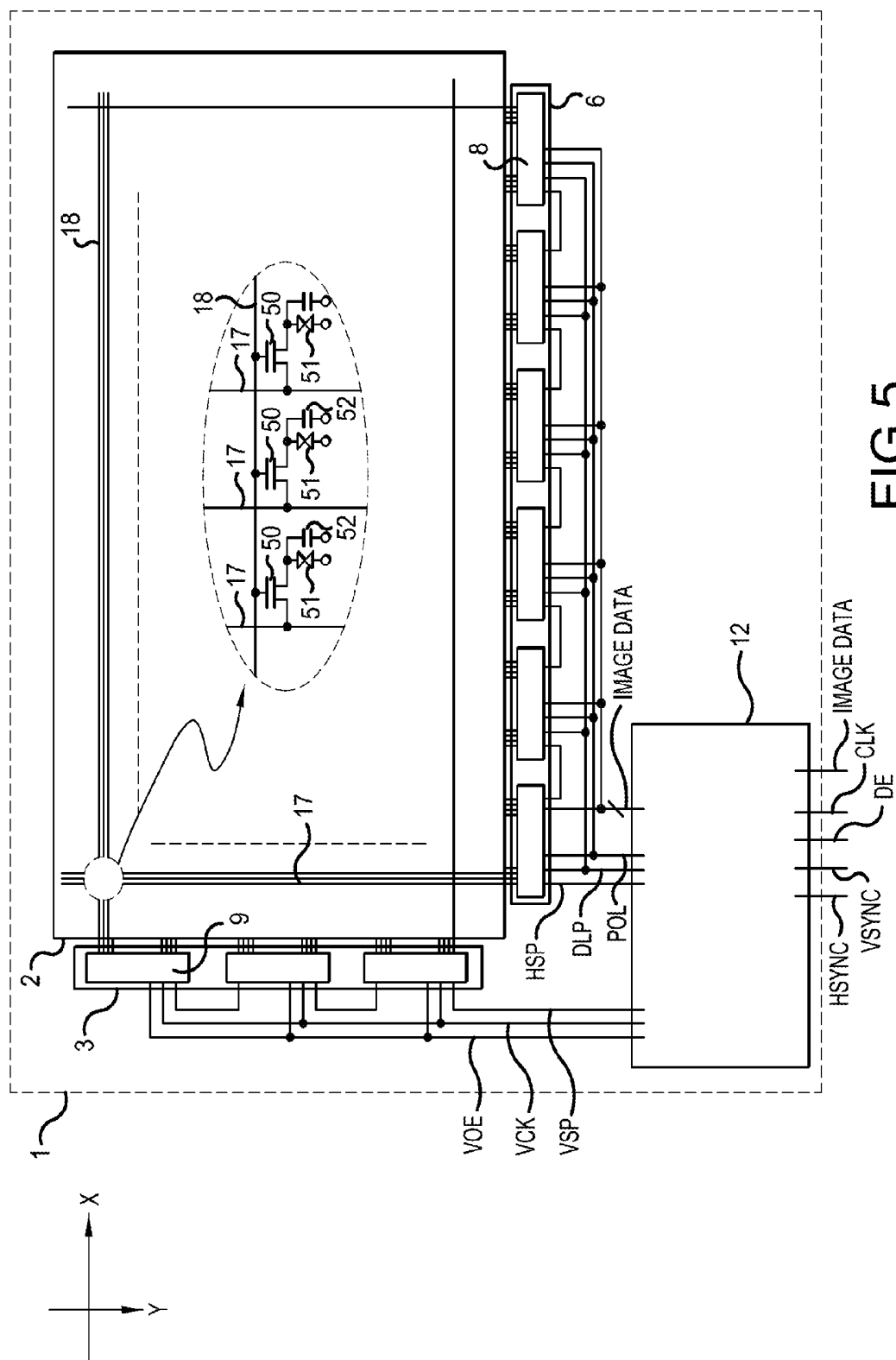


FIG.4



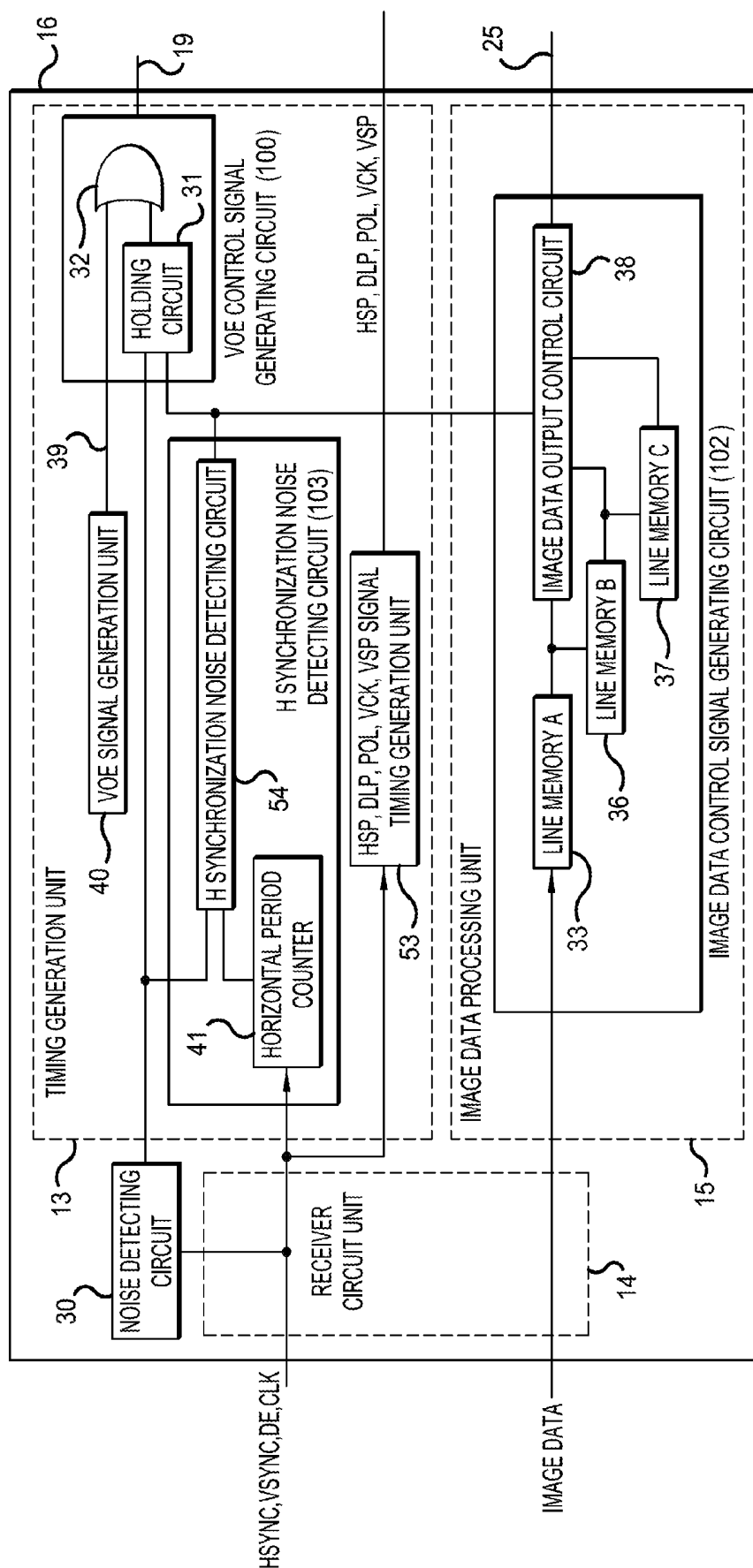


FIG.6

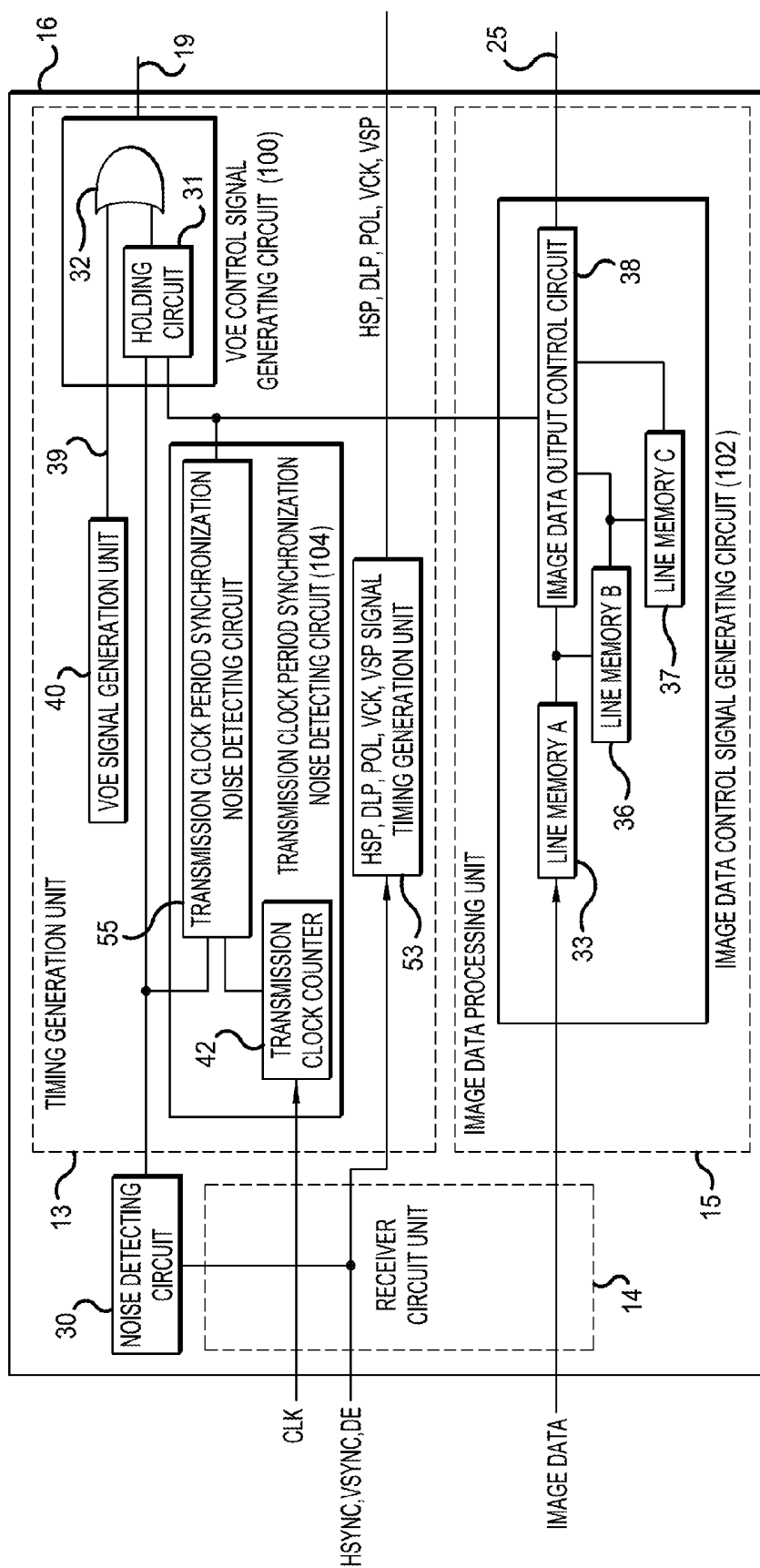


FIG. 7

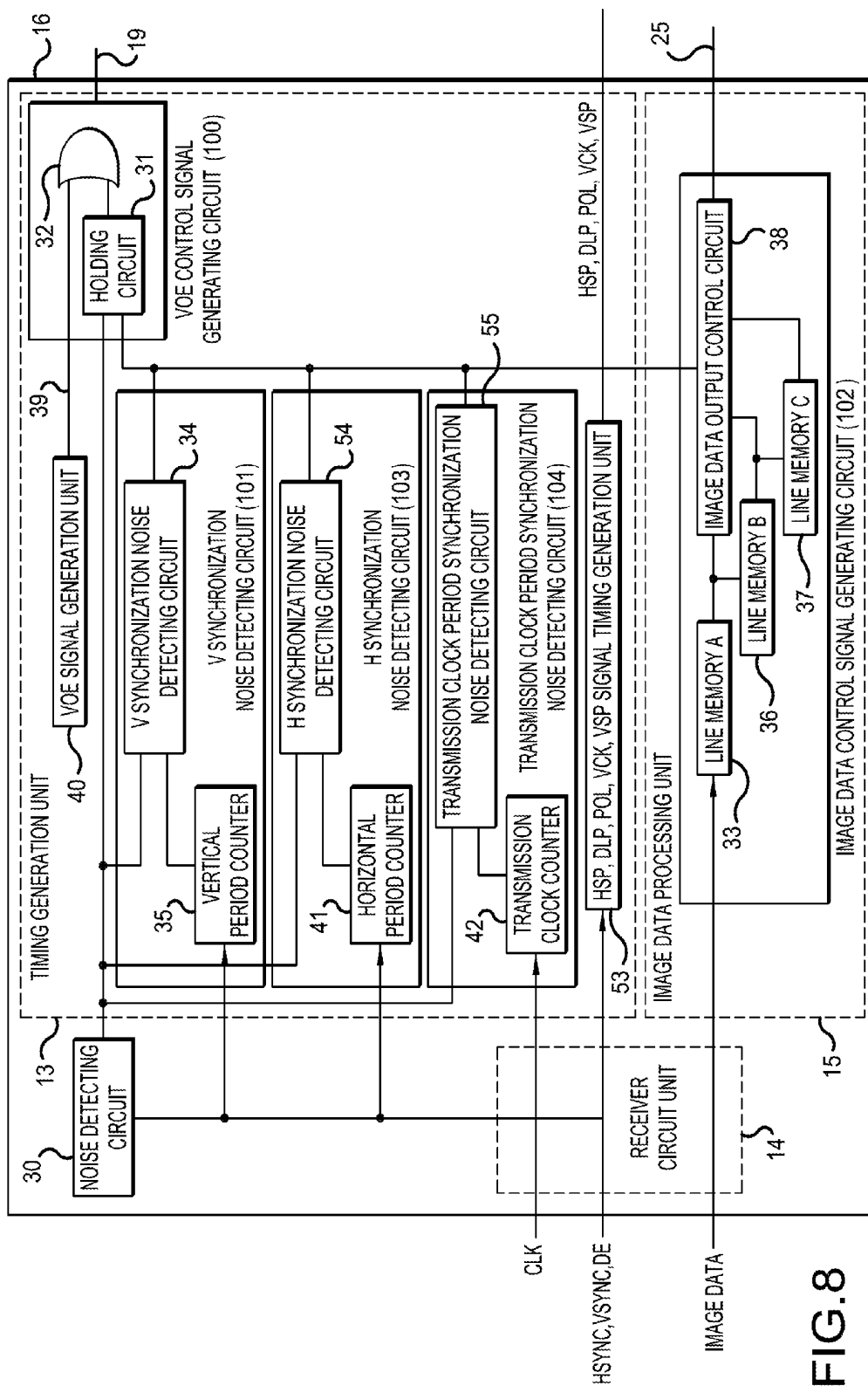


FIG. 8

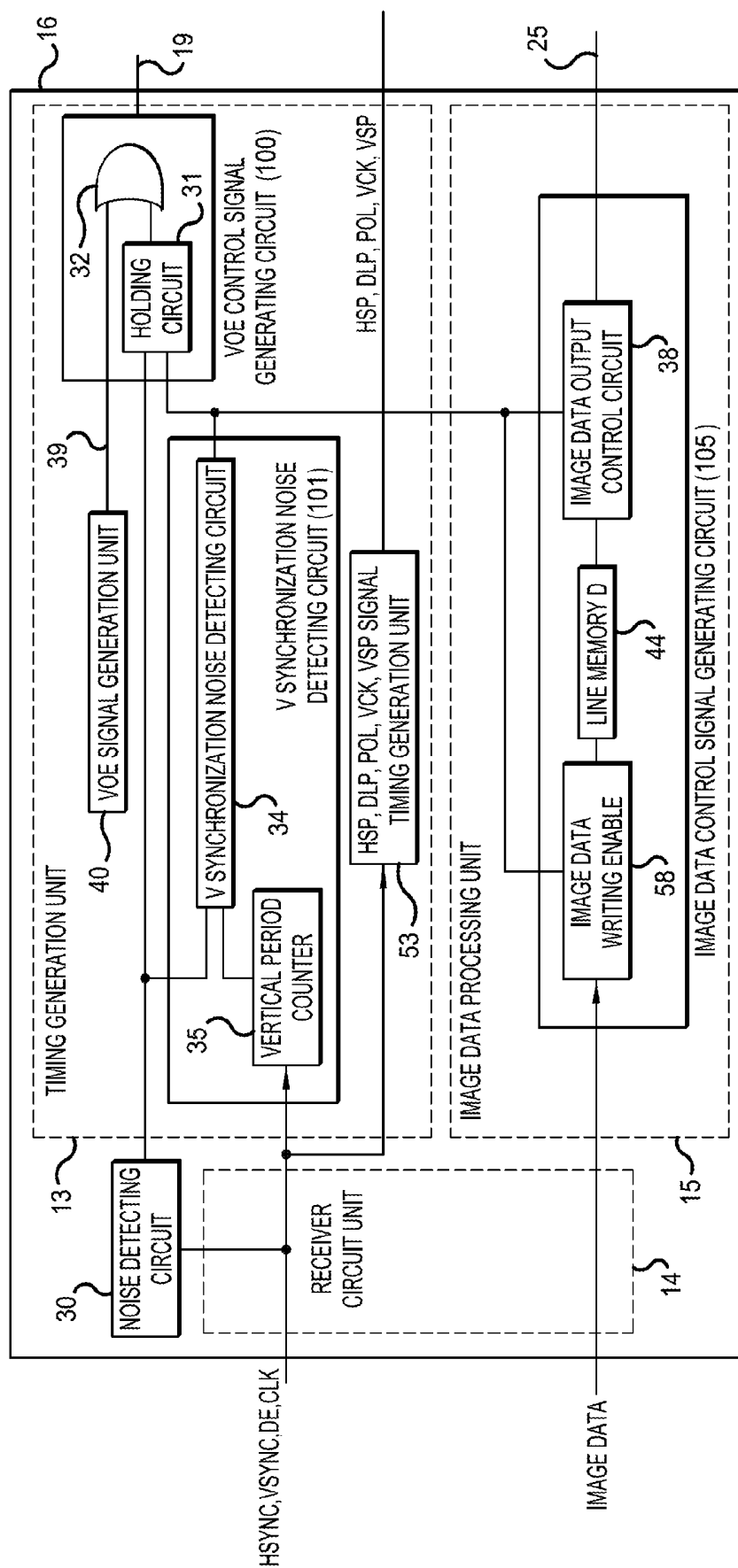


FIG. 9

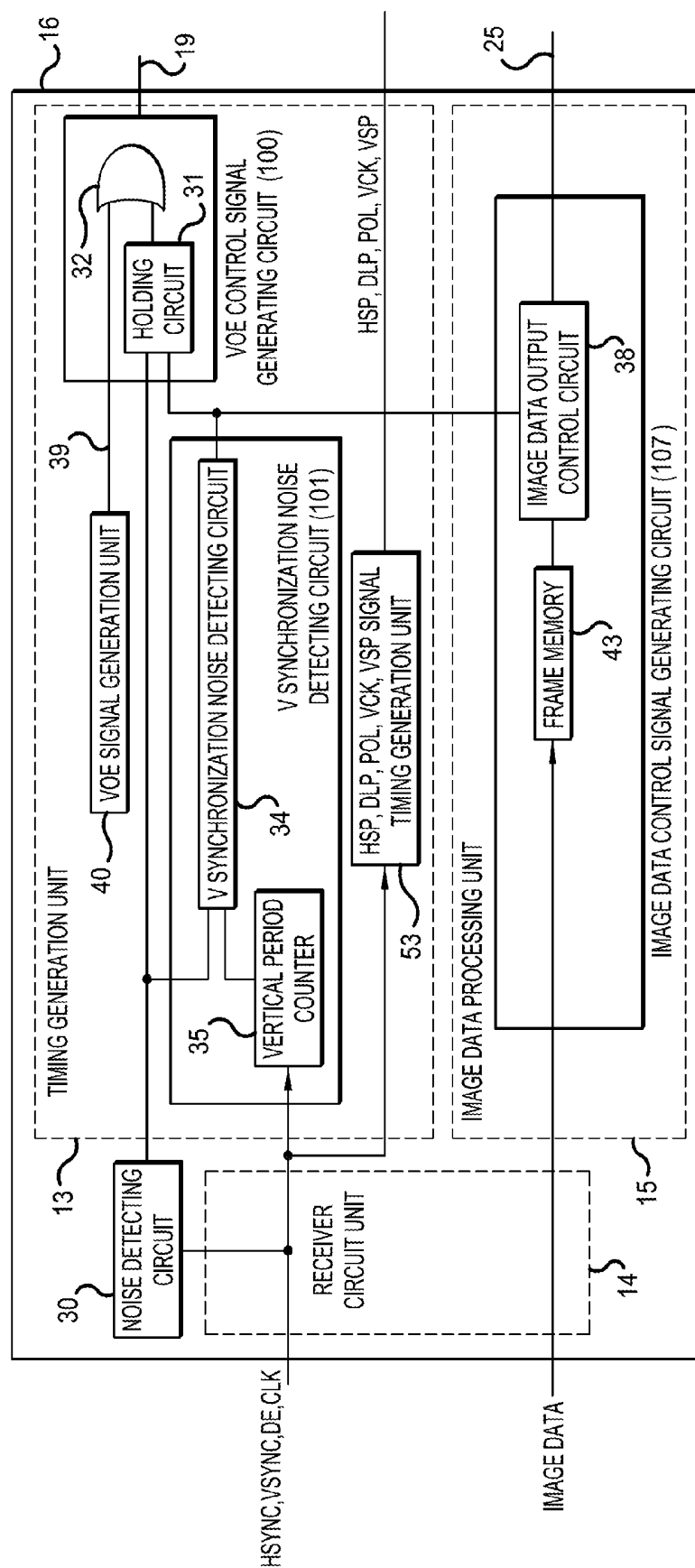


FIG. 10

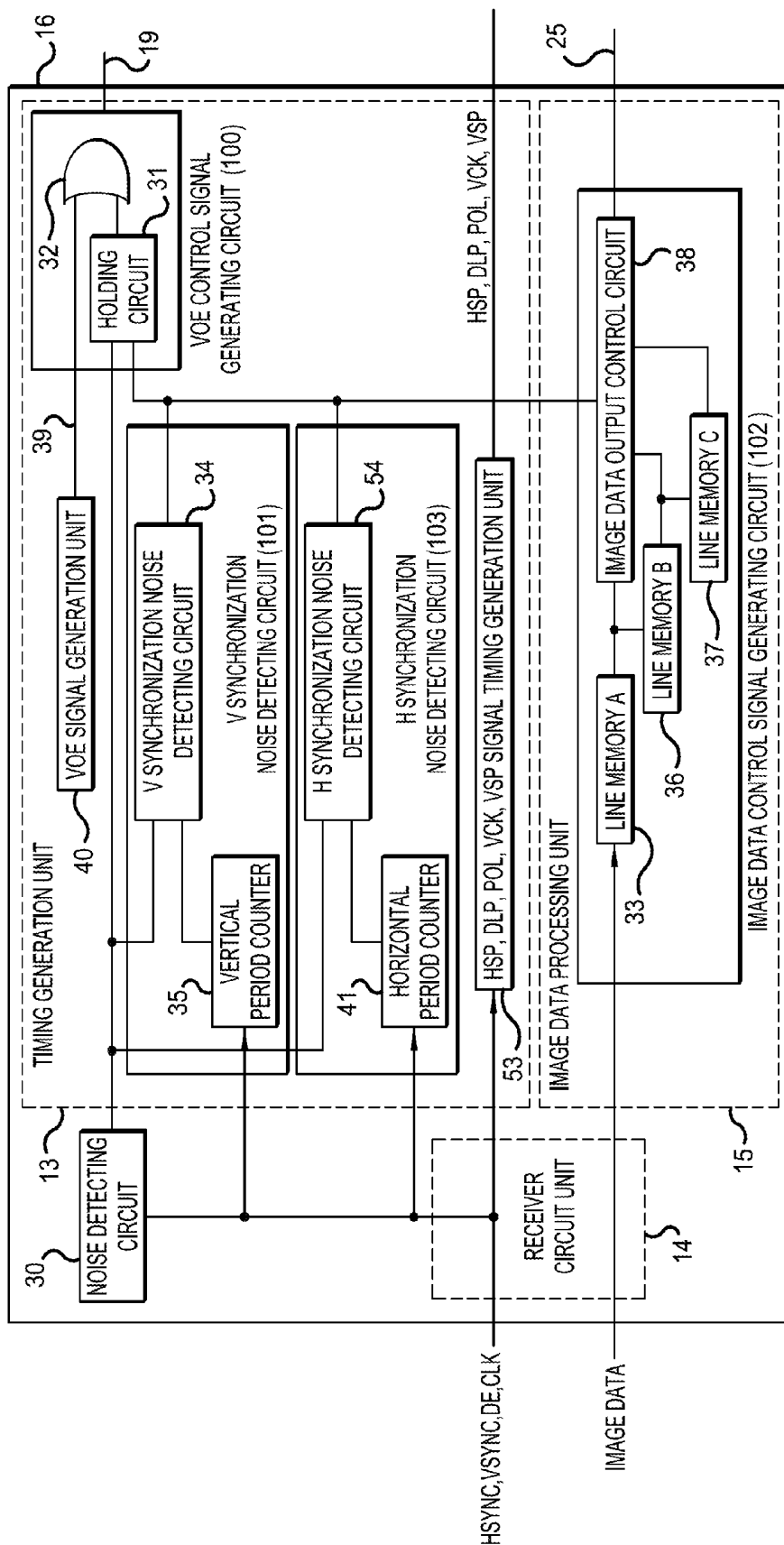


FIG.11

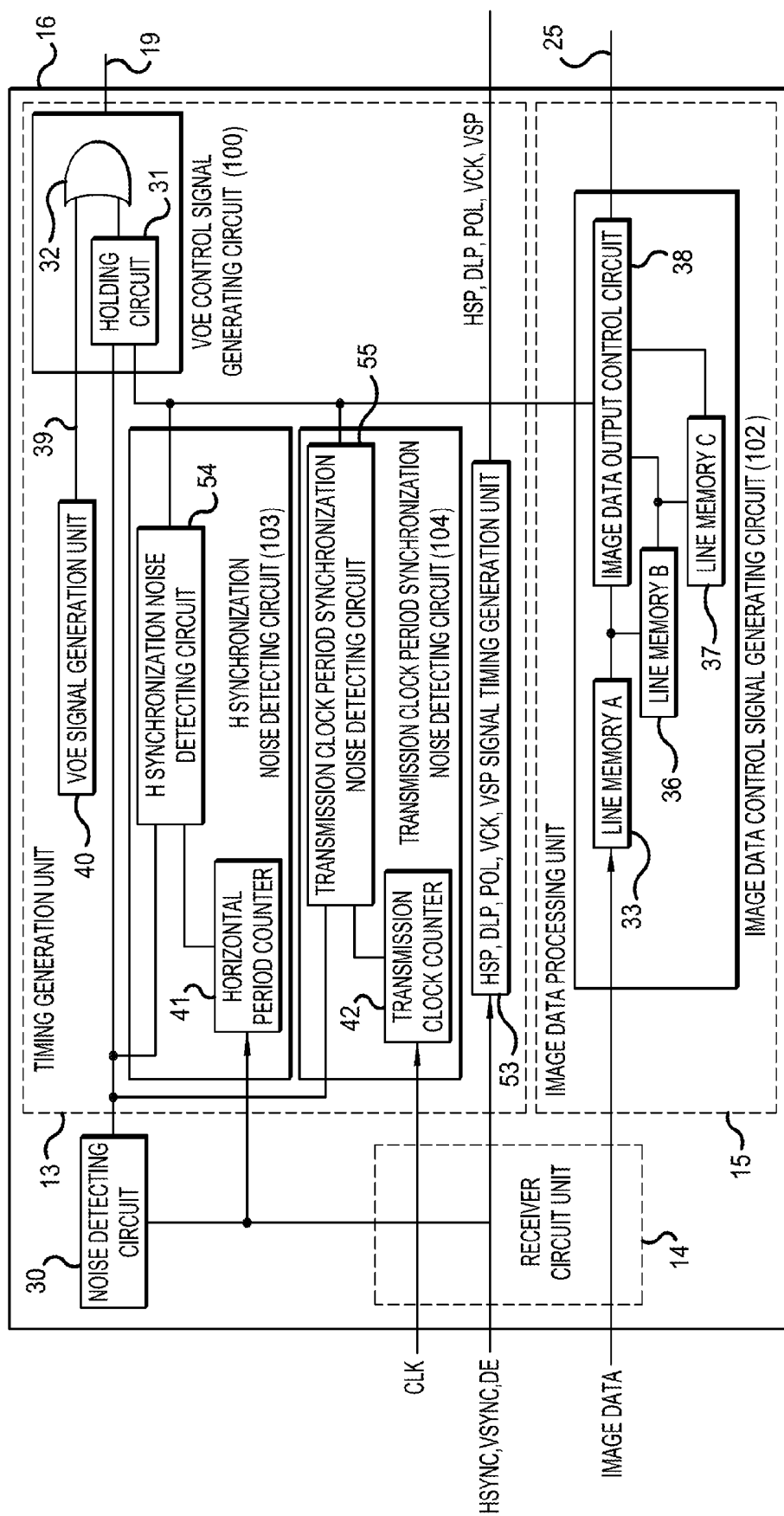


FIG.12

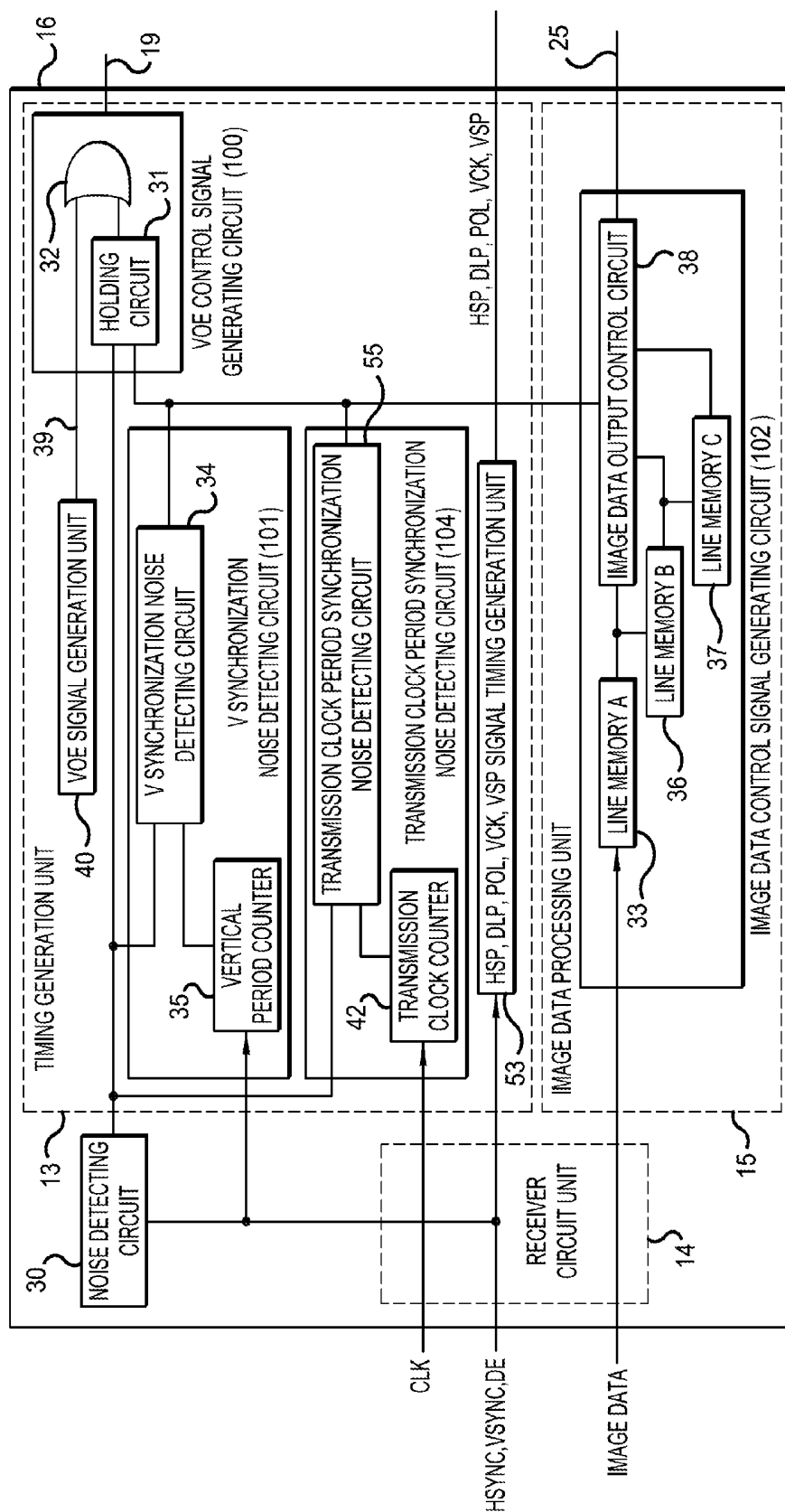


FIG.13

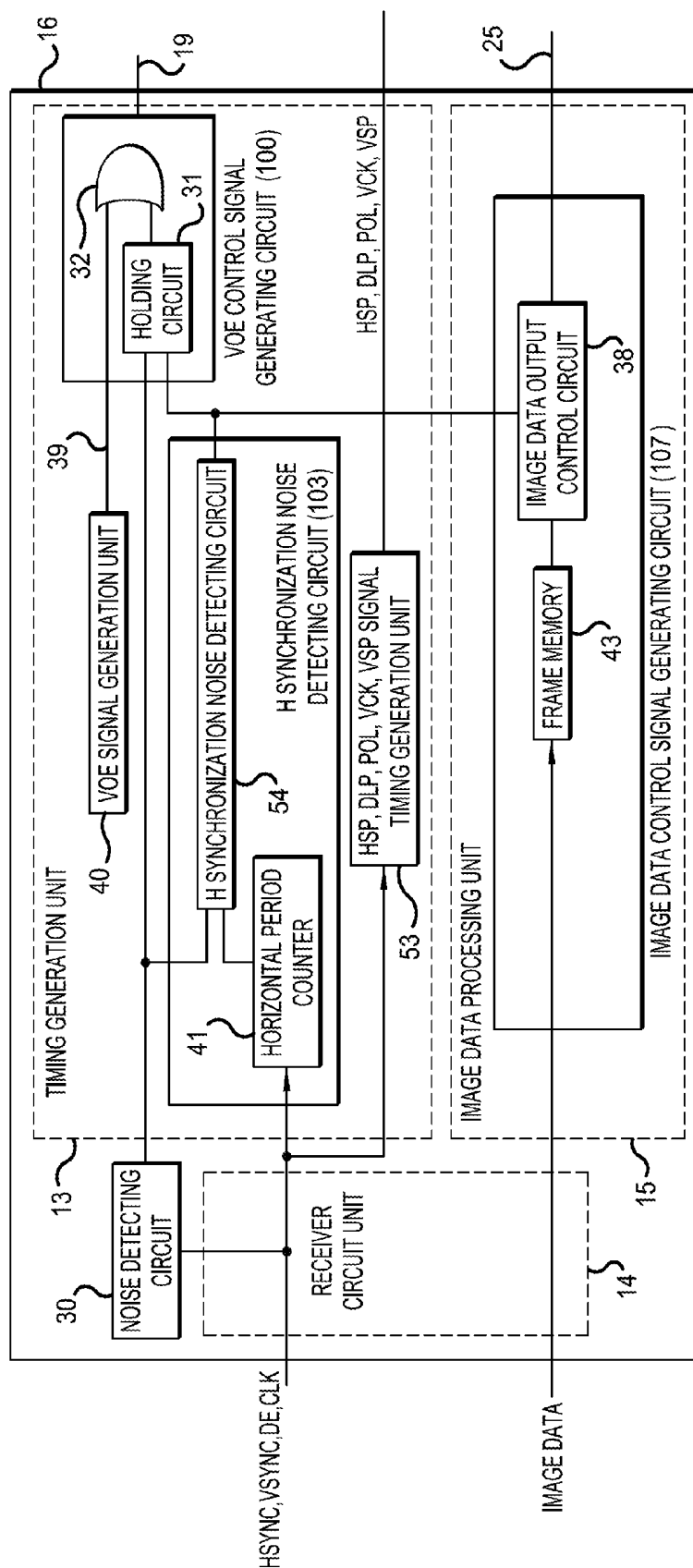


FIG.14

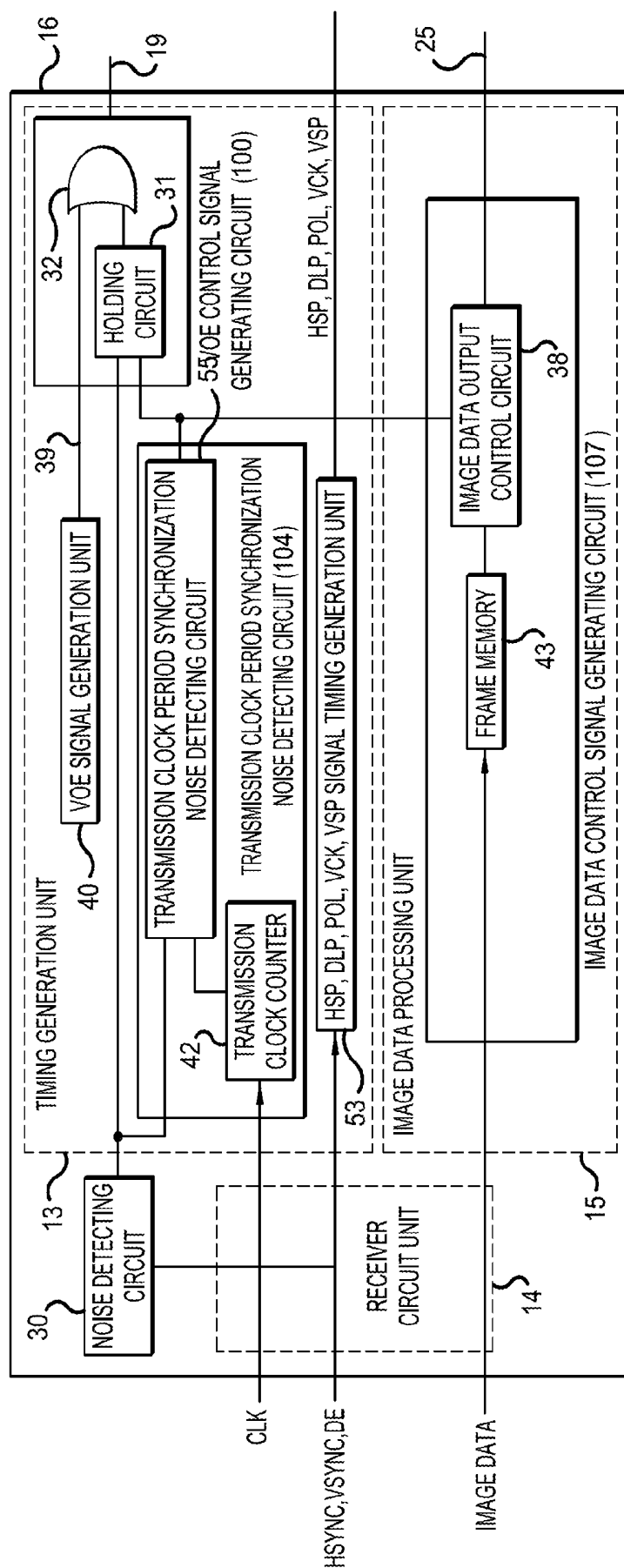


FIG.15

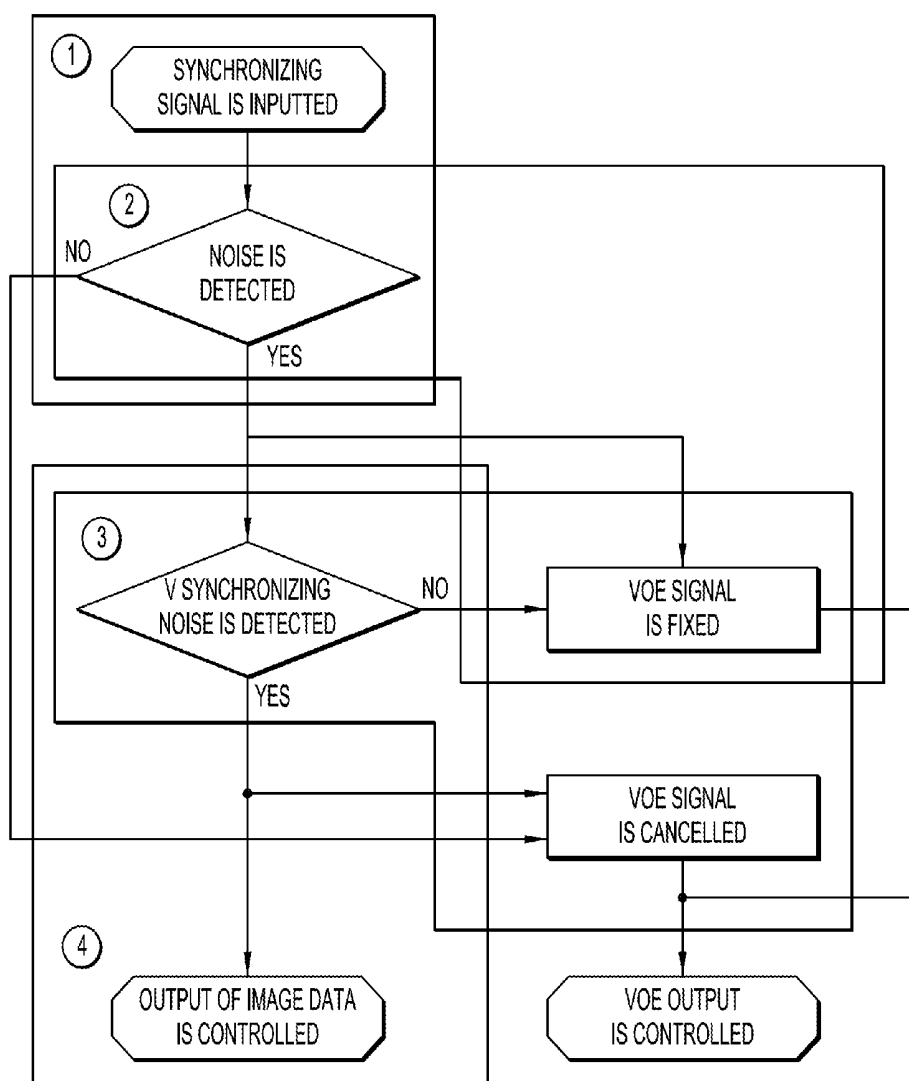


FIG.16

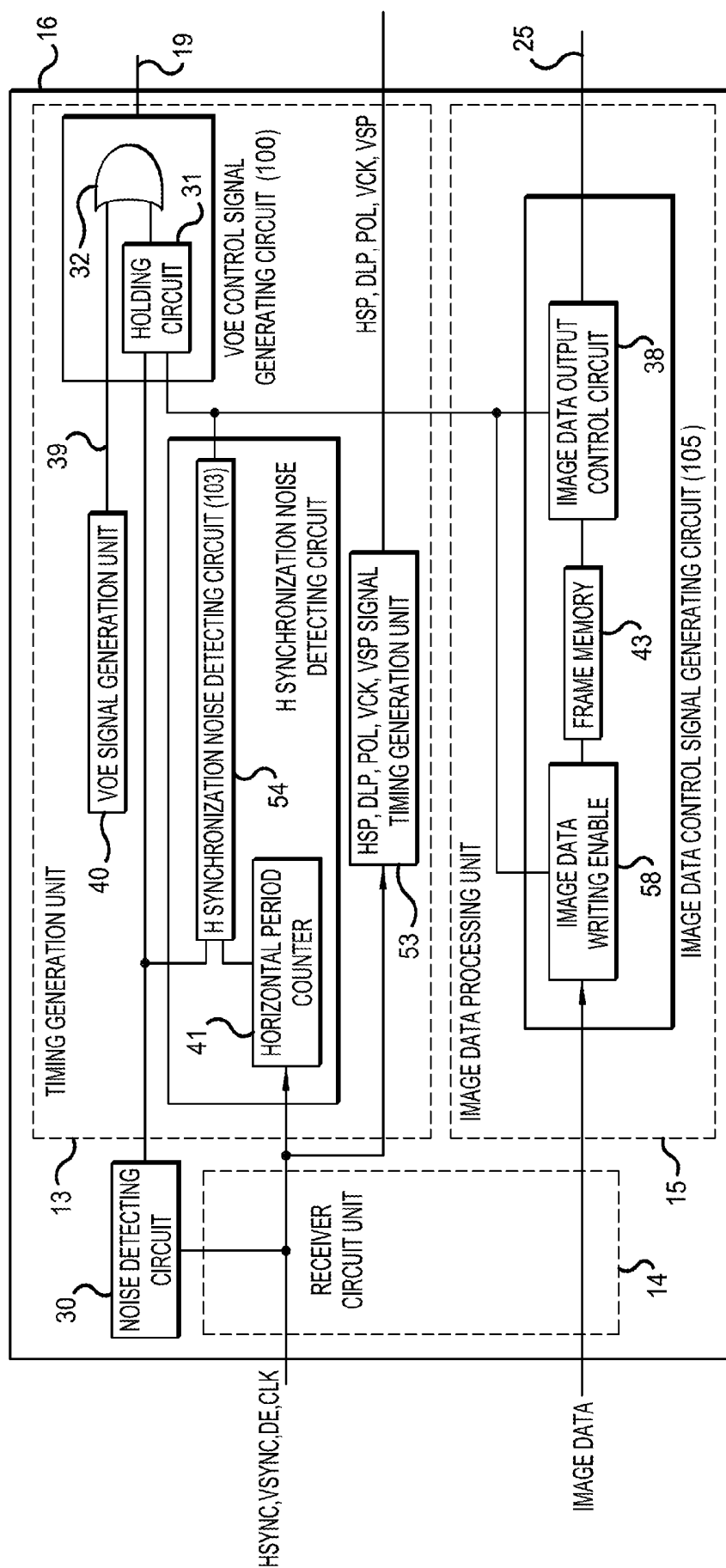


FIG.17

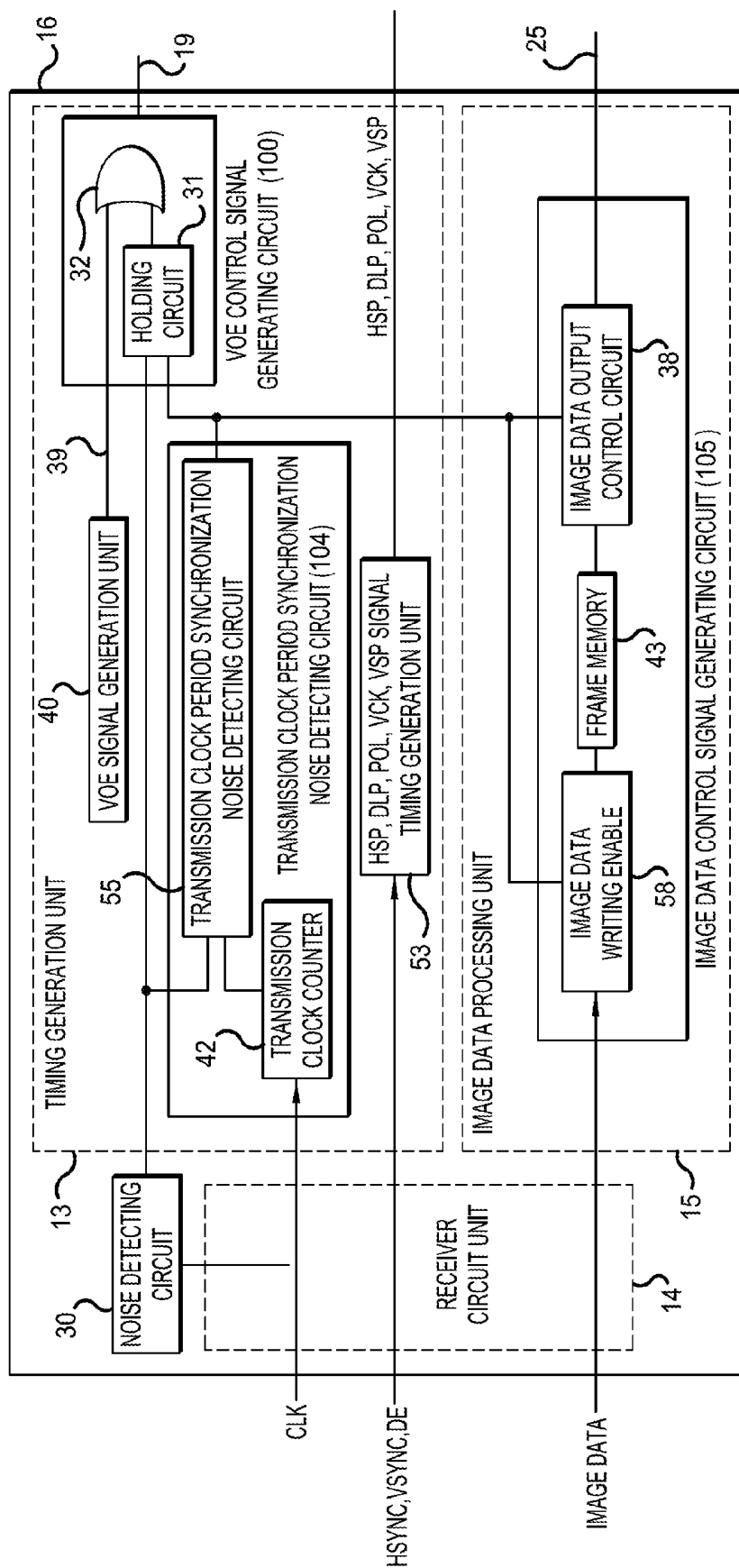


FIG.18

TIMING CONTROLLER AND DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to timing controllers and display devices. In particular, the present invention relates to a timing controller and a display device, which can inhibit an influence by applied exogenous noise from appearing on a liquid crystal display when the exogenous noise such as exogenous noise synchronizing with a synchronizing signal (such as HSYNC, VSYNC, or DE) or a transmission clock period is applied, and can be achieved without enlarging the size of a circuit.

[0003] 2. Description of the Related Art

[0004] A timing controller for a liquid-crystal display device generates a control signal for a liquid crystal driving sorting driver and a liquid crystal driving gate driver based on a reference signal, such as HSYNC (horizontal synchronizing signal), VSYNC (vertical synchronizing signal), or DE (composite synchronizing signal), input into a liquid-crystal display device. Therefore, an incorrect control signal may be outputted, and a malfunction in which noise is generated or a screen is changed on a liquid crystal display may be caused when exogenous noise such as static electricity is mixed into a reference signal during display action.

[0005] Conventional timing controllers have had many configurations in which superimposition of noise synchronizing with each synchronizing signal and transmission clock period on synchronizing signals and image data fed from the outside has such an influence on the display of liquid-crystal display devices that the noise is recognized as a normal signal or a black screen is outputted depending on the size of the noise. In recent years, the number of users performing evaluation in which noise is intentionally introduced from the outside has been increased, so that immunity to synchronizing noise and the like has been needed.

[0006] FIG. 4 illustrates the configuration of a timing controller 12 in a conventional liquid-crystal display device, and FIG. 5 illustrates a conventional liquid-crystal display device 1.

[0007] In FIG. 5, the conventional liquid-crystal display device 1 includes: a liquid crystal display 2 including a plurality of scanning line electrodes 18 disposed at predetermined spacings in an X-direction, a plurality of signal line electrodes 17 disposed at predetermined spacings in a Y-direction, liquid crystal cells 51 that are sandwiched between the electrodes so that the electrodes intersect each other and that have equivalently formed capacitive loads, common electrodes (not illustrated), thin film transistors (TFTs) 50 for driving the corresponding liquid crystal cells 51, and capacitors 52 that accumulates data charge during one vertical synchronization period; a signal line electrode driving circuit 6 including one or more signal line driving source drivers IC8; a scanning line electrode driving circuit 3 including one or more scanning line driving gate drivers IC9; and a timing controller 12.

[0008] In FIG. 4, the timing controller 12 for a conventional display device includes: a receiver circuit unit 14 for synchronizing each synchronizing signal of HSYNC, VSYNC, and DE fed from the outside and an image data signal fed from the outside with a CLK signal fed from the outside; a timing generation unit 13 that generates a control signal VSP for driving a scanning line driving gate driver IC9 and a signal

line driving source driver IC8 (start pulse signal for scanning line driving gate driver IC), VCK (clock signal for scanning line driving gate driver IC), a signal VOE for output control of a scanning line driving gate driver IC9 (output enable signal for scanning line driving gate driver IC), HSP (start pulse signal for signal line driving source driver IC), DLP (data latch pulse signal for signal line driving source driver IC), and POL (alternate-current driving polarity reversion signal); and an image data processing unit 15 that processes image data fed from the outside. Each synchronizing signal and image data outputted from the receiver circuit unit 14 are signals synchronized with CLK (clock signal) fed from the outside.

[0009] The timing controller 12 outputs the image data for each driver and the control signal VOE described above from timing information for display, based on a synchronizing signal, such as a clock (hereinafter "CLK") or horizontal synchronizing signal (hereinafter "HSYNC"), a vertical synchronizing signal (hereinafter "VSYNC"), or a composite synchronizing signal (hereinafter "DE"), and image data, fed from the outside.

[0010] In the signal line electrode driving circuit 6, each signal line driving source driver IC8 takes image data at the timing of HSP (start pulse signal for signal line driving source driver IC), DLP (data latch pulse signal for signal line driving source driver IC), POL (alternate-current driving polarity reversion signal), and CLK outputted from the timing controller 12, and each item of image data in each pixel corresponding to one line is converted into a voltage value, which is fed to a pixel electrode in a panel for liquid crystals, corresponding to one line through a drain electrode in TFT.

[0011] The scanning line driving gate driver IC9 of the scanning line electrode driving circuit 3 controls all scanning line electrodes of each TFT as described above on a one-line basis in synchronism with a VCK signal based on VSP (start pulse signal for scanning line driving gate driver IC), VCK (clock signal for scanning line driving gate driver IC), and VOE (output enable signal for scanning line driving gate driver IC) outputted from the timing controller 12 and applies a gradation voltage, fed from the signal line driving source driver 8 at the time of conduction, to a pixel electrode by starting the sequential conduction of each TFT corresponding to one line in an upper or lower portion in the Y-direction.

[0012] In order to drive the liquid-crystal display device 1 as described above, synchronizing signals such as HSYNC, VSYNC, and DE are required for the timing controller 12, and a control signal for the scanning line driving gate driver IC9 and a control signal for a signal line driving source driver IC8 are generated from the synchronizing signals. Therefore, when external noise is superposed on synchronizing signals such as HSYNC, VSYNC, DE, and CLK, the control signals for the scanning line driving gate driver IC9 and the signal line driving source driver IC8 are synchronized with the incorrect synchronizing signals, on which the noise is superimposed, and therefore differ from normal control signals. When the control signals differ from a normal state, a phenomenon such as a display moved upward and downward with respect to a liquid crystal display (hereinafter "V synchronization displacement"), a display in which lines are horizontally formed (hereinafter "line noise"), the flicker of a screen (hereinafter "screen flash"), or stopping of a screen with a certain fixed color (hereinafter "fixed-colored screen display) is caused (hereinafter "malfunction state").

CITATION LIST

Patent Literature

[0013] [Patent Literature 1] Japanese Patent Laid-Open No. 2008-241828

[0014] [Patent Literature 2] Japanese Patent Laid-Open No. 2006-98923

[0015] [Patent Literature 3] Japanese Patent Laid-Open No. 2009-109955

[0016] [Patent Literature 4] Japanese Patent Laid-Open No. 06-105262

[0017] In a general method for preventing such a malfunction state and a noise screen as described above, noise is prevented from propagating in a timing controller 12 by disposing a noise filter for each synchronizing signal of HSYNC, VSYNC, DE, and CLK, to achieve normal action of a control signal for a scanning line driving gate driver IC9 and a signal line driving source driver IC8. However, only the disposition of the noise filter does not make it possible to completely improve the malfunction state when noise is synchronized with each synchronizing signal at timing where the noise is superimposed. Technologies to use a noise filter in order to prevent false recognition of a synchronizing signal due to exogenous noise in a timing controller 12 used in a liquid-crystal display device are disclosed in, for example, Japanese Patent Laid-Open No. 2008-241828 (Patent Literature 1), Japanese Patent Laid-Open No. 2006-98923 (Patent Literature 2), and Japanese Patent Laid-Open No. 2009-109955 (Patent Literature 3). In the literatures, noise is detected being superimposed on a synchronizing signal, and the output enable (VOE) of a scanning line driving gate driver IC9 is controlled to OFF when the noise is detected, to prevent a voltage from being applied from a signal line driving source driver IC8 to TFT. Since it is impossible to remove noise through a filter from image data outputted from a signal line driving source driver IC8, it is necessary to prevent the noise from being displayed on a liquid crystal display. Since the noise is detected being superimposed on the synchronizing signal, it is considered that the image data on which the noise is superimposed is also outputted for the output of the signal line driving source driver IC8 when it is considered that the noise is also superimposed on the image data. Accordingly, in the methods, the image data on which the noise is superimposed is prevented from being applied to TFT by setting the output enable of the scanning line driving gate driver IC9 at OFF, and the noise superimposed on the image data is inhibited from appearing by keeping a voltage applied to TFT prior to the application of the noise.

[0018] However, the methods are based on the assumption that mainly superimposed noise is randomly generated. For example, when exogenous noise as synchronizing with a synchronizing signal (such as HSYNC, VSYNC, or DE) or a transmission CLK period is applied, the output of the scanning line driving gate driver IC9 always becomes OFF only during a period in which the noise is superimposed, and therefore, a potential applied to TFT is gradually self-discharged. There is a problem that as a result, when a luminance difference appears in a line in scanning line driving, in which the output is OFF, the line is seen as noise.

[0019] Since it is impossible to remove noise superimposed on image data through a filter as mentioned above, image data for being supplemented as the image data in the application of the noise is separately needed. Japanese Patent Laid-Open No. 06-105262 (Patent Literature 4) discloses a method for

detecting the degradation of image data and displaying the data of a frame before degrading without being processed; however, there is a problem that since a frame memory for saving the data of the frame is needed, the size of a circuit is increased, and increase in current and the like occur. In addition, there is a problem that drive in the same place is stopped due to synchronizing noise, whereby alternate-current drive is stopped, a direct-current component remains, the synchronizing noise then disappears, and a ghost, an afterimage, or the like is produced in the case of returning to normal driving.

[0020] An objective of the present invention is to achieve, in the case of applying exogenous noise as synchronizing with a synchronizing signal (such as HSYNC, VSYNC, or DE) or a transmission CLK period, inhibition of an influence by the applied noise from appearing on a liquid crystal display without increasing the size of a circuit.

SUMMARY OF THE INVENTION

[0021] In accordance with the present invention, the output enable (VOE) of a scanning line driving gate driver IC9 is prevented from being always in an OFF state by detecting noise detected in a noise detecting circuit 30 synchronizing with a synchronizing signal or a transmission CLK period. Since it is necessary to cancel the OFF state of the output enable (VOE) of the scanning line driving gate driver IC9 when the detected noise is detected synchronizing with the synchronizing signal or the transmission CLK period, it is further needed to inhibit noise superimposed on image data from appearing. In accordance with the present invention, image data corresponding to three lines is saved using a line memory rather than a frame memory. When noise is detected, line data in which the noise is generated is supplemented using data before a line, in which the noise is detected, by one line, and data following a line in which the noise is detected, whereby the noise can be inhibited from appearing.

[0022] In accordance with the present invention, installation of, in addition to a conventional noise filter, a filter for synchronous detection makes it possible to deal with various types of noise. In particular, by avoiding stop of driving in the same place due to synchronizing noise, alternate-current drive can be continued to avoid display degradation such as a ghost or an afterimage. In addition, the function of controlling image data in application of noise makes it possible to reduce an influence on a liquid crystal display.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] FIG. 1 is a configuration diagram of a timing controller in Example 1 of a display device according to the present invention;

[0024] FIG. 2 is a configuration diagram of a liquid-crystal display device in Example 1 of a display device according to the present invention;

[0025] FIG. 3 is an action timing chart of Example 1 of a display device according to the present invention;

[0026] FIG. 4 is a configuration diagram of a conventional timing controller;

[0027] FIG. 5 is a configuration diagram of a conventional liquid-crystal display device;

[0028] FIG. 6 is a configuration diagram of a timing controller in Example 2 of a display device according to the present invention;

[0029] FIG. 7 is a configuration diagram of a timing controller in Example 3 of a display device according to the present invention;

[0030] FIG. 8 is a configuration diagram of a timing controller in Example 4 of a display device according to the present invention;

[0031] FIG. 9 is a configuration diagram of a timing controller in Example 5 of a display device according to the present invention;

[0032] FIG. 10 is a configuration diagram of a timing controller in Example 6 of a display device according to the present invention;

[0033] FIG. 11 is a configuration diagram of the timing controller in Example 4 of a display device according to the present invention;

[0034] FIG. 12 is a configuration diagram of the timing controller in Example 4 of a display device according to the present invention;

[0035] FIG. 13 is a configuration diagram of the timing controller in Example 4 of a display device according to the present invention;

[0036] FIG. 14 is a configuration diagram of the timing controller in Example 6 of a display device according to the present invention;

[0037] FIG. 15 is a configuration diagram of the timing controller in Example 6 of a display device according to the present invention;

[0038] FIG. 16 is a flowchart of Example 1 of a display device according to the present invention;

[0039] FIG. 17 is a configuration diagram of the timing controller in Example 5 of a display device according to the present invention; and

[0040] FIG. 18 is a configuration diagram of the timing controller in Example 5 of a display device according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Example 1

[0041] FIG. 1 illustrates the configuration of a timing controller for a display device which is one of the examples of the present invention, and FIG. 2 illustrates the configuration of a liquid-crystal display device which is one of the examples of the present invention.

[0042] In FIG. 2, a liquid-crystal display device 1 of the present invention includes: a liquid crystal display 2 including a plurality of scanning line electrodes 18 disposed at predetermined spacings in an X-direction, a plurality of signal line electrodes 17 disposed at predetermined spacings in a Y-direction, liquid crystal cells 51 that are sandwiched between the electrodes so that the electrodes intersect each other and that have equivalently formed capacitive loads, common electrodes (not illustrated), thin film transistors (TFTs) 50 for driving the corresponding liquid crystal cells, and capacitors 52 that accumulates data charge during one vertical synchronization period; a signal line electrode driving circuit 6 including one or more signal line driving source drivers IC8; a scanning line electrode driving circuit 3 including one or more scanning line driving gate drivers IC9; and a timing controller 16.

[0043] In FIG. 1 and FIG. 2, the liquid-crystal timing controller 16 of the present invention includes: a noise detecting circuit 30 for detecting noise for a synchronizing signal such

as HSYNC, VSYNC, or DE fed from the outside; a holding circuit 31 for holding a signal at a High level after detection of noise; a control signal VOE39 for a scanning line driving gate driver IC9 generated from the synchronizing signal; a VOE control signal generating circuit 100 including a circuit for OR of signals from the holding circuit 31 and the control signal VOE39; a V synchronization noise detecting circuit 101 including a V synchronization noise detecting circuit 34 for detecting a line, in which noise is generated, using a vertical period counter 35 for measuring the number of effective lines from the synchronizing signal; a line memory A33, a line memory B36, and a line memory C37 for storing image data fed from the outside in each line; an image data control signal generating circuit 102 including an image data output control circuit 38 for controlling image data stored in the line memory A33, the line memory B36, and the line memory C37 in each detection of V synchronism noise; and a timing generation unit 53 for generating an HSP signal for a signal line driving source driver, a DLP signal, a VCK signal for a scanning line driving gate driver, a VSP signal, and a polarity reversion signal POL for alternate-current-driving a liquid crystal display. Only any one of the synchronizing signals of HSYNC, VSYNC, and DE fed from the outside may also be fed, or DE may also be generated from the signals of HSYNC and VSYNC.

[0044] The timing controller 16 outputs the image data for each driver and the control signal from timing information for display, based on a synchronizing signal, such as a clock or horizontal synchronizing signal (hereinafter "HSYNC"), a vertical synchronizing signal (hereinafter "VSYNC"), or a composite synchronizing signal (hereinafter "DE"), and image data, fed from the outside. The timing controller of the present invention mainly includes a noise detecting circuit, a VOE control signal generating circuit 100, a V synchronization noise detecting circuit 101, and the image data control signal generating circuit 102.

[0045] In the signal line electrode driving circuit 6, which has a multiple-stage configuration in which signal line driving source drivers IC are connected in series, each signal line driving source driver takes image data at the timing of an HSP signal, a DLP signal, a POL signal, and a DCK signal outputted from the timing controller 16, and each item of image data in each pixel corresponding to one line is converted into a voltage value, which is fed to a pixel electrode in a liquid crystal panel, corresponding to one line through a drain electrode in TFT.

[0046] The scanning line driving gate driver IC9 of the scanning line electrode driving circuit 3 controls all scanning line electrodes of each TFT as described above on a one-line basis in synchronism with a VCK signal based on a VSP signal, a VOE signal, and a VCK signal outputted from the timing controller 16 and applies a gradation voltage, fed from the signal line driving source driver at the time of conduction, to a pixel electrode by starting the sequential conduction of each TFT corresponding to one line in an upper or lower portion.

[0047] The action of the timing controller of the present invention will be described below.

[0048] First, a method for controlling the control signal VOE of the scanning line driving gate driver IC9 is explained. The timing chart of action is illustrated in FIG. 3. The explanation is given below with reference to FIG. 3.

[0049] The timing controller 16 which is one of the examples of the present invention first requires a noise detect-

ing circuit 30 in order to detect noise superimposed on each synchronizing signal of HSYNC, VSYNC, and DE fed from the outside.

[0050] The noise detecting circuit 30 generates a normal synchronizing signal 59 for display resolution, within its inside, for example, to a synchronizing signal fed from the outside at a change point, where a signal is switched to from 0 to 1, as a trigger. Noise detection can be achieved by recognizing, as noise, a change at timing that is not timing where a normal change occurs, by comparing the normal synchronizing signal 59 with a synchronizing signal 56 fed from the outside. In accordance with the present invention, a V synchronization noise detecting circuit 34 is further required.

[0051] The V synchronization noise detecting circuit 34 carries out measurement by detecting a line in which a noise signal 57 detected in the noise detecting circuit 30 is generated. A vertical period counter 35 is required for measuring a vertical period using the normal synchronizing signal 59 in order to detect the line in which the noise signal is generated. The line in which the noise is generated using the timing of the noise signal 57 detected in the noise detecting circuit 30 and the vertical period counter 35 is detected, and it is detected whether multiple items of noise are generated on the same line.

[0052] Furthermore, in accordance with the present invention, the output enable control signal VOE19 of a scanning line driving gate driver IC9 is controlled to control the application, to a pixel electrode, a gradation voltage fed from a signal line driving source driver IC8 at the time of conduction. Therefore, the output enable control signal VOE19 of the scanning line driving gate driver IC9 is turned OFF at each timing of generation of noise detected in the noise detecting circuit 30, and the gradation voltage fed from the signal line driving source driver IC8 at the time of conduction is prevented from being applied to the pixel electrode. Furthermore, the output enable control signal VOE19 of the scanning line driving gate driver IC9 is turned ON at the timing of detecting multiple items of noise, in the same line, detected in a V synchronization noise detecting circuit 101, and the gradation voltage fed supplied from the signal line driving source driver IC8 at the time of conduction is applied to the pixel electrode.

[0053] A method for controlling image data will be described below.

[0054] Since image data is fed from the outside, noise may be superimposed on the image data in such a manner as in the case of synchronizing signals. However, the noise is not able to be detected or removed through a filter because of depending on display data. In the present invention, first, image data on an Nth line fed from the outside is stored in a line memory A33. The line memory A33 is fed to a line memory B36 and an image data output control circuit 38 without being processed. As a result, the line memory A33 can newly store image data on an (N+1)th line. The line memory B36 is similarly fed to a line memory C37 and the image data output control circuit 38. In such a manner, image data on an (N+2)th line, the image data on the (N+1)th line, and the image data on the Nth line are stored in the line memory A33, the line memory B36, and the line memory C37, respectively, and the image data corresponding to the three lines can be saved in the timing controller 16. The image data output control circuit 38 allows data fed from the outside to control output image data 25 at the timing of detection in the V synchronization noise detecting circuit 101. As a control method, for example, out-

puts from the line memory A33, the line memory B36, and the line memory C37 can be averaged to achieve the outputs.

[0055] A method for inhibiting noise from appearing on a liquid crystal display in the case of superposing the noise synchronized with a synchronizing signal is described below. A flowchart is illustrated in FIG. 16.

[0056] The output enable control signal VOE19 generated from the VOE control signal generating circuit 100 and V synchronization noise detecting circuit 101 mentioned above and an image data signal 26 generated in the image data control signal generating circuit 102 are required. The flow of the action will be described below.

[0057] (1) When noise is superposed on each synchronizing signal of HSYNC, VSYNC, and DE fed from the outside, the noise is detected by the noise detecting circuit 30.

[0058] (2) The signal of the output enable control signal VOE19 is fixed at High or Low by detecting the noise. The output enable can be turned OFF by the fixation.

[0059] (3) The noise for each synchronizing signal of HSYNC, VSYNC, and DE fed from the outside is noise on each synchronizing signal or transmission CLK period, the High or Low fixation of the signal of the output enable control signal VOE19 is canceled by the V synchronization noise detecting circuit 101.

[0060] (4) As for data on which noise is superposed on image data on the liquid crystal display, a gradation voltage is fed from the signal line driving source driver IC8 at the time of conduction is applied to a pixel electrodes by the canceling, and therefore, the image data on which the noise is superimposed is supplemented with image data outputted from the image data control signal generating circuit 102.

[0061] In the present example, the example in which the timing controller of the present invention is applied to the liquid-crystal display device is described in FIG. 2. However, the timing controller can be applied to other display devices such as organic EL and electronic papers without being limited to the liquid-crystal display device.

[0062] In such a manner, a malfunction state in the case of superimposing noise synchronized in each synchronizing signal is avoided, and noise on a liquid crystal display is inhibited from appearing.

Example 2

[0063] FIG. 6 illustrates the configuration of a timing controller 16 in Example 2 of the present invention.

[0064] In FIG. 6, in the timing controller 16 of the present invention, the vertical period counter is used in Example 1 as mentioned above in order to detect a signal with which noise is synchronized from each synchronizing signal fed from the outside whereas V synchronization noise is detected in this case. Thus, an H synchronization noise detecting circuit 103 is included by replacing the vertical period counter with a horizontal period counter 41 and replacing the V synchronization noise detecting circuit 34 with an H synchronization noise detecting circuit 54, whereby a VOE signal and an image data output can be controlled as in Example 1 mentioned above.

Example 3

[0065] FIG. 7 illustrates the configuration of a timing controller 16 in Example 3 of the present invention.

[0066] In FIG. 7, in the timing controller 16 of the present invention, a transmission clock period synchronization noise

detecting circuit **104** is included by replacing the vertical period counter with a transmission clock counter **42** and replacing the V synchronization noise detecting circuit **34** with a transmission clock period synchronization noise detecting circuit **55** in order to detect a signal with which noise is synchronized from each synchronizing signal fed from the outside, whereby a VOE signal and an image data output can be controlled as in Example 1 mentioned above.

Example 4

[0067] FIG. 8 illustrates the configuration of a timing controller **16** in Example 4 of the present invention.

[0068] In FIG. 8, the V synchronization noise detecting circuit **101** included in Example 1 as mentioned above, the H synchronization noise detecting circuit **103** included in Example 2, and the transmission clock period synchronization noise detecting circuit **104** for included in Example 3 are simultaneously included, whereby noise synchronized with each synchronizing signal and transmission clock can be detected.

[0069] Similarly, FIG. 11, FIG. 12, and FIG. 13 illustrate the configurations of timing controllers **16** in the case of simultaneously including the V synchronization noise detecting circuit **101** included in Example 1 as mentioned above and the H synchronization noise detecting circuit **103** included in Example 2, in the case of simultaneously including the H synchronization noise detecting circuit **103** included in Example 2 as mentioned above and the transmission clock period synchronization noise detecting circuit **104** included in Example 3, and in the case of simultaneously including the V synchronization noise detecting circuit **101** included in Example 1 as mentioned above and the transmission clock period synchronization noise detecting circuit **104** included in Example 3, respectively. In such cases, noise synchronized with each synchronizing signal and transmission clock can also be similarly detected.

Example 5

[0070] FIG. 9 illustrates the configuration of a timing controller **16** in Example 5 of the present invention.

[0071] The line memory **A33**, the line memory **B36**, and the line memory **C37** are included in the image data control signal generating circuit **102** in Example 1 as mentioned above. However, by only a line memory **D44** and detecting noise to control writing in the line memory **D44** in image data writing Enable **58**, the same image data as image data prior to the time of the generation of the noise by one line can be outputted without being processed, and image data on which the noise is superimposed can be suppressed from influencing a display on a liquid crystal display.

[0072] In addition, FIG. 17 and FIG. 18 illustrate the configurations of timing controllers **16** in a case in which the configuration of the present example is carried out in Example 2 as mentioned above and in a case in which the configuration of the present example is carried out in Example 3 as mentioned above, respectively. Such cases can also be similarly carried out.

Example 6

[0073] FIG. 10 illustrates the configuration of a timing controller **16** in Example 6 of the present invention.

[0074] The line memory **A**, the line memory **B**, and the line memory **C** are included in the image data control signal

generating circuit **102** in Example 1 as mentioned above. However, by a frame memory **43**, the same image data as image data prior to the time of the generation of the noise by one frame can be outputted without being processed, and image data on which the noise is superimposed can be suppressed from influencing a display on a liquid crystal display. In addition, FIG. 14 and FIG. 15 illustrate the configurations of timing controllers **16** in a case in which the configuration of the present example is carried out in Example 2 as mentioned above and in a case in which the configuration of the present example is carried out in Example 3 as mentioned above, respectively. Such cases can also be similarly carried out.

REFERENCE SIGNS LIST

- [0075] 1 Liquid-crystal display device
- [0076] 2 Liquid crystal display
- [0077] 3 Scanning line electrode driving circuit
- [0078] 6 Signal line electrode driving circuit
- [0079] 8 Signal line driving source driver IC
- [0080] 9 Scanning line driving gate driver IC
- [0081] 12 Timing controller
- [0082] 13 Timing generation unit
- [0083] 14 Receiver circuit unit
- [0084] 15 Image data processing unit
- [0085] 16 Timing controller
- [0086] 17 Signal line electrode
- [0087] 18 Scanning line electrode
- [0088] 19 Output enable control signal VOE
- [0089] 25 Output image data
- [0090] 26 Image data signal
- [0091] 30 Noise detecting circuit
- [0092] 31 Holding circuit
- [0093] 33 Line memory A
- [0094] 34 V synchronization noise detecting circuit
- [0095] 35 Vertical period counter
- [0096] 36 Line memory B
- [0097] 37 Line memory C
- [0098] 38 Image data output control circuit
- [0099] 39 Control signal VOE
- [0100] 40 VOE signal generation unit
- [0101] 41 Horizontal period counter
- [0102] 42 Transmission clock counter
- [0103] 43 Frame memory
- [0104] 44 Line memory D
- [0105] 50 Thin film transistor (TFT)
- [0106] 51 Liquid crystal cell
- [0107] 52 Capacitor
- [0108] 53 Timing generation unit
- [0109] 54 H synchronization noise detecting circuit
- [0110] 55 Transmission clock period synchronization noise detecting circuit
- [0111] 56 Synchronizing signal
- [0112] 58 Image data writing Enable
- [0113] 57 Noise signal
- [0114] 59 Normal synchronizing signal
- [0115] 100 VOE control signal generating circuit
- [0116] 101 V synchronization noise detecting circuit
- [0117] 102, 105, 107 Image data control signal generating circuit
- [0118] 103 H synchronization noise detecting circuit
- [0119] 104 Transmission clock period synchronization noise detecting circuit

What is claimed is:

1. A timing controller that generates a control signal of a source driver and a gate driver for a signal to be a reference inputted from an outside, the timing controller comprising:

- a noise detecting circuit for detecting an input signal being a signal different from the reference; and
- a V synchronization noise detecting circuit for detecting V synchronization noise in which the input signal that is different from the reference is repeatedly detected in each vertical period,

wherein the timing controller is controlled to:

generate a signal for stopping a control signal of the gate driver in a certain period when the noise detecting circuit detects the signal different from the reference and the V synchronization noise detecting circuit does not detect the V synchronization noise; and

generate a signal for preventing the control signal of the gate driver from stopping when the noise detecting circuit detects the signal different from the reference and the V synchronization noise detecting circuit carries out detection as the V synchronization noise.

2. A timing controller that generates a control signal of a source driver and a gate driver for a signal to be a reference inputted from an outside, the timing controller comprising:

- a noise detecting circuit for detecting an input signal being a signal different from the reference; and
- an H synchronization noise detecting circuit for detecting H synchronization noise in which the input signal that is different from the reference is repeatedly detected in each horizontal period,

wherein the timing controller is controlled to:

generate a signal for stopping a control signal of the gate driver in a certain period when the noise detecting circuit detects the signal different from the reference and the H synchronization noise detecting circuit does not detect the H synchronization noise; and

generate a signal for preventing the control signal of the gate driver from stopping when the noise detecting circuit detects the signal different from the reference and the H synchronization noise detecting circuit carries out detection as the H synchronization noise.

3. A timing controller that generates a control signal of a source driver and a gate driver for a signal to be a reference inputted from an outside, the timing controller comprising:

- a noise detecting circuit for detecting an input signal being a signal different from the reference; and
- an transmission clock synchronization noise detecting circuit for detecting transmission clock synchronization noise in which the input signal that is different from the reference is repeatedly detected in each transmission clock period,

wherein the timing controller is controlled to:

generate a signal for stopping a control signal of the gate driver in a certain period when the noise detecting circuit detects the signal different from the reference and the transmission clock synchronization noise detecting circuit does not detect the transmission clock synchronization noise; and

generate a signal for preventing the control signal of the gate driver from stopping when the noise detecting circuit detects the signal different from the reference and the transmission clock synchronization noise detecting circuit carries out detection as the transmission clock synchronization noise.

4. The timing controller according to claim 1, further simultaneously comprising at least the V synchronization noise detecting circuit and the H synchronization noise detecting circuit.

5. The timing controller according to claim 2, further simultaneously comprising at least the V synchronization noise detecting circuit and the H synchronization noise detecting circuit.

6. The timing controller according to claim 2, further simultaneously comprising at least the H synchronization noise detecting circuit and the transmission clock synchronization noise detecting circuit.

7. The timing controller according to claim 3, further simultaneously comprising at least the H synchronization noise detecting circuit and the transmission clock synchronization noise detecting circuit.

8. The timing controller according to claim 1, further simultaneously comprising at least the V synchronization noise detecting circuit and the transmission clock synchronization noise detecting circuit.

9. The timing controller according to claim 3, further simultaneously comprising at least the V synchronization noise detecting circuit and the transmission clock synchronization noise detecting circuit.

10. The timing controller according to claim 1, wherein input data prior by one line or one frame is outputted to the source driver as output data when the noise detecting circuit detects the signal different from the reference and the V synchronization noise detecting circuit carries out detection as the V synchronization noise.

11. The timing controller according to claim 2, wherein input data prior by one line or one frame is outputted to the source driver as output data when the noise detecting circuit detects the signal different from the reference and the H synchronization noise detecting circuit carries out detection as the H synchronization noise.

12. The timing controller according to claim 3, wherein input data prior by one line or one frame is outputted to the source driver as output data when the noise detecting circuit detects the signal different from the reference and the transmission clock synchronization noise detecting circuit carries out detection as the transmission clock synchronization noise.

13. A display device comprising the timing controller according to claim 1.

14. A display device comprising the timing controller according to claim 2.

15. A display device comprising the timing controller according to claim 3.

* * * * *

当利用同步信号或传输时钟周期施加外源噪声时,抑制施加的噪声的影响不会出现在液晶显示器上,而不会增加电路尺寸。包括:定时控制器,基于作为从外部输入的基准的输入信号,产生扫描线驱动栅极驱动器的控制信号和信号线驱动源驱动器的控制信号;使能信号发生单元,包括:噪声检测电路,用于检测进入输入信号的各种噪声项,并基于来自噪声检测电路的输出,输出用于将栅极驱动器控制信号的输出关闭或接通预定时段的使能信号;当检测在垂直周期中同步的噪声时,图像数据输出控制电路。控制栅极驱动器控制信号以具有空闲时段。

