US 20140362067A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2014/0362067 A1

(43) Pub. Date: Dec. 11, 2014

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(54) SHIFT REGISTER AND DRIVING CIRCUIT FOR LIQUID CRYSTAL DISPLAY

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(21) Appl. No.: **14/301,495**

(22) Filed: **Jun. 11, 2014**

(30) **Foreign Application Priority Data**

Jun. 11, 2013 (CN) 2013102302745

Publication Classification

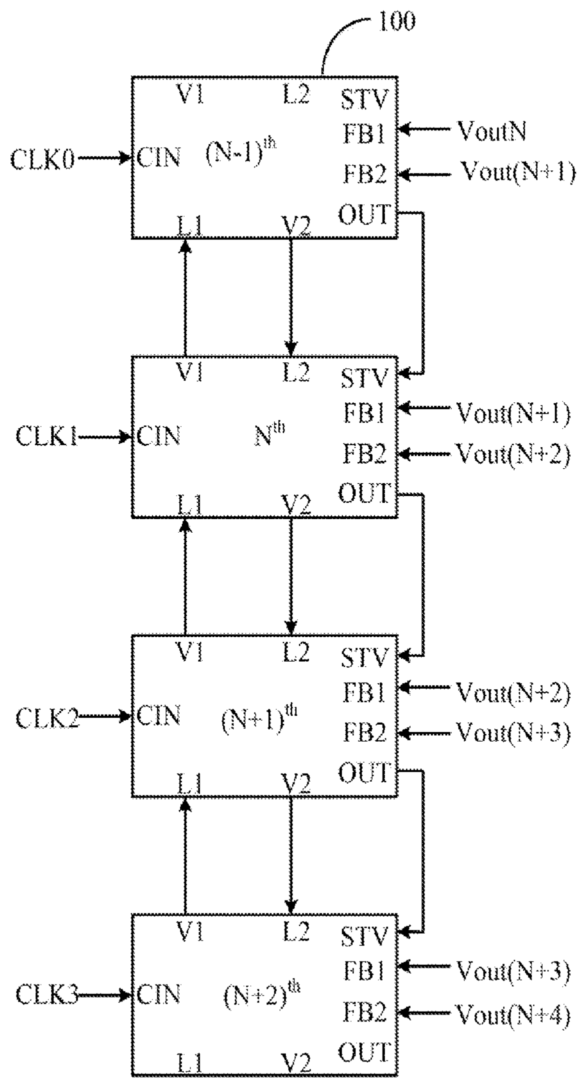
(51) **Int. Cl.**
G09G 3/36 (2006.01)

(52) **U.S. Cl.**
CPC ***G09G 3/3696*** (2013.01)
USPC **345/208**; 345/94

(57) **ABSTRACT**

A shift register for an LCD display includes N shift register units. Each shift register unit outputs a shift signal. An N^{th} shift register unit includes a waveform-shaping unit electrically coupled to an shift signal output terminal of the N^{th} register to perform a waveform-shaping operation on the Nth shift signal according to the $(N+1)^{th}$ shift signal output by an $(N+1)^{th}$ shift register, to reduce the feed-through effect which causes display flicker.

10



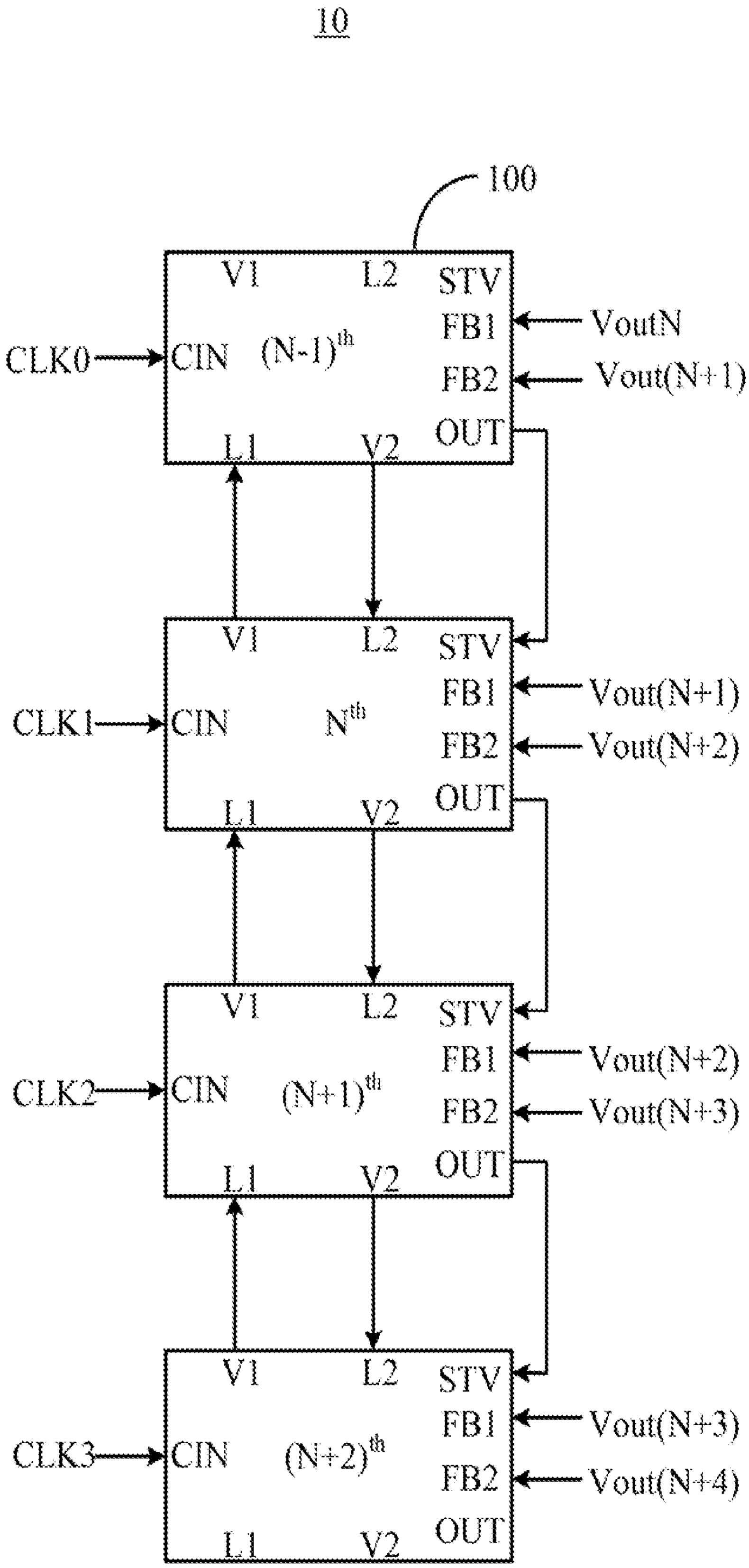

10
100
V1
L2
STV
FB1
VoutN
CLK0
CIN
(N-1)th
FB2
Vout(N+1)
OUT
L1
V2
V1
L2
STV
FB1
Vout(N+1)
CLK1
CIN
Nth
FB2
Vout(N+2)
OUT
L1
V2
V1
L2
STV
FB1
Vout(N+2)
CLK2
CIN
(N+1)th
FB2
Vout(N+3)
OUT
L1
V2
V1
L2
STV
FB1
Vout(N+3)
CLK3
CIN
(N+2)th
FB2
Vout(N+4)
OUT
L1
V2

FIG. 1

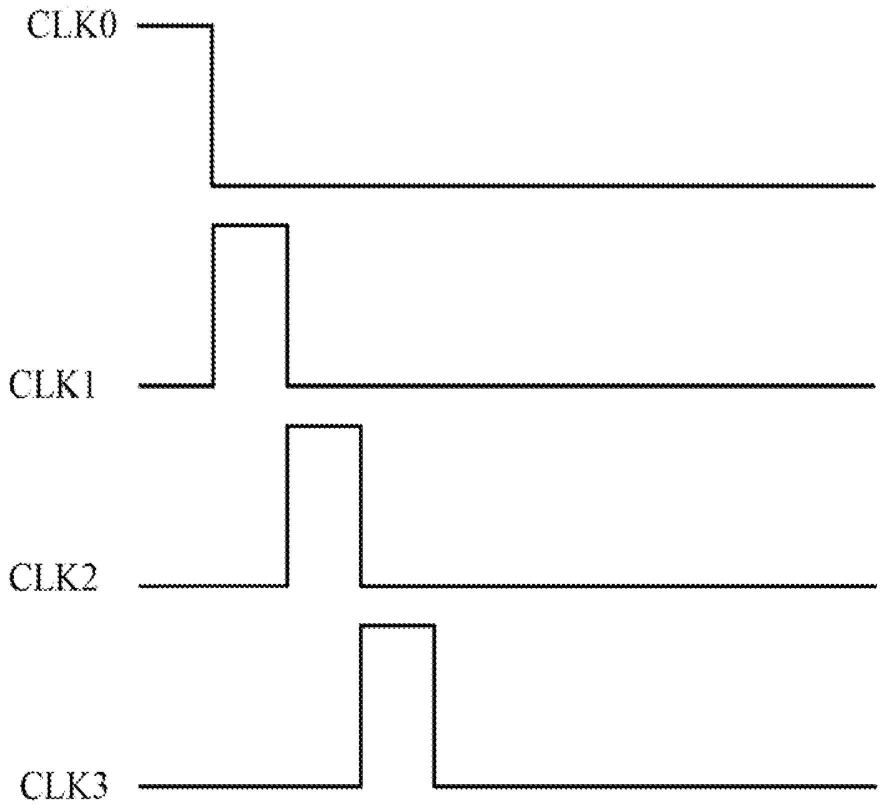


FIG. 2

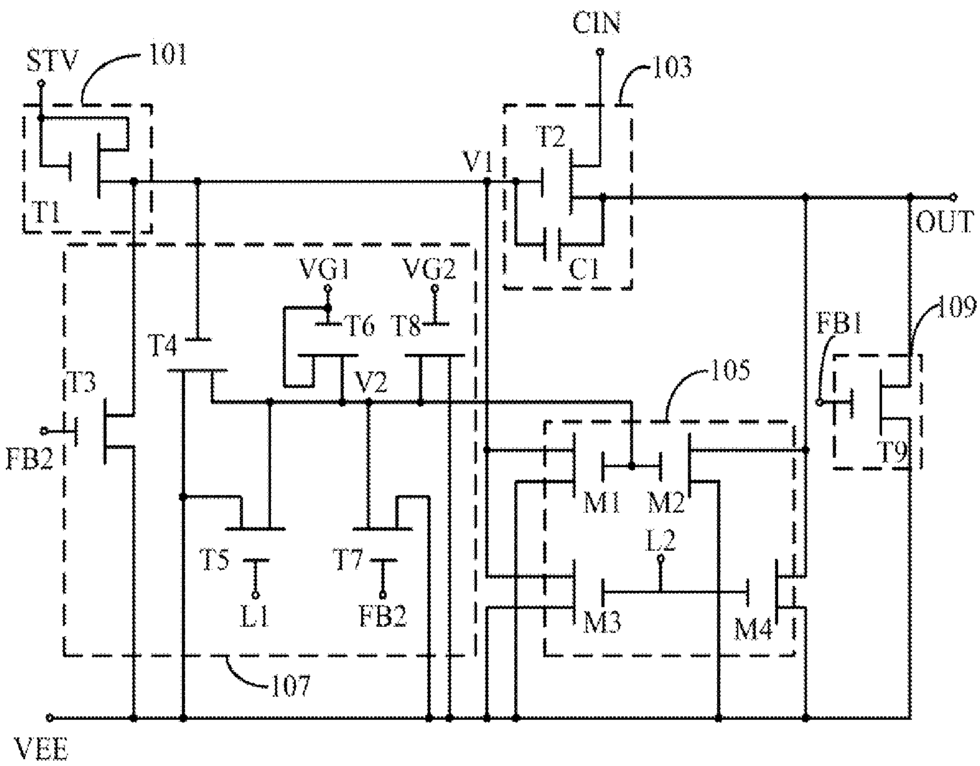

STV
101
CIN
103
T2
V1
T1
C1
OUT
VG1
VG2
T6
T8
109
FB1
T4
V2
105
T3
FB2
T9
M1
M2
T5
T7
L2
L1
FB2
M3
M4
107
VEE

FIG. 3

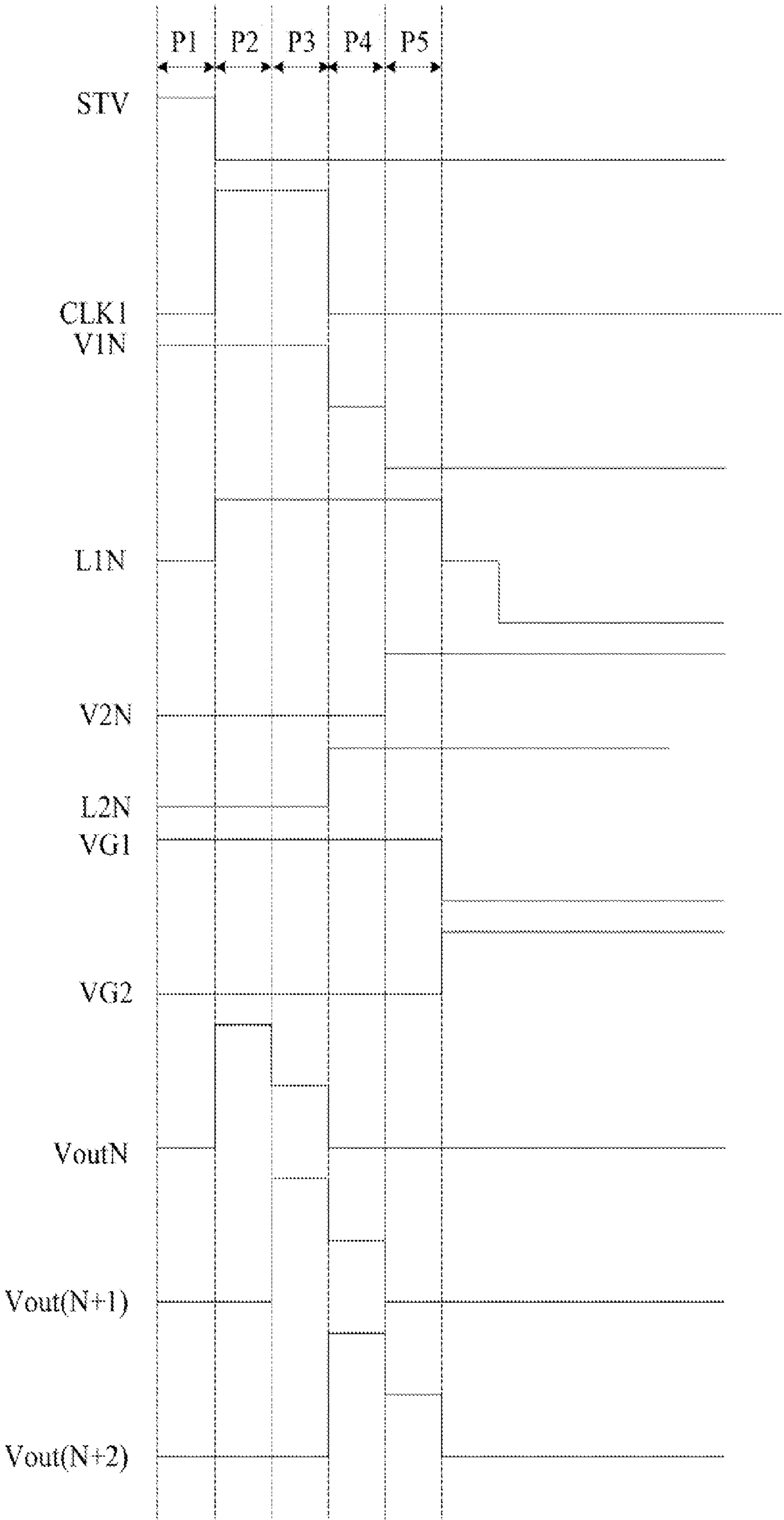

P1
P2
P3
P4
P5
STV
CLK1
V1N
L1N
V2N
L2N
VG1
VG2
VoutN
Vout(N+1)
Vout(N+2)

FIG. 4

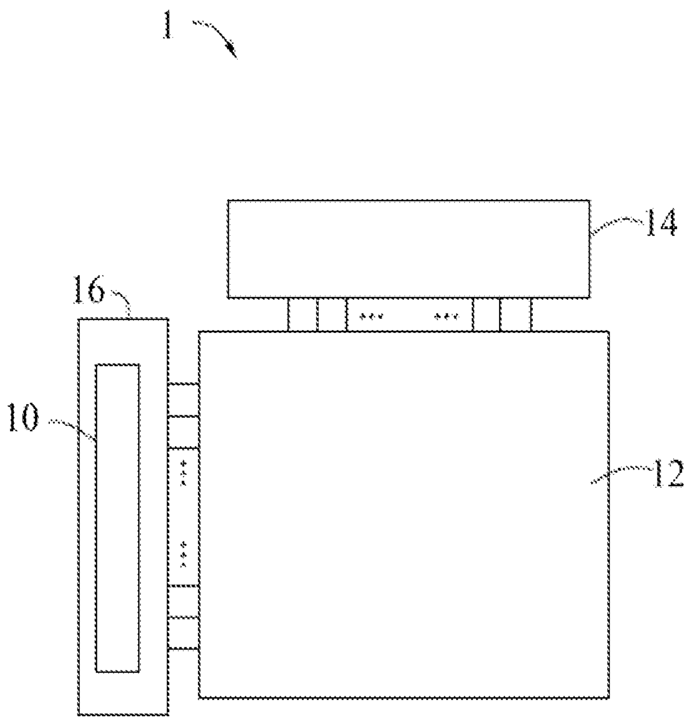


FIG. 5

SHIFT REGISTER AND DRIVING CIRCUIT FOR LIQUID CRYSTAL DISPLAY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Chinese Patent Application No. 201310230274.5 filed on Jun. 11, 2013 in the China Intellectual Property Office, the contents of which are incorporated by reference herein.

FIELD

[0002] The disclosure generally relates to shift registers, and more particularly to a shift register in a driving circuit for a liquid crystal display (LCD).

BACKGROUND

[0003] An LCD panel usually employs a scanning driving circuit and a data driving circuit to provide scanning signals and display data signals, respectively. A shift register is an important component of both the data driving circuit and the scanning driving circuit. Generally, the shift register includes a plurality of shift register units coupled one by one. In the operation of the shift register circuit, the shift register provides the gate signals having periodical pulses to pixel units of the LCD panel for writing the data signals which become pixel voltages of the pixel units. However, each pulse of the gate signals is substantially a square waveform signal, and a falling edge of each pulse may cause an occurrence of pulling down the written pixel voltages due to the coupling effect of the parasitic capacitors corresponding to the pixel units. This phenomenon is referred to as the feed-through effect. The feed-through effect is likely to cause image flicker, and the display quality of liquid crystal displays using the shift register circuit is therefore degraded.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Implementations of the present technology will now be described, by way of example only, with reference to the attached figures.

[0005] FIG. **1** is a block diagram of a shift register including a plurality of shift register units according to an exemplary embodiment of the present disclosure.

[0006] FIG. **2** is a waveform diagram of exemplary clock signals of the shift register of FIG. **1**.

[0007] FIG. **3** is a circuit diagram of an N^{th} shift register of FIG. **1**.

[0008] FIG. **4** is a diagram of sequential waveforms of exemplary pulse signals of the N^{th} shift register of FIG. **3**.

[0009] FIG. **5** is a block diagram of a liquid crystal display including the shift register of FIG. **1**.

DETAILED DESCRIPTION

[0010] It will be appreciated that for simplicity and clarity of illustration, where appropriate, reference numerals have been repeated among the different figures to indicate corresponding or analogous elements. In addition, numerous specific details are set forth in order to provide a thorough understanding of the embodiments described herein. However, it will be understood by those of ordinary skill in the art that the embodiments described herein can be practiced without these specific details. In other instances, methods, procedures, and components have not been described in detail so as not to obscure the related relevant feature being described. The drawings are not necessarily to scale and the proportions of certain parts may be exaggerated to better illustrate details and features. The description is not to be considered as limiting the scope of the embodiments described herein.

[0011] Referring to FIG. **1**, a shift register **10** can include a plurality of shift register units **100**. The shift register units **100** sequentially output a plurality of first shift signals, namely Vout**1**, Vout**2**, Vout**3** . . . Vout(N−1), VoutN, Vout(N+1), Vout(N+2) . . . , wherein N is a natural number.

[0012] Each shift register unit **100** can include a clock signal input terminal CIN, a starting signal input terminal STV, a shift signal output terminal OUT, a first cascade signal output terminal V**1**, a first cascade signal input terminal L**1**, a second cascade signal output terminal V**2**, a second cascade signal input terminal L**2**, a first feedback terminal FB**1**, and a second feedback terminal FB**2**. The clock signal input terminal CIN receives a clock signal. Each of the four shift register units **100** receive different clock signals. For example, in this exemplary embodiment, the $(N-1)^{th}$, N^{th}, $(N+1)^{th}$, and $(N+2)^{th}$ shift register units **100** receive different clock signals, as shown in FIG. **2**.

[0013] In at least one embodiment, the clock signal input terminal CIN of the N^{th} shift register unit **100** receives a first clock signal CLK**1**. The first cascade signal output terminal V**1** of the Nth shift register unit **100** is electrically coupled to the first cascade signal input terminal L**1** of the $(N-1)^{th}$ shift register unit **100**. The second cascade signal input terminal L**2** of the N^{th} shift register unit **100** is electrically coupled to the second cascade signal output terminal V**2** of the $(N-1)^{th}$ shift register unit **100**. The first cascade signal input terminal L**1** of the Nth shift register unit **100** is electrically coupled to the first cascade signal output terminal V**1** of the $(N+1)^{th}$ shift register unit **100**. The second cascade signal output terminal V**2** of the Nth shift register unit **100** is electrically coupled to the second cascade signal input terminal L**2** of the $(N+1)^{th}$ shift register unit **100**. The starting signal input terminal STV of the Nth shift register unit **100** is electrically coupled to the shift signal output terminal OUT of the $(N-1)^{th}$ shift register unit **100**. The $(N-1)^{th}$ shift signal Vout(N−1) is a starting signal of the N^{th} shift register unit **100** which is configured to start the Nth shift register unit **100**. The shift signal output terminal OUT of the N^{th} shift register unit **100** is electrically coupled to the starting signal input terminal STV of the $(N+1)^{th}$ shift register unit **100**. The first feedback terminal FB**1** of the Nth shift register unit **100** is electrically coupled to the shift signal output terminal OUT of the $(N+1)^{th}$ shift register unit **100**, and the $(N+1)^{th}$ shift signal Vout(N+1) output by the $(N+1)^{th}$ shift register unit **100** is defined as a first feedback signal. The second feedback terminal FB**2** of the N^{th} shift register unit **100** is electrically coupled to the shift signal output terminal OUT of the $(N+2)^{th}$ shift register unit **100**, and the $(N+2)^{th}$ shift signal Vout(N+2) output by the $(N+2)^{th}$ shift register unit **100** is defined as a second feedback signal.

[0014] Referring to FIG. **3**, the N^{th} shift register unit **100** can include a starting unit **101**, a pull-up unit **103**, a pull-down unit **105**, a control unit **107**, and a waveform-shaping unit **109**. The starting unit **101** outputs a first driving signal to the pull-up unit **103** according to the starting signal. The pull-up unit **103** is electrically coupled between the starting unit **101** and the shift signal output terminal OUT. The pull-up unit **103** pulls up the value of the shift signal VoutN according to the first driving signal and the first clock signal CLK**1**. The pull-down unit **105** is electrically coupled between the starting unit

101 and the shift signal output terminal OUT to pull down the value of the first driving signal. The control unit **107** is electrically coupled between the starting unit and the pull-down unit **105** to control a working time of the pull-down unit **105** according to the $(N+2)^{th}$ shift signal, a first control signal VG**1**, and a second control signal VG**2**. In the embodiment, the first control signal VG**1** and the second control signal VG**2** are both output by an external controller. The waveform-shaping unit **109** is electrically coupled to the shift signal output terminal OUT to perform a waveform-shaping operation on the Nth shift signal VoutN under the control of the $(N+1)^{th}$ shift signal.

[0015] The starting unit **101** can include a first transistor T**1**. A gate electrode of the first transistor T**1** is electrically coupled to the starting signal input terminal STV and a source electrode of the first transistor T**1**.

[0016] The pull-up unit **103** can include a second transistor T**2** and a first capacitor C**1**. A gate electrode of the second transistor T**2** is electrically coupled to a drain electrode of the first transistor T**1**. The first capacitor C**1** is electrically coupled between the gate electrode of the second transistor T**2** and a drain electrode of the second transistor T**2**. A source electrode of the second transistor T**2** is electrically coupled to the clock signal input terminal CIN to receive the first clock signal CLK**1**. The gate electrode of the second transistor T**2** is electrically coupled to the first cascade signal output terminal V**1** of the Nth shift register **100**.

[0017] The pull-down unit **105** can include a first pull-down transistor M**1**, a second pull-down transistor M**2**, a third pull-down transistor M**3**, and a fourth pull-down transistor M**4**. A gate electrode of the first pull-down transistor M**1** is electrically coupled to a gate electrode of the second pull-down transistor M**2**. Source electrodes of the first and third pull-down transistors M**1** and M**3** are electrically coupled to the gate electrode of the second transistor T**2**. Source electrodes of the second and fourth pull-down transistors M**2** and M**4** are electrically coupled to the shift signal output terminal OUT. Drain electrodes of the first, second, third, and fourth pull-down transistors, M**1**, M**2**, M**3**, and M**4**, receive a logic-low signal provided by an external power source. A node between the gate electrode of the third pull-down transistor M**3** and the gate electrode of the fourth pull-down transistor M**4** is electrically coupled to the second cascade signal input terminal L**2** of the N^{th} shift register unit **100**.

[0018] The control unit **107** can include a third transistor T**3**, a fourth transistor T**4**, a fifth transistor T**5**, a sixth transistor T**6**, a seventh transistor T**7**, and an eighth transistor T**8**. A gate electrode of the third transistor T**3** is the second feedback terminal FB**2** of the N^{th} shift register unit **100**. A source electrode of the third transistor T**3** is electrically coupled to the drain electrode of the first transistor T**1**. A drain electrode of the third transistor T**3** receives the logic-low signal VEE. In the embodiment, the drain electrode of the third transistor T**3** is grounded. A gate electrode of the fourth transistor T**4** is electrically coupled to the drain electrode of the first transistor T**1**, and a drain electrode of the fourth transistor T**4** receives the logic-low signal VEE. A source electrode of the fourth transistor T**4** is electrically coupled to the source electrodes of the fifth, sixth, seventh, and eighth transistors, T**5**-T**8**. The source electrodes of the fourth, fifth, sixth, seventh, and eighth transistors, T**4**-T**8**, receive the logic-low signal VEE. A gate electrode of the sixth transistor T**6** is electrically coupled to the source electrode of the sixth transistor T**6**. The gate electrode of the sixth transistor T**6** receives the first control signal VG**1** from the external controller, and a gate electrode of the eighth transistor T**8** receives the second control signal VG**2** from the external controller. A gate electrode of the fifth transistor T**5** is electrically coupled to the first cascade signal input terminal L**1**. The gate electrode of the fifth transistor T**5** is electrically coupled to the first cascade signal output terminal V**1** of the $(N+1)^{th}$ shift register unit **100**. A gate of the seventh transistor T**7** is electrically coupled to the second feedback terminal FB**2** to receive the $(N+2)^{th}$ shift signal output by the $(N+2)^{th}$ shift register unit **100**. A node between the drain electrode of the sixth transistor T**6** and the drain electrode of the eighth transistor T**8** is electrically coupled to the second cascade signal output terminal V**2** of the Nth shift register unit **100**. In the embodiment, a ratio of width and length of a channel layer of the sixth transistor T**6** is 100 times greater than a ratio of width and length of a channel layer of the eighth transistor T**8**. A ratio of width and length of a channel layer of fifth transistor T**5** is 100 times greater than a ratio of width and length of a channel layer of the eighth transistor T**8**.

[0019] The waveform-shaping unit **109** can include a ninth transistor T**9**. A gate electrode of the ninth transistor T**9** can be electrically coupled to the first feedback terminal FB**1** of the Nth shift register unit **100** to receive the $(N+1)^{th}$ shift signal output by the $(N+1)^{th}$ shift register unit **100**. A source electrode of the ninth transistor T**9** can be electrically coupled to the shift signal output terminal OUT, and a drain electrode of the ninth transistor T**9** to receive the logic-low signal VEE.

[0020] Referring to FIG. **4**, VIN represents a first cascade output signal output by the first cascade signal output terminal V**1** of the N^{th} shift register unit **100**. L1N represents a first cascade input signal to be transmitted to the first cascade signal input terminal L**1** of the N^{th} shift register unit **100**. V**2**N represents a second cascade output signal output by the second cascade signal output terminal V**2** of the N^{th} shift register unit **100**. L2N represents a second cascade input signal to be transmitted to the second cascade signal input terminal L**2** of the N^{th} shift register unit **100**.

[0021] During a first period P**1**, the starting signal STV is at logic-high, the first clock signal CLK**1** is logic-low, the first control signal VG**1** is at logic-high, and the second control signal VG**2** is at logic-low. The first transistor T**1** and the second transistor T**2** are both turned on under control of the starting signal STV and the first control signal VG**1**. The first clock signal CLK**1** is output by the shift signal output terminal OUT, thus the N^{th} shift signal VoutN is at logic-low. The first capacitor C**1** is charged by the starting signal STV, and the first cascade output signal V**1**N is at logic-high. In the control unit **107**, the fourth transistor T**4** and the sixth transistor T**6** are turned on, the second cascade output signal V**2**N is at logic-low, thus the first and second pull-down transistors M**1** and M**2** are turned off.

[0022] During a second period P**2**, the starting signal STV changes to a logic-low to turn off the first transistor T**1** from the logic-high and the first clock signal CLK**1** changes from a logic-low to a logic-high. The first cascade signal output terminal V**1** is at logic-high because of the existence of the first capacitor C**1**. In the control unit **107**, the fourth transistor T**4** and the sixth transistor T**6** are turned on, the second cascade output signal V**2**N is at logic-low to turn off the first and second pull-down transistors M**1** and M**2**.

[0023] During a third period P**3**, the starting signal STV is at logic-low and the first transistor T**1** is turned off. The first cascade signal output terminal V**1** is at logic-high because of the existence of the first capacitor C1. The $(N+1)^{th}$ shift signal Vout(N+1) is at logic-high to turn on the ninth transistor T9, and the logic-low signal VEE performs a waveform-shaping operation on the N^{th} shift signal VoutN to pull it down.

[0024] During a fourth period P4, the $(N+2)^{th}$ shift signal Vout(N+2) is at logic-high, and the third transistor T3 is turned on, the first cascade output signal V1N changes from a logic-high to a logic-low to turn off the second transistor T2 and the fourth transistor T4. The first transistor T1 is turned on. The second cascade output signal V2N is at logic-low.

[0025] During a fifth period P5, the first cascade input signal L1N changes from a logic-high to a logic-low, and the second cascade output signal V2N is at logic-high, thus the first and second pull-down transistors M1 and M2 are turned on and the first cascade output signal V1N changes from a logic-high to a logic-low.

[0026] Referring to FIG. 5, a liquid crystal display 1 can include a liquid crystal panel 12, a data driver 14, and a gate driver 16. The gate driver 16 outputs a plurality of gate signals to control a working state of a plurality of thin film transistors of the liquid crystal panel 12. The data driver 14 outputs a plurality of data signals to the liquid crystal panel 12. The gate driver 16 controls a timing sequence of the gate signals through the shift register 100.

[0027] It is to be understood that even though numerous characteristics and advantages of the present embodiments have been set forth in the foregoing description, with details of the structures and functions of the embodiments, the disclosure is illustrative only; and changes may be in detail, including in the matter of arrangement of parts within the principles of the embodiments to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

What is claimed is:

1. A shift register comprising:

a plurality of shift register units, each shift register unit outputting a shift signal, an N^{th} shift register unit comprising:

a staring unit electrically coupled to an $(N-1)^{th}$ shift register and outputting a first driving signal according to an $(N-1)^{th}$ shift signal output by an $(N-1)^{th}$ shift register;

a pull-up unit electrically coupled between the staring unit and a shift signal output terminal of the N^{th} shift register unit and pulling up an N^{th} shift signal output by an N^{th} shift register according to the first driving signal and a first clock signal;

a pull-down unit electrically coupled between the starting unit and a shift signal output terminal of the N^{th} shift register unit and pulling down the first driving signal;

a control unit electrically coupled between the starting unit and the pull-down unit to control a working time of the pull-down unit according to an $(N+2)^{th}$ shift signal, a first control signal, and a second control signal; and

a waveform-shaping unit electrically coupled to the shift signal output terminal of the N^{th} register to perform a waveform-shaping operation on the N^{th} shift signal according to the $(N+1)^{th}$ shift signal.

2. The shift register of claim **1**, wherein each of the shift register units comprises a first cascade signal output terminal, a first cascade signal input terminal, a second cascade signal input terminal, a second cascade signal output terminal, a first feedback terminal, and a second feedback terminal; the first cascade signal output terminal of the N^{th} shift register unit is electrically coupled to the first cascade signal output terminal of an $(N+1)^{th}$ shift register unit, the first cascade signal output terminal of the N^{th} shift register unit is electrically coupled to the first cascade signal input terminal of the $(N-1)^{th}$ shift register unit, the second cascade signal output terminal of the N^{th} shift register unit is electrically coupled to the second cascade signal input terminal of the $(N-1)^{th}$ shift register unit, the first feedback terminal of the N^{th} shift register unit receives the $(N+1)^{th}$ shift signal, and the second feedback terminal of the N^{th} shift register unit receives the $(N+2)^{th}$ shift signal.

3. The shift register of claim **2**, wherein the starting unit comprises a first transistor, and a gate electrode of the first transistor is electrically coupled to the starting signal input terminal STV and a source electrode of the first transistor.

4. The shift register of claim **3**, wherein the pull-up unit comprises a second transistor and a first capacitor, a gate electrode of the second transistor is electrically coupled to a drain electrode of the first transistor; the first capacitor is electrically coupled between the gate electrode of the second transistor and a drain electrode of the second transistor, a source electrode of the second transistor is electrically coupled to the clock signal input terminal to receive the first clock signal.

5. The shift register of claim **4**, wherein the gate electrode of the second transistor is electrically coupled to the first cascade signal output terminal of the N^{th} shift register.

6. The shift register of claim **4**, wherein the pull-down unit comprises a first pull-down transistor, a second pull-down transistor, a third pull-down transistor, and a fourth pull-down transistor, a gate electrode of the first pull-down transistor is electrically coupled to a gate electrode of the second pull-down transistor, source electrodes of the first and third pull-down transistors and are electrically coupled to the gate of the second transistor, and source electrodes of the second and fourth pull-down transistors are electrically coupled to the shift signal output terminal, and drain electrodes of the first, second, third, and fourth pull-down transistor receive a logic-low signal provided by an external power source.

7. The shift register of claim **6**, wherein a node between the gate electrode of the third pull-down transistor and the gate electrode of the fourth pull-down transistor is electrically coupled to the second cascade signal input terminal of the N^{th} shift register unit.

8. The shift register of claim **6**, wherein the control unit comprises third, fourth, fifth, sixth, seventh, and eighth transistors, and a gate of the third transistor is electrically coupled to the second feedback terminal of the N^{th} shift register unit, and a source electrode of the third transistor is electrically coupled to the drain electrode of the first transistor, a drain electrode of the third transistor receives the logic-low signal; a gate electrode of the fourth transistor is electrically coupled to the drain electrode of the first transistor; a drain electrode of the fourth transistor receives the logic-low signal, and a source electrode of the fourth transistor is electrically coupled to source electrodes of the fifth, sixth, seventh, and eighth transistors, the source electrodes of the fourth, fifth, seventh, and eighth transistors receive the logic-low signal, a gate electrode of the sixth transistor is electrically coupled to the source electrode of the sixth transistor, the gate electrode of the sixth transistor receives the first control signal; and a gate electrode of the eighth transistor receives the second control signal, a gate electrode of the fifth transistor is electrically coupled to the first cascade signal input terminal and the first cascade signal output terminal of the $(N+1)^{th}$ shift register unit, a gate electrode of the seventh transistor is electrically coupled to the second feedback terminal to receive the $(N+2)^{th}$ shift signal output by the $(N+2)^{th}$ shift register unit; and a node between the drain electrode of the sixth transistor and the drain electrode of the eighth transistor is electrically coupled to the second cascade signal output terminal of the Nth shift register unit.

9. The shift register of claim **8**, wherein the waveform-shaping unit comprises a ninth transistor, a gate electrode of the ninth transistor is electrically coupled to the first feedback terminal of the N^{th} shift register unit to receive the $(N+1)^{th}$ shift signal output by the $(N+1)^{th}$ shift register unit, a source electrode of the ninth transistor is electrically coupled to the shift signal output terminal, and a drain electrode of the ninth transistor receives the logic-low signal.

10. A liquid crystal display comprising:

a display panel, a date drive, and a gate driver;

the gate driver comprising a shift register comprising:

a plurality of shift register units, each shift register unit outputting a shift signal, an Nth shift register unit comprising:

a staring unit electrically coupled to an $(N-1)^{th}$ shift register and outputting a first driving signal according to an $(N-1)^{th}$ shift signal output by an $(N-1)^{th}$ shift register;

a pull-up unit electrically coupled between the staring unit and a shift signal output terminal of the N^{th} shift register unit and pulling up an N^{th} shift signal output by an N^{th} shift register according to the first driving signal and a first clock signal;

a pull-down unit electrically coupled between the starting unit and a shift signal output terminal of the N^{th} shift register unit and pulling down the first driving signal;

a control unit electrically coupled between the starting unit and the pull-down unit to control a working time of the pull-down unit according to an $(N+2)^{th}$ shift signal, a first control signal, and a second control signal; and

a waveform-shaping unit electrically coupled to the shift signal output terminal of the N^{th} register to perform a waveform-shaping operation on the Nth shift signal according to the $(N+1)^{th}$ shift signal.

11. The liquid crystal display of claim **10**, wherein each of the shift register units comprises a first cascade signal output terminal, a first cascade signal input terminal, a second cascade signal input terminal, a second cascade signal output terminal, a first feedback terminal, and a second feedback terminal; the first cascade signal output terminal of the N^{th} shift register unit is electrically coupled to the first cascade signal output terminal of an $(N+1)^{th}$ shift register unit, the first cascade signal output terminal of the N^{th} shift register unit is electrically coupled to the first cascade signal input terminal of the $(N-1)^{th}$ shift register unit, the second cascade signal output terminal of the N^{th} shift register unit is electrically coupled to the second cascade signal input terminal of the $(N-1)^{th}$ shift register unit, the first feedback terminal of the N^{th} shift register unit receives the $(N+1)^{th}$ shift signal, and the second feedback terminal of the N^{th} shift register unit receives the $(N+2)^{th}$ shift signal.

12. The liquid crystal display of claim **11**, wherein the starting unit comprises a first transistor, and a gate electrode of the first transistor is electrically coupled to the starting signal input terminal STV and a source electrode of the first transistor.

13. The liquid crystal display of claim **12**, wherein the pull-up unit comprises a second transistor and a first capacitor, a gate electrode of the second transistor is electrically coupled to a drain electrode of the first transistor; the first capacitor is electrically coupled between the gate electrode of the second transistor and a drain electrode of the second transistor, a source electrode of the second transistor is electrically coupled to the clock signal input terminal to receive the first clock signal.

14. The liquid crystal display of claim **13**, wherein the gate electrode of the second transistor is electrically coupled to the first cascade signal output terminal of the N^{th} shift register.

15. The liquid crystal display of claim **13**, wherein the pull-down unit comprises a first pull-down transistor, a second pull-down transistor, a third pull-down transistor, and a fourth pull-down transistor, a gate electrode of the first pull-down transistor is electrically coupled to a gate electrode of the second pull-down transistor, source electrodes of the first and third pull-down transistors and are electrically coupled to the gate of the second transistor, and source electrodes of the second and fourth pull-down transistors are electrically coupled to the shift signal output terminal, and drain electrodes of the first, second, third, and fourth pull-down transistor receive a logic-low signal provided by an external power source.

16. The liquid crystal display of claim **15**, wherein a node between the gate electrode of the third pull-down transistor and the gate electrode of the fourth pull-down transistor is electrically coupled to the second cascade signal input terminal of the N^{th} shift register unit.

17. The liquid crystal display of claim **15**, wherein the control unit comprises third, fourth, fifth, sixth, seventh, and eighth transistors, and a gate of the third transistor is electrically coupled to the second feedback terminal of the N^{th} shift register unit, and a source electrode of the third transistor is electrically coupled to the drain electrode of the first transistor, a drain electrode of the third transistor receives the logic-low signal; a gate electrode of the fourth transistor is electrically coupled to the drain electrode of the first transistor; a drain electrode of the fourth transistor receives the logic-low signal, and a source electrode of the fourth transistor is electrically coupled to source electrodes of the fifth, sixth, seventh, and eighth transistors, the source electrodes of the fourth, fifth, seventh, and eighth transistors receive the logic-low signal, a gate electrode of the sixth transistor is electrically coupled to the source electrode of the sixth transistor, the gate electrode of the sixth transistor receives the first control signal; and a gate electrode of the eighth transistor receives the second control signal, a gate electrode of the fifth transistor is electrically coupled to the first cascade signal input terminal and the first cascade signal output terminal of the $(N+1)^{th}$ shift register unit, a gate electrode of the seventh transistor is electrically coupled to the second feedback terminal to receive the $(N+2)^{th}$ shift signal output by the $(N+2)^{th}$ shift register unit; and a node between the drain electrode of the sixth transistor and the drain electrode of the eighth transistor is electrically coupled to the second cascade signal output terminal of the Nth shift register unit.

18. The liquid crystal display of claim **17**, wherein the waveform-shaping unit comprises a ninth transistor, a gate electrode of the ninth transistor is electrically coupled to the first feedback terminal of the N^{th} shift register unit to receive the $(N+1)^{th}$ shift signal output by the $(N+1)^{th}$ shift register unit, a source electrode of the ninth transistor is electrically coupled to the shift signal output terminal, and a drain electrode of the ninth transistor receives the logic-low signal.

19. A shift register, comprising:

a plurality of shift register units, each shift register unit outputting a shift signal, an N^{th} shift register unit comprising:

a starting unit electrically coupled to an $(N-1)^{th}$ shift register and outputting a first driving signal according to an $(N-1)^{th}$ shift signal output by an $(N-1)^{th}$ shift register;

a pull-up unit electrically coupled between the starting unit and a shift signal output terminal of the N^{th} shift register unit and pulling up an N^{th} shift signal output by an N^{th} shift register according to the first driving signal and a first clock signal;

a pull-down unit electrically coupled between the starting unit and a shift signal output terminal of the N^{th} shift register unit, and pulling down the first driving signal;

a control unit electrically coupled between the starting unit and the pull-down unit to control a working time of the pull-down unit according to an $(N+2)^{th}$ shift signal, a first control signal, and a second control signal; and

a waveform-shaping unit electrically coupled to the shift signal output terminal of the N^{th} register to perform a waveform-shaping operation on the N^{th} shift signal according to the $(N+1)^{th}$ shift signal.

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专利名称(译)	用于液晶显示器的移位寄存器和驱动电路		
公开(公告)号	US20140362067A1	公开(公告)日	2014-12-11
申请号	US14/301495	申请日	2014-06-11
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申请(专利权)人(译)	世纪科技（深圳）股份有限公司		
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IPC分类号	G09G3/36		
CPC分类号	G09G3/3696 G11C19/28 G09G3/3677 G09G2310/0286 G09G2320/0219		
优先权	201310230274.5 2013-06-11 CN		
其他公开文献	US9318218		
外部链接	Espacenet USPTO		

摘要(译)

用于LCD显示器的移位寄存器包括N个移位寄存器单元。每个移位寄存器单元输出移位信号。第N移位寄存器单元包括波形整形单元，其电耦合到第N寄存器的移位信号输出端，以根据由（n）输出的第（N + 1）移位信号对第N移位信号执行波形整形操作。 N + 1）移位寄存器，以减少导致显示闪烁的馈通效应。