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(54) DISPLAY DEVICE

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USPC ........................................................ **349/43**

(57) **ABSTRACT**

The time taken to write a signal to a pixel is shortened in a display device. Further, a signal is written at high speed even when high voltage is applied. The display device includes a pixel including a transistor and a liquid crystal element electrically connected to a source or a drain of the transistor. The transistor includes an intrinsic or substantially intrinsic oxide semiconductor as a semiconductor material and has an off-state current of $1\times10^{-17}$ A/μm or less. The pixel does not include a capacitor. Since it is not necessary to provide a capacitor, the time taken to write a signal can be shortened.

FIG. 1

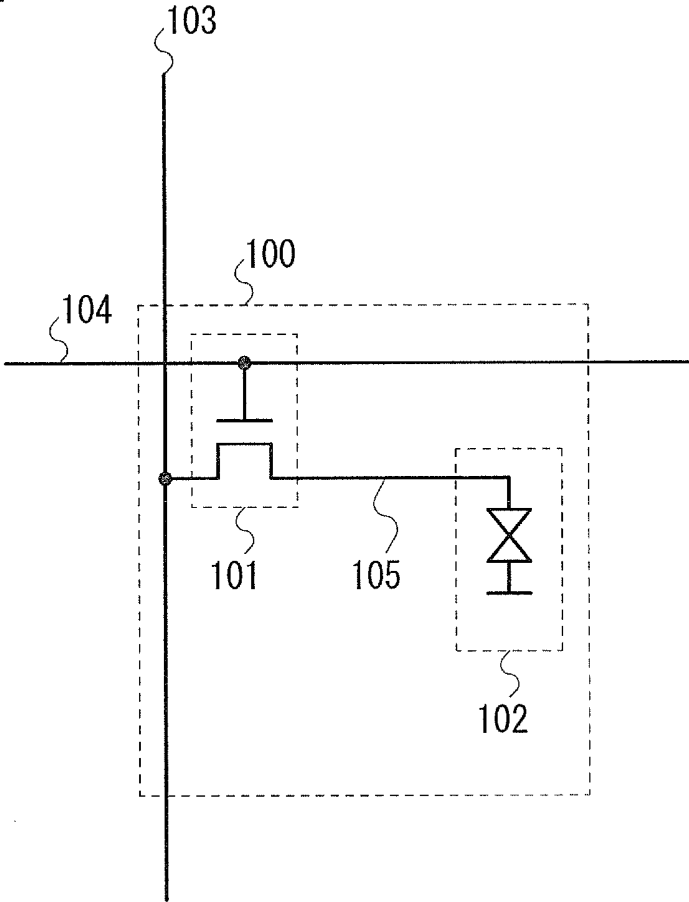


FIG. 2A

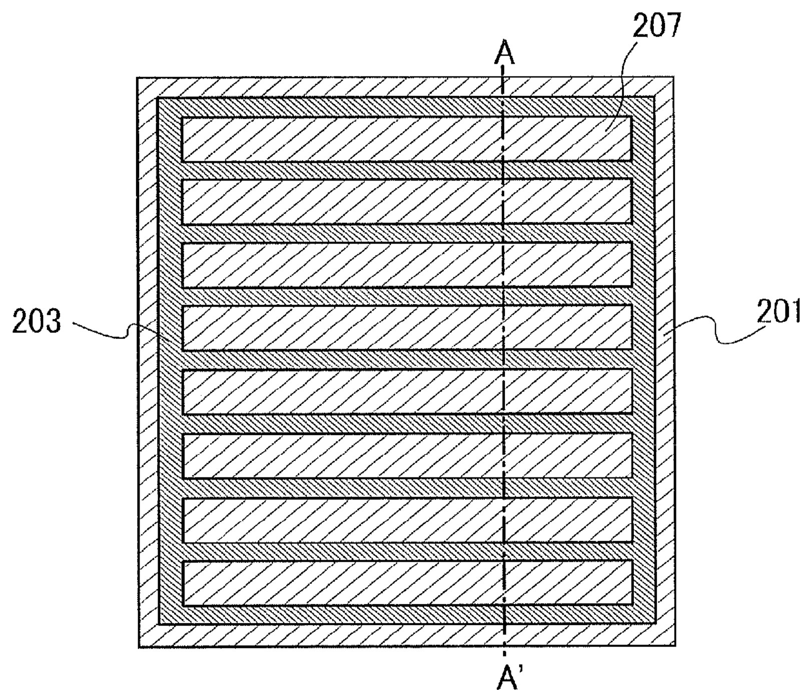



FIG. 2B

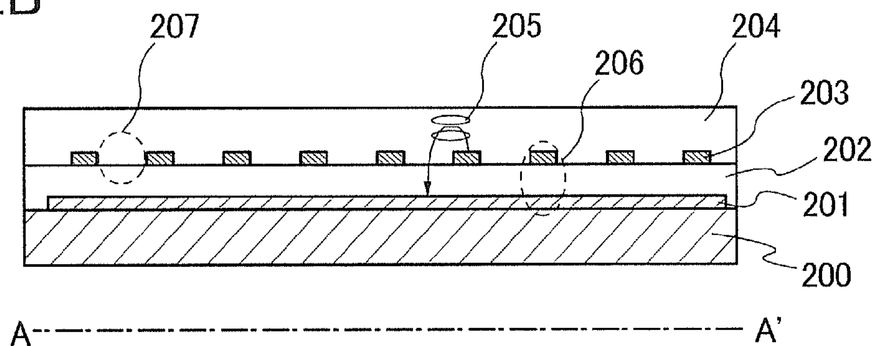


FIG. 3A

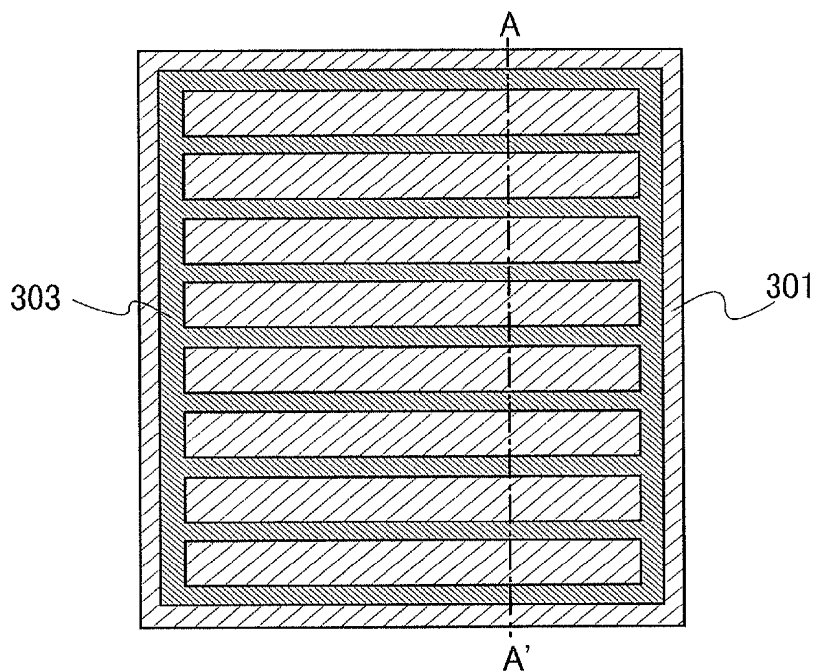



FIG. 3B

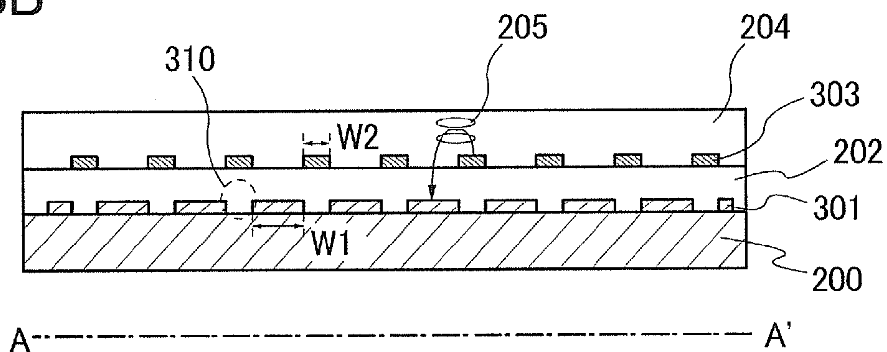


FIG. 4A

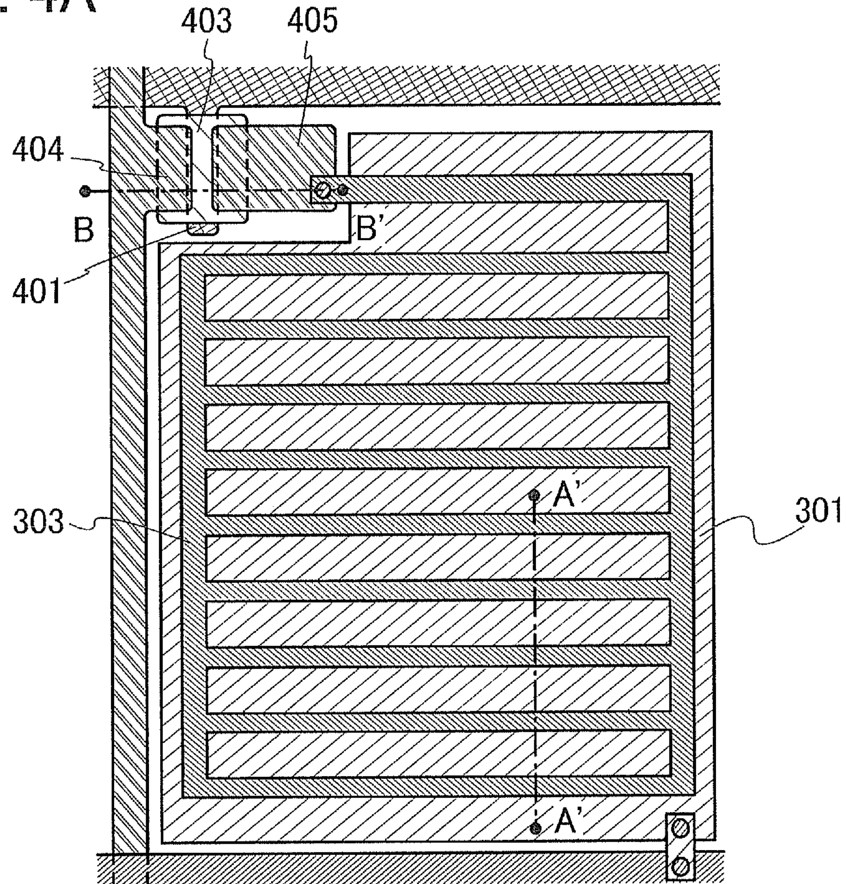



FIG. 4B

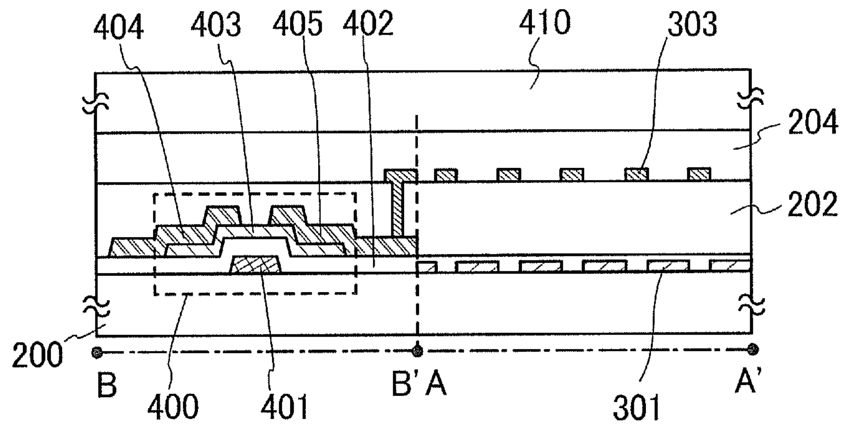


FIG. 5

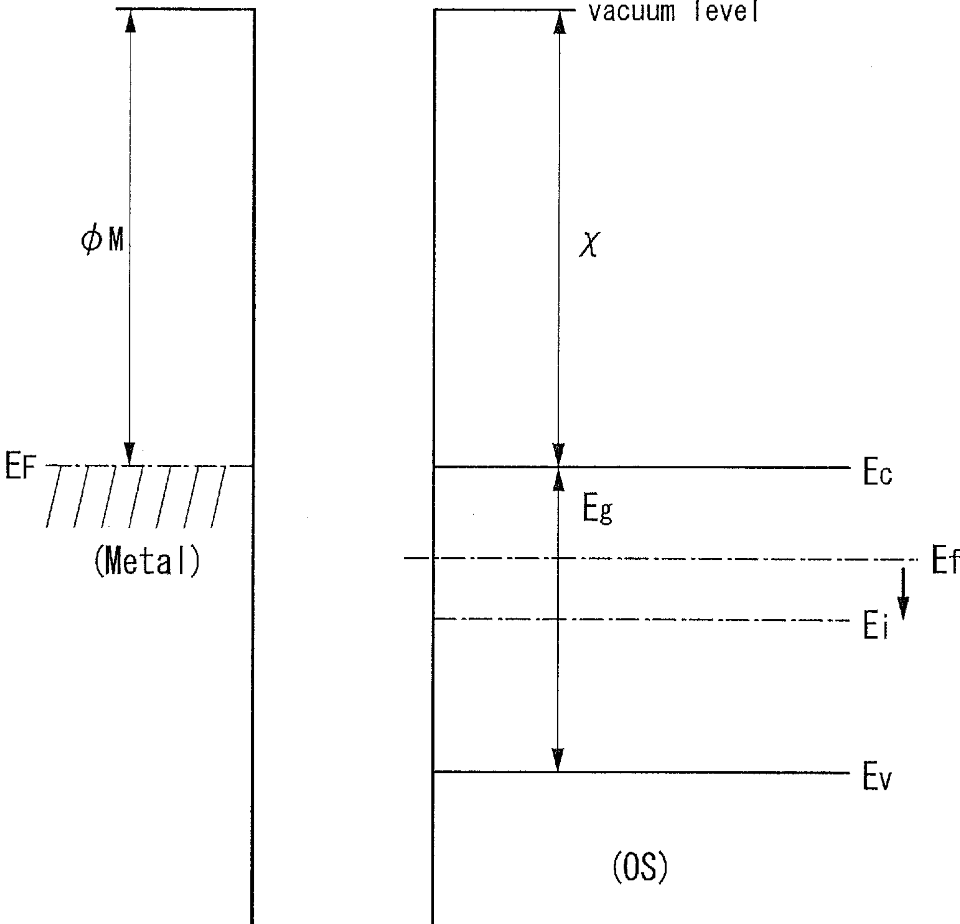


FIG. 6

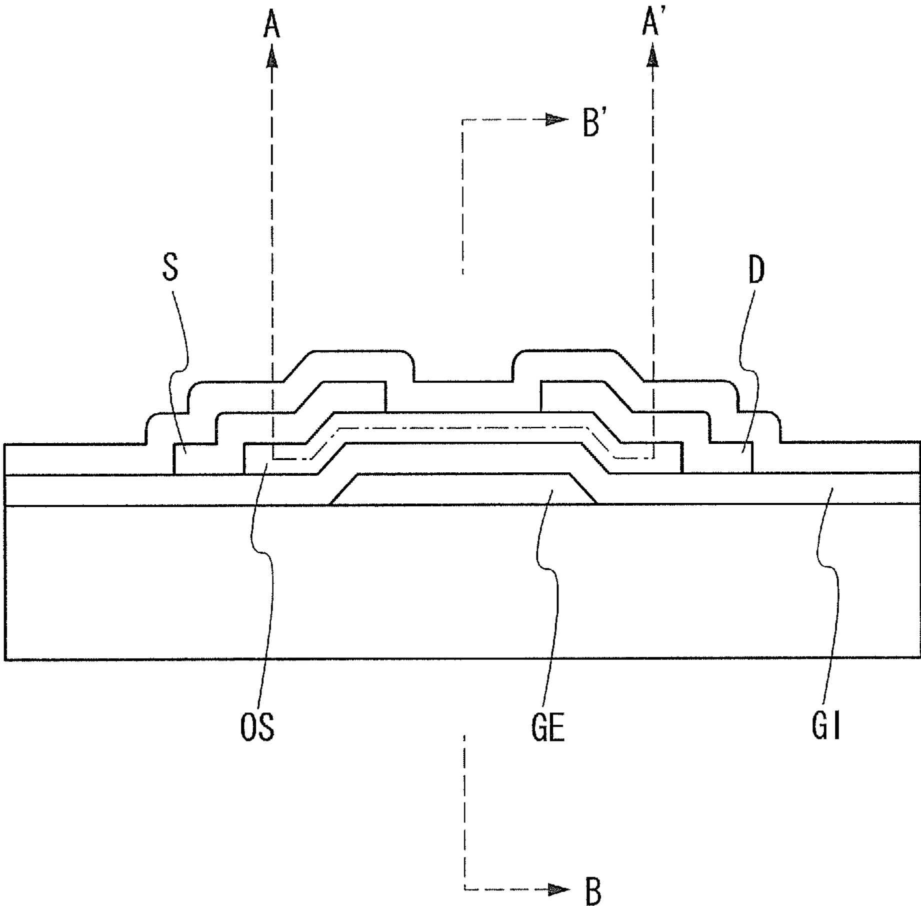
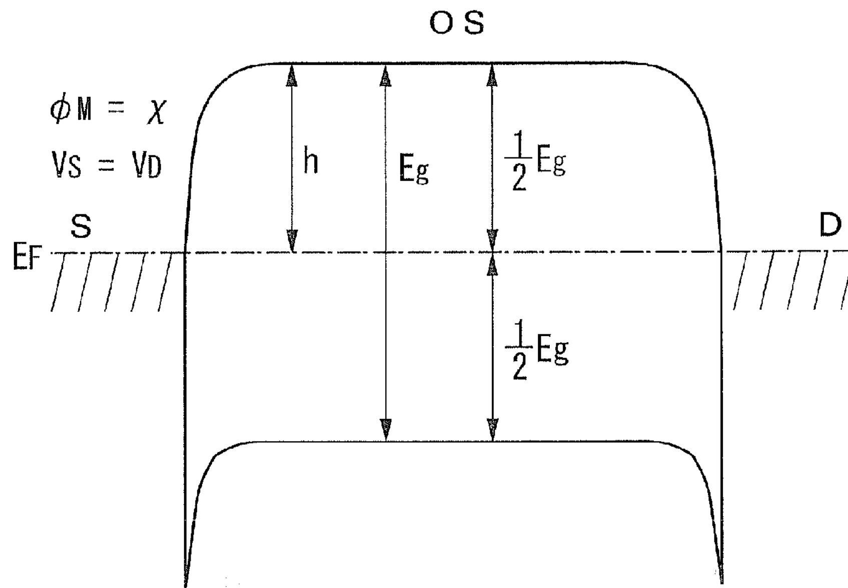
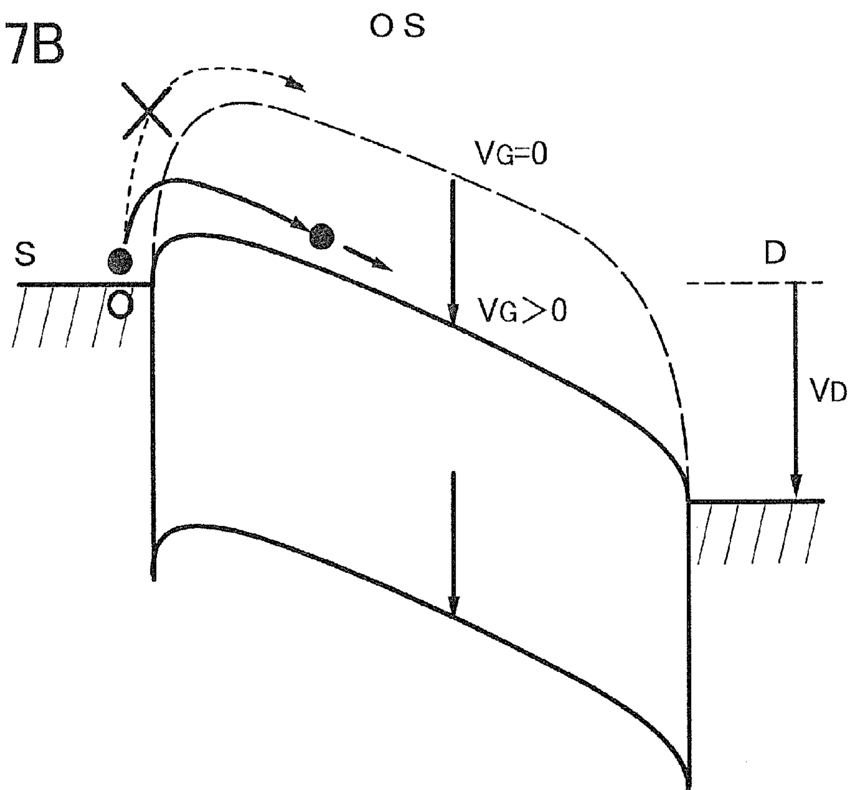


FIG. 7A



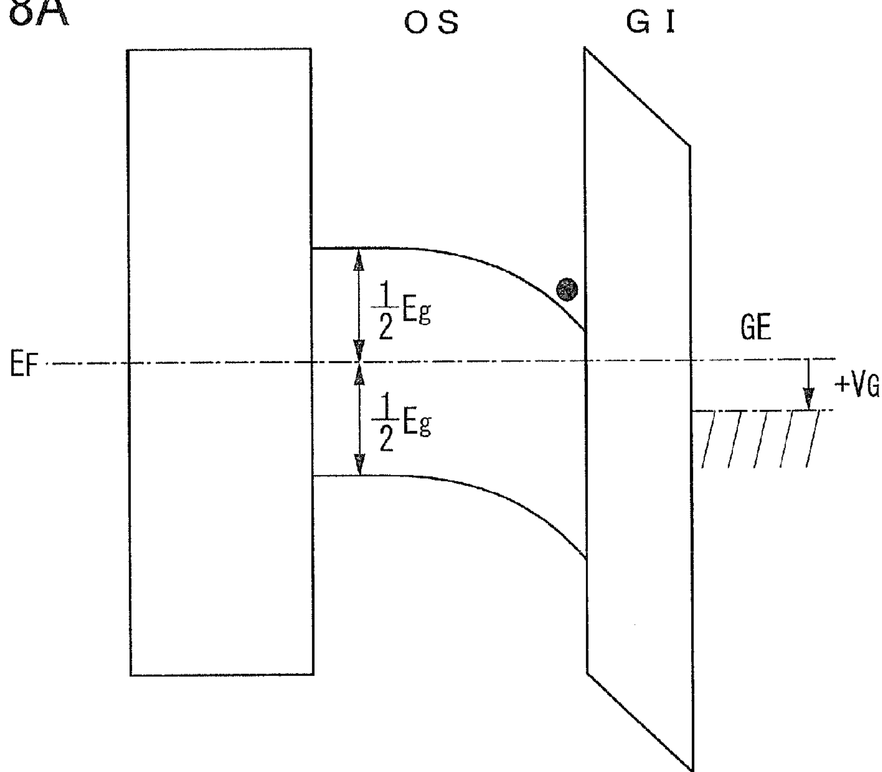

Energy band diagram in A-A′ cross section

FIG. 7B



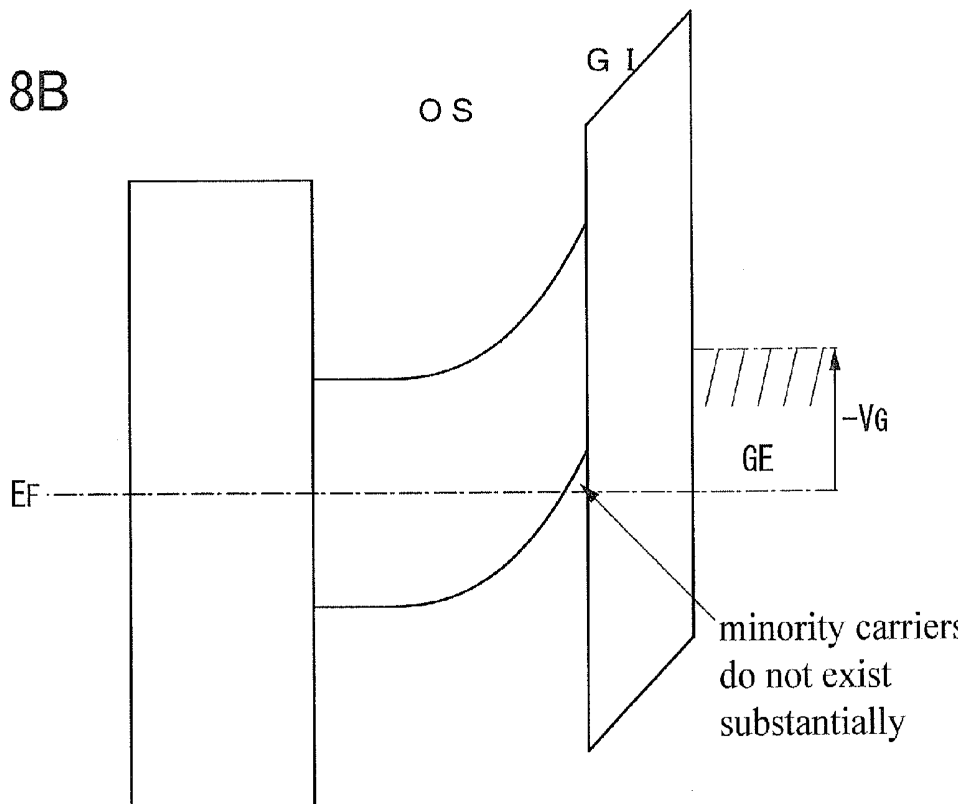

Energy band diagram in A-A′ cross section

FIG. 8A




Energy band diagram in B-B′ cross section (+$V_G$)

FIG. 8B




Energy band diagram in B-B′ cross section (-$V_G$)

FIG. 9A

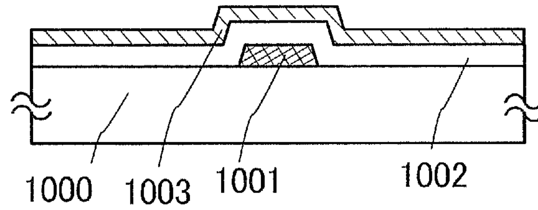



FIG. 9B

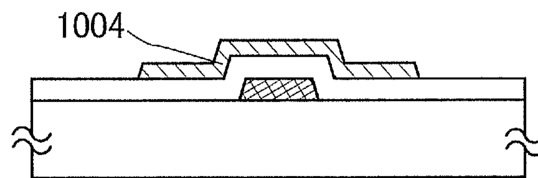



FIG. 9C

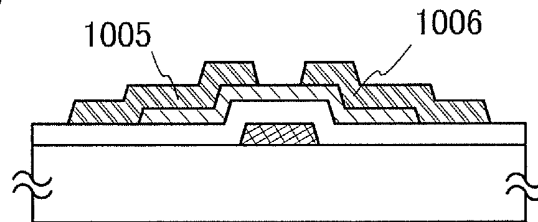



FIG. 9D

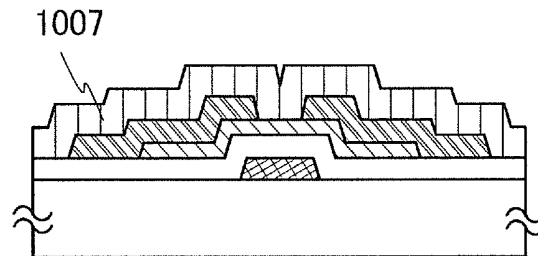



FIG. 9E

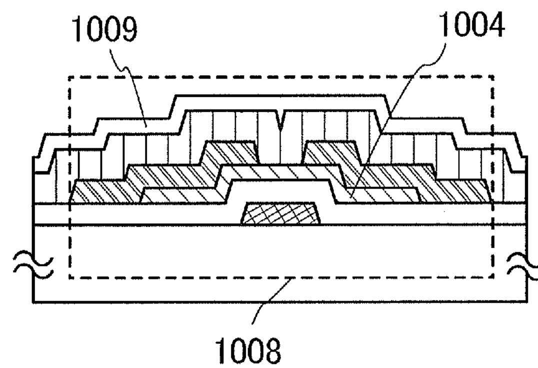


FIG. 10A

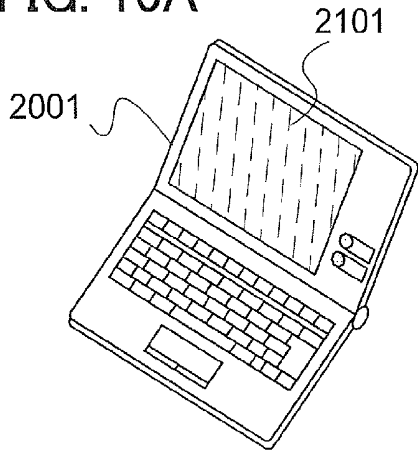



FIG. 10D

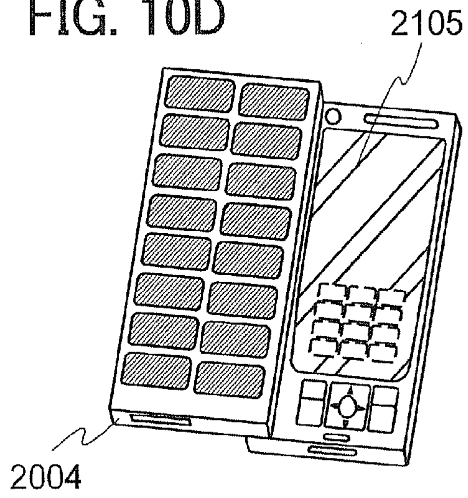



FIG. 10B

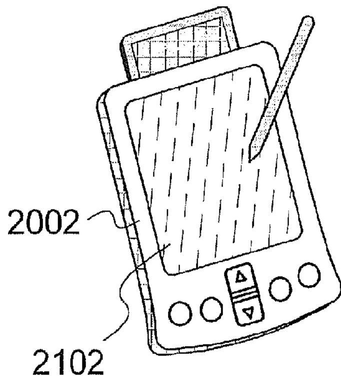



FIG. 10E

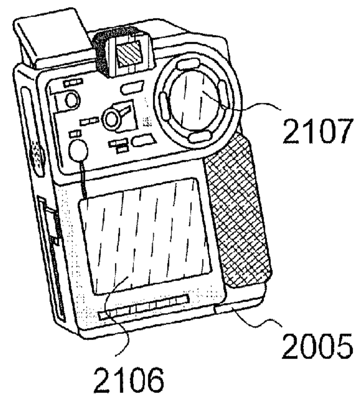



FIG. 10C

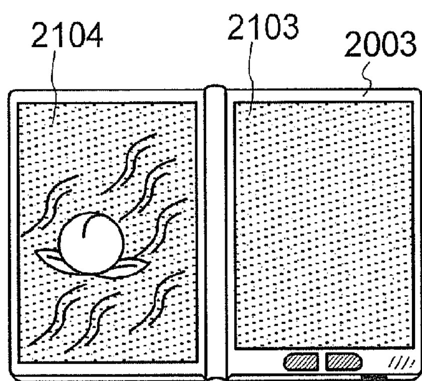



FIG. 10F

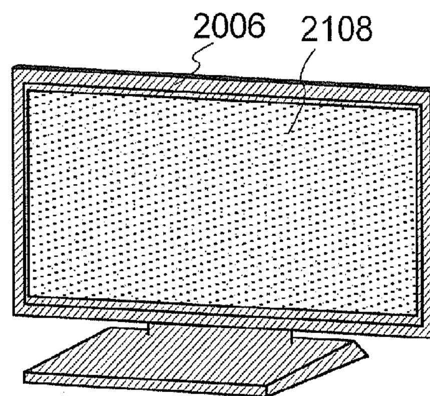


FIG. 11

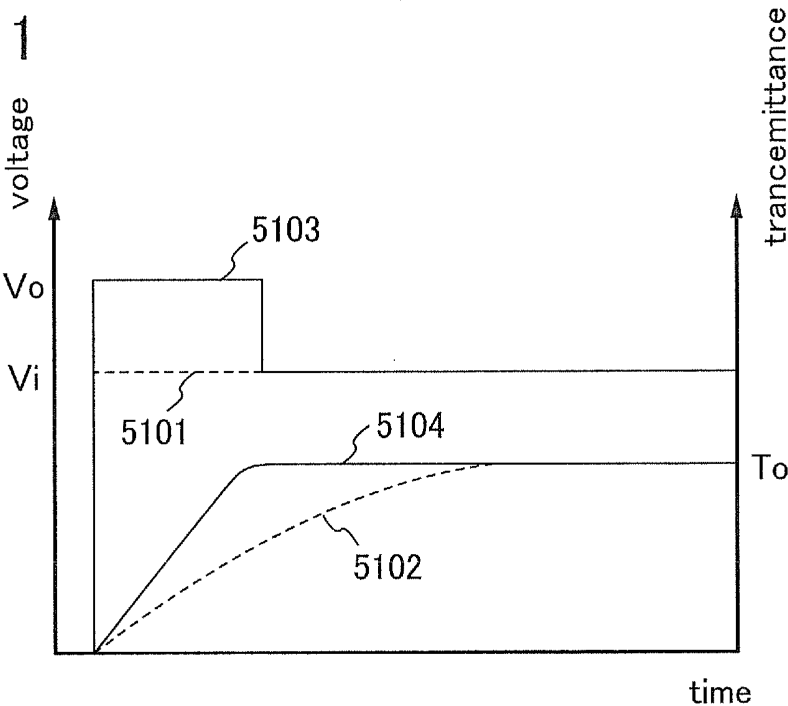


FIG. 12

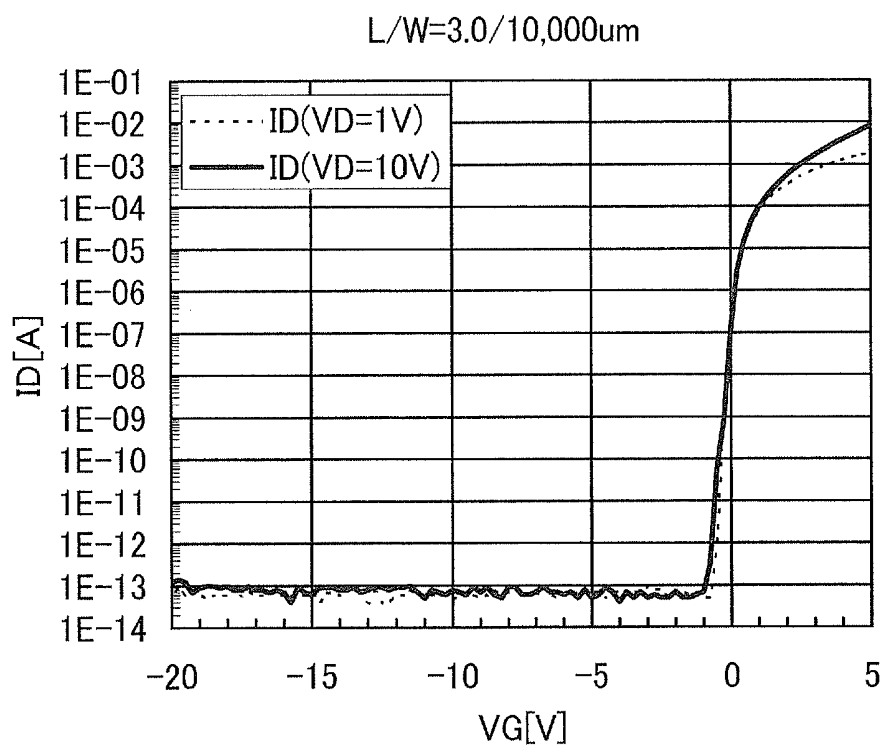
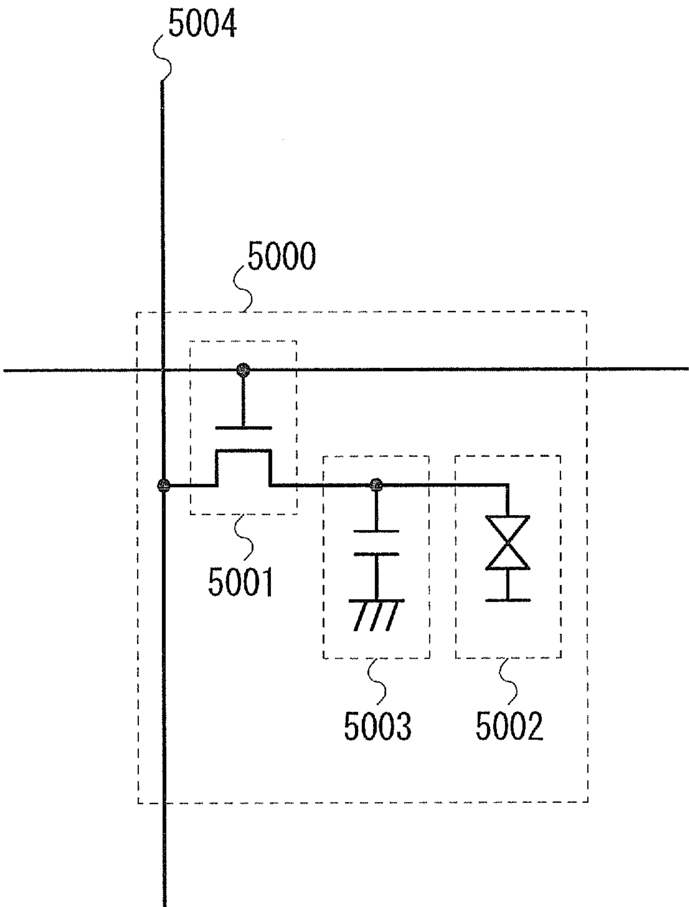


FIG. 13



# DISPLAY DEVICE

## TECHNICAL FIELD

**[0001]** The technical field of the present invention relates to a semiconductor device and a manufacturing method thereof. Further, the technical field of the present invention relates to a display device including the semiconductor device and a driving method thereof.

## BACKGROUND ART

**[0002]** As liquid crystal display devices, active matrix liquid crystal display devices in which pixels include switch elements are widely used. As illustrated in FIG. **13**, a pixel **5000** includes a transistor **5001** which functions as a switch element, a liquid crystal element **5002** to which a video signal is input from a wiring **5004** through the transistor **5001**, and a capacitor element **5003** which holds the video signal written to the liquid crystal element **5002**. With provision of the capacitor element **5003**, a video signal can be held even when the switch element is off.

**[0003]** Silicon, which has broad utility, is used as the semiconductor material of a transistor. However, in recent years, not only broad utility but also improvement in performance has been expected, and a technique related to a field effect transistor (also referred to as FET) including an oxide semiconductor has attracted attention (see Reference 1).

**[0004]** Further, in order to reduce the response time of a liquid crystal, a technique for instantaneously applying high voltage to the liquid crystal before a video signal is written (i.e., overdrive) has been performed (see Reference **2**).

## REFERENCES

**[0005]** [Reference 1] Japanese Published Patent Application No. 2006-165532

**[0006]** [Reference 2] Japanese Published Patent Application No. S64-010299

## DISCLOSURE OF INVENTION

**[0007]** In a conventional liquid crystal display device, it is necessary to store the combined capacitance ($C_{LC}+C_S$) due to the liquid crystal capacitance $C_{LC}$ of a liquid crystal element and the storage capacitance $C_S$ of a capacitor (in general, the capacitance $C_S$ is greater than or equal to 100 fF and less than or equal to 300 fF). Thus, considering a time constant $\tau=R(C_{LC}+C_S)$ which is necessary for storing electric charge, there is a problem in that it takes a longer time to write a signal by the time taken to store the storage capacitance $C_S$. The symbol R indicates the on resistance of a transistor.

**[0008]** In particular, in the case where overdrive is performed as disclosed in Reference 2, it is necessary to apply high voltage instantaneously. However, due to the time taken to store electric charge in a capacitor, the time taken to reach desired voltage becomes longer.

**[0009]** These problems become evident as the storage capacitance $C_S$ becomes higher. However, if a capacitor is not provided, it is difficult to hold a signal by using a transistor of a semiconductor material disclosed in Reference 1 because the off-state current of the transistor is high. Therefore, in the conventional liquid crystal display device, provision of the capacitor is essential.

**[0010]** In view of the foregoing problems, it is an object to shorten the time taken to store electric charge in a capacitor and to write a signal at high speed in a display device.

**[0011]** It is an object to provide a display device in which a signal can be written at high speed even when high voltage is applied, for example, even when overdrive is performed.

**[0012]** One embodiment of the present invention is a display device which includes a pixel having a transistor and a liquid crystal element electrically connected to a source or a drain of the transistor. The transistor includes an oxide semiconductor as a semiconductor material. The capacitance of a capacitor in the pixel is reduced. It is preferable that capacitor be not provided. It is more preferable that a capacitor be not provided intentionally and capacitance (parasitic capacitance) generated unintentionally is actively reduced. The parasitic capacitance is preferably less than or equal to 50 fF, more preferably less than or equal to 10 fF.

**[0013]** Another embodiment of the present invention is a display device which includes a pixel having a transistor, a first electrode electrically connected to a source or a drain of the transistor, a liquid crystal layer formed over the first electrode, and a second electrode provided below the first electrode with an insulating film provided therebetween. The first electrode and the second electrode do not overlap with each other, and an end portion of the first electrode and an end portion of the second electrode are aligned with each other. The transistor includes an oxide semiconductor as a semiconductor material. The pixel does not include a capacitor.

**[0014]** Further, the oxide semiconductor included in the transistor is an intrinsic (also referred to as i-type) or substantially intrinsic oxide semiconductor, and the off-state current of the transistor is $1\times10_{-17}$ A/μm or less.

**[0015]** Furthermore, overdrive is employed by which voltage higher than or equal to the voltage of a video signal is input before the video signal is input to the liquid crystal element.

**[0016]** The time taken to store electric charge in a capacitor can be shortened; thus, a signal can be written to a pixel at high speed.

**[0017]** Further, when the time taken to store electric charge in the capacitor is shortened, even high voltage can be applied in a short time; thus, overdrive can be effectively performed.

## BRIEF DESCRIPTION OF DRAWINGS

**[0018]** In the accompanying drawings:

**[0019]** FIG. **1** illustrates a pixel in a display device;

**[0020]** FIGS. **2**A and **2**B illustrate an electrode structure of a display device;

**[0021]** FIGS. **3**A and **3**B illustrate an electrode structure of a display device;

**[0022]** FIGS. **4**A and **4**B illustrate a pixel in a display device;

**[0023]** FIG. **5** is an energy band diagram;

**[0024]** FIG. **6** illustrates a transistor including an oxide semiconductor;

**[0025]** FIGS. **7**A and **7**B are energy band diagrams;

**[0026]** FIGS. **8**A and **8**B are energy band diagrams;

**[0027]** FIGS. **9**A to **9**E illustrate a method for manufacturing a semiconductor device;

**[0028]** FIGS. **10**A to **10**F illustrate examples of electronic devices;

**[0029]** FIG. **11** illustrates overdrive;

**[0030]** FIG. **12** illustrates electrical characteristics of a transistor; and

**[0031]** FIG. **13** illustrates a pixel in a display device.

## BEST MODE FOR CARRYING OUT THE INVENTION

**[0032]** Examples of embodiments of the present invention will be described below with reference to the drawings. Note that the present invention is not limited to the following description. It will be readily appreciated by those skilled in the art that modes and details of the present invention can be changed in various ways without departing from the spirit and scope of the present invention. Therefore, the present invention should not be construed as being limited to the following description of the embodiments.

**[0033]** Note that the position, size, range, or the like of each component illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like disclosed in the drawings and the like.

**[0034]** Note that in this specification and the like, terms such as "first" and "second" are used in order to avoid confusion among components and do not limit the number.

### Embodiment 1

**[0035]** An example of a pixel in a liquid crystal display device is described with reference to FIG. **1**. Elements included in a pixel **100** are a transistor **101** which functions as a switch element and a liquid crystal element **102**.

**[0036]** A gate of the transistor **101** is electrically connected to a wiring **103** (a gate signal line). One of a source and a drain of the transistor **101** is electrically connected to a wiring **104** (a source signal line). The other is electrically connected to the liquid crystal element **102**.

**[0037]** In this embodiment, an intrinsic or substantially intrinsic oxide semiconductor is used as the semiconductor material of the transistor **101**, and the off-state current per micrometer of the channel width of the transistor **101** is $1\times10^{-17}$ A or less ($1\times10^{-17}$ A/μm or less).

**[0038]** When the off-state current of the transistor **101** is $1\times10^{-17}$ A/μm or less, it means that the amount of leakage current is substantially zero when the transistor **101** is off. In other words, the potential of a node **105** does not fluctuate even when the transistor **101** is off; thus, a signal written to the pixel is held.

**[0039]** Thus, as illustrated in FIG. **1**, the pixel **100** does not necessarily include a capacitor. In other words, a capacitor wiring may be omitted. When the pixel illustrated in FIG. **1** is compared to the conventional pixel illustrated in FIG. **13**, the time taken to store the storage capacitance $C_S$ of a capacitor is not needed; thus, a signal can be written to the pixel at high speed.

**[0040]** With such a pixel structure where a capacitor is not necessarily provided, overdrive can be effectively performed. Overdrive is described with reference to FIG. **11**.

**[0041]** FIG. **11** shows a time change in transmittance of a liquid crystal with respect to voltage applied. When overdrive is not performed, the transmittance changes with respect to voltage Vi of a video signal that is indicated by a broken line **5101** over time as indicated by a broken line **5102** and reaches desired transmittance To.

**[0042]** In contrast, when overdrive is performed, by application of overdrive voltage Vo which is higher than the voltage Vi as indicated by a solid line **5103**, the time taken to reach the desired transmittance To can be shortened as indicated by a solid line **5104**. When voltage applied is made instantaneously high (or low) before writing of a signal in this manner, the response time of a liquid crystal can be reduced.

**[0043]** However, when high voltage such as the overdrive voltage Vo is instantaneously applied, the adverse effect of the time taken to store electric charge in a capacitor becomes more evident, so that the time taken to reach desired voltage becomes longer. Thus, with a pixel structure where a capacitor is not necessarily provided, the time taken to store electric charge in a capacitor can be shortened and even high voltage can be applied in a short time. Therefore, overdriving can be effectively performed.

**[0044]** Further, such a pixel structure is also effective when frame rate doubling is employed in a liquid crystal display device. In the frame rate doubling, the number of frames to be displayed is increased; thus, it is necessary to input a signal to a pixel at higher speed. Thus, with a pixel structure where a capacitor is not necessarily provided, the time taken to store electric charge in a capacitor can be shortened and frame rate doubling can be effectively performed.

**[0045]** The above structure and advantageous effects can be obtained when the transistor **101** is formed using an intrinsic or substantially intrinsic oxide semiconductor and the off-state current of the transistor **101** is $1\times10^{-17}$ A/μm or less.

**[0046]** In contrast, a conventional oxide semiconductor has n-type conductivity and an off-state current of about $1\times10^{-9}$ A/μm at the minimum. Therefore, a capacitor in a pixel is essential, and the time taken to write a signal is long.

**[0047]** Here, the conducting mechanism of a transistor including an oxide semiconductor in this embodiment is described with reference to FIG. **5**, FIG. **6**, FIGS. **7**A and **7**B, and FIGS. **8**A and **8**B. Note that the following description is based on the assumption of an ideal situation for easy understanding and does not necessarily reflect a real situation. Further, the following description is just a consideration and does not influence the validity of the present invention.

**[0048]** FIG. **5** illustrates a relationship between a vacuum level, the work function ($\phi_M$) of a metal (Metal), and the electron affinity ($\chi$) of an oxide semiconductor (OS). The Fermi level of the metal is denoted by $E_F$. The Fermi level of the oxide semiconductor is denoted by $E_f$. The energy at the bottom of the conduction band is denoted by $E_C$. The energy at the top of the valence band is denoted by $E_v$. The intrinsic Fermi level is denoted by $E_i$. The energy band gap of the oxide semiconductor is denoted by $E_g$. Note that the energy band gap ($E_g$) of the oxide semiconductor is 3 to 3.5 eV.

**[0049]** In FIG. **5**, in the case of a conventional oxide semiconductor having n-type conductivity, the Fermi level ($E_f$) is apart from the intrinsic Fermi level ($E_i$) positioned in the middle of the band gap ($E_g$) and is positioned near the conduction band ($E_C$).

**[0050]** Here, when the oxide semiconductor is made closer to an intrinsic semiconductor by the decrease in carrier density, the Fermi level ($E_f$) of the oxide semiconductor becomes closer to the intrinsic Fermi level ($E_i$). In this embodiment, an intrinsic or substantially intrinsic oxide semiconductor is in a state in which carrier density is decreased and the Fermi level ($E_f$) is made closer or equal to the intrinsic Fermi level ($E_i$).

**[0051]** The intrinsic or substantially intrinsic oxide semiconductor in this embodiment is obtained based on the following technical idea.

**[0052]** Hydrogen contained in an oxide semiconductor is one of the factors that make the oxide semiconductor have n-type conductivity. In the oxide semiconductor, part of

hydrogen serves as a donor and forms a shallow level which is 0.1 to 0.2 eV below the conduction band, so that carrier concentration is increased.

**[0053]** Deficiency of oxygen (oxygen deficiency) which is a main component of the oxide semiconductor is also one of the factors that make the oxide semiconductor have n-type conductivity. The oxygen deficiency forms a deep donor level in the oxide semiconductor, so that carrier concentration is increased.

**[0054]** Although many studies on physical properties of a semiconductor, such as density of states (DOS), have been conducted, they do not include an idea of sufficiently reducing a defect level itself In this embodiment, a highly purified intrinsic oxide semiconductor is obtained by removal of water or hydrogen, which might increase the DOS, from the oxide semiconductor. This is based on an idea of sufficiently reducing the DOS itself Thus, excellent industrial products can be manufactured.

**[0055]** In other words, in this embodiment, an impurity such as hydrogen, which is one of the factors that make the oxide semiconductor have n-type conductivity, is removed from an oxide semiconductor as much as possible, and the oxide semiconductor is highly purified by removal of oxygen deficiency. When the oxide semiconductor is highly purified, an intrinsic or substantially intrinsic oxide semiconductor can be obtained. Thus, in FIG. **5**, the Fermi level ($E_f$) can be substantially equal to the intrinsic Fermi level ($E_i$).

**[0056]** Specifically, the concentration of hydrogen in the oxide semiconductor is decreased to $5\times10^{19}/cm^3$ or lower, preferably $5\times10^{18}/cm^3$ or lower, more preferably $5\times10^{17}/cm^3$ or lower. Further, the carrier concentration of the oxide semiconductor is preferably much lower than that of a conventional oxide semiconductor (for example, lower than $1\times10^{12}/cm^3$, preferably $1.45\times10^{10}/cm^3$ or lower).

**[0057]** FIG. **6** illustrates an example of a bottom-gate thin film transistor with an inverted staggered structure that is formed using an intrinsic or substantially intrinsic oxide semiconductor. An oxide semiconductor layer (OS) is provided over a gate electrode (GE) with a gate insulating film (GI) provided therebetween. A source electrode (S) and a drain electrode (D) are provided thereover.

**[0058]** It is preferable that a Schottky electron barrier be not formed between the oxide semiconductor, and the source electrode and the drain electrode. In this embodiment, the electron affinity ($\chi$) of the oxide semiconductor is substantially equal to the work function ($\phi_M$) of a metal used for the source electrode and the drain electrode. For example, it is said that the electron affinity ($\chi$) is 4.3 eV in the case where the band gap ($E_g$) of the oxide semiconductor is 3.15 eV; thus, the source electrode and the drain electrode may be formed with a structure in which titanium (Ti), which has a work function ($\phi_M$) of about 4.3 eV, is in contact with the oxide semiconductor.

**[0059]** FIGS. **7**A and **7**B are energy band diagrams (schematic diagrams) in an A-A' cross section in FIG. **6**. FIG. **7**A illustrates the case where an electrical potential difference between the source electrode (S) and the drain electrode (D) is zero (the source electrode and the drain electrode have the same potential, $V_D$=0 V). FIG. **7**B illustrates the case where the potentials of the drain electrode and the gate electrode are higher than that of the source electrode ($V_D$>0 V). In FIG. **7**B, a broken line indicates the case where voltage is not applied to the gate electrode ($V_G$=0V), and a solid line indicates the case where voltage is applied to the gate electrode ($V_G$>0 V). In the case where voltage is not applied to the gate electrode, a carrier (an electron) is not injected from the electrode to an oxide semiconductor side due to a high potential barrier, so that current does not flow, which means an off state. In contrast, when positive voltage is applied to the gate electrode, the potential barrier is decreased, so that current flows, which means an on state.

**[0060]** In FIG. **7**B, a black circle (●) indicates an electron. When positive potentials are applied to the gate electrode and the drain electrode (D), as indicated by the solid line, the electron is injected into the oxide semiconductor (OS) over a barrier (h) and flows toward the drain electrode (D). The height of the barrier (h) changes depending on the gate voltage and the drain voltage. In the case where positive drain voltage is applied, the height of the barrier (h) is smaller than the height of the barrier in FIG. **7**A where no voltage is applied, i.e., half of the band gap ($E_g$).

**[0061]** In this case, as illustrated in FIG. **8**A, the electron moves in the vicinity of an interface between the gate insulating film (GI) and the oxide semiconductor (OS) (the lowest part of the oxide semiconductor that is energetically stable).

**[0062]** Further, as illustrated in FIG. **8**B, when a negative potential is applied to the gate electrode (GE), the amount of off-state current is extremely close to zero because holes that are minority carriers do not exist substantially.

**[0063]** In this manner, when a transistor is formed using an intrinsic or substantially intrinsic oxide semiconductor, the amount of off-state current can be substantially zero.

**[0064]** In addition, the temperature characteristics of the transistor are favorable. Typically, in the temperature range of from −25 to 150° C., the current-voltage characteristics of the transistor, such as on-state current, off-state current, field-effect mobility, a subthreshold value (an S value), and threshold voltage, hardly change and deteriorate due to temperature.

**[0065]** Note that in the intrinsic or substantially intrinsic oxide semiconductor, interface characteristics with the gate insulating film become noticeable. Therefore, an interface between the gate insulating film and the oxide semiconductor is preferably favorable. Specifically, for example, it is preferable to use an insulating film formed by CVD with the use of high-density plasma generated with a power frequency in the range of the VHF band to the microwave band, an insulating film formed by sputtering, or the like.

**[0066]** Since the band gap ($E_g$) of the oxide semiconductor is larger than the band gap of silicon, avalanche breakdown does not easily occur. Therefore, a transistor including an oxide semiconductor has high drain withstand voltage, so that on-state current does not easily increase sharply in an exponential manner even when a high electric field is applied.

**[0067]** As illustrated in FIG. **1**, the liquid crystal display device including the transistor of this embodiment does not necessarily include a capacitor in the pixel **100**. Therefore, when the pixel illustrated in FIG. **1** is compared to the conventional pixel illustrated in FIG. **13**, the time taken to store the storage capacitance $C_S$ of the capacitor is not needed, so that a signal can be written to the pixel **100** at high speed.

**[0068]** Note the liquid crystal display device can include a capacitor. Even when the liquid crystal display device includes a capacitor, the storage capacitance $C_S$ can be decreased because the leakage current of the transistor **101** is sufficiently low. Thus, the time taken to store electric charge can be shortened.

**[0069]** In this embodiment, the example of a bottom-gate thin film transistor with an inverted staggered structure is

described; however, the thin film transistor may be either a top-gate thin film transistor or a staggered thin film transistor. Alternatively, a channel-etched thin film transistor or a channel-stop thin film transistor can be employed as appropriate.

**[0070]** Note that the following can be used for the liquid crystal element: a nematic liquid crystal, a cholesteric liquid crystal, a smectic liquid crystal, a discotic liquid crystal, a thermotropic liquid crystal, a lyotropic liquid crystal, a low-molecular liquid crystal, a polymer liquid crystal, a polymer dispersed liquid crystal (PDLC), a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, a main-chain liquid crystal, a side-chain polymer liquid crystal, a plasma addressed liquid crystal (PALC), a banana-shaped liquid crystal, and the like.

**[0071]** In addition, the following can be used as the display method of the liquid crystal display device: a TN mode, an STN mode, an IPS mode, an FFS mode, an MVA mode, a PVA mode, an ASV mode, an ASM mode, an OCB mode, an ECB mode, an

**[0072]** FLC mode, an AFLC mode, a PDLC mode, a guest-host mode, a blue phase mode, and the like. Note that the present invention is not limited to this, and a variety of liquid crystal elements and driving methods thereof can be used as a liquid crystal element and a driving method thereof.

**[0073]** This embodiment can be combined with any of the other embodiments as appropriate.

Embodiment 2

**[0074]** In this embodiment, the case where an FFS mode is used as the display method of a liquid crystal display device is described.

**[0075]** First, FIGS. **2**A and **2**B illustrate an example of an electrode structure in a pixel with a conventional FFS mode. In FIGS. **2**A and **2**B, the liquid crystal element **5002** in the pixel circuit in FIG. **13** is illustrated. FIG. **2**A is a top view and FIG. **2**B is a cross-sectional view.

**[0076]** In FIGS. **2**A and **2**B, an electrode **201** is formed over a substrate **200**; an insulating film **202** is formed so as to cover the electrode **201**; an electrode **203** is formed over the insulating film **202**; and a liquid crystal layer **204** is formed over the electrode **203**. One of the electrode **201** and the electrode **203** is a pixel electrode. The other is a common electrode. The electrode **203** has a slit **207** (an opening portion). The electrode **201** is a plate-like (a shape covering the entire surface) electrode. The insulating film **202** may be a single layer or a stacked layer.

**[0077]** When a horizontal electric field is applied to the liquid crystal layer **204** by an FFS mode, a liquid crystal **205** is aligned in a lateral direction; thus, the viewing angle of the liquid crystal display device can be widen.

**[0078]** In a conventional structure, as illustrated in FIGS. **2**A and **2**B, the electrode **201** is a plate-like electrode and a capacitor **206** (storage capacitance $C_S$) is formed in a portion where the electrode **201** and the electrode **203** overlap with each other. In this case, as described in Embodiment 1, the time taken to write a signal becomes longer by the time taken to store the storage capacitance $C_S$.

**[0079]** Therefore, an FFS mode in this embodiment has an electrode structure illustrated in FIGS. **3**A and **3**B. In FIGS. **3**A and **3**B, the liquid crystal element **102** in the pixel circuit in FIG. **1** is illustrated. FIG. **3**A is a top view and FIG. **3**B is a cross-sectional view.

**[0080]** FIGS. **3**A and **3**B differ from FIGS. **2**A and **2**B in that an electrode **301** and an electrode **303** do not overlap with each other or overlap with each other in a smaller area as compared to the conventional structure, as illustrated in FIG. **3**B. In the case of the structure illustrated in FIG. **3**B, a capacitor is not formed between the electrode **301** and the electrode **303**, and parasitic capacitance generated between the electrode **301** and the electrode **303** is greatly decreased. Further, when an end portion of the electrode **301** and an end portion of the electrode **303** are aligned with each other, a horizontal electric field generated by the electrode **301** and the electrode **303** is easily applied.

**[0081]** In other words, with a structure where the electrode **301** and the electrode **303** do not overlap with each other and the end portion of the electrode **301** and the end portion of the electrode **303** are aligned with each other, an advantageous effect of alignment in a lateral direction by an FFS mode and an advantageous effect of the decrease in time taken to write a signal due to the decrease in the storage capacitance $C_S$ can be obtained in a synergistic manner. When the electrode **301** is formed, etching may performed so that a slit **310** (an opening portion) is provided, and the electrode **303** may be formed over the slit **310**. This structure also includes the case where a small part of the electrode **301** is formed below the electrode **303** or a narrow gap is generated between the end portions of the electrodes due to a slight difference in manufacturing steps.

**[0082]** Note that in FIG. **3**B, when the width W**1** of the electrode **301** is larger than the width W**2** of the electrode **303**, a horizontal electric field to be applied to the liquid crystal layer **204** is easily applied, which is particularly effective.

**[0083]** Further, in FIG. **3**B, an interval between the electrodes **303** (the width of the slit **310**) is equal to the width W**1** of the electrode **301**; however, the width W**1** is made smaller than the interval between the electrodes **303** so that an offset state can be obtained.

**[0084]** The electrode structure in FIGS. **3**A and **3**B is particularly effective when an oxide semiconductor of one embodiment of the present invention is used for a transistor. When an intrinsic or substantially intrinsic oxide semiconductor is used and the off-state current of the transistor is $1\times10_{-17}$ A/μm or less, the pixel does not necessarily include a capacitor; thus, the time taken to write a signal can be shortened.

**[0085]** Note that the pixel can include a capacitor. Even when the pixel includes a capacitor, the storage capacitance $C_S$ can be decreased because the leakage current of the transistor is sufficiently low. Thus, the time taken to store electric charge can be shortened. In that case, in FIGS. **3**A and **3**B, the electrode **301** and the electrode **303** partly overlap with each other so that a capacitor with a small area may be formed. Such a structure is effective because it is not necessary to decrease a display region.

**[0086]** FIGS. **4**A and **4**B illustrate a structure where the pixel in FIG. **1** is formed using the electrode structure in FIGS. **3**A and **3**B. FIG. **4**A is a top view and FIG. **4**B is a cross-sectional view. A cross-sectional view taken along line A-A' illustrates the transistor **101**. A cross-sectional view taken along line B-B' illustrates the liquid crystal element **102** in FIG. **1** in which the electrode structure in FIGS. **3**A to **3**B is employed.

**[0087]** In the cross-sectional view taken along line A-A', a gate electrode **401**, a gate insulating film **402**, an oxide semiconductor layer **403**, an electrode **404**, and an electrode **405** are provided between the substrate **200** and a substrate **410** so that a transistor **400** is formed. One of the electrode **404** and

the electrode **405** is a source electrode. The other is a drain electrode. An intrinsic or substantially intrinsic oxide semiconductor of one embodiment of the present invention can be used for the oxide semiconductor layer **403**.

**[0088]** In addition, the electrode **405** is electrically connected to the electrode **303**. FIGS. **4**A and **4**B illustrate just an example, and the electrode **405** may be electrically connected to the electrode **301**. Further, when a structure in which the gate electrode **401** and the electrode **301** are formed in the same layer, a structure in which the electrode **404**, the electrode **405**, and the electrode **301** are formed in the same layer, or a structure in which the electrode **404**, the electrode **405**, and the electrode **303** are formed in the same layer is employed, the number of steps may be reduced.

**[0089]** The electrode **301** and the electrode **303** can be formed to have a single-layer structure or a layered structure including a metal material such as molybdenum (Mo), titanium (Ti), chromium (Cr), tantalum (Ta), tungsten (W), aluminum (Al), copper (Cu), neodymium (Nd), or scandium (Sc), or an alloy containing the metal material as its main component.

**[0090]** Various kinds of metal oxide materials, for example, conductive metal oxides such as indium oxide ($In_2O_3$), tin oxide ($SnO_2$), and zinc oxide (ZnO); an alloy containing indium oxide and tin oxide ($In_2O_3$—$SnO_2$, which is abbreviated as ITO); and an alloy containing indium oxide and zinc oxide ($In_2O_3$—ZnO) can be used. Alternatively, any of these metal oxide materials may contain silicon or silicon oxide. These metal oxide materials have light-transmitting properties.

**[0091]** At least one of the electrode **301** and the electrode **303** is preferably formed using the light-transmitting material.

**[0092]** Note that FIGS. **4**A and **4**B illustrate the example of a bottom-gate thin film transistor with an inverted staggered structure; however, the thin film transistor may be either a top-gate thin film transistor or a staggered thin film transistor. Alternatively, a channel-etched thin film transistor or a channel-stop thin film transistor can be employed as appropriate.

**[0093]** Further, although not illustrated, an alignment film, a color filter, a light-blocking film, a spacer, a filler, or the like can be provided as appropriate.

**[0094]** This embodiment can be combined with any of the other embodiments as appropriate.

## Embodiment 3

**[0095]** In this embodiment, an example of a method for manufacturing a semiconductor device is described with reference to FIGS. **9**A to **9**E.

**[0096]** First, after a conductive film is formed over a substrate **1000** having an insulating surface, a gate electrode **1001** is formed in a first photolithography process. End portions of the gate electrode **1001** are preferably tapered because coverage with a gate insulating film stacked thereover is improved.

**[0097]** Although there is no particular limitation on a substrate which can be used as the substrate **1000** having an insulating surface, it is necessary that the substrate have at least heat resistance high enough to withstand heat treatment to be performed later. For example, various kinds of glass substrates can be used.

**[0098]** In the case where the temperature of the heat treatment to be performed later is high, a substrate whose strain point is higher than or equal to 730° C. is preferably used as a glass substrate. For the glass substrate, for example, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used. By containing more barium oxide (BaO) than boron oxide ($B_2O_3$), a more practical heat-resistant glass substrate can be obtained. Therefore, a glass substrate containing more BaO than $B_2O_3$ is preferably used.

**[0099]** Note that instead of the glass substrate, a substrate formed using an insulator, such as a ceramic substrate, a quartz substrate, or a sapphire substrate, may be used. Alternatively, a crystallized glass substrate or the like can be used. Alternatively, a plastic substrate or the like can be used as appropriate.

**[0100]** An insulating film which serves as a base film may be provided between the substrate **1000** and the gate electrode **1001**. The base film has a function of preventing diffusion of an impurity element from the substrate **1000**, and can be formed to have a single-layer structure or a layered structure including one or more films selected from a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, or a silicon oxynitride film.

**[0101]** In addition, the gate electrode **1001** can be formed to have a single-layer structure or a layered structure including a metal material such as molybdenum (Mo), titanium (Ti), chromium (Cr), tantalum (Ta), tungsten (W), aluminum (Al), copper (Cu), neodymium (Nd), or scandium (Sc), or an alloy containing the metal material as its main component.

**[0102]** Next, a gate insulating film **1002** is formed over the gate electrode **1001**.

**[0103]** The gate insulating film **1002** can be formed to have a single-layer structure or a layered structure including a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, an aluminum oxide layer, an aluminum nitride layer, an aluminum oxynitride layer, an aluminum nitride oxide layer, or a hafnium oxide layer by plasma-enhanced CVD, sputtering, or the like. In the case where a silicon oxide layer is deposited by sputtering, a silicon target or a quartz target is used as a target and oxygen or a mixed gas of oxygen and argon is used as a sputtering gas.

**[0104]** Here, an intrinsic or substantially intrinsic oxide semiconductor (a highly purified oxide semiconductor) which is formed over the gate insulating film **1002** is highly sensitive to an interface state and interface charge. Therefore, the gate insulating film **1002** which forms an interface needs to have high quality.

**[0105]** For example, high-density plasma-enhanced CVD using microwaves (e.g., a frequency of 2.45 GHz) is preferable because a dense high-quality insulating film having high withstand voltage can be formed. This is because when the highly purified oxide semiconductor is closely in contact with the high-quality gate insulating film, the interface state can be reduced and interface properties can be favorable.

**[0106]** Needless to say, a different deposition method such as sputtering or plasma-enhanced CVD can be used as long as a high-quality insulating film can be formed as the gate insulating film **1002**. In addition, any gate insulating film can be used as long as film quality and properties of an interface with an oxide semiconductor of the gate insulating film are modified by heat treatment performed after deposition. In either case, any gate insulating film can be used as long as film quality as a gate insulating film is high, interface state density with an oxide semiconductor is decreased, and a favorable interface can be formed.

**[0107]** The gate insulating film **1002** can have a structure in which a nitride insulating film and an oxide insulating film are sequentially stacked from the gate electrode **1001** side. For example, a 100-nm-thick gate insulating film is formed in such a manner that a silicon nitride film ($SiN_y$ (y>0)) with a thickness of 50 to 200 nm is formed as a first gate insulating film by sputtering and a silicon oxide film ($SiO_x$ (x>0)) with a thickness of 5 to 300 nm is stacked as a second gate insulating film over the first gate insulating film. The thickness of the gate insulating film may be set as appropriate depending on characteristics needed for the transistor and may be approximately 350 to 400 nm.

**[0108]** Then, an oxide semiconductor film **1003** is formed to a thickness of 2 to 200 nm over the gate insulating film **1002** (see FIG. **9**A).

**[0109]** The oxide semiconductor film **1003** can be formed using In—Sn—Ga—Zn—O, In—Ga—Zn—O, In—Sn—Zn—O, In—Al—Zn—O, Sn—Ga—Zn—O, Al—Ga—Zn—O, Sn—Al—Zn—O, In—Zn—O, Sn—Zn—O, Al—Zn—O, Zn—Mg—O, Sn—Mg—O, In—Mg—O, In—O, Sn—O, or Zn—O.

**[0110]** Alternatively, an oxide semiconductor material represented by In-A-B—O may be used. Here, A represents one or more kinds of elements selected from an element which belongs to Group 13, such as gallium (Ga) or aluminum (Al), or an element which belongs to Group 14, such as silicon (Si) or germanium (Ge). Further, B represents one or more kinds of elements selected from an element which belongs to Group 12, such as zinc (Zn). Note that the contents of In, A, and B are given content, and the content of A might be zero. However, the contents of In and B are not zero. That is, the oxide semiconductor material expressed as In-A-B—O might be In—Ga—Zn—O or In—Zn—3O, for example.

**[0111]** In particular, an In—Ga—Zn—O-based oxide semiconductor material has sufficiently high resistance when there is no electric field, can have sufficiently low off-state current, and has high field-effect mobility; thus, it is favorably used as an oxide semiconductor material used in a semiconductor device.

**[0112]** As a typical example of the In—Ga—Zn—O-based oxide semiconductor material, there is an oxide semiconductor material represented by $InGaO_3(ZnO)_m$ (m>0). Further, there is an oxide semiconductor material represented by $InMO_3(ZnO)_m$ (m>0) when M is used instead of Ga. Here, M denotes one or more metal elements selected from gallium (Ga), aluminum (Al), iron (Fe), nickel (Ni), manganese (Mn), cobalt (Co), or the like. For example, M can be Ga, Ga and Al, Ga and Fe, Ga and Ni, Ga and Mn, Ga and Co, or the like. Note that the composition is just an example.

**[0113]** In this embodiment, the oxide semiconductor film **1003** is formed using an In—Ga—Zn—**3**O-based metal oxide as a target by sputtering.

**[0114]** As a target used for forming the oxide semiconductor film **1003** by sputtering, for example, the composition ratio of a target including In, Ga, and Zn is In: Ga: Zn=1:x:y. Here, x is 0 to 2 and y is 1 to 5. For example, a target having a composition ratio of In: Ga: Zn=1:1:1 [atomic ratio] (x=1 and y=1) (i.e., $In_2O_3$: $Ga_2O_3$: ZnO=1:1:2 [molar ratio]) may be used. Alternatively, as the target, a metal oxide having a composition ratio of In: Ga: Zn=1:1:0.5 [atomic ratio], a metal oxide having a composition ratio of In: Ga: Zn=1:1:2 [atomic ratio], or a metal oxide having a composition ratio of In: Ga: Zn=1:0:1 [atomic ratio] (x=0 and y=1) can be used.

**[0115]** The substrate **1000** is held in a treatment chamber kept under reduced pressure and is heated at room temperature or a temperature lower than 400° C. A sputtering gas from which hydrogen and moisture are removed is introduced while moisture remaining in the treatment chamber is removed. Then, the oxide semiconductor film **1003** is deposited using metal oxide as a target. In order to remove moisture remaining in the treatment chamber, an adsorption vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. As an exhaust means, a turbo pump to which a cold trap is added may be used. For example, a hydrogen atom, a compound containing a hydrogen atom, such as water ($H_2O$) (preferably a compound containing a carbon atom), and the like are exhausted from the treatment chamber with the use of a cryopump. Therefore, the concentration of an impurity contained in the oxide semiconductor film deposited in the treatment chamber can be lowered. Further, by performing deposition by sputtering while removing moisture remaining in the treatment chamber with the use of a cryopump, the substrate temperature when the oxide semiconductor film **1003** is deposited can be higher than or equal to room temperature and lower than 400° C.

**[0116]** Then, the oxide semiconductor film is processed into an island-shaped oxide semiconductor layer **1004** in a second photolithography process (see FIG. **9**B).

**[0117]** Next, a conductive film is formed over the gate insulating film **1002** and the oxide semiconductor layer **1004**. The conductive film may be formed by sputtering or vacuum evaporation. As the conductive film, an element selected from aluminum (Al), chromium (Cr), copper (Cu), tantalum (Ta), titanium (Ti), molybdenum (Mo), or tungsten (W); an alloy including any of these elements; an alloy film including any of these elements in combination; or the like can be used. Alternatively, when an Al material to which an element preventing generation of hillocks or whiskers in an Al film, such as Si, Ti, Ta, W, Mo, Cr, Nd, Sc, or Y, is added is used, heat resistance can be increased.

**[0118]** Further, the conductive film may have a single-layer structure or a layered structure of two or more layers. For example, a single-layer structure of an aluminum film including silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in that order, or the like can be used. For example, a structure may be employed in which a refractory metal layer of Cr, Ta, Ti, Mo, W, or the like is stacked over one or both of an upper surface and a lower surface of a metal layer of Al, Cu, or the like.

**[0119]** As the conductive film, a conductive metal oxide such as indium oxide ($In_2O_3$), tin oxide ($SnO_2$), or zinc oxide (ZnO); an alloy containing indium oxide and tin oxide ($In_2O_3$—$SnO_2$, which is abbreviated as ITO); or an alloy containing indium oxide and zinc oxide ($In_2O_3$—ZnO) can be used. Alternatively, the metal oxide material can contain silicon or silicon oxide.

**[0120]** In this embodiment, the conductive film is formed using titanium (Ti).

**[0121]** A source electrode **1005** and a drain electrode **1006** are formed in a third photolithography process (see FIG. **9**C).

**[0122]** Note that each material and etching conditions are adjusted as appropriate so that the oxide semiconductor layer **1004** is not removed when the conductive film is etched.

**[0123]** Note that in the third photolithography process, only part of the oxide semiconductor layer **1004** is etched so that an oxide semiconductor layer having a groove (a depression) is formed in some cases.

**[0124]** Then, an oxide insulating film **1007** which serves as a protective insulating film is formed in contact with part of the oxide semiconductor layer **1004** (see FIG. **9**D).

**[0125]** In this embodiment, the oxide semiconductor layer **1004** and the oxide insulating film **1007** are formed so as to be in contact with each other in a region where the oxide semiconductor layer **1004** does not overlap with the source electrode **1005** and the drain electrode **1006**.

**[0126]** In this embodiment, a silicon oxide layer having a defect is deposited as the oxide insulating film **1007** in such a manner that the substrate **1000** over which the films up to the island-shaped oxide semiconductor layer **1004**, the source electrode **1005**, and the drain electrode **1006** are formed is heated at room temperature or a temperature lower than 100° C., a sputtering gas including high-purity oxygen from which hydrogen and moisture are removed is introduced, and a silicon semiconductor target is used.

**[0127]** Note that the oxide insulating film **1007** is preferably formed while moisture remaining in the treatment chamber is being removed so that hydrogen, a hydroxyl group, or moisture is not contained in the oxide semiconductor layer **1004** and the oxide insulating film **1007**.

**[0128]** In order to remove moisture remaining in the treatment chamber, an adsorption vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. As an exhaust means, a turbo pump to which a cold trap is added may be used. For example, a hydrogen atom, a compound containing a hydrogen atom, such as water ($H_2O$), and the like are exhausted from the treatment chamber with the use of a cryopump. Therefore, the concentration of an impurity contained in the oxide semiconductor film **1007** deposited in the treatment chamber can be lowered.

**[0129]** Note that as the oxide insulating film **1007**, a silicon oxynitride layer, an aluminum oxide layer, an aluminum oxynitride layer, or the like can be used instead of the silicon oxide layer.

**[0130]** In addition, heat treatment may be performed at 100 to 400° C. in a state where the oxide insulating film **1007** and the oxide semiconductor layer **1004** are in contact with each other. Since the oxide insulating film **1007** in this embodiment includes many defects, by the heat treatment, an impurity such as hydrogen, moisture, a hydroxyl group, or hydride contained in the oxide semiconductor layer **1004** is diffused into the oxide insulating film **1007**, so that the impurity contained in the oxide semiconductor layer **1004** can be further reduced. Through the heat treatment, oxygen contained in the semiconductor insulating film **1007** is supplied to the oxide semiconductor layer **1004**.

**[0131]** Through the above steps, a transistor **1008** including the oxide semiconductor layer **1004** can be formed (see FIG. **9**E).

**[0132]** The oxide semiconductor layer **1004** is highly purified by sufficient removal of an impurity such as hydrogen and the supply of oxygen. Specifically, the concentration of hydrogen in the oxide semiconductor layer **1004** is $5\times10^{19}/cm^3$ or lower, preferably $5\times10^{18}/cm^3$ or lower, more preferably $5\times10^{17}/cm^3$ or lower. The carrier concentration of the oxide semiconductor layer **1004** is much lower than a conventional oxide semiconductor layer (e.g., $1\times10^{12}/cm^3$ or lower, preferably $1.45\times10^{10}/cm^3$ or lower). With the use of an intrinsic or substantially intrinsic oxide semiconductor in this manner, the transistor **1008** whose off-state current is $1\times10^{17}$ A/μm or less can be obtained. The concentration of hydrogen can be measured by, for example, secondary ion mass spectroscopy (SIMS) or the like. Further, the carrier concentration can be measured by manufacture of a MOS capacitor with the use of an oxide semiconductor and, for example, by evaluation of the results of CV measurement (CV characteristics) or the like.

**[0133]** A protective insulating film **1009** may be provided over the oxide insulating film **1007**. In this embodiment, the protective insulating film **1009** is formed over the oxide insulating film **1007**. As the protective insulating film **1009**, a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, an aluminum nitride oxide film, or the like is used.

**[0134]** The transistor **1008** formed by the method of this embodiment can be used in the liquid crystal display devices in Embodiments 1 and 2. A capacitor is not necessarily provided in a pixel. When a capacitor is not provided in a pixel, the time taken to store the storage capacitance $C_S$ of the capacitor is not needed; thus, the total time taken to store electric charge can be shortened.

**[0135]** The above steps can be used for manufacture of a backplane (a substrate provided with a thin film transistor) of an electroluminescent display panel, a display device including electronic ink, or the like. Since the above steps are performed at a temperature of 400° C. or lower, they can also be applied to manufacturing steps in which a glass substrate having a thickness of 1 mm or less and a side longer than 1 m is used. In addition, since all the steps can be performed at a treatment temperature of 400° C. or lower, a large amount of energy is not needed for manufacturing a display device.

**[0136]** Note that in this embodiment, an example of a bottom-gate thin film transistor with an inverted staggered structure is described; however, the thin film transistor may be either a top-gate thin film transistor or a staggered thin film transistor. Alternatively, a channel-etched thin film transistor or a channel-stop thin film transistor can be employed as appropriate.

**[0137]** This embodiment can be combined with any of the other embodiments as appropriate.

## Embodiment 4

**[0138]** In this embodiment, FIGS. **10**A to **10**F illustrate examples of electronic devices each including the display device described in the above embodiment.

**[0139]** FIG. **10**A illustrates a laptop personal computer. A main body **2001** includes a display portion **2101**.

**[0140]** FIG. **10**B illustrates a personal digital assistant (PDA). A main body **2002** includes a display portion **2102**.

**[0141]** FIG. **10**C illustrates an e-book reader as an example of electronic paper. A main body **2003** includes a display portion **2103** and a display portion **2104**.

**[0142]** FIG. **10**D illustrates a cellular phone. A main body **2004** includes a display portion **2105**.

**[0143]** FIG. **10**E illustrates a digital camera. A main body **2005** includes a display portion **2106** and a display portion **2107**.

**[0144]** FIG. **10**F illustrates a television set. A main body **2006** includes a display portion **2108**.

**[0145]** In the electronic devices in FIGS. **10**A to **10**F, by provision of the display device described in the above

embodiment as the display portions **2101** to **2108**, provision of a capacitor can be omitted or a capacitance value can be reduced as much as possible; thus, a signal can be written at high speed. Further, overdrive, frame rate doubling, or the like can be efficiently performed, so that the performance of the electronic devices can be drastically improved.

**[0146]** This embodiment can be combined with any of the other embodiments as appropriate.

EXAMPLE 1

**[0147]** FIG. **12** illustrates $V_G$-$I_D$ characteristics as the initial characteristics of a transistor including an intrinsic or substantially intrinsic oxide semiconductor film which is obtained by the method in Embodiment 3.

**[0148]** FIG. **12** illustrates measurement results of a sample in which a transistor having a channel width W of $1\times10^4$ μm and a channel length L of 3 μm is used and the temperature is room temperature. Off-state current was $1\times10^{-13}$ A or less, which was the measurement limit of a measurement device (a parameter analyzer Agilent 4156C Agilent Technologies, Inc.). A subthreshold swing value (an S value) was 0.1 V/dec. Note that off-state current per micrometer of the channel width was $1\times10^{-17}$ A/μm. In the sample, two hundred transistors each having a channel width W of 50 μm and a channel length L of 3 μm are connected in parallel so that the transistor having a channel width W of $1\times10^4$ μm and a channel length L of 3 μm was formed.

**[0149]** This example can be combined with any of the embodiments as appropriate.

**[0150]** This application is based on Japanese Patent Application serial no. 2009-276374 filed with Japan Patent Office on Dec. 4, 2009, the entire contents of which are hereby incorporated by reference.

**1**. (canceled)

**2**. A display device comprising:
a pixel, the pixel comprising:
a transistor; and
a liquid crystal element,
wherein the liquid crystal element is electrically connected to one of a source and a drain of the transistor,
wherein the transistor includes an intrinsic or substantially intrinsic oxide semiconductor layer which includes a channel formation region,
wherein the oxide semiconductor layer comprises a portion in which a concentration of hydrogen is $5\times10^{19}$/cm$^3$ or lower, and
wherein the oxide semiconductor layer comprises a portion in which a carrier concentration is $1\times10^{12}$/cm$^3$ or lower.

**3**. The display device according to claim **2**, wherein an off-state current of the transistor is $1\times10^{-17}$ A/μm or less.

**4**. The display device according to claim **2**, wherein the pixel does not include a capacitor wiring.

**5**. The display device according to claim **2**, wherein a parasitic capacitance in the pixel is less than or equal to 50 fF.

**6**. A display device comprising:
a pixel, the pixel comprising:
a transistor; and
a liquid crystal element,
wherein the liquid crystal element is electrically connected to one of a source and a drain of the transistor,
wherein the transistor includes an oxide semiconductor layer including a channel formation region,
wherein the oxide semiconductor layer comprises a portion in which a concentration of hydrogen is $5\times10^{19}$/cm$^3$ or lower,
wherein the oxide semiconductor layer comprises a portion in which a carrier concentration is $1\times10^{12}$/cm$^3$ or lower, and
wherein a voltage higher than or equal to a voltage of a video signal is input to the liquid crystal element before the video signal is input.

**7**. The display device according to claim **6**, wherein an off-state current of the transistor is $1\times10^{-17}$ A/μm or less.

**8**. The display device according to claim **6**, wherein the pixel does not include a capacitor wiring.

**9**. The display device according to claim **6**, wherein a parasitic capacitance in the pixel is less than or equal to 50 fF.

**10**. A display device comprising:
a pixel, the pixel comprising:
a first electrode;
a second electrode, the second electrode comprising a portion not overlapping with the first electrode;
an insulating film between the first electrode and the second electrode;
a transistor; and
a liquid crystal layer,
wherein the liquid crystal layer is over the first electrode and the second electrode,
wherein the second electrode is electrically connected to one of a source and a drain of the transistor,
wherein the transistor includes an intrinsic or substantially intrinsic oxide semiconductor layer which includes a channel formation region,
wherein the oxide semiconductor layer comprises a portion in which a concentration of hydrogen is $5\times10^{19}$/cm$^3$ or lower, and
wherein the oxide semiconductor layer comprises a portion in which a carrier concentration is $1\times10^{12}$/cm$^3$ or lower.

**11**. The display device according to claim **10**, wherein an off-state current of the transistor is $1\times10^{-17}$ A/μm or less.

**12**. The display device according to claim **10**, wherein the pixel does not include a capacitor wiring.

**13**. The display device according to claim **10**, wherein a parasitic capacitance in the pixel is less than or equal to 50 fF.

**14**. The display device according to claim **10**, wherein a voltage higher than or equal to a voltage of a video signal is input to the first electrode before the video signal is input.

**15**. The display device according to claim **10**, wherein the second electrode is over the first electrode.

**16**. The display device according to claim **10**, wherein the first electrode and the second electrode do not overlap with each other.

* * * * *

patsnap

| 专利名称(译) | 显示设备 | | |
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摘要(译)

在显示设备中缩短了将信号写入像素所花费的时间。此外，即使在施加高电压时也以高速写入信号。该显示装置包括像素，该像素包括晶体管管和电连接到晶体管的源极或漏极的液晶元件。晶体管包括作为半导体材料的本征或基本上本征的氧化物半导体，并且具有1×10-17A /μm或更小的截止态电流。像素不包括电容器。由于不需要提供电容器，因此可以缩短写入信号所花费的时间。