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(54) **LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

(71) Applicant: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi (JP)

(72) Inventors: **Shunpei YAMAZAKI**, Setagaya (JP); **Yoshiharu HIRAKATA**, Atsugi (JP)

(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi (JP)

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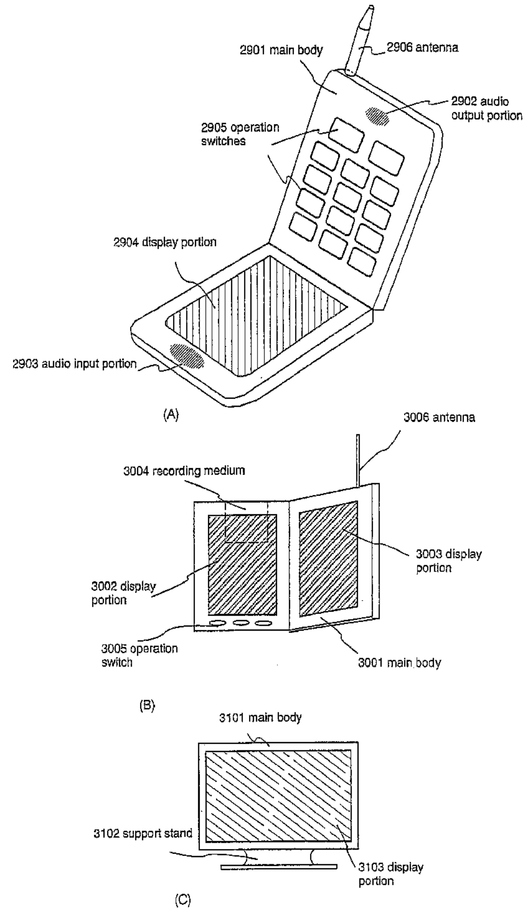
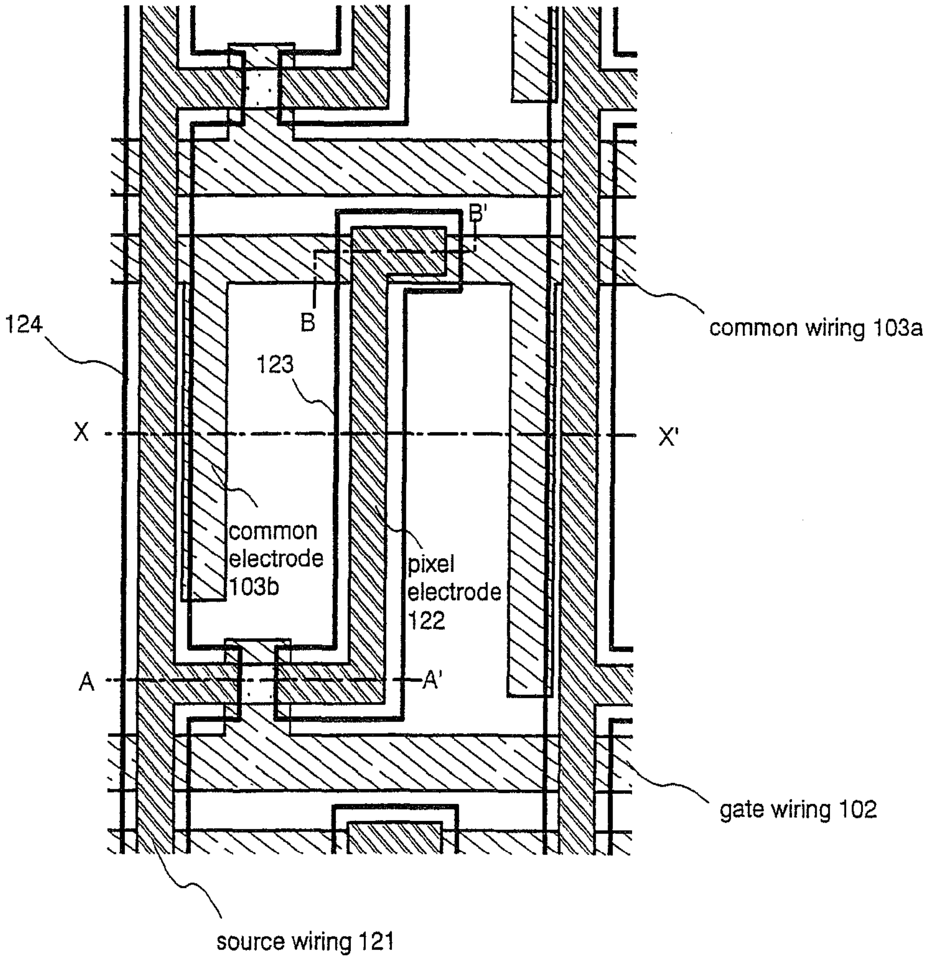
USPC **349/46**

(57) **ABSTRACT**

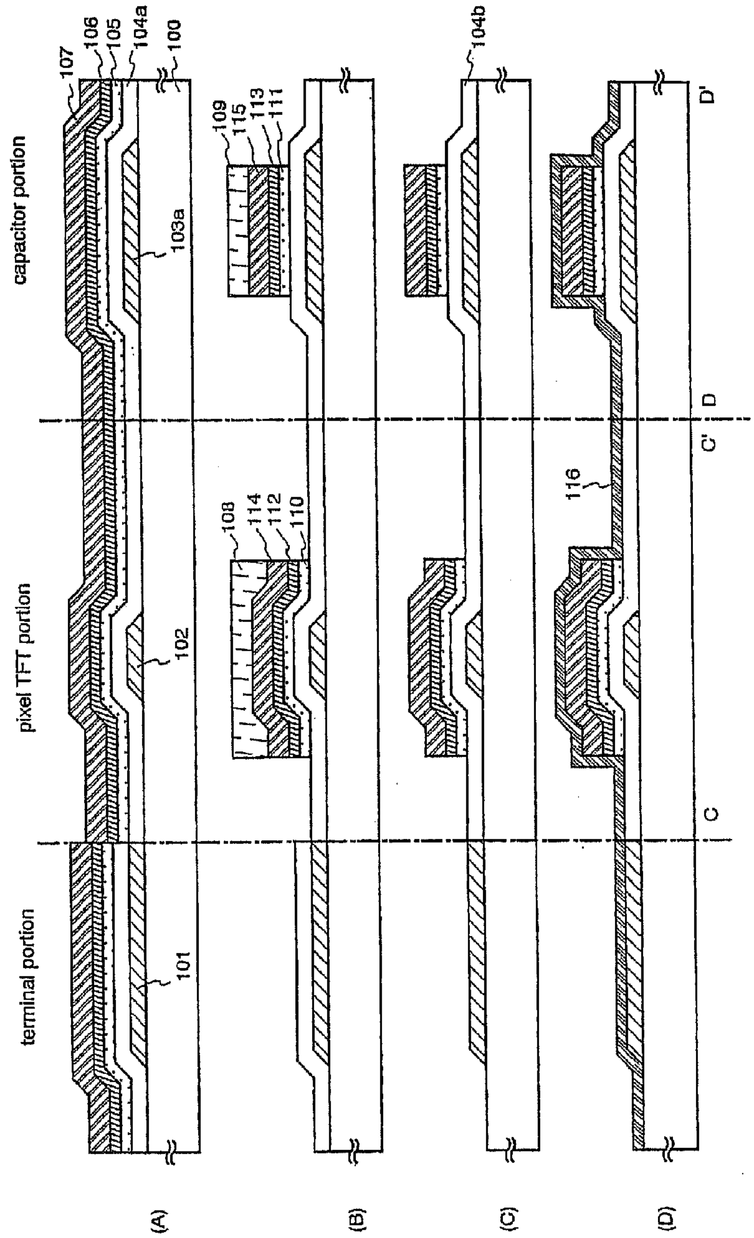
In a liquid crystal display device of an IPS system, to realize reduction of manufacturing cost and improvement of yield by decreasing the number of steps for manufacturing a TFT. A channel etch type bottom gate TFT structure, where patterning of a source region and a drain region and patterning of a source wiring and a pixel electrode are carried out by the same photomask.



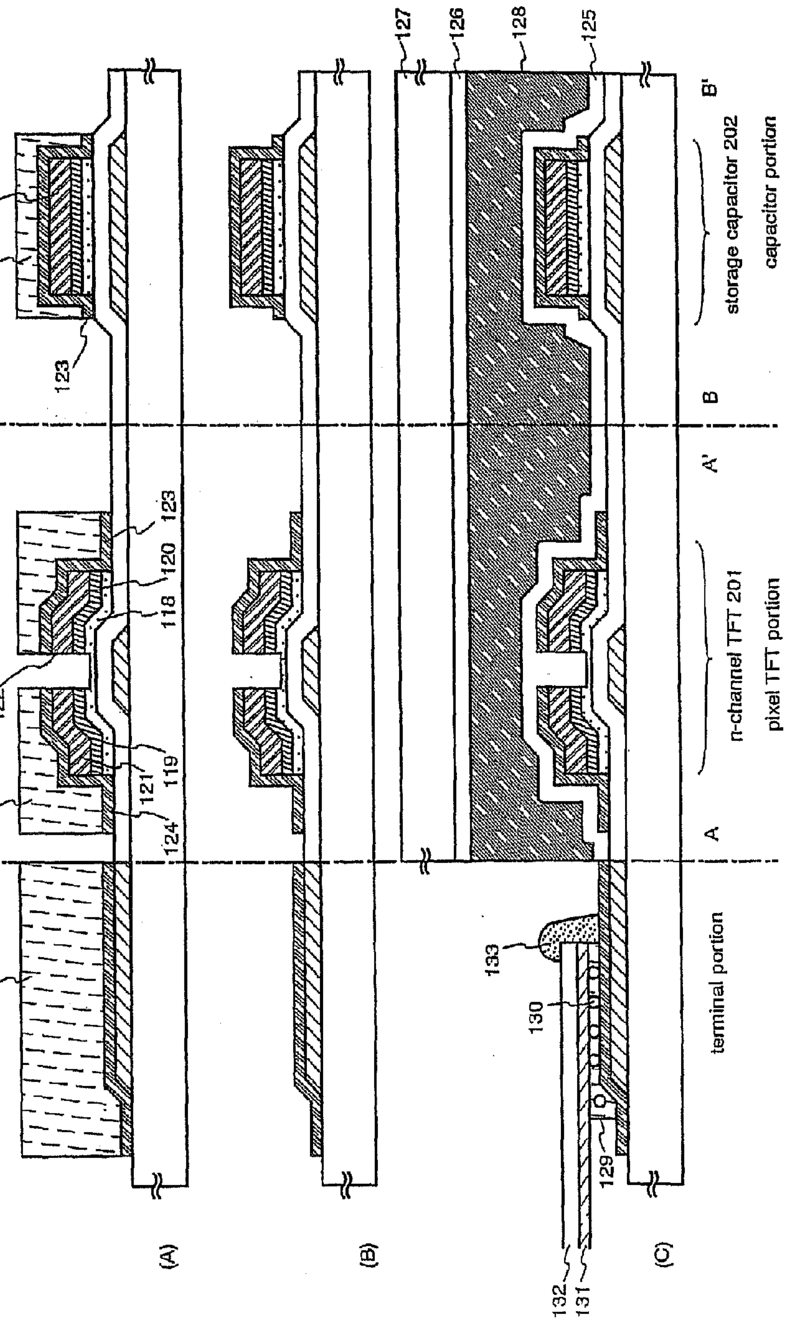
[Fig. 1]


124
123
B'
B
common wiring 103a
X
X'
common electrode 103b
pixel electrode 122
A
A'
gate wiring 102
source wiring 121

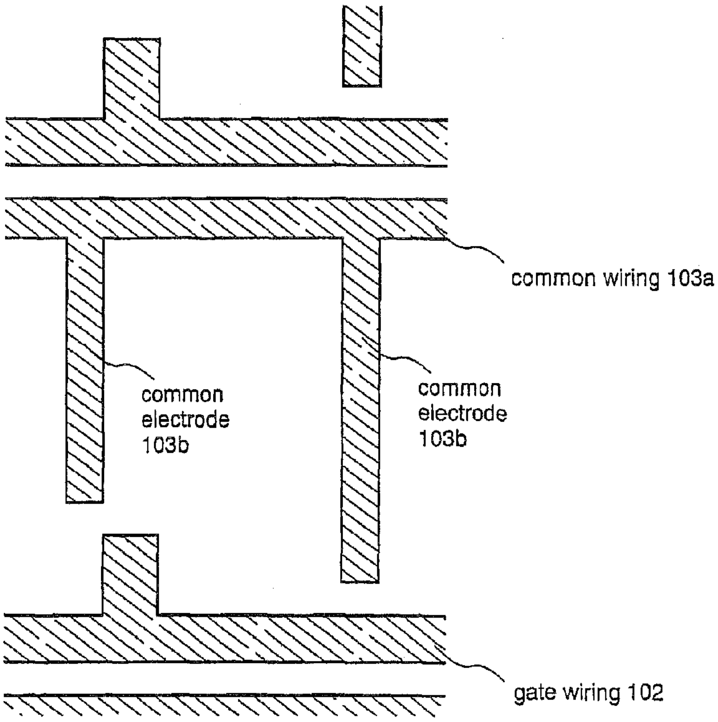
[Fig. 2]


terminal portion
pixel TFT portion
capacitor portion
107
106
105
104a
100
101
102
103a
(A)
109
115
113
111
108
114
112
110
(B)
104b
(C)
116
C
C'
D
D'
(D)

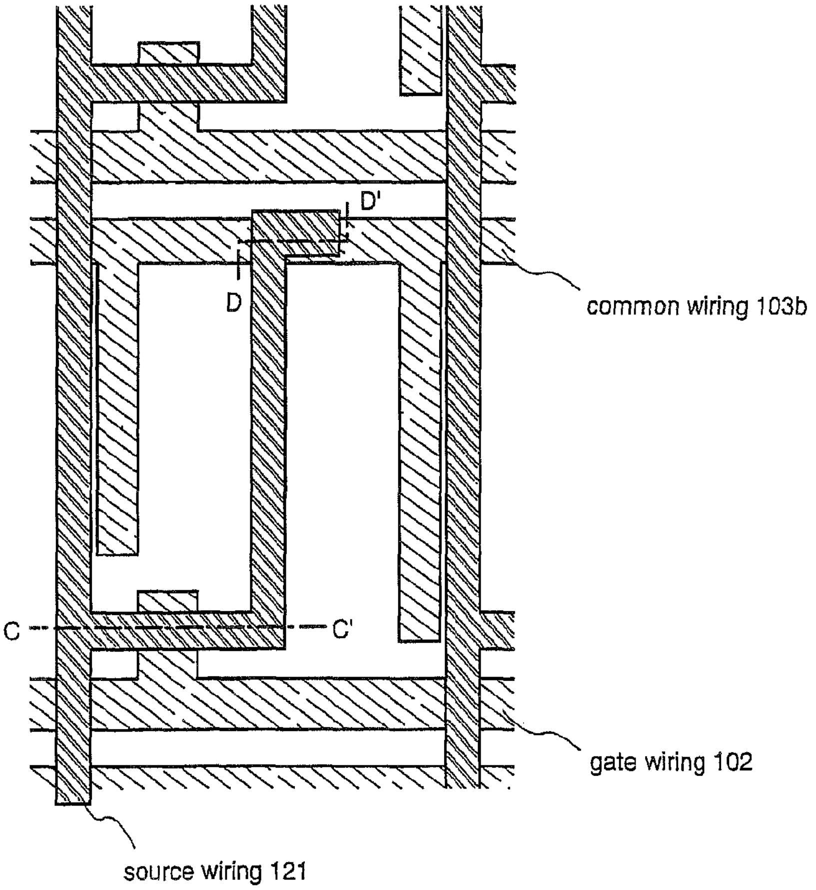
[Fig. 3]


(A)
117c
117a
124
121
119
122
118
120
123
117b 122
123
(B)
(C)
132
131
129
130
133
127
126
128
125
A
A'
B
B'
terminal portion
n-channel TFT 201
pixel TFT portion
storage capacitor 202
capacitor portion

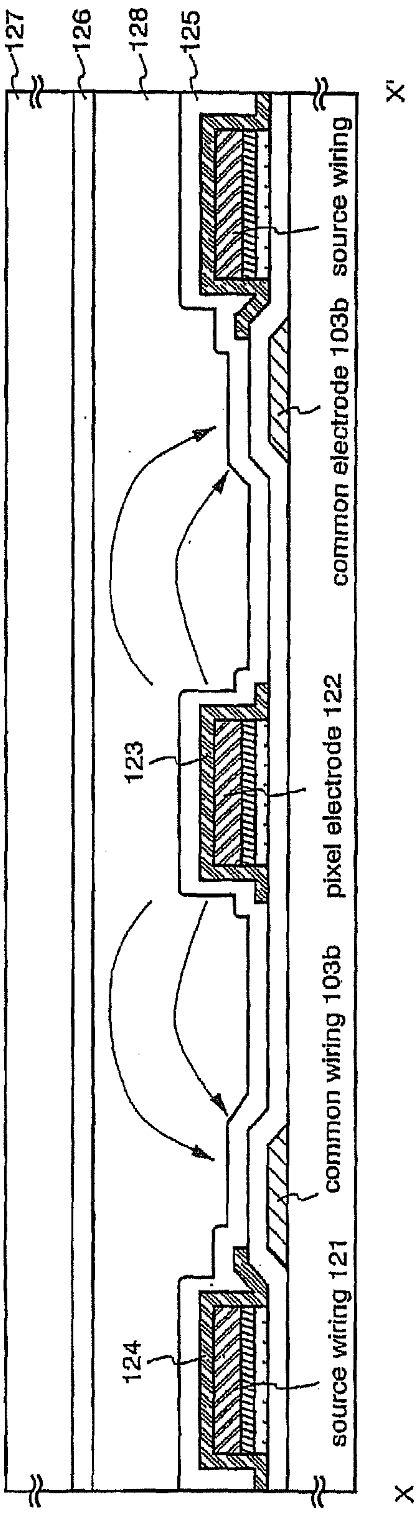
[Fig. 4]


common wiring 103a
common electrode 103b
common electrode 103b
gate wiring 102

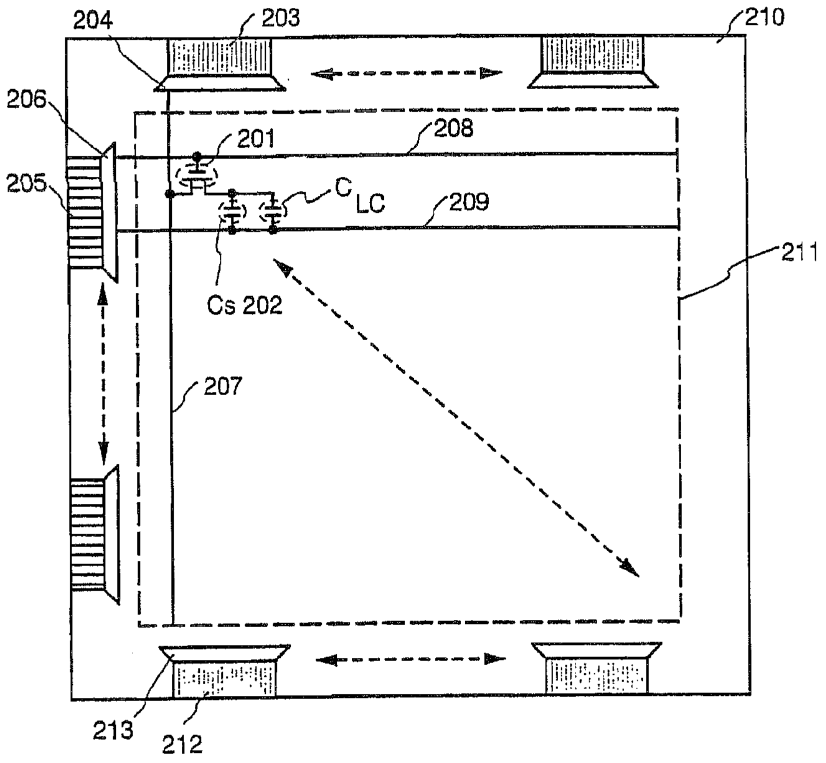
[Fig. 5]



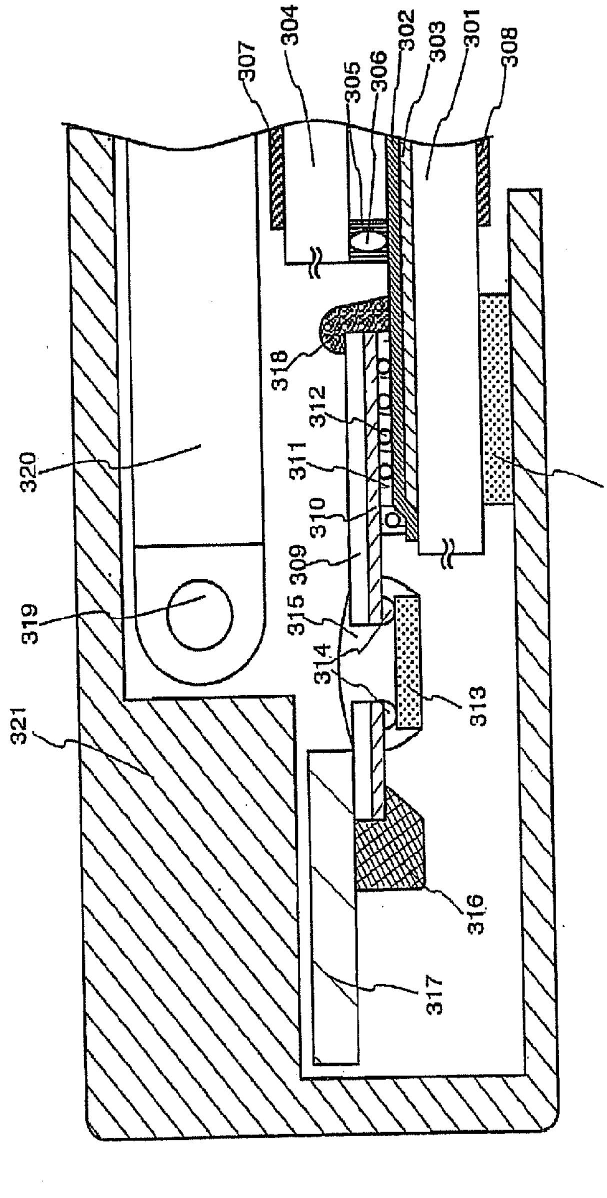
[Fig. 6]


X
source wiring 121
124
common wiring 103b
pixel electrode 122
123
common electrode 103b
source wiring
127
126
128
125
X'

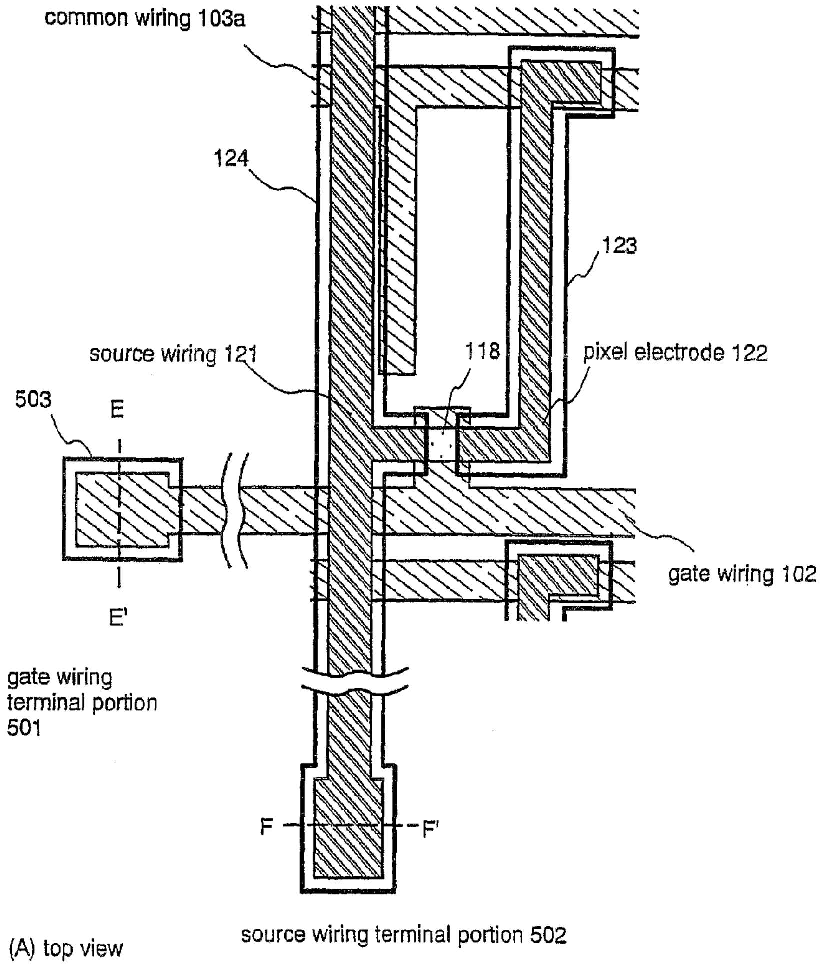
[Fig. 7]



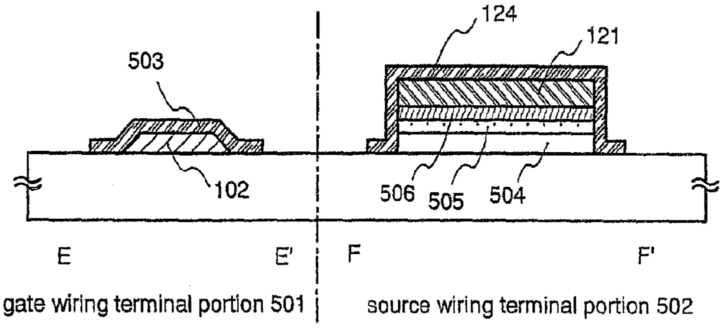
[Fig. 8]


307
304
305
306
302
303
301
308
318
312
311
310
309
315
314
313
320
319
321
322
316
317

[Fig. 9]

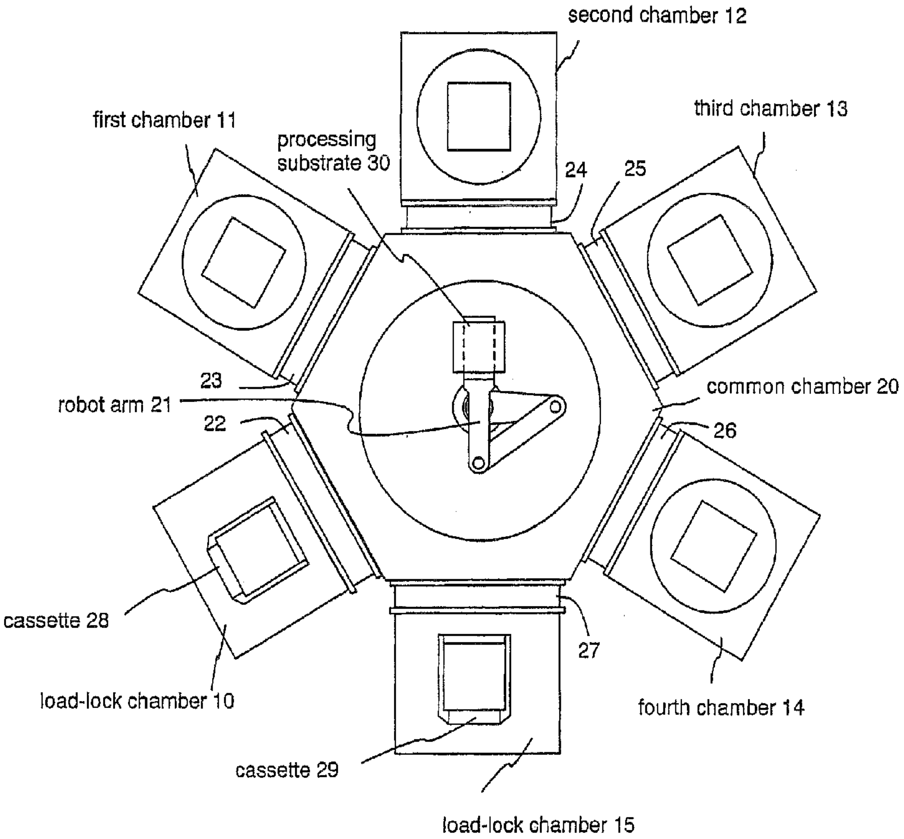


(A) top view

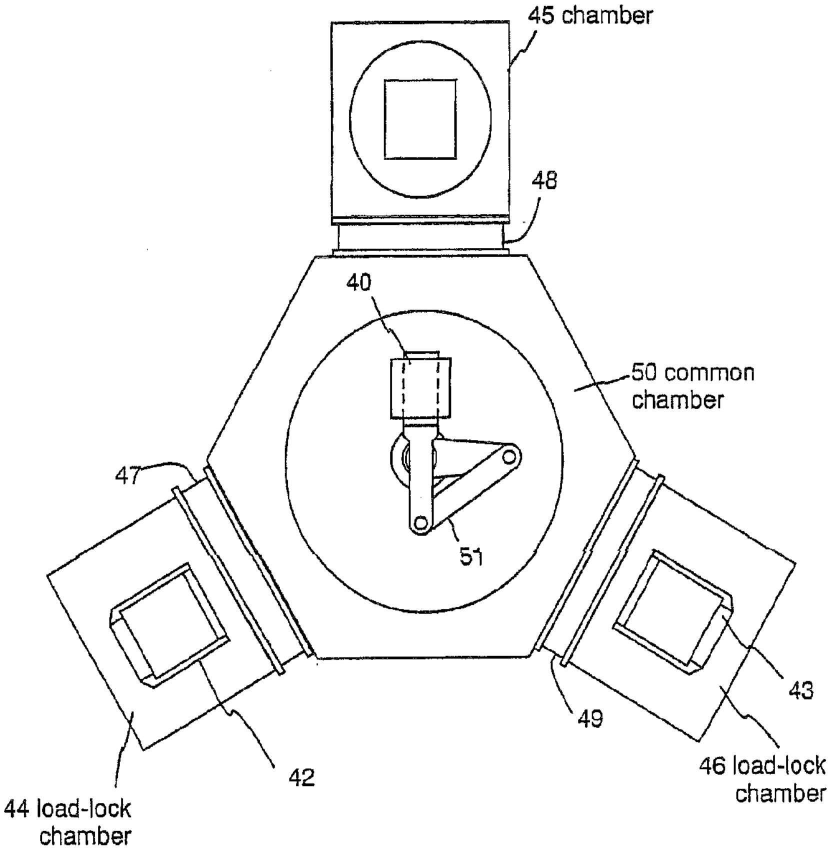


(B) cross sectional view

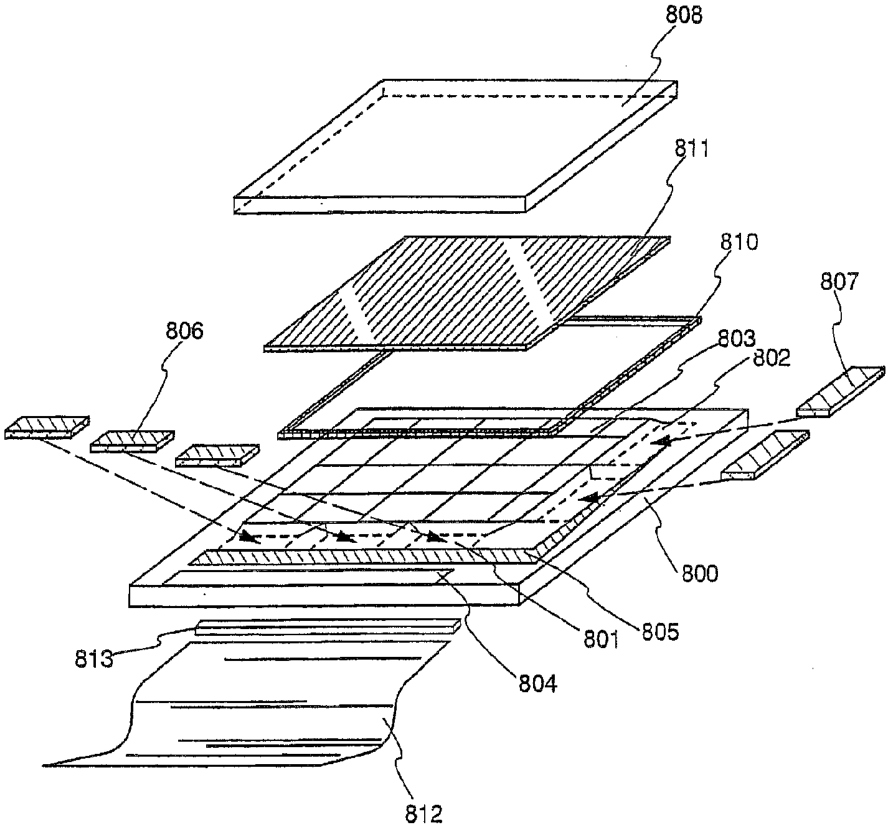
[Fig. 10]


second chamber 12
first chamber 11
processing substrate 30
third chamber 13
24
25
23
robot arm 21
22
common chamber 20
26
cassette 28
load-lock chamber 10
27
fourth chamber 14
cassette 29
load-lock chamber 15

[Fig. 11]

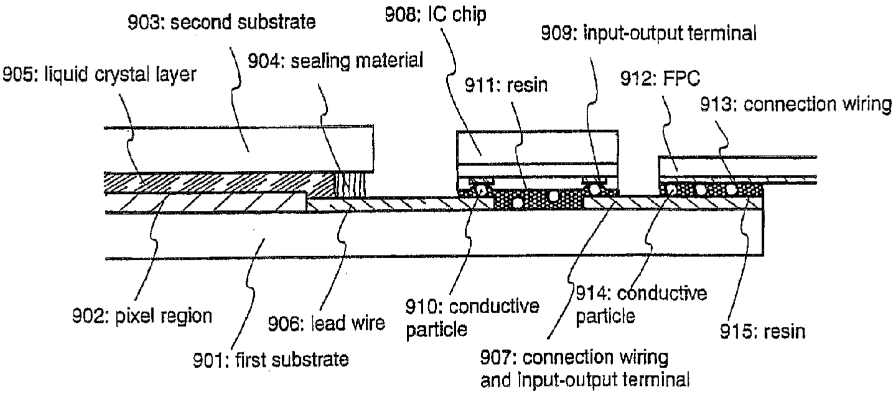

45 chamber
48
40
50 common chamber
47
51
43
49
42
46 load-lock chamber
44 load-lock chamber

[Fig. 12]

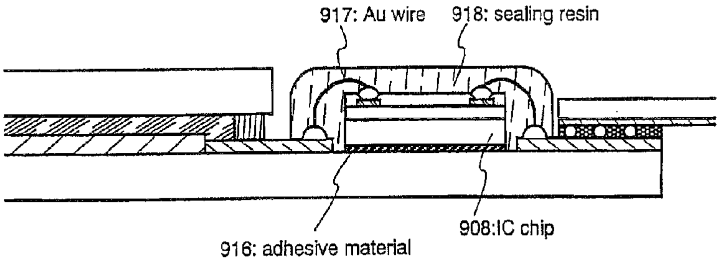


800: first substrate, 801: a region for attaching IC chip (data line),
802: a region for attaching IC chip (scanning line), 803: pixel region
804: input-output terminal, 805: connection wiring, 806,807: IC chip
808: second substrate, 810: sealing material, 811: liquid crystal,
812: FPC, 813: reinforcing plate

[Fig. 13]

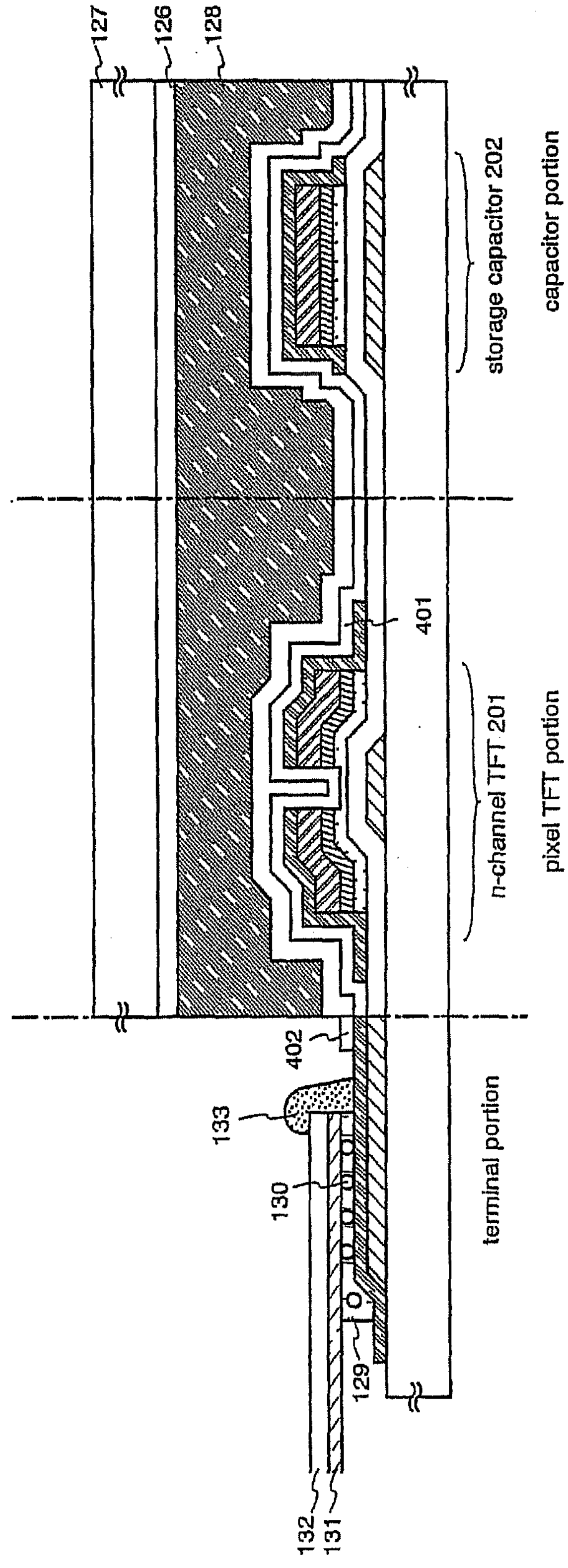

903: second substrate
908: IC chip
909: input-output terminal
905: liquid crystal layer
904: sealing material
911: resin
912: FPC
913: connection wiring
902: pixel region
906: lead wire
910: conductive particle
914: conductive particle
915: resin
901: first substrate
907: connection wiring and input-output terminal

(A)

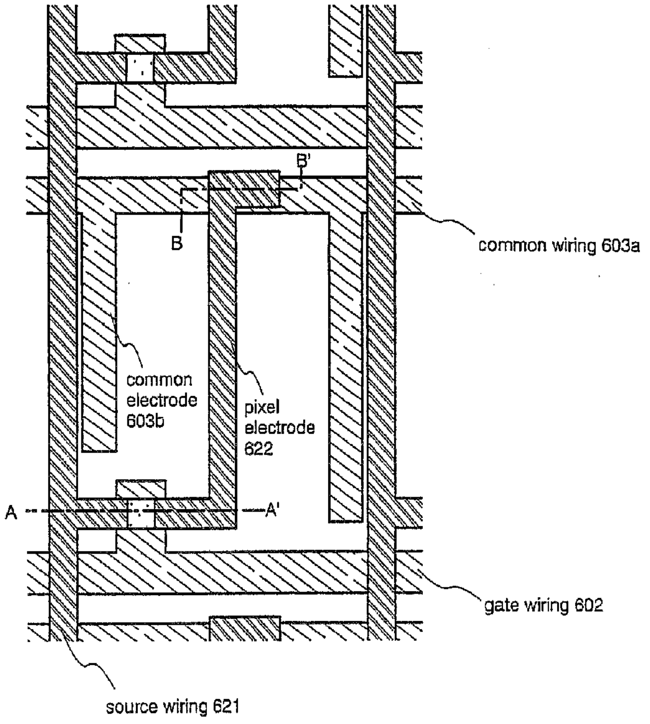

917: Au wire
918: sealing resin
916: adhesive material
908:IC chip

(B)

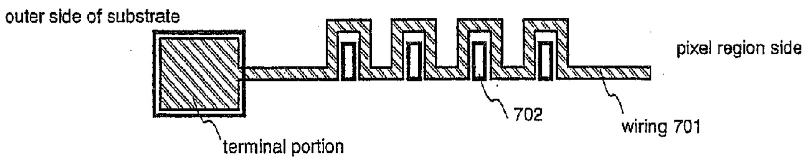
[Fig. 14]


127
126
128
storage capacitor 202
capacitor portion
401
n-channel TFT 201
pixel TFT portion
402
133
130
terminal portion
129
132
131

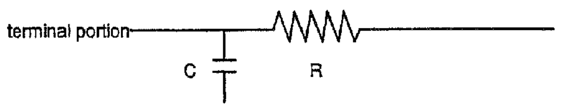
[Fig. 15]



[Fig. 16]

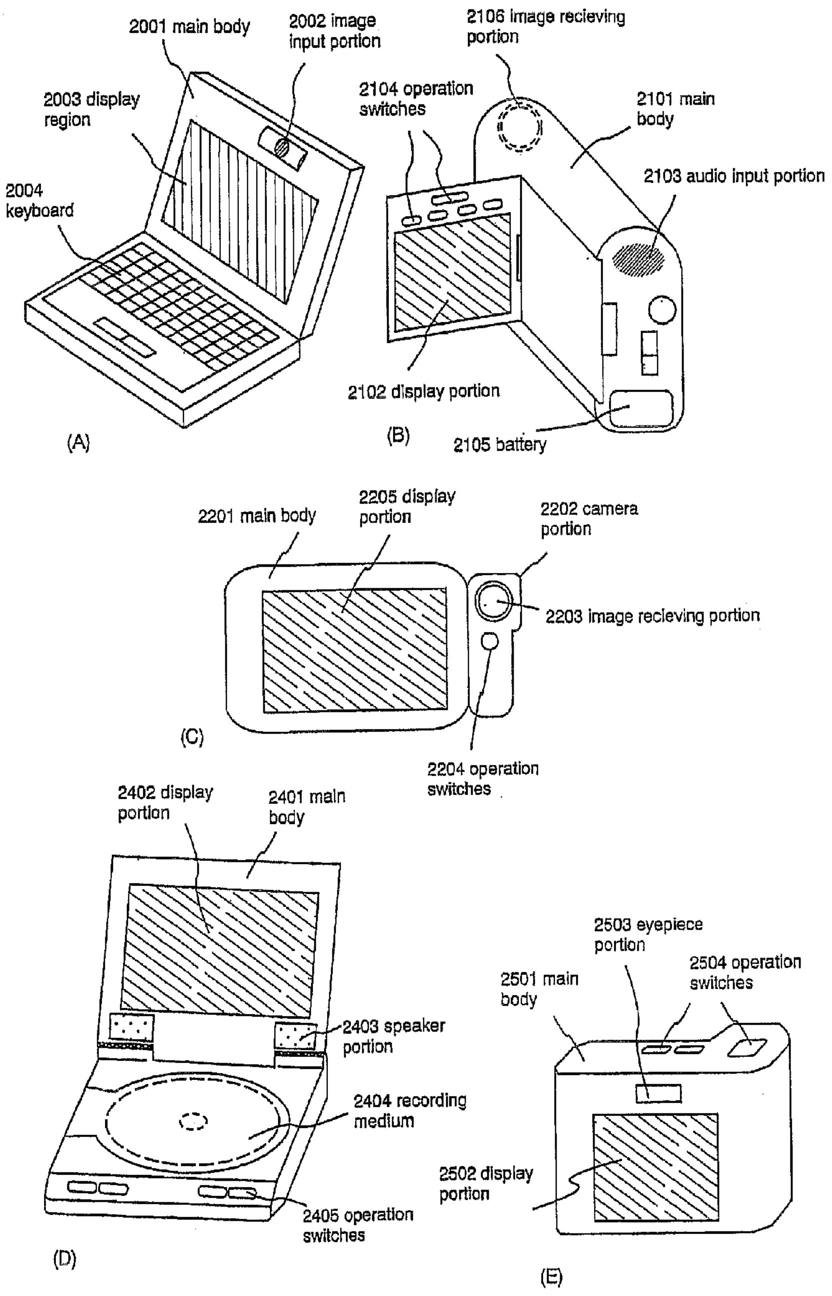


(A) top view

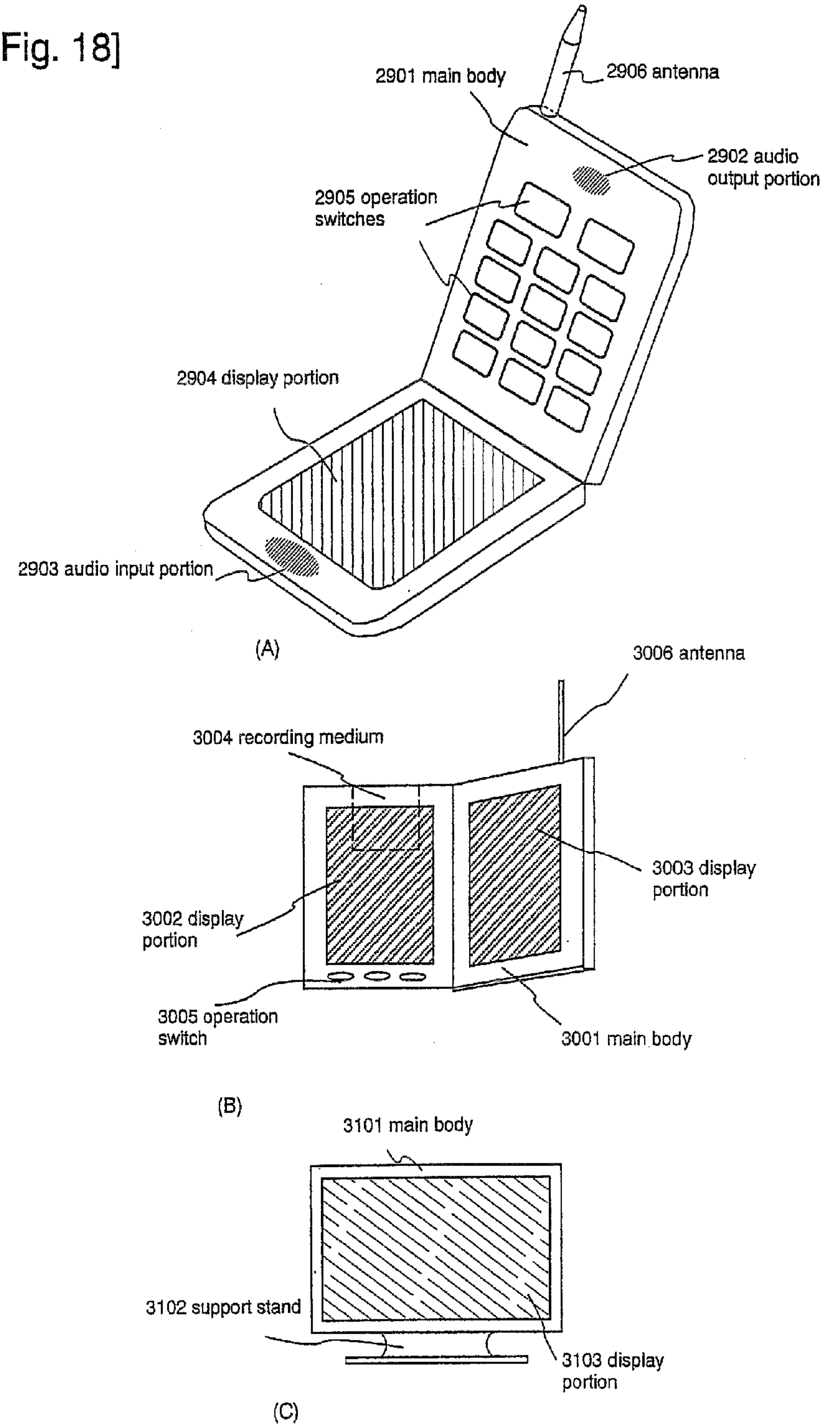


(B) circuit diagram

[Fig. 17]


2001 main body
2002 image input portion
2003 display region
2004 keyboard
(A)
2106 image recieving portion
2104 operation switches
2101 main body
2103 audio input portion
2102 display portion
(B)
2105 battery
2201 main body
2205 display portion
2202 camera portion
2203 image recieving portion
(C)
2204 operation switches
2402 display portion
2401 main body
2403 speaker portion
2404 recording medium
2405 operation switches
(D)
2503 eyepiece portion
2501 main body
2504 operation switches
2502 display portion
(E)

[Fig. 18]


2901 main body
2906 antenna
2902 audio output portion
2905 operation switches
2904 display portion
2903 audio input portion
3006 antenna
3004 recording medium
3003 display portion
3002 display portion
3005 operation switch
3001 main body
3101 main body
3102 support stand
3103 display portion

(A)

(B)

(C)

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an active matrix type liquid crystal display device, and particularly to an active matrix type liquid crystal display device of an IPS (In-Plane Switching) system (=transverse electric field system).

[0003] 2. Description of Related Art

[0004] An active matrix type liquid crystal display device using an active element such as a thin film transistor (TFT) is known. The active matrix type liquid crystal display device can increase pixel density, is small and lightweight, and consumes less power, so that as a substitute for a CRT, a product such as a monitor of a personal computer or a liquid crystal television has been developed. Especially, a technique of forming an active layer of a TFT by a crystalline semiconductor film typified by polycrystalline silicon makes it possible to form a driver circuit as well as a switching TFT for a pixel portion (hereinafter referred to as a pixel TFT) on the same substrate, and is ranked as a technique to contribute to miniaturization and weight lightening of a liquid crystal display device.

[0005] In the liquid crystal display device, a liquid crystal is sealed between a pair of substrates, and liquid crystal molecules are oriented by an electric field which is applied between a pixel electrode (individual electrode) of one of the substrates and an opposite electrode (common electrode) of the other substrate and is approximately vertical to a substrate plane. However, such a driving method of a liquid crystal has a defect that an angle of view is narrow, that is, although a normal display state is obtained when it is viewed in a direction vertical to the substrate plane, a color tone is changed and becomes unclear when it is viewed in an oblique direction.

[0006] As a method of overcoming this defect, there is an IPS system. This system has a feature that both a pixel electrode and a common wiring are formed on one of substrates and an electric field is changed to a transverse direction, and liquid crystal molecules do not rise but their orientation is controlled in the direction almost parallel with a substrate plane. By this operation principle, the angle of view can be widened.

SUMMARY OF THE INVENTION

Problem to be Solved by the Invention

[0007] Usage of a liquid crystal display device has been widened, and also in the IPS system, with enlargement of a screen size, a demand for high fineness, high aperture ratio, and high reliability has increased. At the same time, a demand for improvement of productivity and reduction of cost has also increased.

[0008] In order to improve the productivity and to improve yield, the reduction in the number of steps is considered as an effective means.

[0009] Specifically, it is necessary to reduce the number of photomasks needed to produce the TFT. The photomask is used in a photolithography technique in order to form a photoresist pattern, which becomes an etching process mask, on the substrate.

[0010] By using one photomask, there are applied with steps such as applying resist, pre-baking, exposure, development, and post-baking, and steps of film deposition and etching before and after, and in addition, resist peeling, cleaning, and drying steps are added. Therefore, the entire process becomes complex, which leads to a problem.

[0011] Further, static electricity is generated by causes such as friction during manufacturing steps because the substrate is an insulator. If static electricity is generated, then short circuits develop at an intersection portion of wirings formed on the substrate, and deterioration or breakage of the TFT due to static electricity leads to display faults or deterioration of image quality in electro-optical devices. In particular, static electricity develops during rubbing in the liquid crystal orienting process performed in the manufacturing steps, and this becomes a problem.

[0012] The present invention is for answering these types of problems, and an object of the present invention is to reduce the number of steps for manufacturing a TFT, and to realize a reduction in the production cost and an improvement in a liquid crystal display device of an IPS system.

[0013] Further, an object of the present invention is to provide a structure and a method of manufacturing the structure for resolving the problems of damage to the TFT and deterioration of TFT characteristics due to static electricity.

Means for Solving the Problem

[0014] In order to solve the above problems, the present invention is characterized by employing a channel etch type bottom gate TFT structure, and by performing patterning of a source region, a drain region, and patterning of a source wiring, a pixel electrode by using the same photomask.

[0015] A method of manufacturing of the present invention is simply explained below.

[0016] First, a gate wiring **102** and a common wiring **103***a* (and a common electrode **103***b*) are formed using a first mask (photomask number 1).

[0017] Next, an insulating film (gate insulating film) **104***a*, a first amorphous semiconductor film **105**, a second amorphous semiconductor film **106** containing an impurity element which imparts n-type conductivity, and a first conductive film **107** are laminated in order. (FIG. **2**(A)) Note that a microcrystalline semiconductor film may be used as a substitute for the amorphous semiconductor film, and that a microcrystalline semiconductor film containing an impurity element which imparts n-type conductivity may be used as a substitute for the amorphous semiconductor film containing an impurity element which imparts n-type conductivity. In addition, these films (**104***a*, **105**, **106**, and **107**) can be formed in succession without exposure to the atmosphere in a plurality of chambers, or in the same chamber, using sputtering or plasma CVD. The mixing in of impurities can be prevented by having no exposure to the atmosphere.

[0018] Next, by using a second mask (photomask number 2): the above first conductive film **107** is patterned, forming a wiring (which later becomes a source wiring and a pixel electrode) **114** from the first conductive film; the above second amorphous semiconductor film **106** is patterned, forming a second amorphous semiconductor film **112** containing an impurity element which imparts n-type conductivity; and the above first amorphous semiconductor film **105** is patterned, forming a first amorphous semiconductor film **110**. (FIG. **2**(B))

[0019] Thereafter, a second conductive film **116** is formed on the entire surface (FIG. **2**(D)). Note that as the second conductive film **116**, a transparent conductive film may be used, or a conductive film having reflectivity may be used. This second conductive film is provided for prevention of electro-static damage, protection of a wiring, and electrical connection of a terminal portion.

[0020] Next, by using a third mask (photomask number 3): the above second conductive film **116** is patterned; the above wiring **114** is patterned, forming a source wiring **121** and a pixel electrode **122**; the second amorphous semiconductor film **112** containing an impurity element which imparts n-type conductivity is patterned, forming a source region **119** and a drain region **120** from the second amorphous semiconductor film containing an impurity element which imparts n-type conductivity; and a portion of the above first amorphous semiconductor film **110** is removed, forming a first amorphous semiconductor film **118**. (FIG. **3**(A))

[0021] By using this type of constitution, the number of photomasks used in the photolithography technique can be set to 3 when manufacturing a pixel TFT portion.

[0022] A structure of the present invention disclosed in this specification is:

[0023] a liquid crystal display device including a pair of substrates and a liquid crystal held between the pair of substrates, wherein the liquid crystal display device is characterized in that

[0024] the gate wiring **102** and the common electrode **103***b* is formed on one of the pair of substrates,

[0025] the insulating film **104***b* is formed on the gate wiring **102** and the common electrode **103***b,*

[0026] the amorphous semiconductor film **118** is formed on the insulating film,

[0027] the source region **119** and the drain region **120** are formed on the amorphous semiconductor film,

[0028] the source wiring **121** or the pixel electrode **122** is formed on the source region **119** or the drain region **120**,

[0029] the pixel electrode **122** and the common electrode **103***b* are disposed so that an electric field parallel with a substrate plane of the one substrate is generated, and

[0030] one end face of the drain region **120** or the source region **119** is substantially coincident with an end face of the amorphous semiconductor film **118** and an end face of the pixel electrode **122**.

[0031] Further, another structure of the present invention is:

[0032] a liquid crystal display device including a pair of substrates and a liquid crystal held between the pair of substrates, wherein the liquid crystal display device is characterized in that

[0033] the gate wiring **102** and the common electrode **103***b* are formed on one of the pair of substrates,

[0034] the insulating film **104***b* is formed on the gate wiring **102** and the common electrode **103***b,*

[0035] the amorphous semiconductor film **118** is formed on the insulating film,

[0036] the source region **119** and the drain region **120** are formed on the amorphous semiconductor film **118**,

[0037] the source wiring **121** or the pixel electrode **122** is formed on the source region **119** or the drain region **120**,

[0038] the pixel electrode **122** and the common electrode **103***b* are disposed so that an electric field parallel with a substrate plane of the one substrate is generated, and

[0039] one end face of the drain region **120** or the source region **119** is substantially coincident with an end face of the amorphous semiconductor film **118** and an end face of the pixel electrode **122**, and the other end face is substantially coincident with an end face of the source wiring **122**.

[0040] Further, another structure of the present invention is:

[0041] a liquid crystal display device including a pair of substrates and a liquid crystal held between the pair of substrates, wherein the liquid crystal display device is characterized in that

[0042] the gate wiring **102** and the common electrode **103***b* is formed on one of the pair of substrates,

[0043] the insulating film is formed on the gate wiring **102** and the common electrode **103***b,*

[0044] the amorphous semiconductor film **118** is formed on the insulating film,

[0045] the source region **119** and the drain region **120** are formed on the amorphous semiconductor film,

[0046] the source wiring **121** or the pixel electrode **122** is formed on the source region **119** or the drain region **120**,

[0047] the pixel electrode **122** and the common electrode **103***b* are disposed so that an electric field parallel with a substrate plane of the one substrate is generated, and

[0048] the amorphous semiconductor film **118** and an amorphous semiconductor film containing an impurity element which imparts an n-type conductivity are laminated under the source wiring.

[0049] Further, in the above-mentioned respective structures, the liquid crystal display device is characterized in that the source region and the drain region is made from an amorphous semiconductor film containing an impurity element which imparts n-type conductivity.

[0050] Further, in the above-mentioned respective structures, the liquid crystal display device is characterized in that the gate wiring **102** is formed from a film of an element selected from the group consisting of Al, Cu, Ti, Mo, W, Ta, Nd, and Cr, from an alloy film of said elements, or from a lamination film of said elements.

[0051] Still further, in the above-mentioned respective structures, the liquid crystal display device is characterized in that the source region **119** and the drain region **120** are formed by using the same mask as that of the pixel electrode **122**. Moreover, it is characterized in that the source region **119** and the drain region **120** are formed by using the same mask as that of the source wiring **121**.

[0052] Yet further, in the above-mentioned respective structures, the liquid crystal display device is characterized in that in the amorphous semiconductor film, its thickness in a region where it is in contact with the source region and the drain region is thicker than its thickness in a region between the region where it is in contact with the source region and the region where it is in contact with the drain region.

[0053] Yet further, in the above-mentioned respective structures, the liquid crystal display device is characterized in the pixel electrode is covered with a transparent conductive film. Besides, it is characterized in that the source wiring and a terminal on an extension of the source wiring are covered with a transparent conductive film.

[0054] Further, a structure of the invention to attain the above-mentioned respective structures is a method of manufacturing a liquid crystal display device, characterized in that the method comprises:

[0055] a first step of forming the gate wiring **102** and the common electrode **103***b* (and the common wiring **103***a*) on an insulating surface by using a first mask;

[0056] a second step of forming the insulating film **104***a* covering said gate wiring **102** and said common electrode **103***b;*

[0057] a third step of forming the first amorphous semiconductor film **105** on said insulating film **104***a;*

[0058] a fourth step of forming the second amorphous semiconductor film **106**, containing an impurity element which imparts n-type conductivity, on said first amorphous semiconductor film **105**;

[0059] a fifth step of forming the first conductive film **107** on said second amorphous semiconductor film **106**;

[0060] a sixth step of patterning said first amorphous semiconductor film **105** by using a second mask; of patterning said second amorphous semiconductor film **106** by using said second mask; of patterning said first conductive film **107** by using said second mask; and of forming the wiring **114** from said first conductive film; and

[0061] an eighth step of patterning said wiring **114** by using said third mask, forming the source wiring **121** and the pixel electrode **122**; of patterning said second amorphous semiconductor film **112** by using said third mask, forming the source region **119** and the drain region **120** made from said second amorphous semiconductor film; and of performing removal of a portion of said first amorphous semiconductor film by using said third mask.

[0062] Still further, another structure of the present invention to attain the above-mentioned respective structures is a method of manufacturing a liquid crystal display device characterized in that the method comprises:

[0063] a first step of forming the gate wiring **102** and the common electrode **103***b* (and the common wiring **103***a*) on the insulating surface by using a first mask;

[0064] a second step of forming the insulating film **104***a* covering said gate wiring **102** and said common electrode **103***b;*

[0065] a third step of forming the first amorphous semiconductor film **105** on said insulating film **104***a;*

[0066] a fourth step of forming the second amorphous semiconductor film **106**, containing an impurity element which imparts n-type conductivity, on said first amorphous semiconductor film;

[0067] a fifth step of forming the first conductive film **107** on said second amorphous semiconductor film **106**;

[0068] a sixth step of patterning said first amorphous semiconductor film **105** by using a second mask; of patterning said second amorphous semiconductor film **106** by using said second mask; of patterning said first conductive film **107** by using said second mask; and of forming the wiring **114** from said first conductive film;

[0069] a seventh step of forming the second conductive film **116** contacting and overlapping said wiring **114**; and

[0070] an eighth step of patterning said second conductive film **116** by using a third mask, forming an electrode made from said second conductive film; of patterning said wiring **114** by using said third mask, forming the source wiring **121** and the pixel electrode **122**; of patterning said second amorphous semiconductor film **116** by using said third mask, forming the source region **119** and the drain region **120** made from said second amorphous semiconductor film; and of performing removal of a portion of said first amorphous semiconductor film by using said third mask.

[0071] In the above structure, it is characterized in that the second conductive film **116** is a transparent conductive film.

[0072] Further, in the above-mentioned respective structures, it is characterized in that the pixel electrode and the common electrode are disposed so that an electric field parallel with the insulating surface is generated.

Effect of the Invention

[0073] With the present invention, an electro-optical device of an IPS system prepared with a pixel TFT portion, having a reverse stagger type n-channel TFT, and a storage capacitor can be realized through three photolithography processes using three photomasks.

[0074] Further, when forming a protecting film, an electro-optical device of an IPS system prepared with a pixel TFT portion, having a reverse stagger type n-channel TFT protected by an inorganic insulating film, and a storage capacitor can be realized through four photolithography processes using four photomasks.

BRIEF DESCRIPTION OF THE DRAWINGS

[0075] FIG. **1** is a diagram showing a top view of the present invention.

[0076] FIGS. **2**A-D are cross-sectional views showing a process of manufacturing an active matrix substrate.

[0077] FIGS. **3**A-C are cross-sectional views showing the process of manufacturing the active matrix substrate.

[0078] FIG. **4** is a top view showing the process of manufacturing the active matrix substrate.

[0079] FIG. **5** is a top view showing the process of manufacturing the active matrix substrate.

[0080] FIG. **6** is a cross-sectional view of a liquid crystal display device.

[0081] FIG. **7** is a top view for explaining the arrangement of a pixel portion and an input terminal portion of a liquid crystal display device.

[0082] FIG. **8** is a cross-sectional view showing an implemented structure of a liquid crystal display device.

[0083] FIGS. **9**A-B are top views and a cross-sectional views of an input terminal portion.

[0084] FIG. **10** is a top view of a manufacturing device.

[0085] FIG. **11** is a top view of a manufacturing device.

[0086] FIG. **12** is a diagram showing an implementation of a liquid crystal display device.

[0087] FIGS. **13**A-B are cross-sectional views showing an implementation structure of a liquid crystal display device.

[0088] FIG. **14** is a cross-sectional view showing an implemented structure of a liquid crystal display device.

[0089] FIG. **15** is a diagram showing a top view of the invention

[0090] FIGS. **16**A-B are a top view and a circuit diagram of a protecting circuit.

[0091] FIGS. **17**A-E are diagrams showing examples of electronic equipment.

[0092] FIGS. **18**A-C are diagrams showing examples of electronic equipment.

DETAILED DESCRIPTION OF THE INVENTION

[0093] Embodiment modes of the present invention will be described below.

[0094] FIG. **1** is an example of a plan view showing a pixel structure of an IPS system in the present invention, and here, for simplification, one pixel structure in a plurality of pixels arranged in matrix form is shown. FIG. **2** and FIG. **3** are views showing manufacturing steps.

[0095] As shown in FIG. **1**, this active matrix substrate includes a plurality of gate wirings arranged in parallel with each other and a plurality of source wirings perpendicular to the respective gate wirings. Besides, it includes a plurality of common wirings in the same layer as the gate wirings.

[0096] Besides, a pixel electrode **122** is disposed in a region surrounded by the gate wirings **102** and the source wirings **121**. Besides, two common electrodes **103***b* parallel to each other are disposed at both sides of this pixel electrode **122**. A liquid crystal is driven by using an electric field in a transverse direction formed between this pixel electrode **122** and the common electrodes **103***b*. Besides, in order to decrease a light leakage due to a gap between the common electrode and the source wiring, they may be disposed to partially overlap with each other.

[0097] Further, a TFT is formed in the vicinity of an intersection portion of the gate wirings **102** and the source wirings **121** as a switching element. This TFT is a reverse stagger type TFT (channel etch type) having a channel forming region formed from a semiconductor film possessing an amorphous structure (hereafter referred to as a first amorphous semiconductor film).

[0098] Further, the TFT is formed by a lamination of, in order on an insulating substrate, a gate electrode (formed integrally to the gate wiring **102**), a gate insulating film, a first amorphous semiconductor film, a source region or a drain region made from a second amorphous semiconductor film, containing a impurity element which imparts n-type conductivity, a source electrode (formed as integrated with the source wirings **121**) and a pixel electrode **122**.

[0099] Further, the film thickness of a region between a region contacting the source region and a region contacting the drain region is thinner compared to other regions of the first amorphous semiconductor film. The reason that the film thickness becomes thin is that when forming the source region and the drain region by partitioning the second amorphous semiconductor film, which contains the impurity element for imparting n-type conductivity, by etching, a portion of the first amorphous semiconductor film is also removed. Further, an end surface of the pixel electrode, and an end surface of the drain region coincide by this etching process. This type of reverse stagger type TFT is referred to as a channel etched type TFT. Furthermore, the end surface of the source region, and the end surface of the source wiring coincide.

[0100] Further, under the source wirings (including the source electrode) and the pixel electrode **122**, a gate insulating film, a first amorphous semiconductor film, and a second amorphous semiconductor film containing an impurity element which imparts n-type conductivity are laminated in order on the insulating substrate.

[0101] Besides, a storage capacitance is formed of the common wiring **103***a*, the pixel electrode **122** (or the second amorphous semiconductor film containing the impurity element which imparts the n-type conductivity, the first amorphous semiconductor film), and an insulating film **104***b* existing therebetween.

[0102] A second conductive film **124** made of a transparent electrode and being in contact with the source wiring, and a second conductive film **123** made of a transparent electrode and being in contact with the pixel electrode serve to prevent static electricity generated in a subsequent manufacturing step, especially in a rubbing processing. Besides, this second conductive film **124** facilitates electrical connection when connection with an FPC is made at a terminal portion.

[0103] Besides, although the IPS system is normally a transmission type, it is also possible to make a reflection type display device if a metal substrate or an insulating substrate on which a dielectric multi-layer film is formed is used as an opposite substrate and a substrate interval is made half of that of the transmission type.

[0104] An explanation of the present invention having the above structure is performed in more detail by the embodiments shown below.

EMBODIMENTS

Embodiment 1

[0105] An embodiment of the invention is explained using FIGS. **1** to **7**. This Embodiment shows a method of manufacturing a liquid crystal display device, and a detailed explanation of a method of forming a TFT of a pixel portion on a substrate by a reverse stagger type TFT (channel etching type), and manufacturing a storage capacitor connected to the TFT, is made in accordance with the processes used. Further, a manufacturing process for a terminal section, formed in an edge portion of the substrate, and for electrically connecting to wirings of circuits formed on other substrates, is shown at the same time in the same figures.

[0106] In FIG. **2**(A), a glass substrate, comprising such as barium borosilicate glass or aluminum borosilicate glass, typically Corning Corp. #7059 glass or #1737 glass, can be used as a substrate **100** having translucency. In addition, a translucent substrate such as a quartz substrate or a plastic substrate can also be used.

[0107] Next, after forming a conductive layer on the entire surface of the substrate, a first photolithography process is performed, a resist mask is formed, unnecessary portions are removed by etching, and wirings and electrodes (the gate wiring **102** including a gate electrode, a common wiring **103***a* including a common electrode **103***b* and a terminal **101**) are formed. Etching is performed at this time to form a tapered portion in at least an edge portion of the gate electrode **102**. A top view of this stage is shown in FIG. **4**.

[0108] It is preferable to form the gate wiring **102** including the gate electrode, the common wiring **103***a*, and the terminal **101** of the terminal portion from a low resistivity conductive material such as aluminum (Al), copper (Cu) or the like, but simple Al has problems such as inferior heat resistance and easily corrodes, and therefore it is combined with a heat resistant conductive material. Further, AgPdCu alloy may be used as the low resistivity conductive material. One element selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), Neodymium (Nd), or an alloy comprising the above elements, or an alloy film of a combination of the above element, or a nitrated compound comprising the above element is formed as the heat resistant conductive material. For example, a lamination of Ti and Cu or a lamination of TaN and Cu can be given. Furthermore, forming in combination with a heat resistant conductive material such as Ti, Si, Cr, or Nd, etc., it is preferable because of improved levelness. Further, only such heat resistant conductive film may also be formed, for example, in combination with Mo and W.

[0109] In realizing the liquid crystal display device, it is preferable to form the gate electrode and the gate wiring by a combination of a heat resistant conductive material and a low resistivity conductive material. An appropriate combination in this case is explained.

[0110] Provided that the screen size is on the order of, or less than 5 inch diagonal type, a two layer structure of a lamination of a conductive layer (A) made from a nitride compound of a heat resistant conductive material, and a conductive layer (B) made from a heat resistant conductive material is used. The conductive layer (B) may be formed from an element selected from the group consisting of Al, Cu, Ta, Ti, W, Nd, and Cr, or from an alloy of the above elements, or from an alloy film of a combination of the above elements, and the conductive layer (A) is formed from a film such as a tantalum nitride (TaN) film, a tungsten nitride (WN) film, or a titanium nitride (TiN) film. For example, it is preferable to use a double layer structure of a lamination of Cr as the conductive layer (A) and Al containing Nd as the conductive layer (B). The conductive layer (A) is given a thickness of 10 to 100 nm (preferably between 20 and 50 nm), and the conductive layer (B) is made with a thickness of 200 to 400 nm (preferably between 250 and 350 nm).

[0111] On the other hand, in order to be applied to a large screen, it is preferable to use a three layer structure of a lamination of a conductive layer (A) made from a heat resistant conductive material, a conductive layer (B) made from a low resistivity conductive material, and a conductive layer (C) made from a heat resistant conductive material. The conductive layer (B) made from the low resistivity conductive material is formed from a material comprising aluminum (Al), and in addition to pure Al, Al containing between 0.01 and 5 atomic % of an element such as scandium (Sc), Ti, Nd, or silicon (Si), etc. is used. The conductive layer (C) is effective in preventing generation of hillocks in the Al of the conductive layer (B). The conductive layer (A) is given a thickness of 10 to 100 nm (preferably between 20 and 50 nm), the conductive layer (B) is made from 200 to 400 nm thick (preferable between 250 and 350 nm), and the conductive layer (C) is from 10 to 100 nm thick (preferably between 20 and 50 nm). In Embodiment 1, the conductive layer (A) is formed from a Ti film with a thickness of 50 nm, made by sputtering with a Ti target, the conductive layer (B) is formed from an Al film with a thickness of 200 nm, made by sputtering with an Al target, and the conductive layer (C) is formed from a 50 nm thick Ti film, made by sputtering with a Ti target.

[0112] An insulating film **104***a* is formed next on the entire surface. The insulating film **104***a* is formed using sputtering, and has a film thickness of 50 to 200 nm.

[0113] For example, a silicon nitride film is used as the insulating film **104***a*, and formed to a thickness of 150 nm. Of course, the gate insulating film is not limited to this type of silicon nitride film, and another insulating film such as a silicon oxide film, a silicon oxynitride film, or a tantalum oxide film may also be used, and the gate insulating film may be formed from a single layer or a lamination structure made from these materials. For example, a lamination structure having a silicon nitride film as a lower layer and a silicon oxide film as an upper layer may be used.

[0114] Next, a first amorphous semiconductor film **105** is formed with a thickness of 50 to 200 nm (preferably between 100 and 150 nm) on the insulating film **104***a* over the entire surface by using a known method such as plasma CVD or sputtering (not shown in the figure). Typically, an amorphous silicon (a-Si) film is formed with a thickness of 100 nm by sputtering using a silicon target. In addition, it is also possible to apply a microcrystalline semiconductor film, or a compound semiconductor film having an amorphous structure, such as an amorphous silicon germanium film ($Si_xGe_{(1-x)}$, ($0<x<1$)) and amorphous silicon carbide (Si_xC_y), etc., for the first amorphous semiconductor film.

[0115] A second amorphous semiconductor film containing an impurity element imparting one conductivity type (n-type or p-type) is formed next with a thickness of 20 to 80 nm. The second amorphous semiconductor film containing an impurity element imparting one conductivity type (n-type or p-type) is formed on the entire surface by a known method such as plasma CVD or sputtering. In this Embodiment the second amorphous semiconductor film **106** containing n-type impurity element is deposited by using a silicon target added with phosphorus (P). Alternatively, the second amorphous semiconductor film containing an impurity element imparting n-type may also be formed from a hydrogenated microcrystalline silicon film (pc-Si:H).

[0116] Next, a first conductive film **107** which comprises a metallic material is formed by sputtering or vacuum evaporation. There are no particular limitation on the material of the first conductive film **107** provided that the material is a metallic material which can form ohmic contact with the second amorphous semiconductor film **106**, and an element selected from the group consisting of Al, Cr, Ta, and Ti, or an alloy comprising the above elements, and an alloy film of a combination of the above elements or the like can be given. Sputtering is used in this Embodiment to form a Ti film having 50 to 150 nm thickness, an aluminum (Al) having 300 to 400 nm thickness piled on the Ti film and further on the Al film a Ti film having 100 to 150 nm are formed as the first conductive film **107**. (FIG. **2**(A))

[0117] The insulating film **104***a*, the first amorphous semiconductor film **105**, the second amorphous semiconductor film **106** containing an impurity element which imparts n-type, and the first conductive film **107** are all manufactured by a known method, and can be manufactured by plasma CVD or sputtering. The films (**104***a*, **105**, **106** and **107**) are formed in succession by sputtering, and suitably changing the target or the sputtering gas in Embodiment 1. The same reaction chamber, or a plurality of reaction chambers, in the sputtering apparatus is used at this time, and it is preferable to laminate these films in succession without exposure to the atmosphere. By thus not exposing the films to the atmosphere, the mixing in of impurities can be prevented.

[0118] Next, a second photolithography process is performed, a resist masks **108** and **109** are formed, and by removing unnecessary portions by etching, a wiring (which forms a source wiring and a pixel electrode in the later step) is formed. Wet etching or dry etching is used as the etching process at this time. The first amorphous semiconductor film **105**, the second amorphous semiconductor film **106** containing an impurity element imparting n-type and the conductive metal film **107** are etched, and a first amorphous semiconductor film **110**, a second amorphous semiconductor film containing an impurity element imparting n-type **112** and a conductive metal film **114** are formed in the pixel TFT portion. Accordingly the edge surface of the films approximately coincide. Further in the capacitor portion a first amorphous semiconductor film **111**, a second amorphous semiconductor film **113** containing an impurity element imparting n-type and a conductive metal film **115** are formed. Similarly, the edge surface of these films coincide. The first conductive film **107** formed by laminating a Ti film, an Al film and a Ti film in order is etched by dry etching using reaction gas of mixed gas of $SiCl_4$, Cl_2 and BCl_3 and the first amorphous semiconductor film **105** and the second amorphous semiconductor film **106** containing an impurity element which imparts n-type are selectively removed by changing the reaction gas to the mixed gas of CF_4 and O_2. (FIG. **2**(B)) In the terminal portion a terminal **101** and an insulating film **104**_a_ remained.

[0119] Next after removing resist masks **108** and **109**, a resist mask is formed by a shadow mask, an insulating film **104**_b_ is formed by selectively removing the insulating film **104**_a_ which covers the pad portion of the terminal portion and the resist mask is removed. (FIG. **2**(C)) Further, the resist mask may be formed by screen printing in place of the shadow mask and it may be used as the etching mask.

[0120] Next, a second conductive film **116** comprising a transparent conductive film is deposited over the entire surface. (FIG. **2**(D)) A top view in this state is shown in FIG. **5**. Note however, for simplification, the second conductive film **116** deposited over the entire surface is not shown in FIG. **5**.

[0121] The second conductive film **116** is formed from a material such as indium oxide (In_2O_3) or indium tin oxide alloy (In_2O_3—SnO_2, abbreviated as ITO) using a method such as sputtering or vacuum evaporation. The etching process for this type of material is performed using a solution of hydrochloric acid type. However, a residue is easily generated, particularly by ITO etching, and therefore an indium oxide zinc oxide alloy (In_2O_3—ZnO) may be used in order to improve the etching workability. The indium oxide zinc oxide alloy has superior surface smoothing characteristics, and has superior thermal stability compared to ITO, and therefore even if the wiring **111** contacting the second conductive film **116** is made from an Al film, a corrosion reaction can be prevented. Similarly, zinc oxide (ZnO) is also a suitable material, and in addition, in order to increase the transmittivity of visible light and increase the conductivity, a material such as zinc oxide in which gallium (Ga) is added (ZnO:Ga) can be used.

[0122] Resist masks **117**_a_ to **117**_c_ are formed next by a third photolithography process. Unnecessary portions are then removed by etching, forming a first amorphous semiconductor film **118**, a source region **119**, a drain region **120**, the source wiring **121** and the pixel electrode **122**, and the second conducive films **123** and **124**. (FIG. **3**(A))

[0123] The third photolithography process patterns the second conductive film **116**, and at the same time removes a part of the wiring **114**, the second amorphous semiconductor film containing an impurity element which imparts n-type **112** and the first amorphous semiconductor film **110** by etching, forming an opening. In this Embodiment, the second conductive film **116** comprising ITO is selectively removed first by wet etching using a mixed solution of nitric acid and hydrochloric acid, or a ferric chloride solution, and after removing the wiring **114** by wet etching, a part of the second amorphous semiconductor film **112** containing an impurity element which imparts n-type and the amorphous semiconductor film **110** are etched by dry etching. Note that wet etching and dry etching are used in this Embodiment, but the operator may perform only dry etching by suitably selecting the reaction gas, and the operator may perform only wet etching by suitably selecting the reaction solution.

[0124] Further, the lower portion of the opening reaches the first amorphous semiconductor film, and the amorphous semiconductor film **118** is formed having a concave portion. The wiring **114** is separated into the source wiring **121** and the pixel electrode **122** by the opening, and the second amorphous semiconductor film containing an impurity element which imparts n-type **112** is separated into the source region **119** and the drain region **120**. Furthermore, the second conductive film **124** contacting the source wiring covers the source wiring, and during subsequent manufacturing processes, especially during a rubbing process, fulfills a role of preventing static electricity from developing. Further, as shown in FIG. **9**, this second conductive film **124** plays an important role in forming connection with FPC in the terminal portion. Also, this second conductive film **124** plays a role of protecting the source wiring.

[0125] Further, a storage capacitor is formed, in this third photolithography process, between the common wiring **103**_a_ and the pixel electrode **122** with the insulating film **104**_b_ in the capacitor portion as a dielectric.

[0126] In this third photolithography process, the second conductive film comprising a transparent conductive film formed in the terminal portion is remained by covering with the resist mask **117**_c_.

[0127] Resist masks **113**_a_ to **113**_c_ are next removed. The cross sectional view of this state is shown in FIG. **3**(B).

[0128] Furthermore, FIG. **9**(A) shows top views of a gate wiring terminal portion **501** and a source wiring terminal portion **502** in this state. Note that the same symbols are used for area corresponding to those of FIG. **1** to FIG. **3**. Further, FIG. **9**(B) corresponds to a cross-sectional view taken along the lines E-E' and F-F' in FIG. **9**(A). Reference numeral **503** in FIG. **9**(A) comprising a transparent conductive film denotes a connecting electrode which functions as an input terminal and it enables easy electrical connection. In addition, in FIG. **9**(B) reference numeral **504** denotes an insulating film (extended from **104**_b_), reference numeral **505** denotes a first amorphous semiconductor film (extended from **118**), and reference numeral **506** denotes a second amorphous semiconductor film containing an impurity element which imparts n-type (extended from **119**).

[0129] Thus by thus using three photomasks and performing three photolithography processes, the pixel TFT portion having the reverse stagger type n-channel type TFT **201** and the storage capacitor **202** can be completed. By placing these in a matrix state corresponding to each pixel and thus composing the pixel portion, one substrate can be made in order to manufacture an active matrix type electro-optical device. For convenience, this type of substrate is referred to as an active matrix substrate throughout this specification.

[0130] An alignment film **125** is selectively formed next in only the pixel portion of the active matrix substrate. Screen printing may be used as a method of selectively forming the alignment film **125**, and a method of removal in which a resist mask is formed using a shadow mask after application of the alignment film may also be used. Normally, a polyimide resin is often used in the alignment film of the liquid crystal display element. In this Embodiment AL 3046 (manufactured by JSR Corporation) is used as the alignment film.

[0131] Next, a rubbing process is then performed on the alignment film **125**, orienting the liquid crystal elements so as to possess a certain fixed pre-tilt angle. In case of the IPS method, the preferable pre-tilt angle is approximately 0.5° to 3°, in order to prevent coloring and to obtain good viewing angle, and in this Embodiment it is set at 1.5°.

[0132] After the active matrix substrate and an opposing substrate **127** on which an alignment film **126** is formed are next joined together by a sealant while maintaining a gap between the substrates using spacers, a liquid crystal material **128** is injected into the space between the active matrix substrate and the opposing substrate. Sphere shaped spacers or columnar spacers can be used as the spacers. The number of mask is reduced by one when the columnar spacers are used, and the space between the substrates can be made more uniform and further the process for spraying can be omitted. Note that though not shown in the figure, there is a region on the opposing substrate, which does not substantially function as the display region is covered with a black mask here. A known n-type liquid crystal or a p-type liquid crystal used in the IPS method may be applied to the liquid crystal material **128**.

[0133] In this Embodiment a p-type liquid crystal material ZLI-4792 (manufactured by Merck) in which a pair of substrates are held 3 to 5 μm distance is preferable, is used in this Embodiment. In case of using ZLI-2806 (manufactured by Merck) is used, a pair of substrates are held a distance of 6 to 8 μm, and the transmitting light and the response speed may be optimized. The angle formed between the pixel electrode and the rubbing direction is preferably set 0.5° to 40° in absolute value since a p-type liquid crystal is used, and it is set at 15° in this Embodiment. On the other hand, in case of using n-type liquid crystal, the angle formed between the pixel electrode and the rubbing direction with respect to the axis intersecting perpendicular to the pixel electrode is set at between 0.5° to 40° in absolute value.

[0134] After injecting liquid crystal material next, the opening for injection is sealed by a resin material.

[0135] Next, a flexible printed circuit (FPC) is connected to the input terminal **101** of the terminal portion. The FPC is formed by a copper wiring **131** on an organic resin film **132** such as polyimide, and is connected to the transparent conductive film which covers the input terminal by an anisotropic conductive adhesive. The anisotropic conductive adhesive comprises an adhesive **129** and particles **130**, with a diameter of several tens to several hundreds of μm and having a conductive surface plated by a material such as gold, which are mixed therein. The particles **130** form an electrical connection in this portion by connecting the transparent conductive film on the input terminal **101** and the copper wiring **131**. In addition, in order to increase the mechanical strength of this region, a resin layer **133** is formed. (FIG. **3**(C))

[0136] Note that FIG. **1** is a top view of one pixel and the cross sections taken along A-A' line and B-B' line corresponds respectively to FIG. **3**(C). For simplification the opposing substrate on which the alignment film is disposed and the liquid crystal are not shown in the figure.

[0137] FIG. **6** is a cross sectional view taken along the chain line X-X' in FIG. **1**. The common wiring **103***a* is divided into branches and the portion divided into branches is referred to as common electrode **103***b* and the portion parallel to the gate wiring is referred to as common wiring **103***a* through the Specification, for convenience. The pixel electrode **122** is disposed between two common electrodes **103***b*. Further, the pixel electrode **122** and the common electrode **103***b* are formed in different layers. An electric field is applied by them, between the pixel electrode **122** and the common electrode **103***b* on one substrate, and the direction is set to be approximately parallel to the substrate interface.

[0138] FIG. **7** is a diagram explaining the arrangement of the pixel section and the terminal section of an active matrix substrate. A pixel section **211** is disposed on the substrate **210**, a gate wiring **208** and a source wiring **207** are formed to intersect in the pixel section and an n-channel TFT **201** is disposed connected to these is disposed corresponding to each pixel. A pixel electrode **119** and a storage capacitor **202** are connected to the drain side of the n-channel TFT **201** and the other terminal of the storage capacitor **202** is connected to the common wiring **209**. The structures of the n-channel TFT **201** and the storage capacitor **202** are the same as the n-channel TFT **201** and the storage capacitor **202** shown in FIG. 3(B).

[0139] An input terminal section **205** which inputs scanning signal is formed in one edge portion of the substrate and is connected to the gate wiring **208** by the connecting wiring **206**. Further, an input terminal portion **203** which inputs image signal is formed in another edge portion and it is connected to the source wiring **207** by the connecting wiring **204**. Gate wiring **208**, source wiring **207** and common wiring **209** are disposed in plural numbers corresponding to the pixel density. It is also appropriate to dispose an input terminal **212** which inputs image signals and the connecting wiring **213**, and connect to the source wiring alternately with the input terminal portion **203**. The input terminal portions **203**, **205** and **212** may be disposed in arbitrary number respectively, and it may be properly determined by the operator.

Embodiment 2

[0140] FIG. **8** is an example of a method of mounting a liquid crystal display device. The liquid crystal display device has an input terminal portion **302** formed in an edge portion of a substrate **301** on which TFTs are formed, and as shown by embodiment 1, this is formed by a terminal **303** formed from the same material as a gate wiring. An opposing substrate **304** is joined to the substrate **301** by a sealant **305** encapsulating spacers **306**, and in addition, polarizing plates **307** and **308** and a color filter (not shown) are disposed. Note that the arrangement of one of the polarizing plate may be adjusted to the longer axis of the liquid crystal molecule and the arrangement of the other polarizing plate may be adjusted to the shorter axis of the liquid crystal molecule. This is then fixed to a casing **321** by spacers **322**.

[0141] Note that the TFT obtained in Embodiment 1 having an active layer formed by an amorphous silicon film has a low electric field effect mobility, and only approximately 1 cm^2/Vsec is obtained. Therefore, a driver circuit for performing image display is formed by an IC chip, and mounted by a TAB (tape automated bonding) method or by a COG (chip on glass) method. In this Embodiment, an example is shown of forming the driver circuit in an IC chip **313**, and mounting by using the TAB method. A flexible printed circuit (FPC) is used, and the FPC is formed by a copper wiring **310** on an organic resin film **309**, such as polyimide, and is connected to the input terminal **302** by an anisotropic conductive adhesive. The input terminal is a transparent conductive film formed on and contacting the wiring **303**. The anisotropic conductive adhesive is structured by an adhesive **311** and particles **312**, with a diameter of several tens to several hundreds of μm and having a conductive surface plated by a material such as gold, which are mixed therein. The particles **312** form an electrical connection in this portion by connecting the input terminal **302** and the copper wiring **310**. In addition, in order to increase the mechanical strength of this region, a resin layer **318** is formed.

[0142] The IC chip **313** is connected to the copper wiring **310** by a bump **314**, and is sealed by a resin material **315**. The copper wiring **310** is then connected to a printed substrate **317** on which other circuits such as a signal processing circuit, an amplifying circuit, and a power supply circuit are formed, through a connecting terminal **316**. A light source **319** and a light conductor **320** are formed on the opposing substrate **304** and used as a back light in the transmission type liquid crystal display device.

Embodiment 3

[0143] In this Embodiment, an example of forming a protecting film is shown in FIG. **14**. Note that this Embodiment is identical to Embodiment 1 through the state of FIG. **3**(B), and therefore only points of difference are explained. Further, the same symbols are used for locations corresponding to those in FIG. **3**(B).

[0144] After first forming through the state of FIG. **3**(B) in accordance with Embodiment 1, a thin inorganic insulating film is formed on the entire surface. An inorganic insulating film formed by using plasma CVD or sputtering such as a silicon oxide film, a silicon nitride film, a silicon oxynitride film, or a tantalum oxide film is used as the thin inorganic insulating film, and a single layer or a lamination structure made from these materials may be formed.

[0145] A forth photolithography process is performed next, forming a resist mask, and unnecessary portions are removed by etching, forming an insulating film **402** in the pixel TFT portion, and an inorganic insulating film **401** in the terminal portion. These inorganic insulating films **401** and **402** function as passivation films. Further, the thin inorganic insulating film **401** is removed in the terminal portion by the fourth photolithography process, exposing the second conductive film comprising a transparent conductive film formed on the terminal **101** of the terminal portion.

[0146] The reverse stagger type n-channel type TFT and the storage capacitor, protected by the inorganic insulating film, can thus be completed in this Embodiment by performing the photolithography process using four photomasks four times in total. By thus structuring the pixel portion by arranging these into a matrix state corresponding to each pixel, one substrate for manufacturing the active matrix electro-optical device can be made.

[0147] Note that it is possible to freely combine the present Embodiment with constitutions of Embodiment 1 or Embodiment 2.

Embodiment 4

[0148] In Embodiment 1 an example centering on laminating an insulating film, a first amorphous semiconductor film, a second amorphous semiconductor film containing an impurity element which imparts n-type conductivity, and a first conductive film by sputtering, but this Embodiment shows an example of using plasma CVD to form the films.

[0149] The insulating film, the first amorphous semiconductor film, and the second amorphous semiconductor film containing an impurity element which imparts n-type conductivity are formed by plasma CVD in this Embodiment.

[0150] In this Embodiment, a silicon oxynitride film is used as the insulating film, and formed with a thickness of 150 nm by plasma CVD. Deposition may be performed at this point in a plasma CVD apparatus with a power supply frequency of 13 to 70 MHz, preferably between 27 and 60 MHz. By using a power supply frequency of 27 to 60 MHz, a dense insulating film can be formed, and the voltage resistance can be increased as a gate insulating film. Further, a silicon oxynitride film manufactured by adding N_2O to SiH_4 and NH_3 has a reduced fixed electric charge density in the film, and therefore is a material which is preferable for this use. Of course, the gate insulating film is not limited to this type of silicon oxynitride film, and a single layer or a lamination structure using other insulating films such as s silicon oxide film, a silicon nitride film, or a tantalum oxide film may be formed. Further, a lamination structure of a silicon nitride film in a lower layer, and a silicon oxide film in an upper layer may be used.

[0151] For example, when using a silicon oxide film, it can be formed by plasma CVD using a mixture of tetraethyl orthosilicate (TEOS) and O_2, with the reaction pressure set to 40 Pa, a substrate temperature of 250 to 350° C., and discharge at a high frequency (13.56 MHz) power density of 0.5 to 0.8 W/cm^2. Good characteristics as the gate insulating film can be obtained for the silicon oxide film thus formed by a subsequent thermal anneal at 300 to 400° C.

[0152] Typically, a hydrogenated amorphous silicon (a-Si:H) film is formed with a thickness of 100 nm by plasma CVD as the first amorphous semiconductor film. At this point, the deposition may be performed with a power supply frequency of 13 to 70 MHz, preferably between 27 and 60 MHz, in the plasma CVD apparatus. By using a power frequency of 27 to 60 MHz, it becomes possible to increase the film deposition speed, and the deposited film is preferable because it becomes an a-Si film having a low defect density. In addition, it is also possible to apply a microcrystalline semiconductor film and a compound semiconductor film having an amorphous structure, such as an amorphous silicon germanium film, as the first amorphous semiconductor film.

[0153] Further, if 100 to 100 kHz pulse modulation discharge is performed in the plasma CVD film deposition of the insulating film and the first amorphous semiconductor film, then particle generation due to the plasma CVD gas phase reaction can be prevented, and pinhole generation in the film deposition can also be prevented, and therefore is preferable.

[0154] Further, in this Embodiment a second amorphous semiconductor film containing an impurity element which imparts n-type conductivity is formed with a thickness of 20 to 80 nm as a semiconductor film containing a single conductivity type impurity element. For example, an a-Si:H film containing n-type impurity element may be formed, and in order to do so, phosphine (PH_3) is added at a 0.1 to 5% concentration to silane (SiH_4). Alternatively, a hydrogenated microcrystalline silicon film (pc-Si:H) may also be used as a substitute for the second amorphous semiconductor film **106** containing an impurity element which imparts n-type conductivity.

[0155] These films can be formed in succession by appropriately changing the reaction gas. Further, these films can be laminated successively without exposure to the atmosphere at this time by using the same reaction chamber or a plurality of reaction chambers in the plasma CVD apparatus. By thus depositing successively these films without exposing the films to the atmosphere, the mixing in of impurities into the first amorphous semiconductor film can be prevented.

[0156] Note that it is possible to combine this Embodiment with any one of Embodiments 1 to 3.

Embodiment 5

[0157] Examples are shown in Embodiment 1 and Embodiment 4 of laminating an insulating film, a first amorphous semiconductor film, a second amorphous semiconductor film containing an impurity element which imparts n-type, and a first conductive film, in order and in succession. An example of an apparatus prepared with a plurality of chambers, and used for cases of performing this type of successive film deposition is shown in FIG. **10**.

[0158] An outline as seen from above of an apparatus (successive film deposition system), shown by this Embodiment, is shown in FIG. **10**. Reference numerals **10** to **15** in FIG. **10** denote chambers having airtight characteristics. A vacuum evacuation pump and an inert gas introduction system are arranged in each of the chambers.

[0159] The chambers denoted by reference numerals **10** and **15** are load-lock chambers for bringing test pieces (processing substrates) **30** into the system. The chamber denoted by reference numeral **11** is a first chamber for deposition of the insulating film **104**. The chamber denoted by reference numeral **12** is a second chamber for deposition of the first amorphous semiconductor film **105**. The chamber denoted by reference numeral **13** is a third chamber for deposition of the second amorphous semiconductor film **106** which imparts n-type conductivity. The chamber denoted by reference numeral **14** is a fourth chamber for deposition of the first conductive film **107**. Further, reference numeral **20** denotes a common chamber of the test pieces, arranged in common with respect to each chamber.

[0160] An example of operation is shown below.

[0161] After pulling a high vacuum state in all of the chambers at first, a purge state (normal pressure) is made by using an inert gas, nitrogen here. Furthermore, a state of closing all gate valves **22** to **27** is made.

[0162] First, a cassette **28** loaded with a multiple number of processing substrates is placed into the load-lock chamber **10**. After the cassette is placed inside, a door of the load-lock chamber (not shown in the figure) is closed. In this state, the gate valve **22** is opened and one of the processing substrates **30** is removed from the cassette, and is taken out to the common chamber **20** by a robot arm **21**. Position alignment is performed in the common chamber at this time. Note that a substrate on which the wirings **101**, **102**, **103***a* and **103***b* are formed, obtained in accordance with Embodiment 1, is used for the substrate **30**.

[0163] The gate valve **22** is then closed, and a gate valve **23** is opened next. The processing substrate **30** is then moved into the first chamber **11**. Film deposition processing is performed within the first chamber at a temperature of 150 to 300° C., and the insulating film **104** is obtained. Note that a film such as a silicon nitride film, a silicon oxide film, a silicon oxynitride film, or a lamination film of these films, can be used as the insulating film. A single layer silicon nitride film is employed in this Embodiment, but a two-layer, three-layer, or higher layer lamination structure film may also be used. Note that a chamber capable of plasma CVD is used here, but a chamber which is capable of sputtering by use of a target may also be used.

[0164] After completing the deposition of the insulating film, the processing substrate is pulled out into the common chamber by the robot arm, and is then transported to the second chamber **12**. Film deposition is performed within the second chamber at a temperature of 150 to 300° C., similar to that of the first chamber, and the first amorphous semiconductor film **105** is obtained by plasma CVD. Note that a film such as a microcrystalline semiconductor film, an amorphous germanium film, an amorphous silicon germanium film, or a lamination film of these films, etc., can be used as the first amorphous semiconductor film. Further, a heat treatment process for reducing the concentration of hydrogen may be omitted with a formation temperature of 350 to 500° C. for the first amorphous semiconductor film. Note that a chamber capable of plasma CVD is used here, but a chamber which is capable of sputtering by use of a target may also be used.

[0165] After completing deposition of the first amorphous semiconductor film, the processing substrate is pulled out into the common chamber and then transported to the third chamber **13**. Film deposition process is performed within the third chamber at a temperature of 150° C. to 300° C., similar to that of the second chamber, and the second amorphous semiconductor film **106**, containing an impurity element which imparts n-type conductivity (P or As), is obtained by plasma CVD. Note that a chamber capable of plasma CVD is used here, but a chamber which is capable of sputtering by use of a target may also be used.

[0166] After completing deposition of the second amorphous semiconductor film containing an impurity element which imparts n-type conductivity, the processing substrate is pulled out into the common chamber, and then is transported to the fourth chamber **14**. The first conductive film **107** is obtained within the fourth chamber by sputtering using a metallic target.

[0167] The processed substrate, on which four layers have thus been formed in succession, is then transported to the load-lock chamber **15** by the robot arm, and is contained in a cassette **29**.

[0168] Note that the apparatus shown in FIG. **10** is only one example. Further, it is possible to freely combine this Embodiment with any one of Embodiments 1 to 4.

Embodiment 6

[0169] In Embodiment 5, an example of successive lamination using a plurality of chambers is shown, but in this Embodiment a method of successive lamination within one chamber maintained at high vacuum using the apparatus shown in FIG. **11** is employed.

[0170] The apparatus system shown in FIG. **11** is used in this Embodiment. In FIG. **11**, reference numeral **40** denotes a processing substrate, reference numeral **50** denotes a common chamber, **44** and **46** denote load-lock chambers, **45** denotes a chamber, and reference numerals **42** and **43** denote cassettes. In order to prevent contamination developing during transport of the substrate, lamination is performed in the same chamber in this Embodiment.

[0171] It is possible to freely combine this Embodiment with any one of Embodiments 1 to 4.

[0172] Note however, when applied to Embodiment 1, a plurality of targets are prepared in the chamber **45**, and the insulating film **104**, the first amorphous semiconductor film **105**, the second amorphous semiconductor film **106** containing an impurity element which imparts n-type conductivity, and the first conductive film **107** may be laminated by changing the reaction gas in order.

[0173] Further, when applied to Embodiment 4, the insulating film **104**, the first amorphous semiconductor film **105**, and the second amorphous semiconductor film **106** containing an impurity element which imparts n-type conductivity, may be laminated by changing the reaction gas in order.

Embodiment 7

[0174] In Embodiment 1, an example of forming the second amorphous semiconductor film containing an impurity element which imparts n-type by using sputtering is shown, but in this Embodiment an example of forming it by using plasma

CVD is shown. Note that, except for the method of forming the second amorphous semiconductor film containing an impurity element which imparts n-type, this Embodiment is identical to Embodiment 1, and therefore only differing points are stated below.

[0175] If phosphine (PH_3) is added at a concentration of 0.1 to 5% with respect to silane (SiH_4) as a reaction gas using plasma CVD, then the second amorphous semiconductor film containing an impurity element which imparts n-type can be obtained.

Embodiment 8

[0176] In Embodiment 7, an example of forming the second amorphous semiconductor film containing an impurity element which imparts n-type by using plasma CVD is shown, and in this Embodiment, an example of using a microcrystalline semiconductor film containing an impurity element which imparts n-type conductivity is shown.

[0177] By setting the deposition temperature from 80 to 300° C., preferably between 140 and 200° C., taking a gas mixture of silane diluted by hydrogen (SiH_4: H_2=1:10 to 100) and phosphine (PH_3) as the reaction gas, setting the gas pressure from 0.1 to 10 Torr, and setting the discharge power from 10 to 300 mW/cm^2, a microcrystalline silicon film can be obtained. Further phosphorous may be added by plasma doping after film deposition of this microcrystalline silicon film.

Embodiment 9

[0178] FIG. **12** is a diagram which schematically shows a state of constructing an electro-optical display device by using the COG method. A pixel region **803**, an external input-output terminal **804**, and a connection wiring **805** are formed on a first substrate. Regions surrounded by dotted lines denote a region **801** for attaching a scanning line side IC chip, and a region **802** for attaching a data line side IC chip. An opposing electrode **809** is formed on a second substrate **808**, and this is joined to the first substrate **800** by using a sealing material **810**. A liquid crystal layer **811** is formed inside the sealing material **810** by injecting a liquid crystal. The first substrate and the second substrate are joined with a predetermined gap, and this is set from 3 to 8•for a nematic liquid crystal.

[0179] IC chips **806** and **807** have circuit structures which differ between the data line side and the scanning line side. The IC chips are mounted on the first substrate. An FPC (flexible printed circuit) **812** is attached to the external input-output terminal **804** in order to input power supply and control signals from the outside. In order to increase the adhesion strength of the FPC **812**, a reinforcing plate **813** may be formed. The electro-optical device can thus be completed. If an electrical inspection is performed before mounting the IC chips on the first substrate, then the final process yield of the electro-optical device can be improved, and the reliability can be increased.

[0180] Further, a method such as a method of connection using an anisotropic conductive material or a wire bonding method, can be employed as the method of mounting the IC chips on the first substrate. FIG. **13** show an example of such. FIG. **13**(A) shows an example in which an IC chip **908** is mounted on a first substrate **901** using an anisotropic conductive material. A pixel region **902**, a lead wire **906**, a connection wiring and an input-output terminal **907** are formed on the first substrate **901**. A second substrate is bonded to the first substrate **901** by using a sealing material **904**, and a liquid crystal layer **905** is formed therebetween.

[0181] Further, an FPC **912** is bonded to one edge of the connection wiring and the input-output terminal **907** by using an anisotropic conductive material. The anisotropic conductive material is made from a resin **915** and conductive particles **914** having a diameter of several tens to several hundreds of μm and plated by a material such as Au, and the connection wiring **913** formed with the FPC **912** and the connection wiring and input-output terminal **907** are electrically connected by the conductive particles **914**. The IC chip **908** is also similarly bonded to the first substrate by an anisotropic conductive material. An input-output terminal **909** provided with the IC chip **908** and the lead wire **906**, or a connection wiring and the input-output terminal **907** are electrically connected by conductive particles **910** mixed into a resin **911**.

[0182] Furthermore, as shown by FIG. **13**(B), the IC chip may be fixed to the first substrate by an adhesive material **916**, and an input-output terminal of an IC chip and a lead wire or a connection wiring may be connected by an Au wire **917**. Then, this is all sealed by a resin **918**.

[0183] The method of mounting the IC chip is not limited to the method based on FIGS. **12** and **13**, and it is also possible to use a known method not explained here, such as a COG method, a wire bonding method or a TAB method.

[0184] It is possible to freely combine this Embodiment with Embodiment 1, 3 or 8.

Embodiment 10

[0185] In the embodiment 1, although the description has been made on the example in which the transparent conductive film covering the pixel electrode and the source electrode is formed, in this embodiment, an example in which a transparent conductive film is not formed will be described by use of FIG. **15**.

[0186] In accordance with the embodiment 1, the state of FIG. **2**(C), that is, a gate wiring **602**, a common wiring **603***a*, a common electrode **603***b*, and a wiring (which becomes a source wiring and a pixel electrode in a subsequent step) are obtained.

[0187] Resist mask is formed next by a third photolithography process. Unnecessary portion is then removed by etching, forming a first amorphous semiconductor film, a source region, a drain region, the source wiring **621**, and the pixel electrode **622**.

[0188] The third photolithography process removes the wiring the second amorphous semiconductor film containing an impurity element which imparts n-type conductivity and a portion of the first amorphous semiconductor film by etching, forming an opening. In the embodiment 1, after selectively removing the wiring **111** by wet etching and forming the source wiring **621** and the pixel electrode **622**, the second amorphous semiconductor film, containing the impurity element which imparts n-type conductivity, and a portion of the amorphous semiconductor film are etched by dry etching. Note that wet etching and dry etching are used in the embodiment 1, but the operator may perform only dry etching by suitably selecting the reaction gas, and the operator may perform only wet etching by suitably selecting the reaction solution.

[0189] Further, the lower portion of the opening reaches the first amorphous semiconductor film, and the first amorphous semiconductor film is formed having a concave portion. The wiring is separated into the source wiring **621** and the pixel electrode **622** by the opening, and the second amorphous semiconductor film, containing an impurity element which imparts n-type conductivity is separated into the source region and the drain region.

[0190] If subsequent steps are performed in accordance with the embodiment 1 and fabrication is made, an active matrix substrate is obtained.

[0191] It is possible to freely combine the embodiment 6 with any one of the embodiments 1 to 9.

Embodiment 11

[0192] The present Embodiment shows an example of using a plastic substrate (or a plastic film) for the substrate. Note that since this Embodiment is almost identical to Embodiment 1 without the use of plastic substrate for the substrate, only different points are described.

[0193] PES (polyethylene sulfone), PC (polycarbonate), PET (polyethylene terephthalate) and PEN (polyethylene naphthalate) can be used as the plastic substrate material.

[0194] An active matrix substrate is completed using the plastic substrate provided that manufacturing is performed in accordance with Embodiment 1. Note that it is preferable to form the insulating film, the first amorphous semiconductor film, and the second amorphous semiconductor film containing an impurity element which imparts n-type conductivity by sputtering with the relatively low film deposition temperature.

[0195] A TFT having good characteristics can be formed on the plastic substrate, and the resulting display device can be made low weight. Further, it is possible to make a flexible electro-optical device because the substrate is plastic. Furthermore, assembly becomes easy.

[0196] Note that this Embodiment can be freely combined with any one of Embodiments 1 to 3, 9 and 10.

Embodiment 12

[0197] In the present embodiment, an example of forming a protecting circuit in a region other than a pixel portion in the same process in which second conductive films **123** and **124** covering the pixel electrode and source wiring can be formed is shown in FIG. **16**.

[0198] In FIG. **16**(A), reference numeral **701** denotes a wiring, and shows a gate wiring, a source wiring, or a common wiring extended from the pixel portion. Further, electrodes **701** are laid down in regions in which the wiring **701** is not formed, and are formed so as not to overlap the wiring **701**. The present embodiment shows an example of forming the protecting circuit without increasing the number of masks, but there is no need to limit the structure to that of FIG. **16**(A). For example, the number of masks may be increased and then, the protecting circuit may be formed by a protecting diode or a TFT.

[0199] Further, FIG. **16**(B) shows an equivalent circuit diagram.

[0200] By making this type of constitution, the generation of static electricity due to friction between production devices and an insulating substrate can be prevented during the production process. In particular, the TFTs etc. can be protected from static electricity developing during a liquid crystal orienting process of rubbing performed during manufacture.

[0201] Note that the present embodiment can be freely combined with any one of the embodiments 1 to 11.

Embodiment 13

[0202] A bottom gate type TFT formed by implementing any one of the above embodiments 1 to 12 can be used in various electro-optical devices (such as an active matrix type liquid crystal display device). Namely, the present invention can be implemented in all electronic equipment in which these electro-optical devices are built into a display portion.

[0203] The following can be given as such electronic equipment: a video camera, a digital camera, a projector (rear type or front type), a head-mounted display (goggle type display), a car navigation system, a car stereo, a personal computer, and a portable information terminal (such as a mobile computer, a portable telephone or an electronic book). Examples of these are shown in FIGS. **17** and **18**.

[0204] FIG. **17**(A) is a personal computer, and it includes a main body **2001**, an image input portion **2002**, a display portion **2003**, and a keyboard **2004**. The present invention can be applied to the display portion **2003**.

[0205] FIG. **17**(B) is a video camera, and it includes a main body **2101**, a display portion **2102**, an audio input portion **2103**, operation switches **2104**, a battery **2105**, and an image receiving portion **2106**. The present invention can be applied to the display portion **2102**.

[0206] FIG. **17**(C) is a mobile computer, and it includes a main body **2201**, a camera portion **2202**, an image receiving portion **2203**, operation switches **2204**, and a display portion **2205**. The present invention can be applied to the display portion **2205**.

[0207] FIG. **17**(D) is a player that uses a recording medium on which a program is recorded (hereafter referred to as a recording medium), and the player includes a main body **2401**, a display portion **2402**, a speaker portion **2403**, a recording medium **2404**, and operation switches **2405**. Note that this player uses a recording medium such as a DVD (digital versatile disk) or a CD, and the appreciation of music, the appreciation of film, game playing and the Internet can be performed. The present invention can be applied to the display portion **2402**.

[0208] FIG. **17**(E) is a digital camera, and it includes a main body **2501**, a display portion **2502**, an eyepiece portion **2503**, operation switches **2504**, and an image receiving portion (not shown in the figure). The present invention can be applied to the display portion **2502**.

[0209] FIG. **18**(A) is a portable telephone, and it includes a main body **2901**, an audio output portion **2902**, an audio input portion **2903**, a display portion **2904**, operation switches **2905**, and an antenna **2906**. The present invention can be applied to the display portion **2904**.

[0210] FIG. **18**(B) is a portable book (electronic book), and it includes a main body **3001**, display portions **3002** and **3003**, a recording medium **3004**, operation switches **3005**, and an antenna **3006**. The present invention can be applied to the display portions **3002** and **3003**.

[0211] FIG. **18**(C) is a display, and it includes a main body **3101**, a support stand **3102**, and a display portion **3103**. The present invention can be applied to the display portion **3103**. The display of the present invention is advantageous for a large size screen in particular, and is advantageous for a display equal to or greater than 10 inches (especially equal to or greater than 30 inches) in the opposite angle.

[0212] The applicable range of the present invention is thus extremely wide, and it is possible to apply the present invention to electronic equipment in all fields. Further, the electronic equipment of the embodiment 13 can be realized by using a constitution of any combination of the embodiments 1 to 12.

What is claimed is:

1. A liquid crystal display device including a pair of substrates and a liquid crystal held between the pair of substrates, wherein the liquid crystal display device is characterized in that:

a gate wiring and a common electrode is formed on one of the pair of substrates,

an insulating film is formed on the gate wiring and the common electrode,

an amorphous semiconductor film is formed on the insulating film,

a source region and a drain region are formed on the amorphous semiconductor film,

a source wiring or a pixel electrode is formed on the source region or the drain region,

the pixel electrode and the common electrode are disposed so that an electric field parallel with a substrate plane of the one substrate is generated, and

one end face of the drain region or the source region is substantially coincident with an end face of the amorphous semiconductor film and an end face of the pixel electrode.

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当前申请(专利权)人(译)	半导体能源研究所有限公司.		
[标]发明人	YAMAZAKI SHUNPEI HIRAKATA YOSHIHARU		
发明人	YAMAZAKI, SHUNPEI HIRAKATA, YOSHIHARU		
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摘要(译)

在IPS系统的液晶显示装置中，通过减少制造TFT的步骤数来实现制造成本的降低和产量的提高。沟道蚀刻型底栅TFT结构，其中源区和漏区的图案化以及源布线和像素电极的图案化由相同的光掩模执行。