



(19) **United States**

(12) **Patent Application Publication**
Misaki

(10) **Pub. No.: US 2013/0201420 A1**

(43) **Pub. Date: Aug. 8, 2013**

(54) **THIN FILM TRANSISTOR SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE PROVIDED WITH SAME**

Publication Classification

(75) Inventor: **Katsunori Misaki**, Yonago-shi (JP)

(51) **Int. Cl.**

G02F 1/1362 (2006.01)

H01L 29/786 (2006.01)

(73) Assignee: **Sharp Kabushiki Kaisha**, Osaka-shi, Osaka (JP)

(52) **U.S. Cl.**

CPC **G02F 1/136227** (2013.01); **H01L 29/7869** (2013.01)

USPC **349/46; 257/43**

(21) Appl. No.: **13/814,022**

(22) PCT Filed: **May 27, 2011**

(57) **ABSTRACT**

(86) PCT No.: **PCT/JP2011/002959**

§ 371 (c)(1),

(2), (4) Date: **Feb. 22, 2013**

A source section (S) is made of a source metal (25s) provided above a gate insulating film (23) and an oxide semiconductor film (24a), and a drain section (DR) includes a low resistance portion (24ad) which is part of the oxide semiconductor film (24a), where the part includes a surface of the oxide semiconductor film (24a) opposite to the gate insulating film (23), and the resistance of the part is reduced.

(30) **Foreign Application Priority Data**

Aug. 7, 2010 (JP) 2010-178226

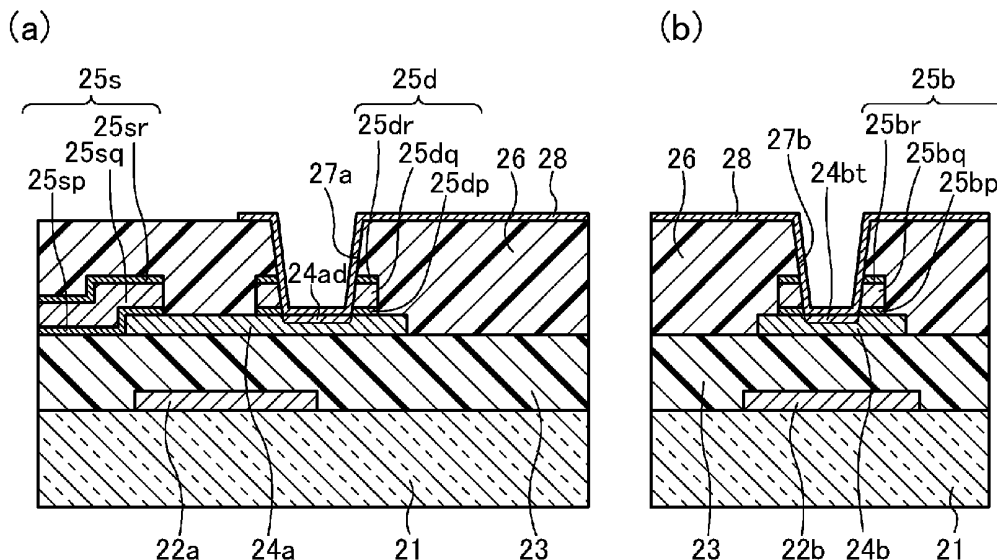


FIG.1

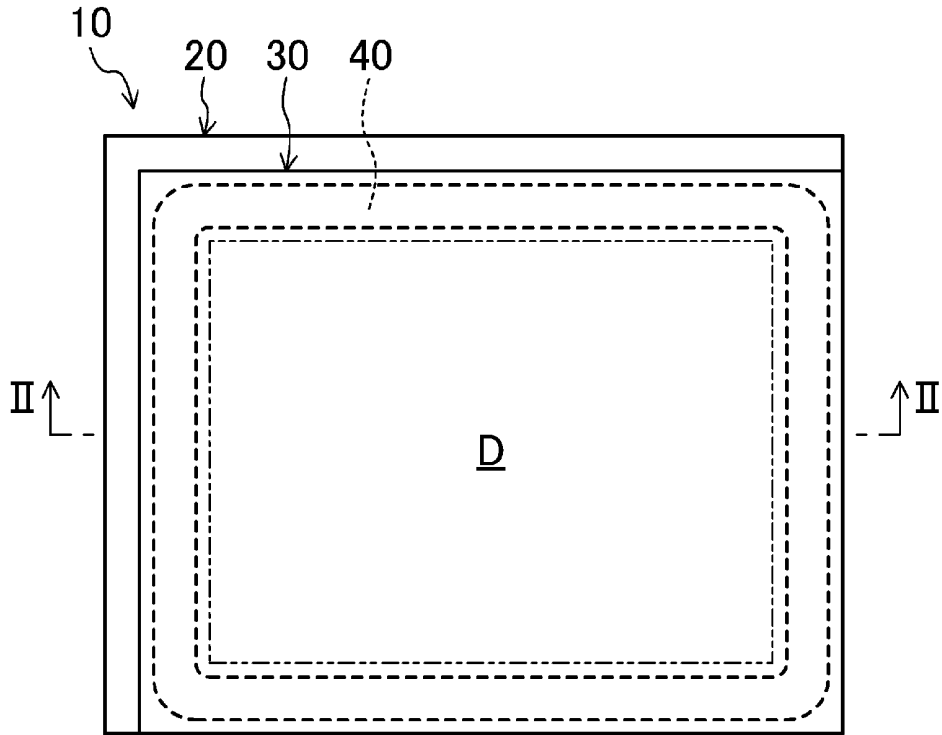


FIG.2

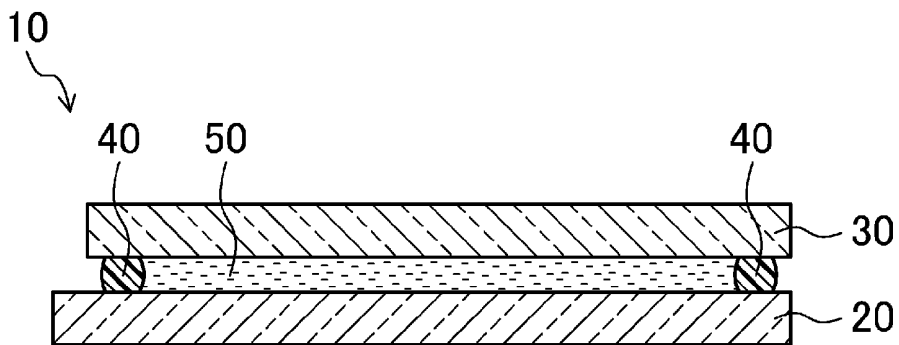


FIG.3

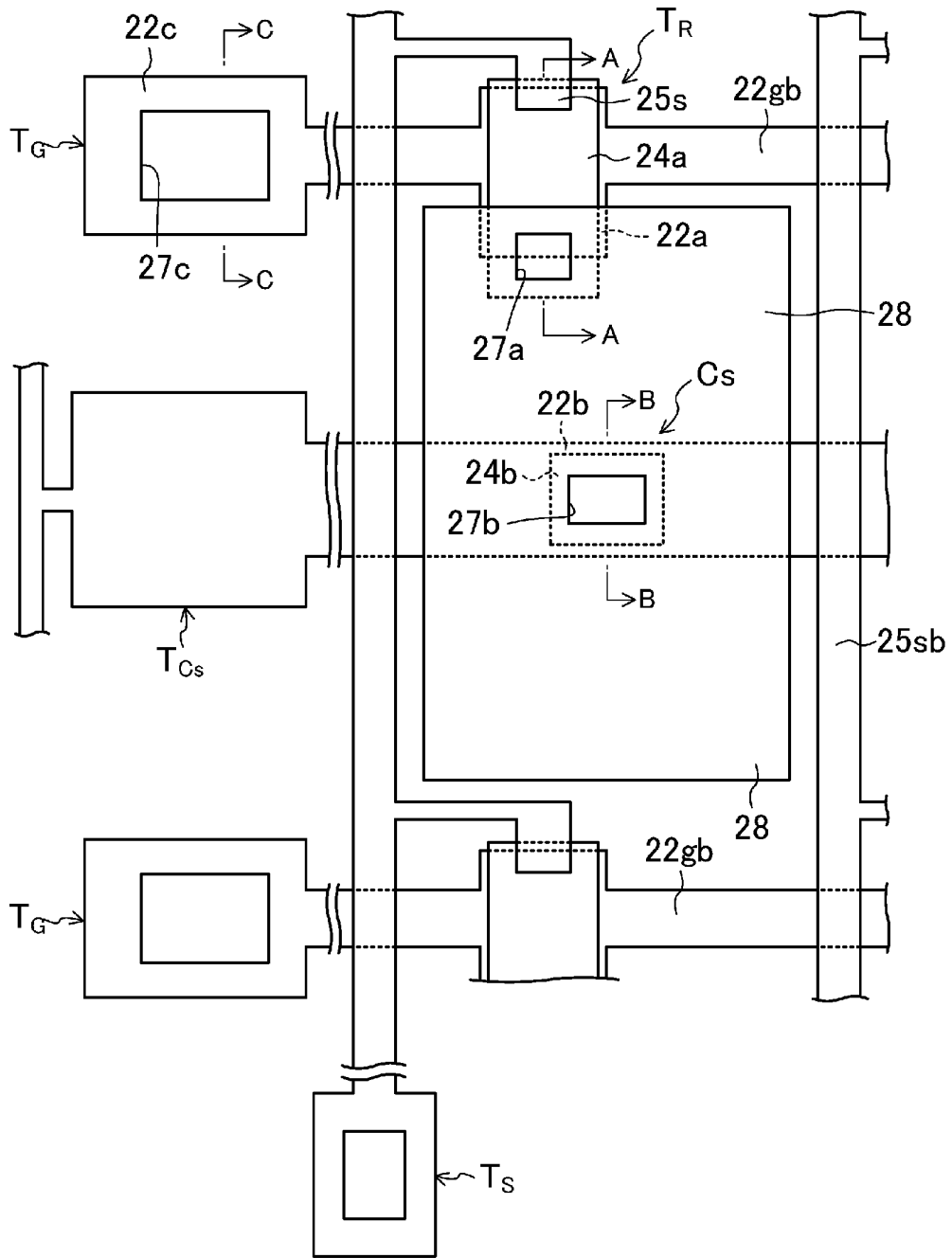


FIG.4

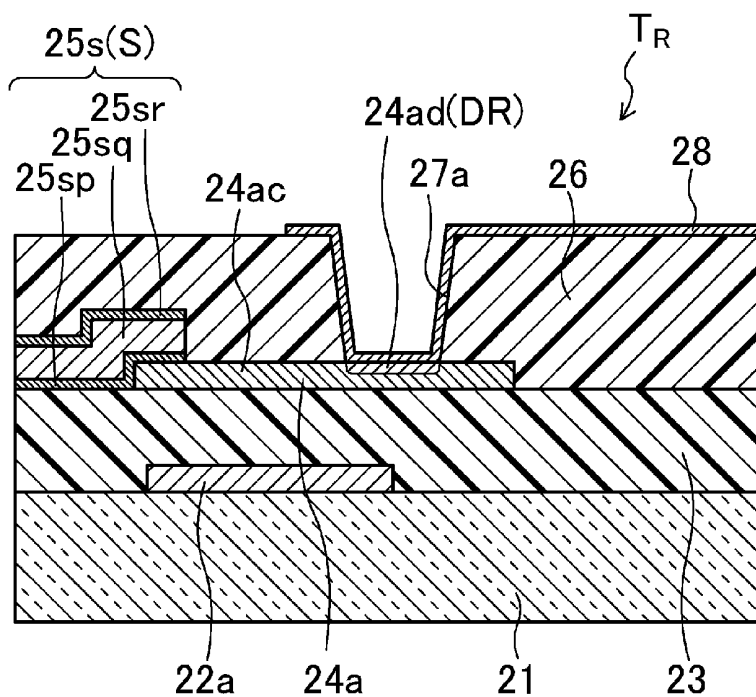


FIG.5

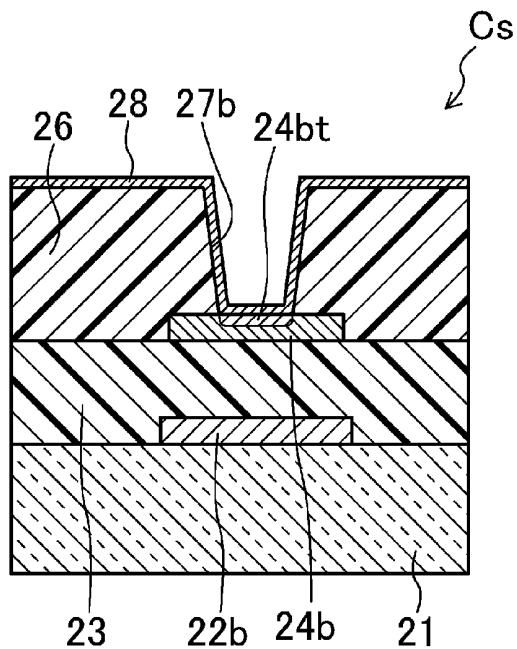


FIG.6

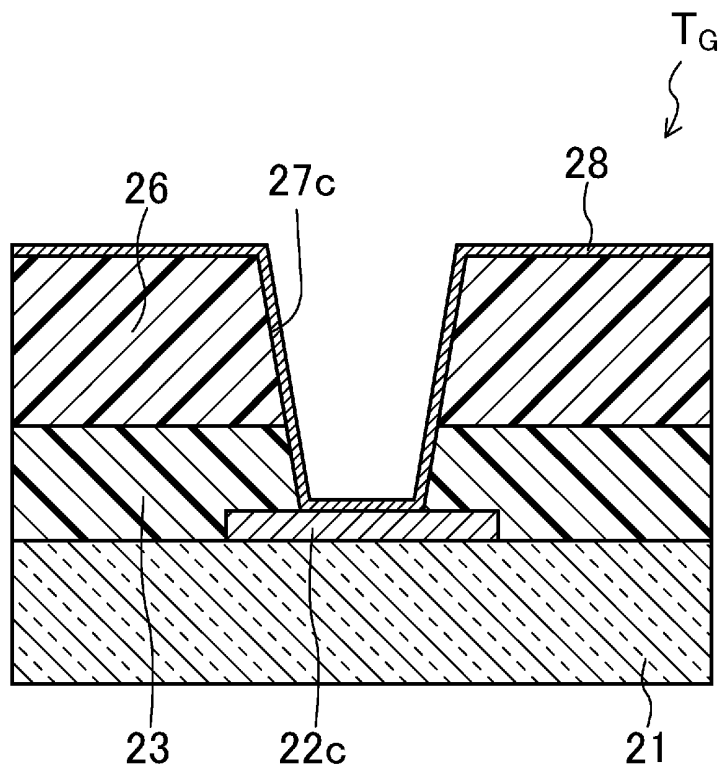


FIG. 7

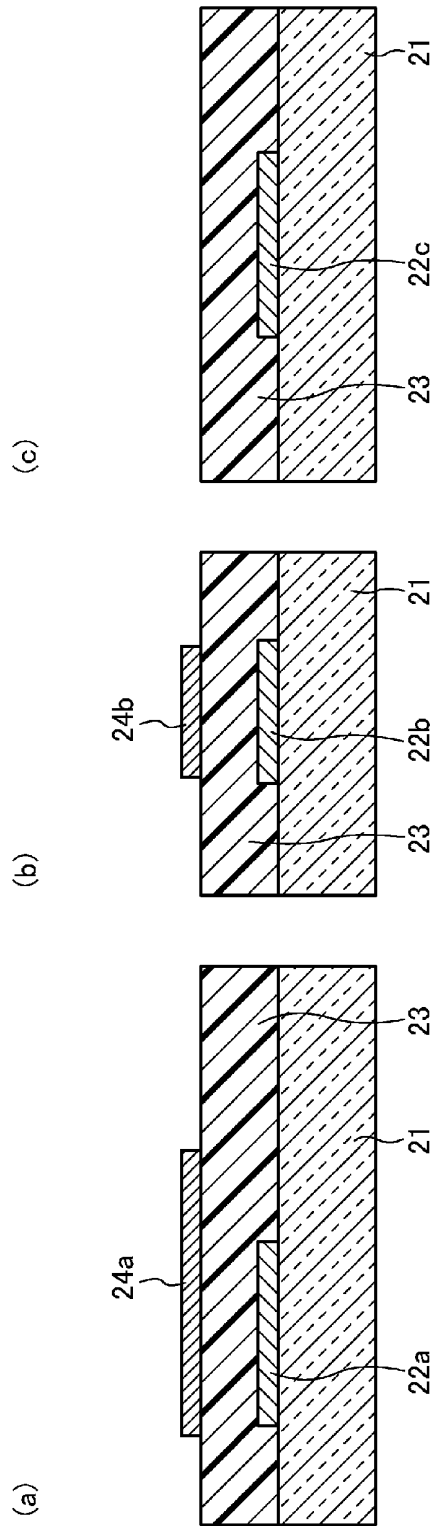


FIG.8

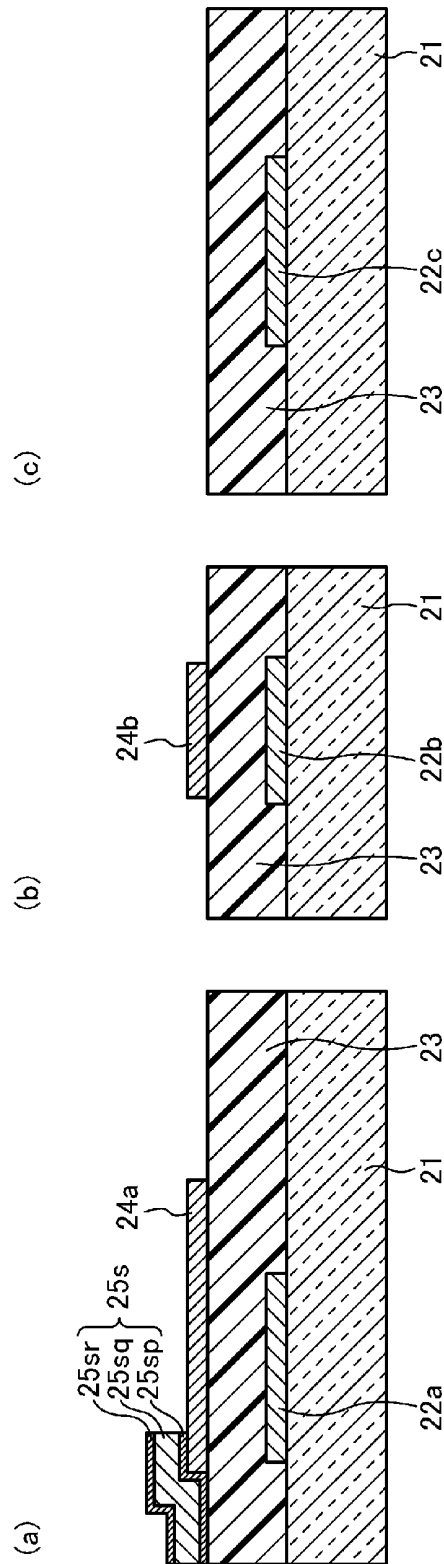


FIG.9

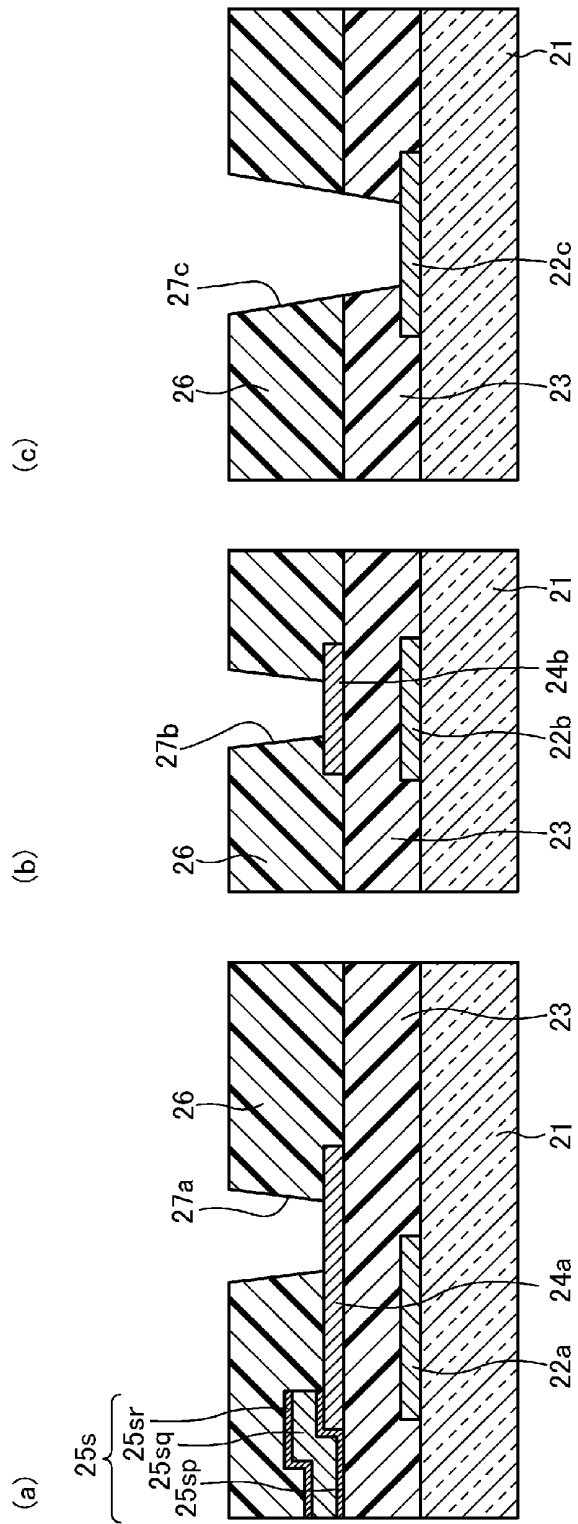


FIG.10

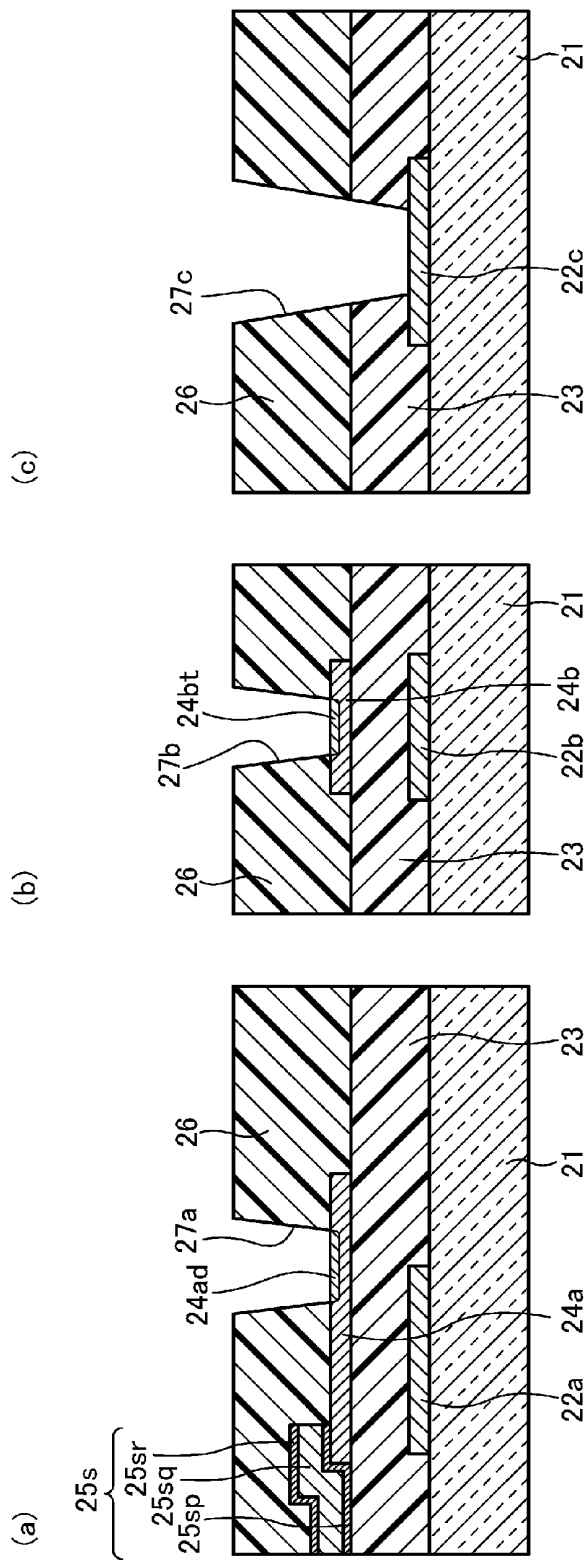


FIG. 11

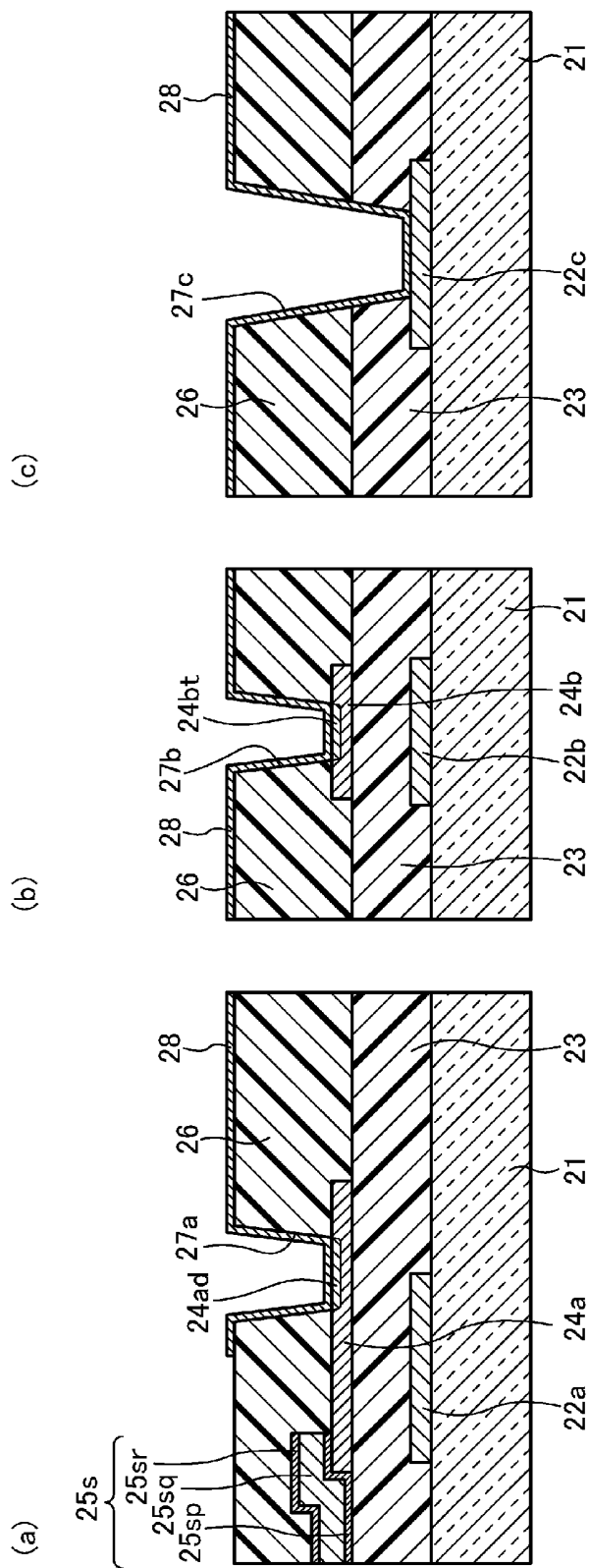


FIG.12

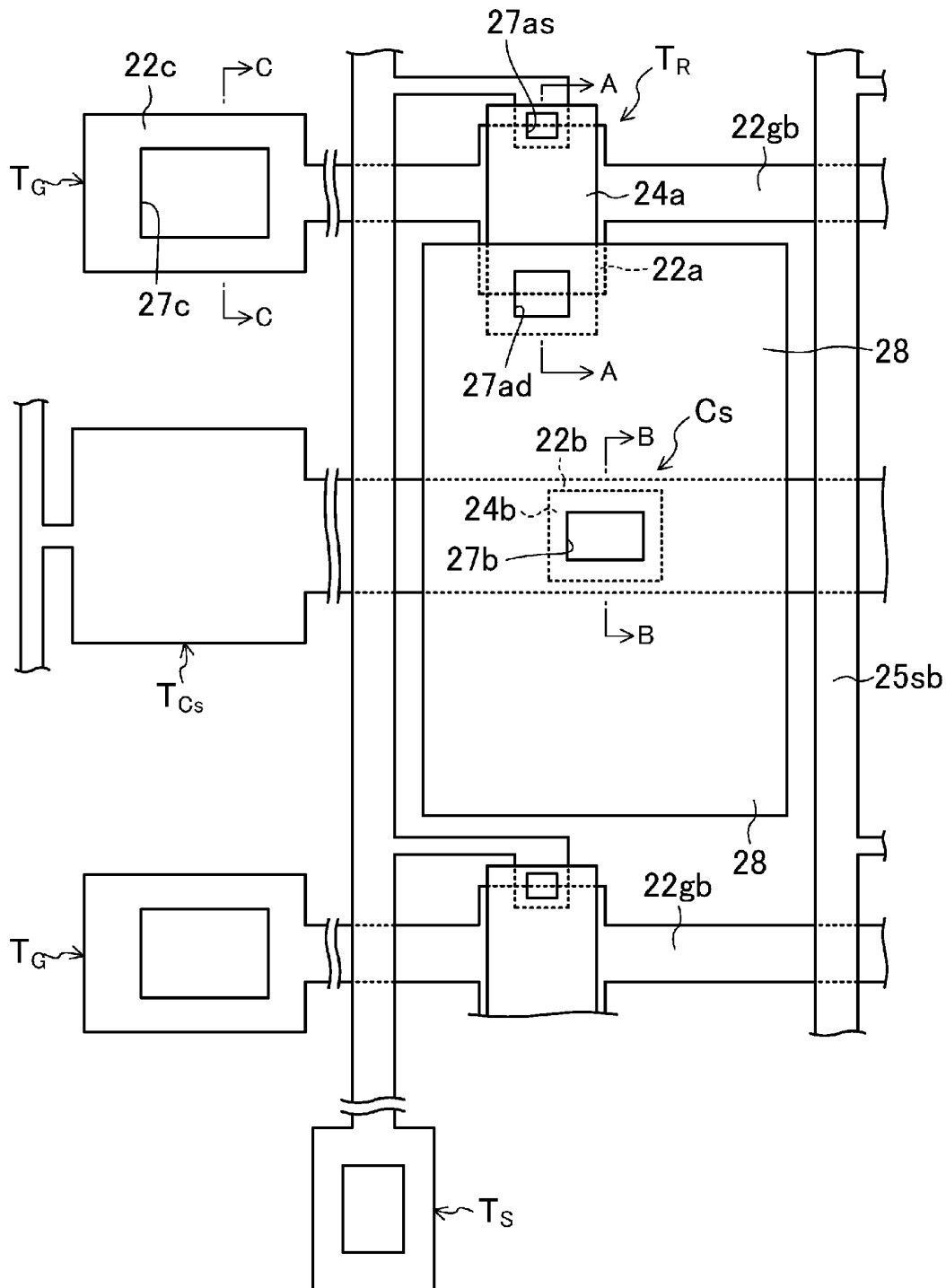


FIG. 13

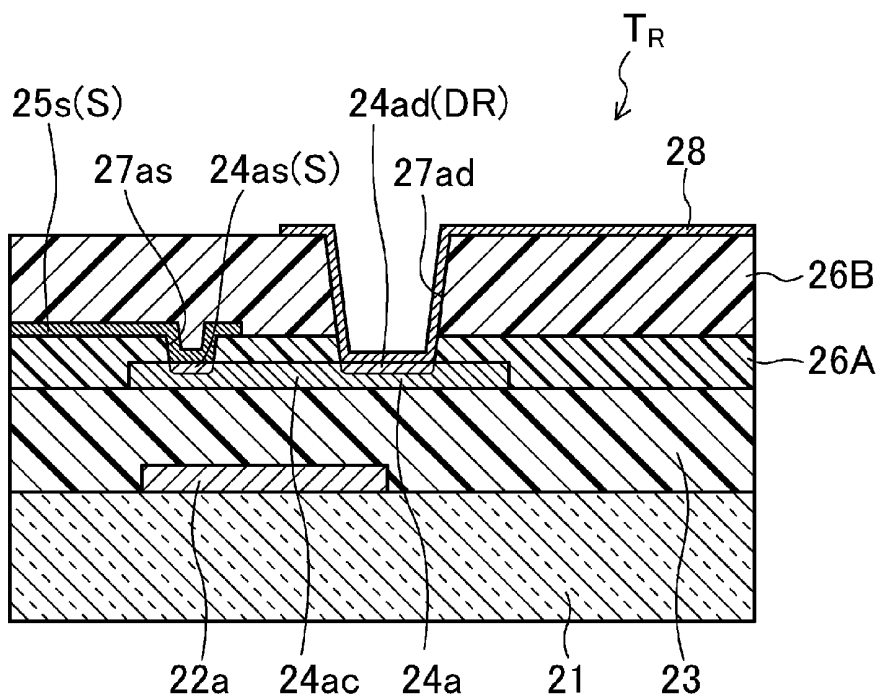


FIG. 14

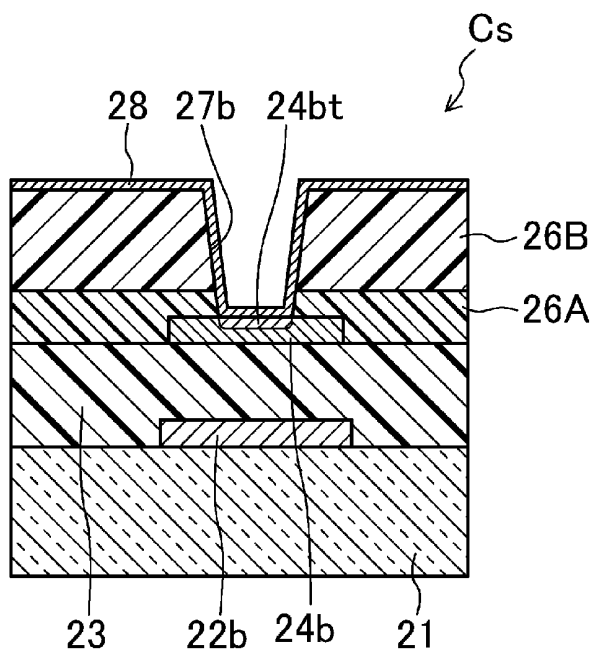


FIG.15

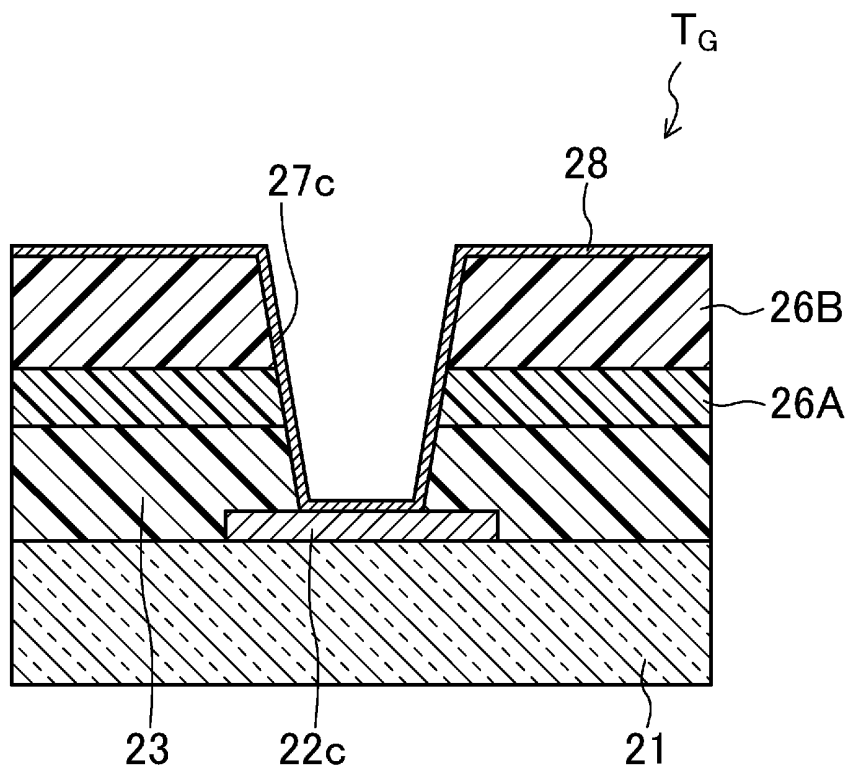


FIG. 16

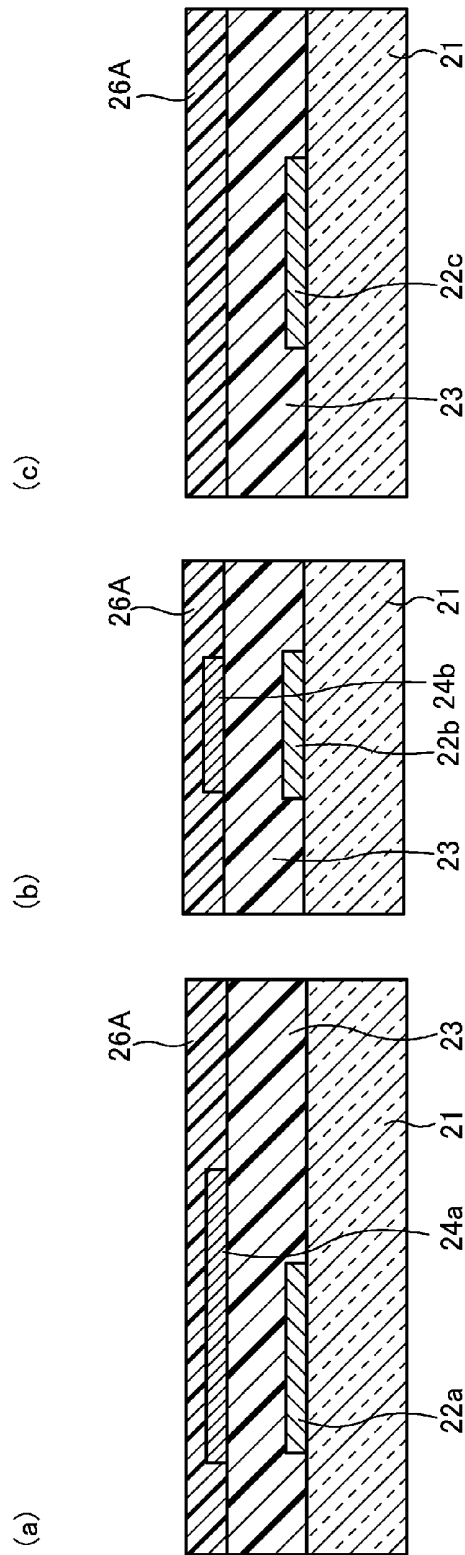


FIG.17

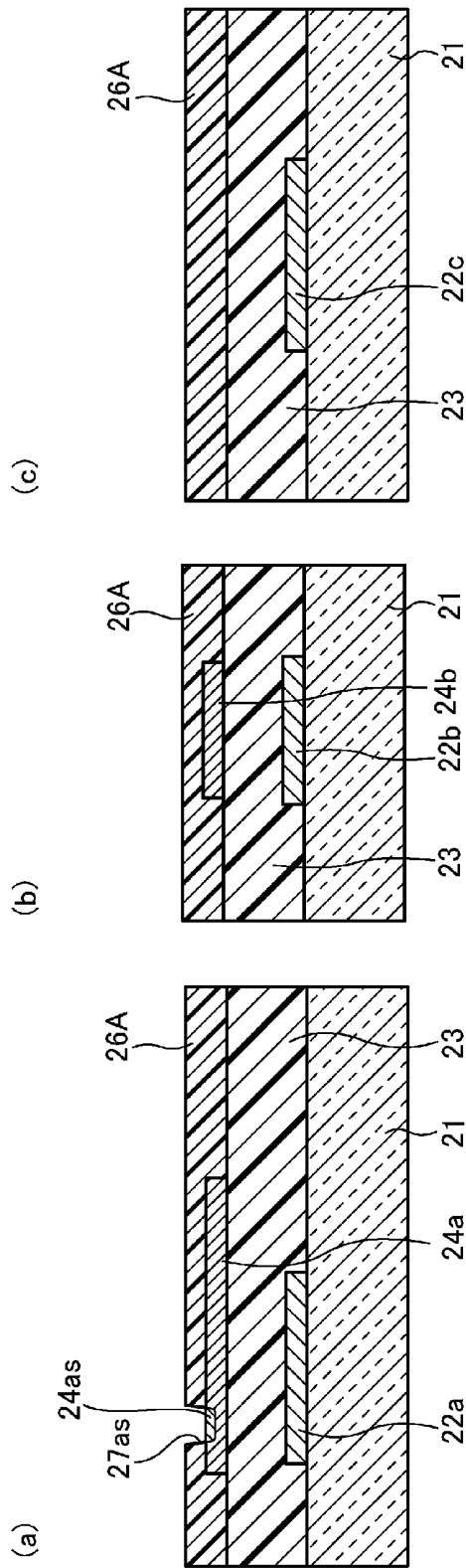


FIG.18

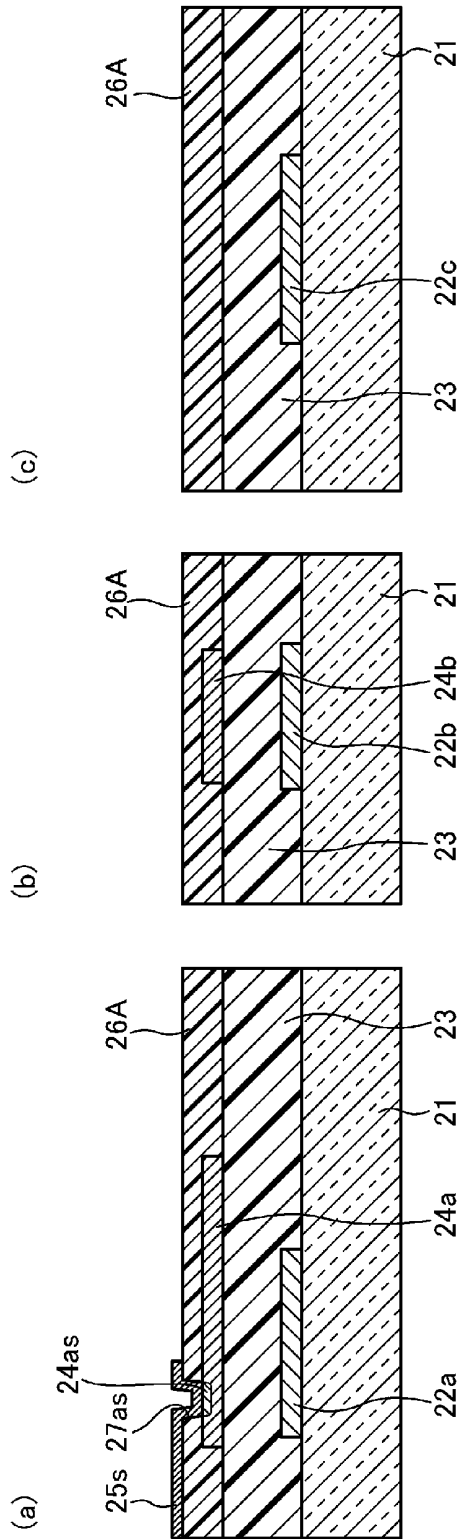


FIG.19

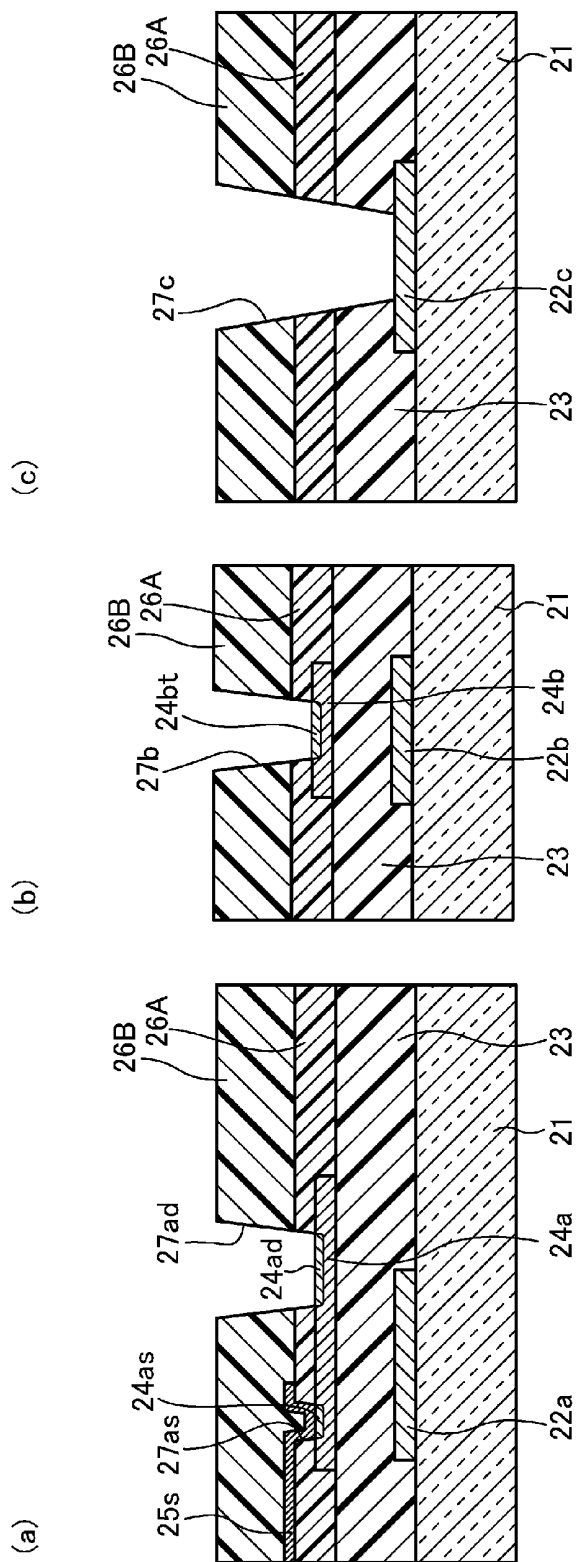


FIG.20

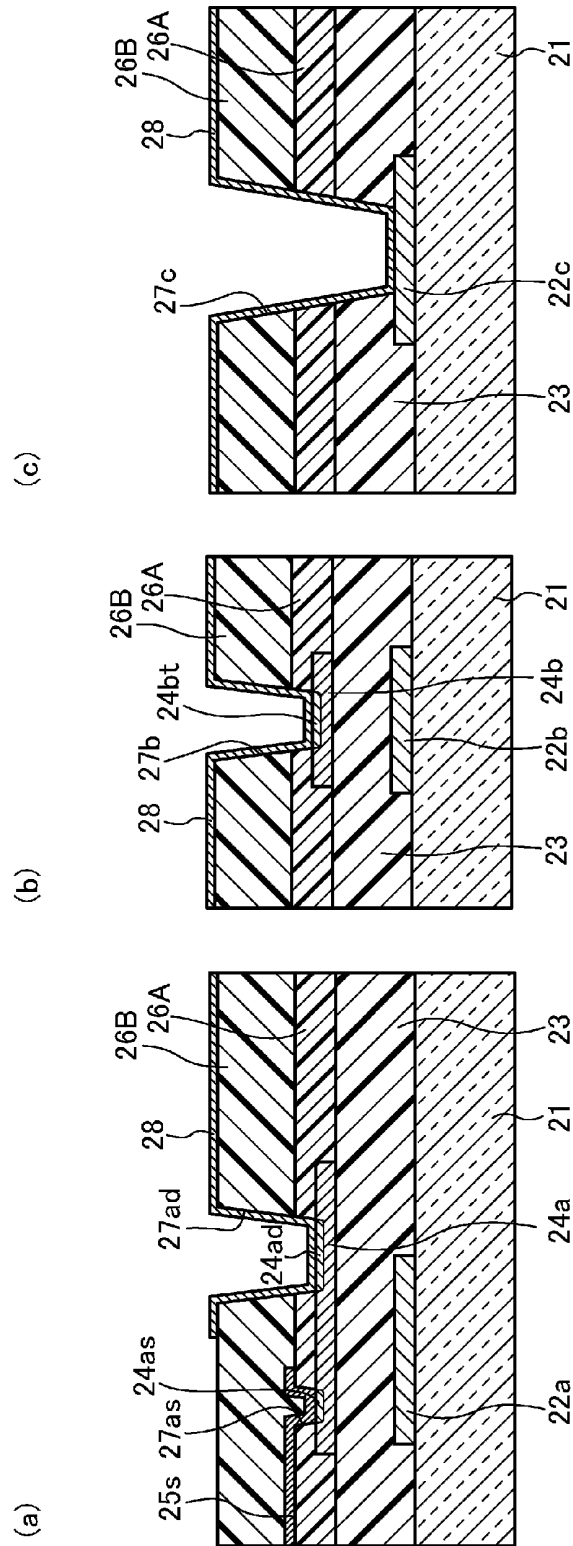


FIG.21

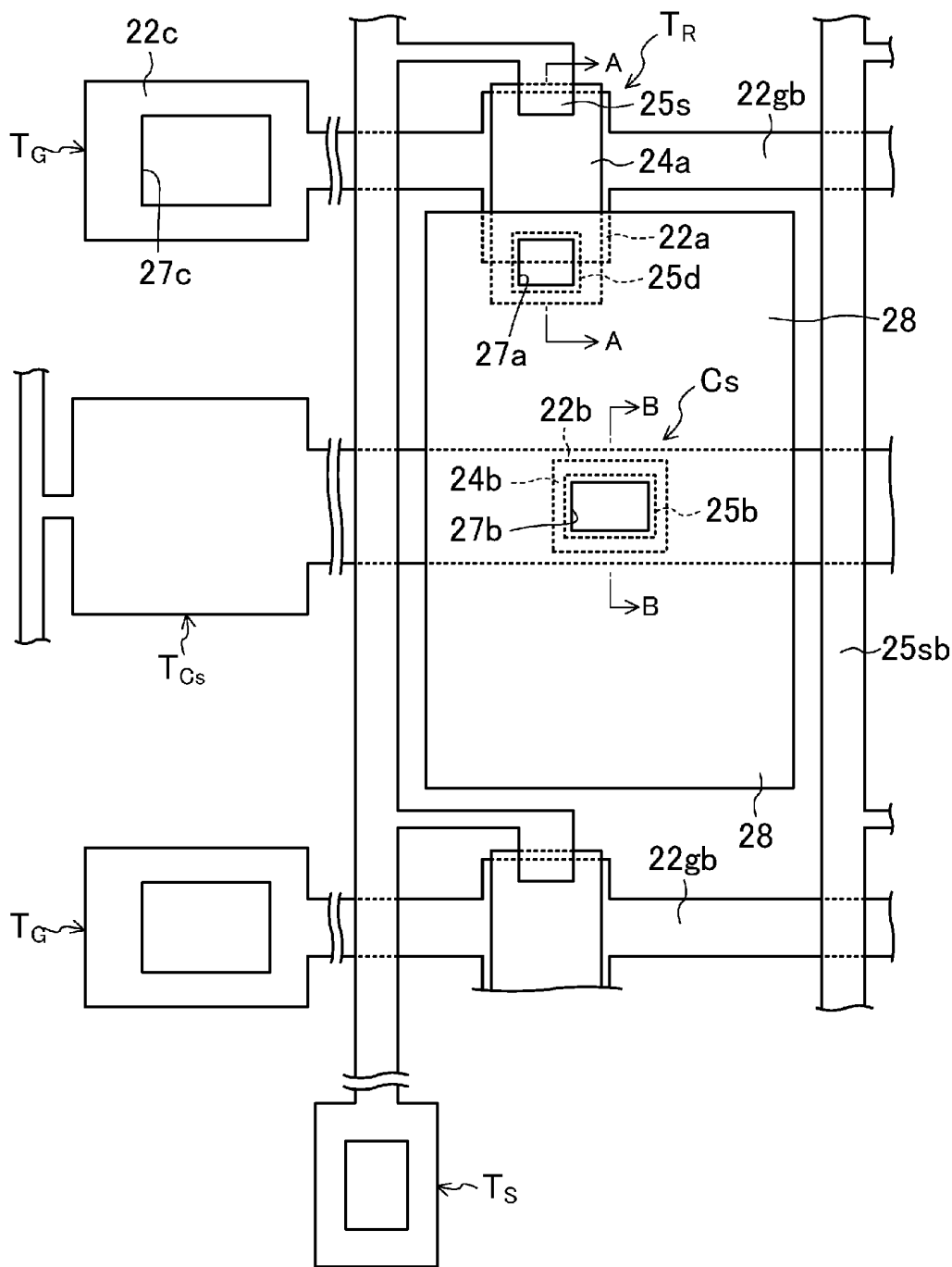


FIG.24

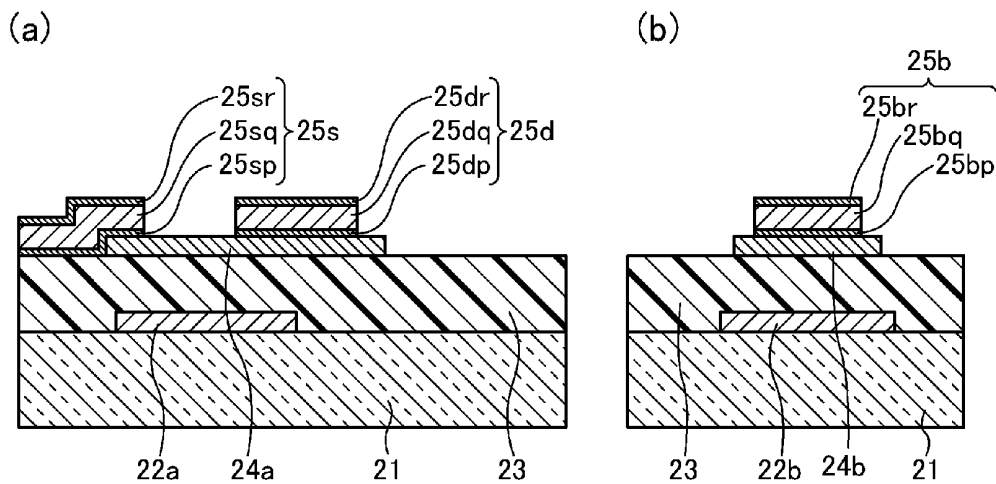


FIG.25

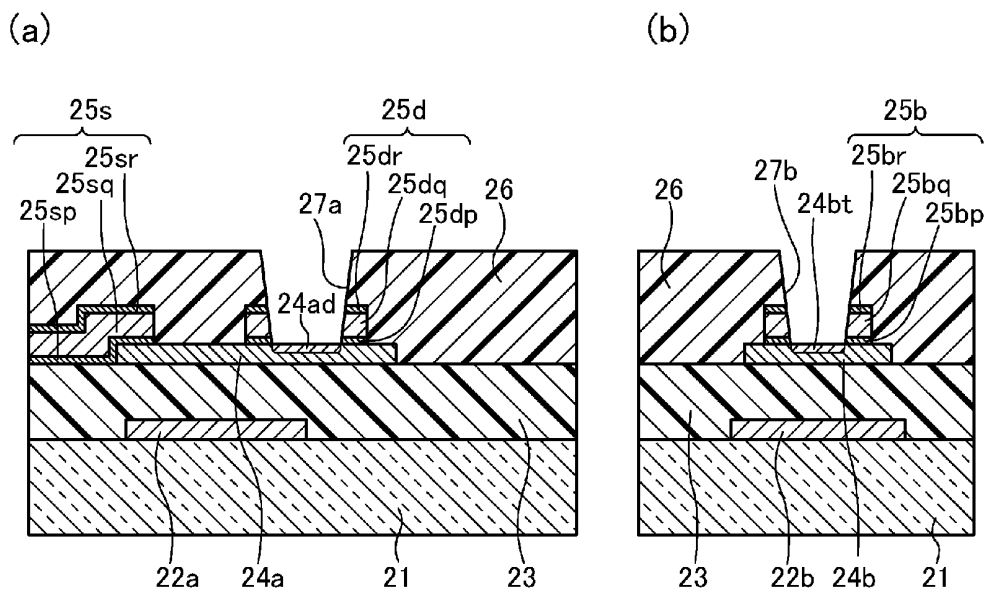
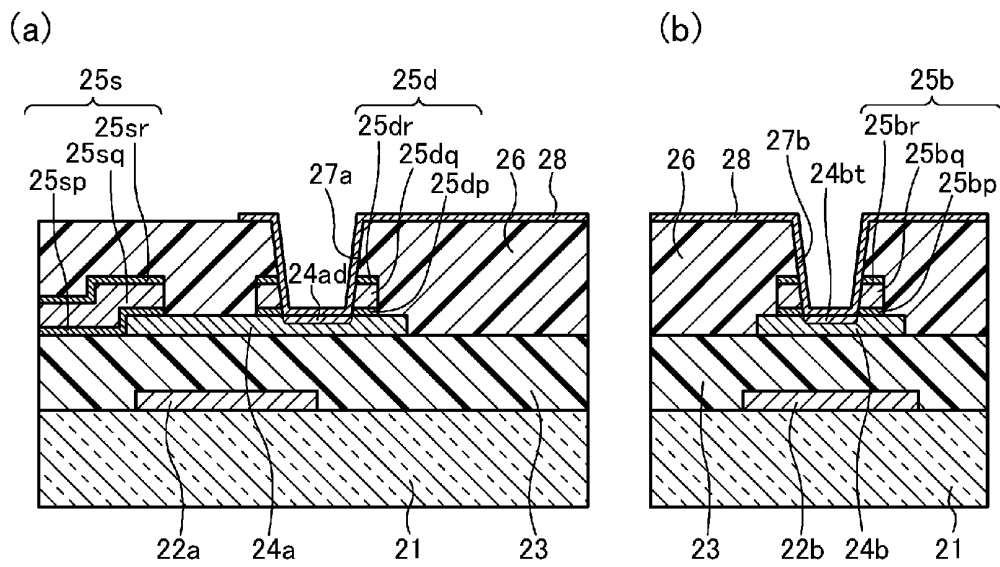


FIG.26



**THIN FILM TRANSISTOR SUBSTRATE AND
LIQUID CRYSTAL DISPLAY DEVICE
PROVIDED WITH SAME**

TECHNICAL FIELD

[0001] The present invention relates to thin film transistors and to liquid crystal display devices including the thin film transistors, and specifically to a thin film transistor substrate including a thin film transistor having a semiconductor layer made of an oxide semiconductor, and to a liquid crystal display device.

BACKGROUND ART

[0002] In thin film transistor substrates included in liquid crystal display devices, thin film transistors (hereinafter also referred to as "TFTs") are used as switching elements of pixels each of which is the smallest unit of an image. Conventionally, TFTs whose semiconductor layers are made of amorphous silicon have been used. However, in recent years, instead of the TFTs including the semiconductor layers made of amorphous silicon, TFTs including oxide semiconductor films as semiconductor layers have been proposed. The TFTs including the oxide semiconductor films as the semiconductor layers exhibit satisfactory characteristics such as high mobility, high reliability, and a low off current, and thus have been actively researched and developed.

[0003] A TFT having a bottom gate structure generally includes a gate electrode provided on a glass substrate, a gate insulating film provided to cover the gate electrode, a semiconductor layer provided on the gate insulating film to overlap the gate electrode, and a source electrode included in a source section and a drain electrode included in a drain section which are provided on the gate insulating film to be spaced apart from each other and to overlap the semiconductor layer, wherein a channel section is formed in a portion of the semiconductor layer exposed between the source electrode and the drain electrode. The TFT is covered with an interlayer insulating film provided on the source electrode and the drain electrode. A contact hole extending to the drain electrode is formed in the interlayer insulating film, and an inner surface of the contact hole is covered with a pixel electrode made of a transparent conductive film, thereby electrically connecting the pixel electrode to the drain electrode.

[0004] Here, the drain electrode generally has a configuration in which a plurality of metal thin films are stacked. An example of a layered structure of the drain electrode includes a configuration in which a first conductive film made of a titanium film, a second conductive film made of an aluminum film, and a third conductive film made of a molybdenum nitride film are sequentially stacked on the gate insulating film.

[0005] In etching to form the contact hole, the contact hole is formed to extend from a surface of the interlayer insulating film to the drain electrode. The etching is performed, for example, by dry etching using a fluorine-based gas as an etching gas. Here, when the contact hole is extended to the drain electrode by the etching gas, and the contact hole passes through the third conductive film, the second conductive film (the aluminum film) is exposed in the contact hole.

[0006] When the aluminum film exposed in the contact hole is brought into contact with the etching gas, an aluminum fluoride film is formed on a surface of the aluminum film. Then, oxygen ashing is performed after the dry etching,

thereby a surface of the aluminum fluoride film is oxidized, which results in that the surface of the aluminum film is covered with an aluminum oxide film containing fluorine (that is, a passivation coating).

[0007] Thus, when an ITO film, or the like is provided as the pixel electrode on the inner surface of the contact hole, the ITO film is brought into contact with the drain electrode, but part of the drain electrode which will be brought into contact with the pixel electrode is covered with the passivation coating, and thus defective conduction is caused, which may lead to quality degradation.

[0008] Patent Document 1 discloses that a channel section, a source section, and a drain section of a thin film transistor as well as a pixel electrode, and connection terminal sections at ends of a gate signal line and a source signal line are made of an identical oxide semiconductor film, all layer structures of a thin film transistor array are formed, an opening is formed at a desired location in an uppermost protective insulating film, and a plasma treatment is performed via the opening, thereby simultaneously reducing the resistance of the connection terminal sections, the source section, the drain section, and the pixel electrode to obtain the thin film transistor array.

CITATION LIST

Patent Document

[0009] PATENT DOCUMENT 1: Japanese Patent Publication No. 2008-40343

SUMMARY OF THE INVENTION

Technical Problem

[0010] However, when a thin film transistor array is formed by the method disclosed in Patent Document 1, the resistance of the entirety of the oxide semiconductor film has to be reduced, and thus the plasma treatment takes time. Moreover, the channel section is also influenced by the reduction in resistance, which causes problems such as leakage between the source and the drain, a high threshold value, etc. Moreover, the oxide semiconductor film cannot be satisfactorily protected, so that long-term reliability of the thin film transistor array may be insufficient. Moreover, since the pixel electrode is made of the oxide semiconductor film whose resistance is reduced, the resistance is high compared to the case where the pixel electrode is a transparent electrode made of an ITO film, an IZO film, or the like, so that a satisfactory display quality cannot be obtained.

[0011] It is an objective of the present invention to provide a thin film transistor substrate in which satisfactory contact is achieved between a drain section and a pixel electrode.

Solution to the Problem

[0012] A thin film transistor substrate of the present invention includes: a substrate; a thin film transistor including a gate electrode provided on the substrate, a gate insulating film provided to cover the gate electrode, an oxide semiconductor film provided on the gate insulating film and including a channel section formed at a position facing the gate electrode, and a source section and a drain section provided to be spaced apart from each other with the channel section sandwiched therebetween; a protective film which is provided to cover the thin film transistor and in which a pixel contact hole extending to the drain section is formed; and a pixel electrode

provided on the protective film and electrically connected to the drain section via the pixel contact hole, wherein the source section is made of a source metal provided above the gate insulating film and the oxide semiconductor film, and the drain section is a low resistance portion which is part of the oxide semiconductor film, where the part includes a surface of the oxide semiconductor film opposite to the gate insulating film, and resistance of the part is reduced.

[0013] With this configuration, the drain section is a low resistance portion which is part of the oxide semiconductor film, where the part includes a surface of the oxide semiconductor film opposite to the gate insulating film, and the resistance of the part is reduced. Thus, there is no possibility that a contact failure occurs between pixel electrode provided on the inner surface of the pixel contact hole and the drain section.

[0014] In the thin film transistor substrate of the present invention, the low resistance portion which is the drain section preferably has a thickness of less than or equal to $\frac{1}{2}$ of a thickness of the oxide semiconductor film.

[0015] The thin film transistor substrate of the present invention may further include: an interlayer insulating film provided above the gate insulating film and the oxide semiconductor film and under the protective film, wherein the source metal included in the source section is formed above the interlayer insulating film, a source contact hole extending from a surface of the interlayer insulating film to the oxide semiconductor film is formed in the interlayer insulating film, and the source metal is formed on an inner surface of the source contact hole to electrically connect the source metal to the oxide semiconductor film, and part of the oxide semiconductor film is a low resistance portion whose resistance is reduced, where the part includes a surface of the oxide semiconductor film which is in contact with the source metal.

[0016] The thin film transistor substrate of the present invention is preferably used when the source metal includes a first conductive film, and a second conductive film made of aluminum, and the first conductive film and the second conductive film are sequentially stacked on the gate insulating film.

[0017] In this case, the first conductive film may be made of a refractory metal film. Examples of the refractory metal film include: metal films such as a titanium (Ti) film, a molybdenum (Mo) film, a tantalum (Ta) film, a tungsten (W) film, a chromium (Cr) film, and a nickel (Ni) film; metal films made of nitride of these metals, alloys of these metals, etc.

[0018] In the thin film transistor substrate of the invention, the source metal further may include a third conductive film stacked on a surface of the second conductive film opposite to the first conductive film.

[0019] The thin film transistor substrate is preferably used in a liquid crystal display device, including: the thin film transistor substrate; a counter substrate arranged to face the thin film transistor substrate; and a liquid crystal layer provided between the thin film transistor substrate and the counter substrate.

Advantages of the Invention

[0020] According to the present invention, the drain section is a low resistance portion which is part of the oxide semiconductor film, where the part includes a surface of the oxide semiconductor film opposite to the gate insulating film, and the resistance of the part is reduced. Thus, there is no possi-

bility that a contact failure occurs between the pixel electrode provided on an inner surface of the pixel contact hole and the drain section.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] FIG. 1 is a plan view schematically illustrating a liquid crystal display device.

[0022] FIG. 2 is a cross-sectional view along the line II-II of FIG. 1.

[0023] FIG. 3 is a plan view illustrating a substantial portion of the thin film transistor substrate according to the first embodiment in an enlarged manner.

[0024] FIG. 4 is a cross-sectional view along the line A-A of FIG. 3.

[0025] FIG. 5 is a cross-sectional view along the line B-B of FIG. 3.

[0026] FIG. 6 is a cross-sectional view along the line C-C of FIG. 3.

[0027] FIGS. 7A-7C are views illustrating a method for fabricating the thin film transistor substrate of the first embodiment, wherein FIG. 7A is a cross-sectional view along the line A-A of FIG. 3, FIG. 7B is a cross-sectional view along the line B-B of FIG. 3, and FIG. 7C is a cross-sectional view along the line C-C of FIG. 3.

[0028] FIGS. 8A-8C are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 7A-7C.

[0029] FIGS. 9A-9C are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 8A-8C.

[0030] FIGS. 10A-10C are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 9A-9C.

[0031] FIGS. 11A-11C are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 10A-10C.

[0032] FIG. 12 is a plan view illustrating a substantial portion of a thin film transistor substrate according to a second embodiment in an enlarged manner.

[0033] FIG. 13 is a cross-sectional view along the line A-A of FIG. 12.

[0034] FIG. 14 is a cross-sectional view along the line B-B of FIG. 12.

[0035] FIG. 15 is a cross-sectional view along the line C-C of FIG. 12.

[0036] FIGS. 16A-16C are views illustrating a method for fabricating the thin film transistor substrate of the second embodiment, wherein FIG. 16A is a cross-sectional view along the line A-A of FIG. 12, FIG. 16B is a cross-sectional view along the line B-B of FIG. 12, and FIG. 16C is a cross-sectional view along the line C-C of FIG. 12.

[0037] FIGS. 17A-17C are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 16A-16C.

[0038] FIGS. 18A-18C are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 17A-17C.

[0039] FIGS. 19A-19C are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 18A-18C.

[0040] FIGS. 20A-20C are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 19A-19C.

[0041] FIG. 21 is a plan view illustrating a substantial portion of a thin film transistor substrate according to a third embodiment in an enlarged manner.

[0042] FIG. 22 is a cross-sectional view along the line A-A of FIG. 21.

[0043] FIG. 23 is a cross-sectional view along the line B-B of FIG. 21.

[0044] FIGS. 24A, 24B are views illustrating a method for fabricating the thin film transistor substrate of the third embodiment, wherein FIG. 24A is a cross-sectional view along the line A-A of FIG. 21, and FIG. 24B is a cross-sectional view along the line B-B of FIG. 21.

[0045] FIGS. 25A, 25B are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 24A, 24B.

[0046] FIGS. 26A, 26B are views illustrating a process step in the method for fabricating the thin film transistor substrate following the process step of FIGS. 25A, 25B.

DESCRIPTION OF EMBODIMENTS

[0047] Embodiments of the present invention will be described in detail below with reference to the drawings. The following embodiments are not intended to limit the present invention. In the embodiments, the same reference numerals are used to represent equivalent elements.

First Embodiment

[0048] <Configuration of Liquid Crystal Display Device>

[0049] FIGS. 1 and 2 illustrate a liquid crystal display device 10 according to a first embodiment. The liquid crystal display device 10 includes a TFT substrate 20 and a counter substrate 30 which are arranged to face each other. The substrates 20 and 30 are adhered to each other by a sealing material 40 provided to have a frame-like shape at outer peripheral parts of the substrates 20 and 30. In the space surrounded by the sealing material 40 between the substrates 20 and 30, a liquid crystal layer 50 is provided as a display layer. The liquid crystal display device 10 has a display region D which is surrounded by the sealing material 40 and in which a plurality of pixels are arranged in a matrix pattern. A region by which the display region D is surrounded is a picture-frame region.

[0050] (TFT Substrate)

[0051] FIGS. 3-6 illustrate the TFT substrate 20 of the first embodiment. FIG. 3 is a plan view illustrating the TFT substrate 20. The TFT substrate 20 is formed by stacking, on a substrate 21 made of, for example, a glass substrate, a first metal of which a gate electrode 22a, a lower electrode 22b, a terminal 22c, a gate line 22gb, transfer pads (not shown), etc. are made; a gate insulating film 23 made of SiO₂, a multilayer structure of SiO₂ and SiN, or the like; oxide semiconductor films 24a, 24b made of an IGZO film, or the like; a second metal of which a source metal 25s, a source line 25sb, etc. forming a source section are made; a protective film 26 made of SiO₂, SiN, a transparent insulating resin, or the like; a pixel electrode 28 made of an indium tin oxide (ITO) film, or the like; and an alignment layer (not shown) made of a polyimide film, or the like.

[0052] The TFT substrate 20 is formed such that part of the picture-frame region of the TFT substrate 20 protrudes beyond the counter substrate 30, thereby forming a terminal region to which external connection terminals (not shown) of

mounted components, etc. are attached. In the picture-frame region, the transfer pads (not shown) via which a common potential is applied to a common electrode of the counter substrate 30 are formed, and each transfer pad is connected to a transfer bus line (not shown) arranged in the terminal region.

[0053] Note that a polarizing plate (not shown) is provided on a surface of the TFT substrate 20 opposite to the liquid crystal layer 50.

[0054] FIG. 4 is a cross-sectional view along the line A-A of FIG. 3.

[0055] As illustrated in FIG. 4, the gate electrode 22a is covered with the gate insulating film 23, and on the gate insulating film 23, the oxide semiconductor film 24a including a channel section 24ac formed at a position facing the gate electrode 22a is provided, and on the oxide semiconductor film 24a, a source section S and a drain section DR are provided to be spaced apart from each other with the channel section 24ac sandwiched therebetween. These components are included in a thin film transistor T_R.

[0056] The gate electrode 22a is made of the first metal, and includes for example, an aluminum film, a titanium film, and a titanium nitride film which are sequentially stacked from bottom to top.

[0057] The source section S is made of the source metal 25s (the second metal) provided above the gate insulating film 23 and the oxide semiconductor film 24a.

[0058] The source metal 25s includes a first conductive film 25sp, a second conductive film 25sq, and a third conductive film 25sr which are sequentially stacked. The first conductive film 25sp is made of, for example, a titanium (Ti) film, and has a thickness of, for example, 50 nm. The second conductive film 25sq is made of, for example, an aluminum film, and has a thickness of, for example, 100 nm. The third conductive film 25sr is made of, for example, a refractory metal film such as a molybdenum nitride (MoN) film, and has a thickness of, for example, 150 nm.

[0059] The drain section DR is a low resistance portion 24ad. The low resistance portion 24ad is a portion including part of the oxide semiconductor film 24a which is exposed in a pixel contact hole 27a, and the resistance of the portion is reduced.

[0060] The low resistance portion 24ad is the portion including the part of the oxide semiconductor film 24a which is exposed in the pixel contact hole 27a, and the resistance of the portion is reduced, and thus the portion has high conductivity leading to a resistivity of about 1/1000000000 to 1/100 of the resistivity of the channel section 24ac. The low resistance portion 24ad includes a surface of the oxide semiconductor film 24a, and preferably has a thickness of less than or equal to 1/2 of the thickness of the oxide semiconductor film 24a. The resistance value of the low resistance portion 24ad is not uniform, but for example, the resistance gradually increases from the surface of the oxide semiconductor film 24a toward the gate insulating film 23. Moreover, in FIG. 4, the low resistance portion 24ad is illustrated as a discrete portion defined by a line frame for convenience, but the low resistance portion 24ad is not necessarily a discrete portion as long as it is a portion of a region integrated with the oxide semiconductor film 24a.

[0061] The pixel contact hole 27a is formed in the protective film 26, and extends from a surface of the protective film 26 to the low resistance portion 24ad of the oxide semiconductor film 24a. An inner surface of the pixel contact hole 27a

is covered with the pixel electrode 28, and the pixel electrode 28 is electrically connected to the low resistance portion 24ad which is the drain section DR.

[0062] FIG. 5 is a cross-sectional view along the line B-B of FIG. 3.

[0063] As illustrated in FIG. 5, the lower electrode 22b is covered with the gate insulating film 23, and on the gate insulating film 23, an etch stopper layer 24b made of an oxide semiconductor is provided at a position facing the lower electrode 22b. In the protective film 26 covering the etch stopper layer 24b, an auxiliary capacitor contact hole 27b extending to the etch stopper layer 24b is formed. A low resistance portion 24bt is formed by reducing the resistance of a portion including part of the etch stopper layer 24b which is exposed in the auxiliary capacitor contact hole 27b compared to the resistance of the other portions. These components are included in an auxiliary capacitor element Cs.

[0064] The lower electrode 22b is made of the first metal, and includes, for example, an aluminum film, a titanium film, and a titanium nitride film which are sequentially stacked from bottom to top. Note that the lower electrode 22b is connected to an auxiliary capacitor terminal T_{Cs} provided in the terminal region.

[0065] An inner surface of the auxiliary capacitor contact hole 27b formed in the protective film 26 is covered with the pixel electrode 28, and the pixel electrode 28 is in contact with and electrically connected to the low resistance portion 24bt provided in the etch stopper layer 24b.

[0066] FIG. 6 is a cross-sectional view along the line C-C of FIG. 3.

[0067] As illustrated in FIG. 6, the terminal 22c is covered with the gate insulating film 23 and the protective film 26. The terminal 22c is made of the first metal, and includes, for example, an aluminum film, a titanium film, and a titanium nitride film which are sequentially stacked from bottom to top.

[0068] A contact hole 27c is formed in the gate insulating film 23 and the protective film 26 to extend from the surface of the protective film 26 to the terminal 22c. An inner surface of the contact hole 27c is covered with the pixel electrode 28, and the pixel electrode 28 is electrically connected to the terminal 22c, thereby forming a gate terminal section T_G .

[0069] Note that FIG. 6 illustrates a cross section of the gate terminal section T_G , but a source terminal section T_s also has a similar cross-sectional structure.

[0070] (Counter Substrate)

[0071] Although not illustrated, on a surface of a substrate body of the counter substrate 30, each of colored layers including red, green, and blue layers 22R, 22G, 22B are provided to a different pixel in the display region D. Moreover, the common electrode, which has a thickness of, for example, 100 nm, and is made of ITO, or the like, is provided above the colored layers 22R, 22G, 22B. Further, an alignment layer is formed to cover the common electrode. The colored layers described above include three types of layers, that is, the red, green, and blue layers. However, the colored layers are not limited to these layers, but may include, for example, four types of layers: red, green, blue, and yellow layers.

[0072] Note that a polarizing plate (not shown) is provided on a surface of the counter substrate 30 opposite to the liquid crystal layer 50.

[0073] (Sealing Material)

[0074] At the outer peripheral parts of the TFT substrate 20 and the counter substrate 30, the sealing material 40 is provided to have the shape of a ring along the picture-frame region. The TFT substrate 20 and the counter substrate 30 are adhered to each other by the sealing material 40.

[0075] The sealing material 40 is obtained by curing a starting material of the sealing material by heating or by ultraviolet irradiation, where the starting material contains an adhesive of a thermosetting resin, an ultraviolet curable resin, etc. having flowability (e.g., an acryl-based resin and an epoxy-based resin) as a main component. The sealing material 40 includes, for example, conductive beads mixed therewith, and serves as a medium by which the common electrode is electrically connected to the transfer pads.

[0076] (Liquid Crystal Layer)

[0077] The liquid crystal layer 50 is made of, for example, a nematic liquid crystal material having electro-optic characteristics.

[0078] The liquid crystal display device 10 having the above-described configuration is configured such that each of pixel electrodes forms a pixel, and in each pixel, when the thin film transistor T_R is turned on by a gate signal sent via the gate line 22gb, a source signal is sent via the source line 25sb, so that a predetermined charge is applied to the pixel electrode 28 via the source section S (the source metal 25s) and the drain section DR (the low resistance portion 24ad), which causes a potential difference between the pixel electrode 28 and the common electrode of the counter substrate 30, thereby applying a predetermined voltage to a liquid crystal capacitor including the liquid crystal layer 50. The liquid crystal display device 10 displays an image by adjusting transmittance of light coming from the outside, based on the phenomenon that the alignment of liquid crystal molecules changes according to the magnitude of the applied voltage.

[0079] In the above description, the second metal, of which the source metal 25s, and the like of the TFT substrate 20 is made, has a configuration in which the first conductive film 25sp, the second conductive film 25sq, and the third conductive film 25sr are sequentially stacked. However, a configuration which does not include the third conductive film 25sr (that is, a configuration in which two layers, the first conductive film 25sp and the second conductive film 25sq are stacked) may be possible, or other configurations may be possible.

[0080] Moreover, in the above description, the second conductive film 25sq of the second metal, of which the source metal 25s, and the like of the TFT substrate 20 is made, is an aluminum film. However, a film made of an aluminum alloy, a film made of copper (Cu) or made of a copper alloy, etc. may be used.

[0081] <Method for Fabricating TFT Substrate>

[0082] With reference to FIGS. 7-11, a method for fabricating the TFT substrate 20 of the present embodiment will be described below.

[0083] (Formation of First Metal, Gate Insulating Film, Oxide Semiconductor Film)

[0084] First, as illustrated in FIGS. 7A-7C, a first metal is provided on a substrate 21 to form a gate electrode 22a, a lower electrode 22b, a terminal 22c, a gate line 22gb (see FIG. 3), transfer pads (not shown), etc. Specifically, an aluminum film, a titanium film, and a titanium nitride film are successively formed by, for example, sputtering. Thereafter, a resist pattern is left on portions which will be the gate electrode 22a,

the lower electrode **22b**, the terminal **22c**, etc. by using photolithography. Then, a multilayer structure which is a conductive film composed of the aluminum film, the titanium film, and the titanium nitride film is etched by, for example, dry etching (RIE) using a chlorine-based gas. After that, the resist is removed by a resist remover solution.

[0085] Next, as a gate insulating film **23**, a SiO₂ film is formed by, for example, CVD.

[0086] Next, an oxide semiconductor film **24a** and an etch stopper layer **24b** are formed. Specifically, an oxide semiconductor film such as an IGZO film is formed by, for example, sputtering, and then a resist pattern is left by photolithography on portions which will be the oxide semiconductor film **24a** and the etch stopper layer **24b**. Then, the IGZO film is etched by, for example, wet etching using an oxalic acid solution as an etchant. After that, the resist is removed by a resist remover solution.

[0087] (Formation of Second Metal)

[0088] Subsequently, as illustrated in FIGS. **8A-8C**, a source metal **25s** is formed. Specifically, a titanium film (having a thickness of about 50 nm) which will be a first conductive film **25sp**, an aluminum film (having a thickness of about 150 nm) which will be a second conductive film **25sq**, and a molybdenum nitride film (having a thickness of about 100 nm) which will be a third conductive film **25sr** are successively formed by, for example, sputtering. Then, a resist pattern is left by photolithography on a portion which will be the source metal **25s**. Then, the second conductive film and the third conductive film are etched by, for example, wet etching using a mixed acid solution of phosphoric acid/acetic acid/nitric acid as an etchant. Further, the titanium film which is the first conductive film is etched by dry etching (RIE) using a chlorine-based gas. Thereafter, the resist is removed by a resist remover solution.

[0089] (Formation of Protective Film•Contact Hole)

[0090] Next, as illustrated in FIGS. **9A-9C**, a SiO₂ film is formed as a protective film **26** by, for example, CVD. Then, the protective film **26** is dry etched, thereby forming a pixel contact hole **27a**, an auxiliary capacitor contact hole **27b**, and a contact hole **27c**. Specifically, first, a photosensitive resist is applied to the protective film **26**. Then, the resist is left by photolithography on portions except portions which will be the contact holes **27a-27c**. Then, the protective film **26** is etched by, for example, dry etching (RIE), thereby forming the contact holes **27a-27c**. Here, the oxide semiconductor film **24a**, the etch stopper layer **24b**, and the terminal **22c** serve as an etch stopper.

[0091] (Process of Reducing Resistance)

[0092] Subsequently, as illustrated in FIGS. **10A, 10B**, a process of reducing resistance is performed on parts of the oxide semiconductor film **24a** and the etch stopper layer **24b** which are respectively exposed in the pixel contact hole **27a** and the auxiliary capacitor contact hole **27b** to reduce the resistance of portions including the exposed parts of the oxide semiconductor film **24a** and the etch stopper layer **24b**, thereby forming low resistance portions **24ad, 24bt**. Examples of the process of reducing resistance include plasma treatment, vacuum annealing, etc. For example, when the process of reducing resistance is performed by plasma treatment, the plasma treatment is preferably performed under plasma treatment conditions that, for example, the hydrogen gas flow rate is 2000 sccm, the pressure is 200 Pa, the RF electric power is 1000 W, the temperature is 250° C., and the processing time is longer than or equal to 30 sec. Here,

other than a hydrogen gas, a NH₃ gas, a SiH₄ gas, etc. may be used. Alternatively, for example, the plasma treatment may be performed under plasma treatment conditions that the CF₄ gas flow rate is 270 sccm, the O₂ gas flow rate is 30 sccm, the pressure is 7 Pa, the RF electric power is 1000 W, and the processing time is longer than or equal to 30 sec. Alternatively, for example, the plasma treatment may be performed under plasma treatment conditions that the SF₆ gas flow rate is 200 sccm, the O₂ gas flow rate is 200 sccm, the pressure is 8 Pa, the RF electric power is 600 W, the processing time is longer than or equal to 30 sec. Alternatively, for example, the plasma treatment is preferably performed under conditions that the Cl₂ gas flow rate is 80 sccm, the BCl₃ gas flow rate is 120 sccm, the pressure is 4 Pa, the RF electric power is 1000 W, and the processing time is longer than or equal to 30 sec. Alternatively, when the process of reducing resistance is performed by vacuum annealing, the vacuum annealing is preferably performed under vacuum annealing conditions that the temperature is higher than or equal to 250° C., the pressure is lower than or equal to 500 Pa, and the processing time is longer than or equal to 1 minute. With this process of reducing resistance, a portion having a thickness of less than or equal to ½ of the thickness of the oxide semiconductor film **24a** is formed into the low resistance portion **24ad** having a resistance lower than that of the oxide semiconductor film **24a**. Moreover, a portion having a thickness of less than or equal to ½ of the thickness of the etch stopper layer **24b** is formed into the low resistance portion **24bt** having a resistance lower than that of the etch stopper layer **24b**. The low resistance portion **24ad** formed by reducing the resistance of part of the oxide semiconductor film **24a** serves as a drain section DR. Moreover, the low resistance portion **24bt** formed by reducing the resistance of part of the etch stopper layer **24b** serves as an upper electrode portion of an auxiliary capacitor element Cs. **[0093]** Note that in a gate terminal section T_G, as illustrated in FIG. **11C**, the process of reducing resistance is not performed on the contact hole **27c**.

[0094] (Formation of Pixel Electrode)

[0095] Finally, as illustrated in FIGS. **11A-11C**, a pixel electrode **28** is formed. Specifically, first, an ITO film is formed by, for example, sputtering. Then, a resist pattern is left on a portion which will be the pixel electrode **28** by photolithography. Then, the ITO film is etched by using, for example, an oxalic acid solution as an etchant to remove the resist by a resist remover solution, thereby forming the pixel electrode **28**.

[0096] As described above, the TFT substrate **20** is fabricated. The TFT substrate **20** fabricated by the above-described method and the counter substrate **30** including pixels each provided with a color filter are arranged to face each other and are adhered to each other by the sealing material **40**, and a liquid crystal material is filled between the substrates, thereby forming the liquid crystal layer **50**, so that the liquid crystal display device **10** can be obtained.

[0097] (Advantages of First Embodiment)

[0098] The thin film transistor T_R of the present embodiment has the above-described configuration, and thus the pixel electrode **28** is directly in contact with and is electrically connected to the drain section DR, which can reduce the occurrence of a contact failure between the pixel electrode **28** and the drain section DR. In particular, when the second metal is formed to have a multilayer structure composed of a first conductive film and a second conductive film, and the second conductive film is an aluminum film, if the drain section DR

is made of a drain metal, the aluminum film serving as the second conductive film is oxidized in forming the pixel contact hole 27a, and a surface of the aluminum film is covered with a passivation coating, which may cause a contact failure between the drain metal and the pixel electrode 28 provided on a surface of the pixel contact hole 27a. However, the drain section DR is made of the low resistance portion 24ad obtained by reducing the resistance of part of the oxide semiconductor film 24a. Thus, there is no possibility that the problem as described above arises, and satisfactory contact can be achieved.

Second Embodiment

[0099] <Configuration of Liquid Crystal Display Device>

[0100] Similar to the first embodiment, a liquid crystal display device 10 according to a second embodiment includes a TFT substrate 20 and a counter substrate 30 which are arranged to face each other. The substrates 20 and 30 are adhered to each other by a sealing material 40 provided to have a frame-like shape at outer peripheral parts of the substrates 20 and 30. In the space surrounded by the sealing material 40 between the substrates 20 and 30, a liquid crystal layer 50 is provided as a display layer. The liquid crystal display device 10 has a display region D which is surrounded by the sealing material 40 and in which a plurality of pixels are arranged in a matrix pattern. A region by which the display region D is surrounded is a picture-frame region. The configurations, etc. of the counter substrate 30, the sealing material 40, and the liquid crystal layer 50 are the same as those of the first embodiment, and thus the description thereof is omitted.

[0101] (TFT Substrate)

[0102] FIGS. 12-15 illustrate the TFT substrate 20 of the second embodiment. FIG. 12 is a plan view illustrating the TFT substrate 20. The TFT substrate 20 is formed by stacking, on a substrate 21, a first metal (of which a gate electrode 22a, a lower electrode 22b, a terminal 22c, a gate line 22gb, and transfer pads (not shown) are made), a gate insulating film 23, oxide semiconductor films 24a, 24b, an interlayer insulating film 26A, a second metal (of which a source metal 25s and a source line 25sb are made), a protective film 26B, a pixel electrode 28, and an alignment layer (not shown).

[0103] FIG. 13 is a cross-sectional view along the line A-A of FIG. 12.

[0104] As illustrated in FIG. 13, the gate electrode 22a is covered with the gate insulating film 23, and on the gate insulating film 23, the oxide semiconductor film 24a including a channel section 24ac formed at a position facing the gate electrode 22a is provided, and on the oxide semiconductor film 24a, a source section S and a drain section DR are provided to be spaced apart from each other with the channel section 24ac sandwiched therebetween.

[0105] The gate electrode 22a is made of the first metal, and includes, for example, an aluminum film, a titanium film, and a titanium nitride film which are sequentially stacked from bottom to top.

[0106] The source section S includes a low resistance portion 24as obtained by reducing the resistance of a portion including part of the oxide semiconductor film 24a which is exposed in a source contact hole 27as, and the source metal 25s provided above the gate insulating film 23, the oxide semiconductor film 24a, and the interlayer insulating film 26A.

[0107] The low resistance portion 24as is a portion including the part of the oxide semiconductor film 24a which is exposed in the source contact hole 27as, and the resistance of the portion is reduced, and thus the portion has high conductivity leading to a resistivity of about $1/1000000000$ to $1/100$ of the resistivity of the channel section 24ac. The low resistance portion 24as includes a surface of the oxide semiconductor film 24a, and preferably has a thickness of less than or equal to $1/2$ of the thickness of the oxide semiconductor film 24a. The resistance value of the low resistance portion 24as is not uniform, but for example, the resistance gradually increases from the surface of the oxide semiconductor film 24a toward the gate insulating film 23. Moreover, in FIG. 13, the low resistance portion 24as is illustrated as a discrete portion defined by a line frame for convenience, but the low resistance portion 24as is not necessarily a discrete portion as long as it is a portion of a region integrated with the oxide semiconductor film 24a.

[0108] The source metal 25s is made of the second metal, and includes, similar to the first embodiment, for example, a first conductive film 25sp, a second conductive film 25sq, and a third conductive film 25sr which are sequentially stacked.

[0109] The drain section DR is a low resistance portion 24a. The low resistance portion 24a is a portion including part of the oxide semiconductor film 24a which is exposed in a pixel contact hole 27ad, and the resistance of the portion is reduced.

[0110] The low resistance portion 24ad is the portion including the part of the oxide semiconductor film 24a which is exposed in the pixel contact hole 27ad, and the resistance of the portion is reduced, and thus the portion has high conductivity leading to a resistivity of about $1/1000000000$ to $1/100$ of the resistivity of the channel section 24ac. The low resistance portion 24ad includes a surface of the oxide semiconductor film 24a, and preferably has a thickness of less than or equal to $1/2$ of the thickness of the oxide semiconductor film 24a. The resistance value of the low resistance portion 24ad is not uniform, but for example, the resistance gradually increases from the surface of the oxide semiconductor film 24a toward the gate insulating film 23. Moreover, in FIG. 13, the low resistance portion 24ad is illustrated as a discrete portion defined by a line frame for convenience, but the low resistance portion 24ad is not necessarily a discrete portion as long as it is a portion of a region integrated with the oxide semiconductor film 24a.

[0111] The pixel contact hole 27ad is formed in the interlayer insulating film 26A and the protective film 26B, and extends from a surface of the protective film 26B to the low resistance portion 24ad of the oxide semiconductor film 24a. An inner surface of the pixel contact hole 27ad is covered with the pixel electrode 28, and the pixel electrode 28 is electrically connected to the low resistance portion 24ad which is the drain section DR.

[0112] A thin film transistor T_R of the present embodiment has the above-described configuration, and thus the pixel electrode 28 is directly in contact with and is electrically connected to the drain section DR, which can reduce the occurrence of a contact failure between the pixel electrode 28 and the drain section DR. In particular, when the second metal is formed to have a multilayer structure composed of a first conductive film, a second conductive film, and a third conductive film, and the second conductive film is an aluminum film, if the drain section DR is made of a drain metal, the aluminum film serving as the second conductive film is oxi-

dized in forming the pixel contact hole 27ad, and a surface of the aluminum film is covered with a passivation coating, which may cause a contact failure between the drain metal and the pixel electrode 28 provided on a surface of the pixel contact hole 27ad. However, the drain section DR is made of the low resistance portion 24ad obtained by reducing the resistance of part of the oxide semiconductor film 24a. Thus, there is no possibility that the problem as described above arises, and satisfactory contact can be achieved.

[0113] FIG. 14 is a cross-sectional view along the line B-B of FIG. 12.

[0114] As illustrated in FIG. 14, the lower electrode 22b is covered with the gate insulating film 23, and on the gate insulating film 23, the etch stopper layer 24b made of an oxide semiconductor is provided at a position facing the lower electrode 22b. In the interlayer dielectric film 26A and the protective film 26 covering the etch stopper layer 24b, an auxiliary capacitor contact hole 27b extending to the etch stopper layer 24b is formed. A low resistance portion 24bt is formed by reducing the resistance of a portion including part of the etch stopper layer 24b which is exposed in the auxiliary capacitor contact hole 27b compared to the resistance of the other portions. These components are included in an auxiliary capacitor element Cs.

[0115] The lower electrode 22b is made of the first metal, and has a configuration in which, for example, an aluminum film, a titanium film, and a titanium nitride film are sequentially stacked from bottom to top. Note that the lower electrode 22b is connected to an auxiliary capacitor terminal T_{Cs} provided in the terminal region.

[0116] The auxiliary capacitor contact hole 27b is formed in the interlayer insulating film 26A and the protective film 26B, and extends from the surface of the protective film 26B to the low resistance portion 24bt of the etch stopper layer 24b. An inner surface of the auxiliary capacitor contact hole 27b is covered with the pixel electrode 28, and the pixel electrode 28 is electrically connected to the low resistance portion 24bt.

[0117] FIG. 15 is a cross-sectional view along the line C-C of FIG. 12.

[0118] As illustrated in FIG. 15, the terminal 22c is covered with the gate insulating film 23, the interlayer dielectric film 26A, and the protective film 26B. The terminal 22c is made of the first metal, and has a configuration in which, for example, an aluminum film, a titanium film, and a titanium nitride film are sequentially stacked from bottom to top.

[0119] A contact hole 27c is formed in the gate insulating film 23, the interlayer dielectric film 26A, and the protective film 26B to extend from the surface of the protective film 26 to the terminal 22c. An inner surface of the contact hole 27c is covered with the pixel electrode 28, and the pixel electrode 28 is electrically connected to the terminal 22c, thereby forming a gate terminal section T_G.

[0120] Note that FIG. 15 illustrates a cross section of the gate terminal section T_G, but a source terminal section T_S also has a similar cross-sectional structure.

[0121] The liquid crystal display device 10 having the above-described configuration is configured such that each of pixel electrodes forms a pixel, and in each pixel, when the thin film transistor T_R is turned on by a gate signal sent via the gate line 22gb, a source signal is sent via the source line 25sb, so that a predetermined charge is applied to the pixel electrode 28 via the source section S (the low resistance portion 24as and the source metal 25s) and the drain section DR (the low

resistance portion 24ad), which causes a potential difference between the pixel electrode 28 and the common electrode of the counter substrate 30, thereby applying a predetermined voltage to a liquid crystal capacitor including the liquid crystal layer 50. The liquid crystal display device 10 displays an image by adjusting transmittance of light coming from the outside, based on the phenomenon that the alignment of liquid crystal molecules changes according to the magnitude of the applied voltage.

[0122] In the above description, the second metal, of which the source metal 25s, and the like of the TFT substrate 20 is made, has a configuration in which the first conductive film 25sp, the second conductive film 25sq, and the third conductive film 25sr are sequentially stacked. However, a configuration which does not include the third conductive film 25sr (that is, a configuration in which two layers, the first conductive film 25sp and the second conductive film 25sq are stacked) may be possible, or other configurations may be possible.

[0123] Moreover, in the above description, the second conductive film 25sq of the second metal, of which the source metal 25s, and the like of the TFT substrate 20 is made, is an aluminum film. However, for example, a film made of an aluminum alloy, a film made of copper (Cu) or made of a copper alloy, etc. may be used.

[0124] <Method for Fabricating TFT Substrate>

[0125] With reference to FIGS. 16A-20C, a method for fabricating the TFT substrate 20 of the present embodiment will be described below.

[0126] (Formation of First Metal, Gate Insulating Film, Oxide Semiconductor Film, Interlayer Insulating Film)

[0127] First, as illustrated in FIGS. 16A-16C, a first metal having a multilayer structure composed of an aluminum film, a titanium film, and a titanium nitride film is provided on a substrate 21 to form a gate electrode 22a, a lower electrode 22b, a terminal 22c, etc.

[0128] Next, as a gate insulating film 23, a SiO₂ film is formed by, for example, CVD.

[0129] Next, an oxide semiconductor film 24a and an etch stopper layer 24b are formed. Specifically, an oxide semiconductor film such as an IGZO film is formed by, for example, sputtering, and then a resist pattern is left by photolithography on portions which will be the oxide semiconductor film 24a and the etch stopper layer 24b. Then, the IGZO film is etched by, for example, wet etching using an oxalic acid solution as an etchant. After that, the resist is removed by a resist remover solution.

[0130] Moreover, above the gate insulating film 23, a SiO₂ film is formed as an interlayer insulating film 26A to cover the oxide semiconductor film 24a and the etch stopper layer 24b by, for example, CVD.

[0131] (Formation of Contact Hole•First Process of Reducing Resistance)

[0132] Subsequently, as illustrated in FIG. 17A, the interlayer insulating film 26A is dry etched, thereby forming a source contact hole 27as extending to the oxide semiconductor film 24a. A process of reducing resistance is performed on part of the oxide semiconductor film 24a which is exposed in the source contact hole 27as to reduce the resistance of the exposed part of the oxide semiconductor film 24a, thereby forming a low resistance portion 24as. The process of reducing resistance can be performed by the same methods as listed in the first embodiment. With this process of reducing resistance, a portion having a thickness of less than or equal to 1/2

of the thickness of the oxide semiconductor film **24a** is formed into a low resistance portion **24ad** having a resistance lower than that of the oxide semiconductor film **24a**. The low resistance portion **24as** obtained by reducing the resistance of part of the oxide semiconductor film **24a** serves as a source section S.

[0133] Note that as illustrated in FIGS. 17B, 17C, here, no contact hole is formed in regions which will be an auxiliary capacitor element and a gate terminal section T_G .

[0134] (Formation of Second Metal)

[0135] Subsequently, as illustrated in FIG. 18A, a source metal **25s** is formed to cover an inner surface of the source contact hole **27as**. The source metal **25s** can be formed, in a manner similar to that of the first embodiment. For example, a titanium film (having a thickness of about 50 nm) which will be a first conductive film **25sp**, an aluminum film (having a thickness of about 150 nm) which will be a second conductive film **25sq**, and a molybdenum nitride film (having a thickness of about 100 nm) which will be a third conductive film **25sr** are successively formed by, for example, sputtering. Then, a resist pattern is left by, for example, photolithography on a portion which includes the source metal **25s**. After that, the second conductive film and the third conductive film are etched by, for example, wet etching using a mixed acid solution of phosphoric acid/acetic acid/nitric acid as an etchant. Further, the titanium film which is the first conductive film is etched by dry etching (RIE) using a chlorine-based gas. Thereafter, the resist is removed by a resist remover solution, thereby forming the source metal **25s**.

[0136] Note that a source line **25sb**, and the like made of a second metal are formed simultaneously with the formation of the source metal **25s**. As illustrated in FIGS. 18B, 18C, the second metal is not formed in regions which will be an auxiliary capacitor element Cs and the gate terminal section T_G .

[0137] (Formation of Protective Film, Contact Hole•Second Process of Reducing Resistance)

[0138] Next, as illustrated in FIGS. 19A-19C, a SiO_2 film is formed as a protective film **26B** by, for example, CVD. Then, the protective film **26B** and the interlayer insulating film **26A** are simultaneously dry etched, thereby forming a pixel contact hole **27ad**, an auxiliary capacitor contact hole **27b**, and a contact hole **27c**. As illustrated in FIGS. 19A, 19B, a process of reducing resistance is performed on parts of the oxide semiconductor film **24a** and the etch stopper layer **24b** which are respectively exposed in the pixel contact hole **27ad** and the auxiliary capacitor contact hole **27b** to reduce the resistance of portions including the exposed parts of the oxide semiconductor film **24a** and the etch stopper layer **24b**, thereby forming low resistance portions **24ad**, **24bt**. With this process of reducing resistance, a portion having a thickness of less than or equal to $\frac{1}{2}$ of the thickness of the oxide semiconductor film **24a** is formed into the low resistance portion **24ad** having a resistance lower than that of the oxide semiconductor film **24a**. Moreover, a portion having a thickness of less than or equal to $\frac{1}{2}$ of the thickness of the etch stopper layer **24b** is formed into the low resistance portion **24bt** having a resistance lower than that of the etch stopper layer **24b**. The low resistance portion **24ad** formed by reducing the resistance of part of the oxide semiconductor film **24a** serves as a drain section DR. Moreover, the low resistance portion **24bt** formed by reducing the resistance of part of the etch stopper layer **24b** serves as an upper electrode portion of an auxiliary capacitor element Cs.

[0139] (Formation of Pixel Electrode)

[0140] Finally, as illustrated in FIGS. 20A-20C, a pixel electrode **28** is formed in a manner similar to that of the first embodiment.

[0141] As described above, the TFT substrate **20** is fabricated. The TFT substrate **20** fabricated by the above-described method and the counter substrate **30** including pixels each provided with a color filter are arranged to face each other and are adhered to each other by the sealing material **40**, and a liquid crystal material is filled between the substrates, thereby forming the liquid crystal layer **50**, so that the liquid crystal display device **10** can be obtained.

[0142] (Advantages of Second Embodiment)

[0143] In the thin film transistor T_R of the present embodiment, the pixel electrode **28** is in contact with and is electrically connected to the drain section DR in a manner similar to that of the first embodiment, which can reduce the occurrence of a contact failure between the pixel electrode **28** and the drain section DR.

[0144] In addition to the advantages obtained in the first embodiment, according to the configuration of the second embodiment, the source section S includes the low resistance portion **24as** and the source metal **25s**, so that contact of the source section S can also be ensured in the low resistance portion **24as** even when the electrode area of the source metal **24as** is reduced. Thus, satisfactory contact can be achieved. Therefore, the configuration of the second embodiment provides the advantage that the aperture ratio is increased by reducing the electrode area of source metal **24as**.

Third Embodiment

[0145] <Configuration of Liquid crystal Display Device>

[0146] Similar to the first embodiment, a liquid crystal display device **10** according to a third embodiment includes a TFT substrate **20** and a counter substrate **30** which are arranged to face each other. The substrates **20** and **30** are adhered to each other by a sealing material **40** arranged to have a frame-like shape at outer peripheral parts of the substrates **20** and **30**. In the space surrounded by the sealing material **40** between the substrates **20** and **30**, a liquid crystal layer **50** is provided as a display layer. The liquid crystal display device **10** has a display region D which is surrounded by the sealing material **40** and in which a plurality of pixels are arranged in a matrix pattern. A region by which the display region D is surrounded is a picture-frame region. The configurations, etc. of the counter substrate **30**, the sealing material **40**, and the liquid crystal layer **50** are the same as those of the first embodiment, and thus the description thereof is omitted.

[0147] (TFT Substrate)

[0148] FIGS. 21-23 illustrate the TFT substrate **20** of the third embodiment. FIG. 21 is a plan view illustrating the TFT substrate **20**. The TFT substrate **20** is formed, in a manner similar to that of the first embodiment, by stacking, on a substrate **21**, a first metal (of which a gate electrode **22a**, a lower electrode **22b**, a terminal **22c**, a gate line **22gb**, transfer pads (not shown), etc. are made), a gate insulating film **23**, oxide semiconductor films **24a**, **24b**, a second metal (of which a source metal **25s**, a drain metal **25d**, an upper metal **25b**, a source line **25sb**, etc. are made), a protective film **26**, a pixel electrode **28**, and an alignment layer (not shown).

[0149] FIG. 22 is a cross-sectional view along the line A-A of FIG. 21.

[0150] As illustrated in FIG. 22, the gate electrode 22a is covered with the gate insulating film 23, and on the gate insulating film 23, the oxide semiconductor film 24a including a channel section 24ac formed at a position facing the gate electrode 22a is provided, and on the oxide semiconductor film 24a, a source section S and a drain section DR are provided to be spaced apart from each other with the channel section 24ac sandwiched therebetween.

[0151] The gate electrode 22a is made of the first metal, and includes, for example, an aluminum film, a titanium film, and a titanium nitride film which are sequentially stacked from bottom to top.

[0152] The source section S is made of the source metal 25s provided above the gate insulating film 23 and the oxide semiconductor film 24a.

[0153] The source metal 25s is made of the second metal, and includes, similar to the first embodiment, for example, a first conductive film 25sp, a second conductive film 25sq, and a third conductive film 25sr which are sequentially stacked.

[0154] The drain section DR is a low resistance portion 24ad. The low resistance portion 24ad is a portion including part of the oxide semiconductor film 24a which is exposed in a pixel contact hole 27a, and the resistance of the portion is reduced.

[0155] The low resistance portion 24ad is the portion including the part of the oxide semiconductor film 24a which is exposed in the pixel contact hole 27a, and the resistance of the portion is reduced, and thus the portion has high conductivity leading to a resistivity of about $1/10000000000$ to $1/100$ of the resistivity of the channel section 24ac. The low resistance portion 24ad includes a surface of the oxide semiconductor film 24a, and preferably has a thickness of less than or equal to $1/2$ of the thickness of the oxide semiconductor film 24a. The resistance value of the low resistance portion 24ad is not uniform, but for example, the resistance gradually increases from the surface of the oxide semiconductor film 24a toward the gate insulating film 23. Moreover, in FIG. 22, the low resistance portion 24ad is illustrated as a discrete portion defined by a line frame for convenience, but the low resistance portion 24ad is not necessarily a discrete portion as long as it is a portion of a region integrated with the oxide semiconductor film 24a.

[0156] Above the oxide semiconductor film 24a, the drain metal 25d is provided. The drain metal 25d is provided at the same level as the source metal 25s, and includes, for example, a first conductive film 25dp made of a titanium film, a second conductive film 25dq made of an aluminum film, and a third conductive film 25dr made of a molybdenum nitride film which are sequentially stacked.

[0157] The pixel contact hole 27a is formed in the protective film 26, and extends through the drain metal 25d to the oxide semiconductor film 24a. An inner surface of the pixel contact hole 27a is covered with the pixel electrode 28, and the pixel electrode 28 is electrically connected to the low resistance portion 24ad which is the drain section DR.

[0158] A thin film transistor T_R of the present embodiment has the above-described configuration, and thus the pixel electrode 28 is directly in contact with and is electrically connected to the drain section DR, which can reduce the occurrence of a contact failure between the pixel electrode 28 and the drain section DR. In particular, when the drain metal 25d is formed as a multilayer structure composed of the first conductive film 25dp, the second conductive film 25dq, and the third conductive film 25dr, and the second conductive film

25dq is an aluminum film, the aluminum film is oxidized, and a surface of the aluminum film is covered with a passivation coating, which may cause unsatisfactory conduction between the drain metal 25d and the pixel electrode 28, thereby leading to a contact failure. However, the drain section DR is made of the low resistance portion 24ad obtained by reducing the resistance of part of the oxide semiconductor film 24a. Thus, the conduction between the pixel electrode 28 and the drain metal 25d can be ensured in the low resistance portion 24ad, so that satisfactory contact can be achieved.

[0159] FIG. 23 is a cross-sectional view along the line B-B of FIG. 23.

[0160] As illustrated in FIG. 23, the lower electrode 22b is covered with the gate insulating film 23, and on the gate insulating film 23, the etch stopper layer 24b made of an oxide semiconductor is provided at a position facing the lower electrode 22b. Above the etch stopper layer 24b, the upper metal 25b is provided. In the protective film 26 covering the etch stopper layer 24b, an auxiliary capacitor contact hole 27b extending through the upper metal 25b to the etch stopper layer 24b is formed. A low resistance portion 24bt is formed by reducing the resistance of a portion including part of the etch stopper layer 24b which is exposed in the auxiliary capacitor contact hole 27b compared to the resistance of the other portions. These components are included in an auxiliary capacitor element Cs.

[0161] The lower electrode 22b is made of the first metal, and includes for example, an aluminum film, a titanium film, and a titanium nitride film which are sequentially stacked from bottom to top. Note that the lower electrode 22b is connected to an auxiliary capacitor terminal T_{Cs} provided in the terminal region.

[0162] The upper metal 25b is provided at the same level as the source metal 25s and the drain metal 25d, and includes, for example, a first conductive film 25bp made of a titanium film, a second conductive film 25bq made of the aluminum film, and a third conductive film 25br made of the molybdenum nitride film which are sequentially stacked.

[0163] An inner surface of the auxiliary capacitor contact hole 27b formed in the protective film 26 is covered with the pixel electrode 28. The pixel electrode 28 is in contact with and is electrically connected to the low resistance portion 24bt provided in the etch stopper layer 24b.

[0164] Note that cross sections of a gate terminal section T_G and a source terminal section T_S are not illustrated, but have configurations similar to those of the cross sections of the gate terminal section T_G of the first embodiment (FIG. 6).

[0165] The liquid crystal display device 10 having the above-described configuration is configured such that each of pixel electrodes forms a pixel, and in each pixel, when the thin film transistor T_R is turned on by a gate signal sent via the gate line 22gb, a source signal is sent via the source line 25sb, so that a predetermined charge is applied to the pixel electrode 28 via the source section S (the source metal 25s) and the drain section DR (the low resistance portion 24ad), which causes a potential difference between the pixel electrode 28 and the common electrode of the counter substrate 30, thereby applying a predetermined voltage to a liquid crystal capacitor including the liquid crystal layer 50. The liquid crystal display device 10 displays an image by adjusting transmittance of light coming from the outside, based on the phenomenon that the alignment of liquid crystal molecules changes according to the magnitude of the applied voltage.

[0166] In the above description, the second metal, of which the source metal **25s**, the drain metal **25d**, the upper metal **25b**, etc. of the TFT substrate **20** are made, has a configuration in which the first conductive film **25sp**, **25dp**, **25bp**, the second conductive film **25sq**, **25dq**, **25bq**, and the third conductive film **25sr**, **25dr**, **25br** are sequentially stacked. However, a configuration which does not include the third conductive film **25sr**, **25dr**, **25br** (that is, a configuration in which two layers, the first conductive film **25sp**, **25dp**, **25bp** and the second conductive film **25sq**, **25dq**, **25bq** are stacked) may be possible, or other configurations may be possible.

[0167] Moreover, in the above description, the second conductive film **25sq**, **25dq**, **25bq** of the second metal, of which the source metal **25s**, the drain metal **25d**, the upper metal **25b**, etc. of the TFT substrate **20** are made, is an aluminum film. However, for example, a film made of an aluminum alloy, a film made of copper (Cu) or made of a copper alloy, etc. may be used.

[0168] <Method for Fabricating TFT Substrate>

[0169] With reference to FIGS. **24A-26B**, a method for fabricating the TFT substrate **20** of the present embodiment will be described below.

[0170] (Formation of First Metal, Gate Insulating Film, Oxide Semiconductor Film, Second Metal)

[0171] First, as illustrated in FIGS. **24A**, **24B**, a first metal having a multilayer structure composed of, for example, an aluminum film, a titanium film, and a titanium nitride film is provided on a substrate **21** to form a gate electrode **22a**, a lower electrode **22b**, etc.

[0172] Next, as a gate insulating film **23**, a SiO₂ film is formed by, for example, CVD.

[0173] Next, an oxide semiconductor film **24a** and an etch stopper layer **24b** are formed.

[0174] Subsequently, a second metal having a multilayer structure composed of a first conductive film, a second conductive film, and a third conductive film is formed so that a source metal **25s** and a drain metal **25d** are formed above the gate insulating film **23** and the oxide semiconductor film **24a**, and an upper metal **25b** is formed above the gate insulating film **23** and the etch stopper layer **24b**. Here, the second metal is formed as a pattern by which a source line **25sb**, and the like are formed simultaneously with the source metal **25s**, the drain metal **25d**, and the upper metal **25b**.

[0175] (Formation of Protective Film, Contact Hole•Process of Reducing Resistance)

[0176] Next, as illustrated in FIGS. **25A**, **25B**, a SiO₂ film is formed as a protective film **26** by, for example, CVD. Then, the protective film **26** are dry etched, thereby forming a pixel contact hole **27a**, an auxiliary capacitor contact hole **27b**, and a contact hole **27c** (see FIG. **21**). Then, a process of reducing resistance is performed on parts of the oxide semiconductor film **24a** and the etch stopper layer **24b** which are respectively exposed in the pixel contact hole **27a** and the auxiliary capacitor contact hole **27b** to reduce the resistance of portions including the exposed parts of the oxide semiconductor film **24a** and the etch stopper layer **24b**, thereby forming low resistance portions **24ad**, **24bt**. The process of reducing resistance can be performed by methods similar to those listed as the process of reducing resistance in the first embodiment. With this process of reducing resistance, a portion having a thickness of less than or equal to 1/2 of the thickness of the oxide semiconductor film **24a** is formed into the low resistance portion **24ad** having a resistance lower than that of the oxide semiconductor film **24a**. Moreover, a portion having a

thickness of less than or equal to 1/2 of the thickness of the etch stopper layer **24b** is formed into the low resistance portion **24bt** having a resistance lower than that of the etch stopper layer **24b**. The low resistance portion **24ad** formed by reducing the resistance of part of the oxide semiconductor film **24a** serves as a drain section DR. Moreover, the low resistance portion **24bt** formed by reducing the resistance of part of the etch stopper layer **24b** serves as an upper electrode portion of an auxiliary capacitor element Cs.

[0177] (Formation of Pixel Electrode)

[0178] Finally, as illustrated in FIGS. **26A**, **26B**, a pixel electrode **28** is formed in a manner similar to that of the first embodiment.

[0179] As described above, the TFT substrate **20** is fabricated. The TFT substrate **20** fabricated by the above-described method and the counter substrate **30** including pixels each provided with a color filter are arranged to face each other and are adhered to each other by the sealing material **40**, and a liquid crystal material is filled between the substrates, thereby forming the liquid crystal layer **50**, so that the liquid crystal display device **10** can be obtained.

[0180] (Advantages of Third Embodiment)

[0181] In the thin film transistor T_R of the present embodiment, even when conductive performance at a surface of the drain metal **25d** is degraded, the pixel electrode **28** is in contact with and is electrically connected to the drain section DR in a manner similar to that of the first embodiment, which can reduce the occurrence of a contact failure between the pixel electrode **28** and the drain section DR.

[0182] In addition to the advantages obtained in the first embodiment, in the configuration of the third embodiment, overetching of the protective film **26** in forming the pixel contact hole **27a** and the auxiliary capacitor contact hole **27b** can be reduced by the drain metal **25d** and the upper metal **25b** because the drain metal **25d** is provided in the drain section DR, and the upper metal **25b** is provided in the auxiliary capacitor element Cs. Thus, as a result, plasma damage to the oxide semiconductor film **24a** or slight etching of the oxide semiconductor film **24a** can be reduced.

INDUSTRIAL APPLICABILITY

[0183] The present invention is useful for thin film transistor substrates and liquid crystal display devices including the same.

DESCRIPTION OF REFERENCE CHARACTERS

- [0184] T_R Thin Film Transistor
- [0185] D Drain Section
- [0186] S Source Section
- [0187] **10** Liquid Crystal Display Device
- [0188] **20** Thin Film Transistor Substrate (TFT Substrate)
- [0189] **21** Substrate
- [0190] **22a** Gate Electrode
- [0191] **23** Gate Insulating Film
- [0192] **24a** Oxide Semiconductor Film
- [0193] **24ac** Channel Section
- [0194] **25a** Oxide Semiconductor Film
- [0195] **25sp** First Conductive Film
- [0196] **25sq** Second Conductive Film
- [0197] **25sr** Third Conductive Film
- [0198] **25s** Source Metal
- [0199] **26**, **26B** Protective Film
- [0200] **26A** Interlayer Insulating Film

[0201] 27a, 27ad Pixel Contact Hole

[0202] 27as Source Contact Hole

[0203] 28 Pixel Electrode

[0204] 30 Counter Substrate

[0205] 50 Liquid Crystal Layer

1. A thin film transistor substrate comprising:
 - a substrate;
 - a thin film transistor including
 - a gate electrode provided on the substrate,
 - a gate insulating film provided to cover the gate electrode,
 - an oxide semiconductor film provided on the gate insulating film and including a channel section formed at a position facing the gate electrode, and
 - a source section and a drain section provided to be spaced apart from each other with the channel section sandwiched therebetween;
 - a protective film which is provided to cover the thin film transistor and in which a pixel contact hole extending to the drain section is formed; and
 - a pixel electrode provided on the protective film and electrically connected to the drain section via the pixel contact hole, wherein
 - the source section is made of a source metal provided above the gate insulating film and the oxide semiconductor film, and
 - the drain section is a low resistance portion which is part of the oxide semiconductor film, where the part includes a surface of the oxide semiconductor film opposite to the gate insulating film, and resistance of the part is reduced.
2. The thin film transistor substrate of claim 1, wherein the low resistance portion which is the drain section has a thickness of less than or equal to 1/2 of a thickness of the oxide semiconductor film.
3. The thin film transistor substrate of claim 1, further comprising:

- an interlayer insulating film provided above the gate insulating film and the oxide semiconductor film and under the protective film, wherein
 - the source metal included in the source section is formed above the interlayer insulating film,
 - a source contact hole extending from a surface of the interlayer insulating film to the oxide semiconductor film is formed in the interlayer insulating film, and the source metal is formed on an inner surface of the source contact hole to electrically connect the source metal to the oxide semiconductor film, and
 - part of the oxide semiconductor film is a low resistance portion whose resistance is reduced, where the part includes a surface of the oxide semiconductor film which is in contact with the source metal.
- 4. The thin film transistor substrate of claim 1, wherein the source metal includes
 - a first conductive film, and
 - a second conductive film made of aluminum, and
 - the first conductive film and the second conductive film are sequentially stacked on the gate insulating film.
- 5. The thin film transistor substrate of claim 4, wherein the first conductive film is made of a refractory metal film.
- 6. The thin film transistor substrate of claim 4, wherein the source metal further includes a third conductive film stacked on a surface of the second conductive film opposite to the first conductive film.
- 7. A liquid crystal display device, comprising:
 - the thin film transistor substrate of claim 1;
 - a counter substrate arranged to face the thin film transistor substrate; and
 - a liquid crystal layer provided between the thin film transistor substrate and the counter substrate.

* * * * *

专利名称(译)	薄膜晶体管基板和具有该薄膜晶体管基板的液晶显示装置		
公开(公告)号	US20130201420A1	公开(公告)日	2013-08-08
申请号	US13/814022	申请日	2011-05-27
[标]申请(专利权)人(译)	MISAKI胜则		
申请(专利权)人(译)	MISAKI, 胜则		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	MISAKI KATSUNORI		
发明人	MISAKI, KATSUNORI		
IPC分类号	G02F1/1362 H01L29/786		
CPC分类号	H01L27/1225 H01L29/41733 H01L29/458 H01L27/124 G02F1/136286 G02F2001/136295 G02F1/136227 H01L29/7869		
优先权	2010178226 2010-08-07 JP		
其他公开文献	US9069219		
外部链接	Espacenet USPTO		

摘要(译)

源极部分 (S) 由设置在栅极绝缘膜 (23) 和氧化物半导体膜 (24a) 上方的源极金属 (25s) 制成, 并且漏极部分 (DR) 包括低电阻部分 (24ad), 其是低电阻部分 (24ad)。氧化物半导体膜 (24a) 的一部分, 其中该部分包括与栅极绝缘膜 (23) 相对的氧化物半导体膜 (24a) 的表面, 并且该部分的电阻减小。

