US 20170162151A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2017/0162151 A1**

CAO (43) **Pub. Date: Jun. 8, 2017**

(54) **GOA CIRCUIT AND A LIQUID CRYSTAL DISPLAY**

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(21) Appl. No.: **14/786,088**

(22) PCT Filed: **Sep. 23, 2015**

(86) PCT No.: **PCT/CN2015/090352**

§ 371 (c)(1),
(2) Date: **Oct. 21, 2015**

(30) **Foreign Application Priority Data**

Sep. 17, 2015 (CN) 201510594063.9

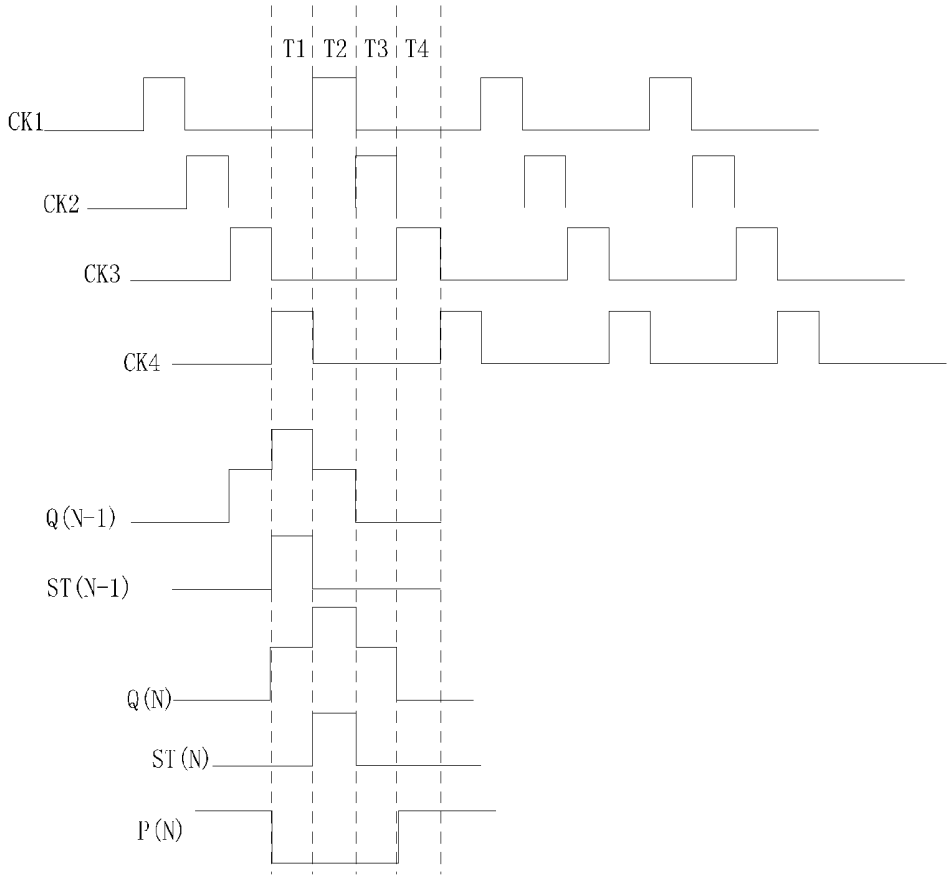
Publication Classification

(51) **Int. Cl.**
G09G 3/36 (2006.01)

(52) **U.S. Cl.**
CPC ***G09G 3/3677*** (2013.01); ***G09G 3/3696*** (2013.01); *G09G 2300/0809* (2013.01); *G09G 2310/08* (2013.01); *G09G 2300/0426* (2013.01); *G09G 2310/0213* (2013.01)

(57) **ABSTRACT**

The application disclosure a GOA circuit and a liquid crystal display. The GOA circuit including a plurality of GOA unit connected in series, wherein a Nth level GOA unit including a fifth transistor, a eighth transistor and a leakage control module. wherein the leakage control module is connected in series between the Nth level gate terminal signal and the drain terminal of the eighth transistor and/or between the Nth level pull-down signal and the drain terminal of the fifth transistor; in the valid period of the Nth level scanning signal can block the Nth level gate terminal signal through the leakage pathway of the eighth transistor and/or to block the Nth level pull-down signal through the leakage pathway of the fifth transistor to achieve the stability of the GOA circuit.



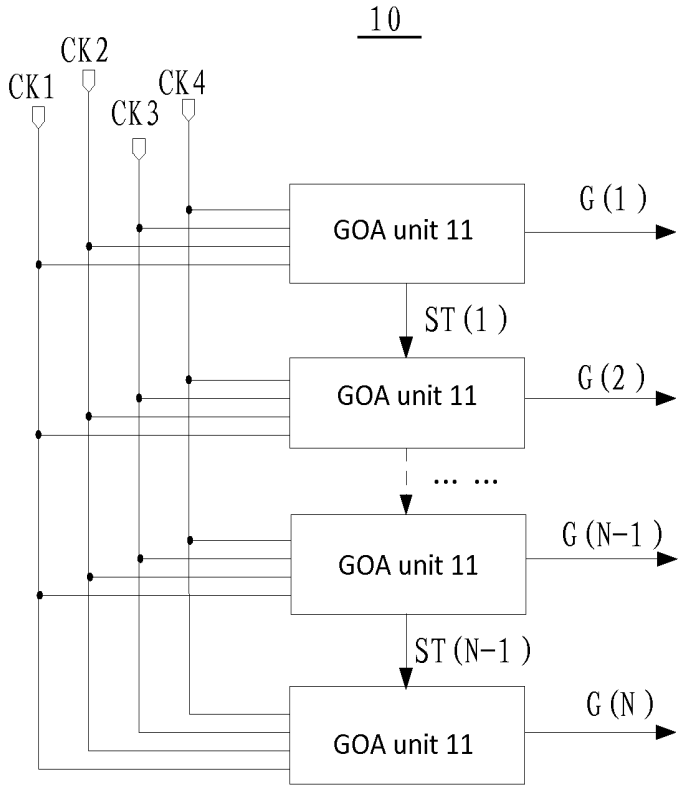

10
CK1
CK2
CK3
CK4
GOA unit 11
GOA unit 11
GOA unit 11
GOA unit 11
G(1)
G(2)
G(N-1)
G(N)
ST(1)
ST(N-1)
... ...

FIG1

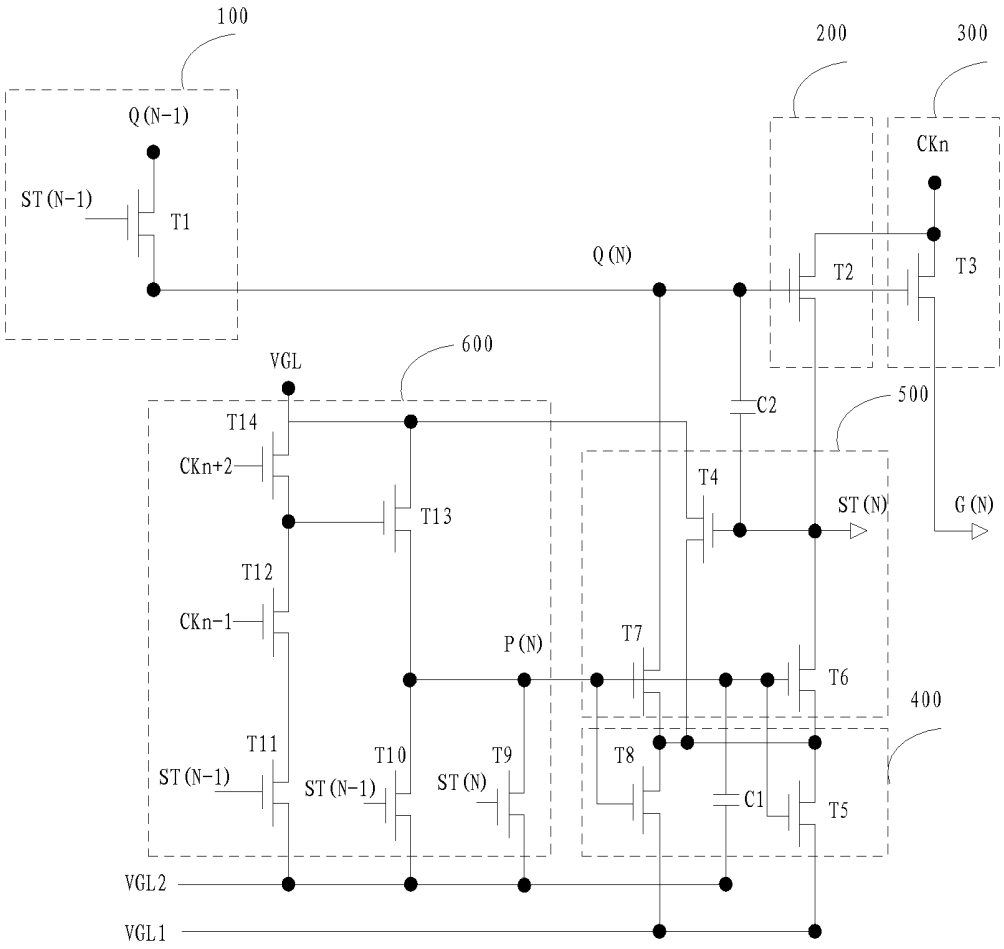

100
200
300
Q(N-1)
CKn
ST(N-1)
T1
Q(N)
T2
T3
VGL
600
C2
500
T14
CKn+2
T4
T13
ST(N)
G(N)
T12
CKn-1
P(N)
T7
T6
400
T11
T10
T9
T8
ST(N-1)
ST(N-1)
ST(N)
C1
T5
VGL2
VGL1

FIG 2

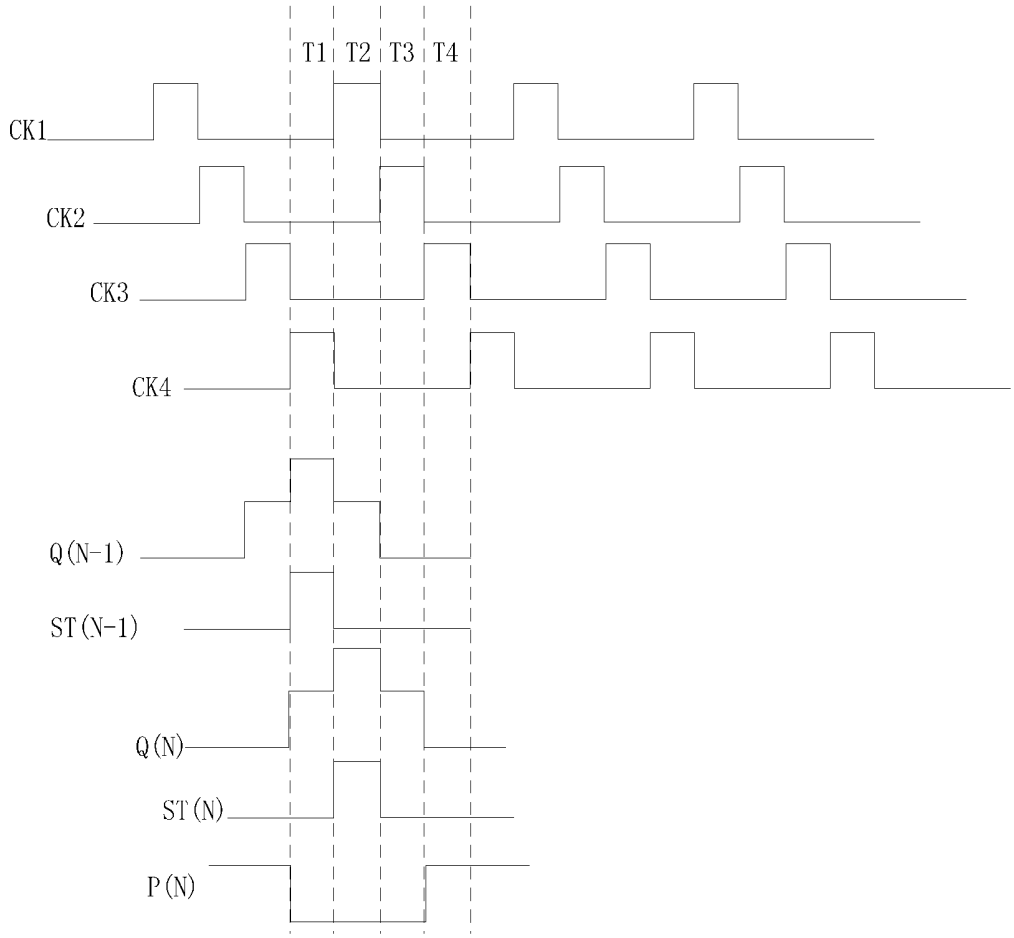


FIG 3

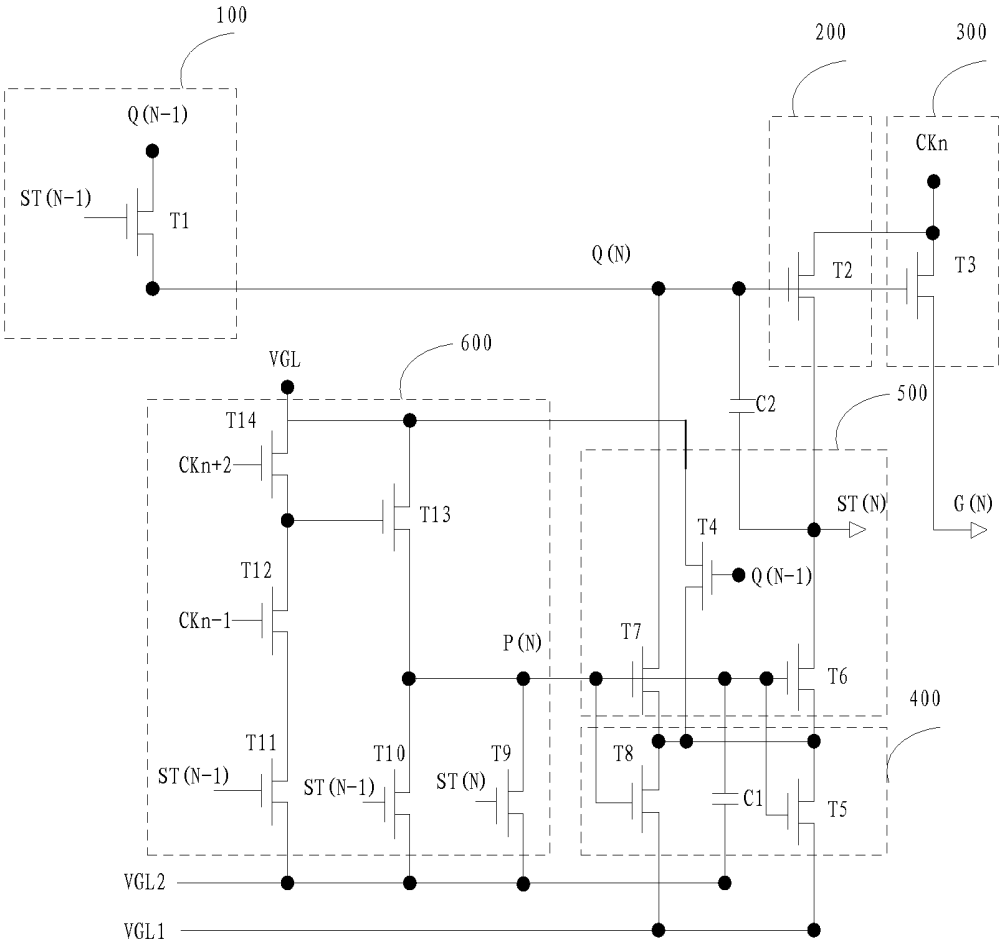

100
200
300
Q(N-1)
CKn
ST(N-1)
T1
Q(N)
T2
T3
VGL
600
C2
500
T14
CKn+2
T13
ST(N)
G(N)
T4
T12
Q(N-1)
CKn-1
P(N)
T7
T6
400
T11
T10
T9
T8
ST(N-1)
ST(N-1)
ST(N)
C1
T5
VGL2
VGL1

FIG 4

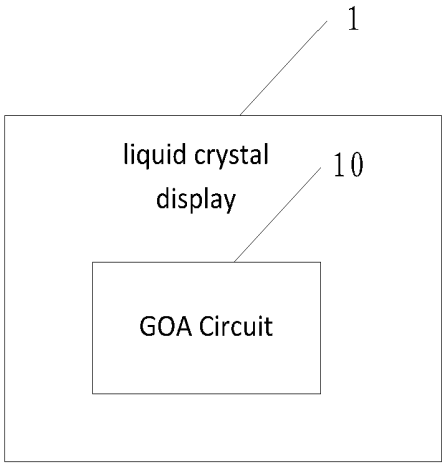

1
liquid crystal display
10
GOA Circuit

FIG 5

GOA CIRCUIT AND A LIQUID CRYSTAL DISPLAY

FIELD OF THE INVENTION

[0001] The present invention relates to the field of liquid crystal display technology, and in particular to a GOA circuit structure.

BACKGROUND

[0002] Nowadays, in order to fill the requirement of the narrow bezel or zero bezel of the liquid crystal display, the Indium-Gallium-Zinc Oxidethin film transistor (IGZO TFT) is usually used on the gate driver on array (GOA). Since the IGZO TFT has lower threshold voltage (Vth) and lower subthreshold swing (SS). When the gate-source voltage (Vgs) is zero, the IGZO TFT still cannot close normally. The larger leakage will decrease the stability of the GOA circuit and increase the power loss of the GOA circuit.

SUMMARY OF THE INVENTION

[0003] AGOA circuit and a liquid crystal display are provided in this application to solve the technical problem of blocking the leakage pathway of the IGZO TFT in GOA circuit to achieve the stability of the GOA circuit.

[0004] In order to solve the technical problem, the technical approach of this application is: providing a GOA circuit for liquid crystal display wherein the GOA circuit including a plurality of GOA unit connected in series, wherein a Nth level GOA unit including a pull-up control module, a pull-down module, a pull-up module, a pull-down holding module and a leakage control module; the pull-up control module including a first transistor, a gate terminal of the first transistor is connected to a N-1th level pull-down signal, a drain terminal of the first transistor is connected to the first leakage control signal and the source terminal of the first transistor is connected to the Nth levelgate terminal signal; the pull-down module including a second transistor, the gate terminal of the second transistor is connected to the Nth levelgate terminal signal, the drain terminal of the second transistor is connected to the Nth level clock signal line, and the source terminal of the second transistor output the Nth level pull-down signal; the pull-up module including a third transistor, the gate terminal of the third transistor is connected to the Nth levelgate terminal signal, the drain terminal of the third transistor is connected to the Nth level clock signal line, and the source terminal of the third transistor output the Nth level scanning signal; the pull-down holding module including a fifth transistor and a eighth transistor, the gate terminal of the fifth transistor is connected to the Nth level common signal, the drain terminal of the fifth transistor is connected to the Nth level pull-down signal, the source terminal of the fifth transistor is connected to a first low direct current voltage source; and the gate terminal of the eighth transistor is connected to the Nth level common signal, the source terminal of the eighth transistor is connected to the first low direct current voltage source and the drain terminal of the eighth transistor is connected to the Nth levelgate terminal signal; the leakage control module is connected in series between the Nth level gate terminal signal and the eighth transistor and/or between the Nth level pull-down signal and the fifth transistor; in the valid period of the Nth level scanning signal, a second leakage control signal is to block the Nth level gate terminal signal through the leakage pathway of the eighth transistor and/or to block the Nth level pull-down signal through the leakage pathway of the fifth transistor; wherein the leakage control module including a fourth transistor and a seventh transistor, the gate terminal of the fourth transistor is connected to the second leakage control signal, the drain terminal of the fourth transistor is connected to the direct current signaling source, the source terminal of the fourth transistor is connected to the drain terminal of the eighth transistor; the seventh transistor is connected between the Nth levelgate terminal signal and the drain terminal of the eighth transistor, the gate terminal of the seventh transistor is connected to the Nth level common signal, the drain terminal of the seventh transistor is connected to the Nth levelgate terminal signal and the source terminal of the seventh transistor is connected to the drain terminal of the eighth transistor to block the Nth levelgate terminal signal through the leakage pathway of the eighth transistor in the valid period of the Nth level scanning signal. Wherein the first leakage control signal is the N−1th levelgate terminal signal to block the Nth levelgate terminal signal through the leakage pathway of the first transistor in the valid period of the Nth level scanning signal.

[0005] wherein the second leakage control signal is the Nth level pull-down signal.

[0006] In order to solve the technical problem, the another technical approach of this application is: providing a GOA circuit for liquid crystal display wherein the GOA circuit including a plurality of GOA unit connected in series, wherein a Nth level GOA unit including a pull-up control module, a pull-down module, a pull-up module, a pull-down holding module and a leakage control module; the pull-up control module including a first transistor, a gate terminal of the first transistor is connected to a N−1th level pull-down signal, a drain terminal of the first transistor is connected to the first leakage control signal and the source terminal of the first transistor is connected to the Nth levelgate terminal signal; the pull-down module including a second transistor, the gate terminal of the second transistor is connected to the Nth levelgate terminal signal, the drain terminal of the second transistor is connected to the Nth level clock signal line, and the source terminal of the second transistor output the Nth level pull-down signal; the pull-up module including a third transistor, the gate terminal of the third transistor is connected to the Nth levelgate terminal signal, the drain terminal of the third transistor is connected to the Nth level clock signal line, and the source terminal of the third transistor output the Nth level scanning signal; the pull-down holding module including a fifth transistor and a eighth transistor, the gate terminal of the fifth transistor is connected to the Nth level common signal, the drain terminal of the fifth transistor is connected to the Nth level pull-down signal, the source terminal of the fifth transistor is connected to a first low direct current voltage source; and the gate terminal of the eighth transistor is connected to the Nth level common signal, the source terminal of the eighth transistor is connected to the first low direct current voltage source and the drain terminal of the eighth transistor is connected to the Nth levelgate terminal signal. The leakage control module is connected in series between the Nth level gate terminal signal and the eighth transistor and/or between the Nth level pull-down signal and the fifth transistor; a second leakage control signal is to block the Nth level gate terminal signal through the leakage pathway of the eighth

transistor and/or to block the Nth level pull-down signal through the leakage pathway of the fifth transistor in the valid period of the Nth level scanning signal.

[0007] wherein the leakage control module including a fourth transistor and a seventh transistor, the gate terminal of the fourth transistor is connected to the second leakage control signal, the drain terminal of the fourth transistor is connected to the direct current signaling source, the source terminal of the fourth transistor is connected to the drain terminal of the eighth transistor; the seventh transistor is connected between the Nth levelgate terminal signal and the drain terminal of the eighth transistor, the gate terminal of the seventh transistor is connected to the Nth level common signal, the drain terminal of the seventh transistor is connected to the Nth levelgate terminal signal and the source terminal of the seventh transistor is connected to the drain terminal of the eighth transistor to block the Nth levelgate terminal signal through the leakage pathway of the eighth transistor in the valid period of the Nth level scanning signal.

[0008] wherein the second leakage control signal is the Nth level pull-down signal. wherein the second leakage control signal is the N−1th level gate terminal signal. wherein the leakage control module further including a sixth transistor, wherein the sixth transistor is connected between the Nth level pull-down signal and the drain terminal of the fifth transistor, the gate terminal of the sixth transistor is connected to the Nth level common signal, the drain terminal of the sixth transistor is connected to the Nth level pull-down signal, the source terminal of the sixth transistor is connected to the drain terminal of the fifth transistor and the source terminal of the fourth transistor to block the Nth level pull-down signal through the leakage pathway of the fifth transistor in the valid period of the Nth level scanning signal.

[0009] wherein the first leakage control signal is the N−1th level gate terminal signal to block the Nth levelgate terminal signal through the leakage pathway of the first transistor in the valid period of the Nth level scanning signal.

[0010] wherein the Nth level GOA unit further including a pull-down module, the pull-down module including a ninth level transistor, a tenth level transistor, an eleventh level transistor, a twelfth transistor, a thirteenth level transistor and a fourteenth level transistor; wherein the gate terminal of the ninth level transistor is connected to the Nth level pull-down signal, the source terminal of the ninth level transistor is connected to the a second low direct current voltage source, the drain terminal of the ninth level transistor is connected to the Nth level common signal, the gate terminal of the tenth level transistor is connected to the N−1th level pull-down signal, the source terminal of the tenth level transistor is connected to the second low direct current voltage source, the drain terminal of the tenth level transistor is connected to the Nth level common signal, the gate terminal of the eleventh level transistor is connected to the N−1th level pull-down signal, the source terminal of the eleventh level transistor is connected to the second low direct current voltage source, the drain terminal of the eleventh level transistor is connected to the source terminal of the twelfth transistor, the gate terminal of the twelfth transistor is connected to the N−1th level clock signal line, the drain terminal of the twelfth transistor is connected to the gate terminal of the thirteenth level transistor and the source terminal of the fourteenth level transistor, the source terminal of the thirteenth level transistor is connected to the Nth level common signal, the drain terminals of the thirteenth level transistor and the fourteenth level transistor are connected to the direct current signaling source, the gate terminal of the fourteenth transistor is connected to the N+2th level clock signal line.

[0011] wherein the electric potential of the first low direct current voltage source is smaller than the electric potential of the second low direct current voltage source, the lower electric potential of the N−1th level pull-down signal, the Nth level pull-down signal are smaller than the electric potential of the of the second low direct current voltage source to block the leakage pathway of the Nth level common signal through the ninth transistor, the tenth transistor, the eleventh transistor in the invalid period of the Nth level scanning signal.

[0012] wherein the Nth level GOA unit received a first clock signal, a second clock signal, a third clock signal, and a fourth clock signal, and the first clock signal, the second clock signal, the third clock signal, and the fourth clock signal CK**4** are timely valid in orderly during one working period, wherein when the Nth level clock signal line is the first clock signal, the N+2 clock signal line is the third clock signal and the N−1 clock signal line is the fourth clock signal.

[0013] In order to solve the technical problem, the another technical approach of this application is: providing a liquid crystal display having a GOA circuit, the GOA circuit including a plurality of GOA unit connected in series, wherein a Nth level GOA unit including a pull-up control module, a pull-down module, a pull-up module, a pull-down holding module and a leakage control module; the pull-up control module including a first transistor, a gate terminal of the first transistor is connected to a N−1th level pull-down signal, a drain terminal of the first transistor is connected to the first leakage control signal and the source terminal of the first transistor is connected to the Nth levelgate terminal signal; the pull-down module including a second transistor, the gate terminal of the second transistor is connected to the Nth levelgate terminal signal, the drain terminal of the second transistor is connected to the Nth level clock signal line, and the source terminal of the second transistor output the Nth level pull-down signal; the pull-up module including a third transistor, the gate terminal of the third transistor is connected to the Nth levelgate terminal signal, the drain terminal of the third transistor is connected to the Nth level clock signal line, and the source terminal of the third transistor output the Nth level scanning signal; the pull-down holding module including a fifth transistor and a eighth transistor, the gate terminal of the fifth transistor is connected to the Nth level common signal, the drain terminal of the fifth transistor is connected to the Nth level pull-down signal, the source terminal of the fifth transistor is connected to a first low direct current voltage source; and the gate terminal of the eighth transistor is connected to the Nth level common signal, the source terminal of the eighth transistor is connected to the first low direct current voltage source and the drain terminal of the eighth transistor is connected to the Nth levelgate terminal signal. The leakage control module is connected in series between the Nth level gate terminal signal and the eighth transistor and/or between the Nth level pull-down signal and the fifth transistor; a second leakage control signal is to block the Nth level gate terminal signal through the leakage pathway of the eighth transistor and/or to block the Nth level pull-down signal

through the leakage pathway of the fifth transistor in the valid period of the Nth level scanning signal.

[0014] Wherein the leakage control module including a fourth transistor and a seventh transistor, the gate terminal of the fourth transistor is connected to the second leakage control signal, the drain terminal of the fourth transistor is connected to the direct current signaling source, the source terminal of the fourth transistor is connected to the drain terminal of the eighth transistor; the seventh transistor is connected between the Nth levelgate terminal signal and the drain terminal of the eighth transistor, the gate terminal of the seventh transistor is connected to the Nth level common signal, the drain terminal of the seventh transistor is connected to the Nth levelgate terminal signal and the source terminal of the seventh transistor is connected to the drain terminal of the eighth transistor to block the Nth levelgate terminal signal through the leakage pathway of the eighth transistor in the valid period of the Nth level scanning signal.

[0015] wherein the second leakage control signal is the Nth level pull-down signal. wherein the second leakage control signal is the N−1th level gate terminal signal. wherein the leakage control module further including a sixth transistor, the sixth transistor is connected between the Nth level pull-down signal and the drain terminal of the fifth transistor, the gate terminal of the sixth transistor is connected to the Nth level common signal, the drain terminal of the sixth transistor is connected to the Nth level pull-down signal, the source terminal of the sixth transistor is connected to the drain terminal of the fifth transistor and the source terminal of the fourth transistor to block the Nth level pull-down signal through the leakage pathway of the fifth transistor in the valid period of the Nth level scanning signal.

[0016] wherein the first leakage control signal is the N−1th level gate terminal signal to block the Nth levelgate terminal signal through the leakage pathway of the first transistor in the valid period of the Nth level scanning signal.

[0017] wherein the Nth level GOA unit further including a pull-down module, the pull-down module including a ninth transistor, a tenth transistor, an eleventh transistor, a twelfth transistor, a thirteenth transistor and a fourteenth transistor; wherein the gate terminal of the ninth transistor is connected to the Nth level pull-down signal, the source terminal of the ninth transistor is connected to the a second low direct current voltage source, the drain terminal of the ninth transistor is connected to the Nth level common signal, the gate terminal of the tenth transistor is connected to the N−1th level pull-down signal, the source terminal of the tenth transistor is connected to the second low direct current voltage source, the drain terminal of the tenth transistor is connected to the Nth level common signal, the gate terminal of the eleventh transistor is connected to the N−1th level pull-down signal, the source terminal of the eleventh transistor is connected to the second low direct current voltage source, the drain terminal of the eleventh transistor is connected to the source terminal of the twelfth transistor, the gate terminal of the twelfth transistor is connected to the N−1th level clock signal line, the drain terminal of the twelfth transistor is connected to the gate terminal of the thirteenth transistor and the source terminal of the fourteenth transistor, the source terminal of the thirteenth transistor is connected to the Nth level common signal, the drain terminals of the thirteenth transistor and the fourteenth transistor are connected to the direct current signaling source, the gate terminal of the fourteenth transistor is connected to the N+2th level clock signal line.

[0018] wherein the electric potential of the first low direct current voltage source is smaller than the electric potential of the second low direct current voltage source, the lower electric potential of the N−1th level pull-down signal, the Nth level pull-down signal are smaller than the electric potential of the of the second low direct current voltage source to block the leakage pathway of the Nth level common signal through the ninth transistor, the tenth transistor, the eleventh transistor in the invalid period of the Nth level scanning signal.

[0019] Wherein the Nth level GOA unit received a first clock signal, a second clock signal, a third clock signal, and a fourth clock signal, and the first clock signal, the second clock signal, the third clock signal, and the fourth clock signal CK**4** are timely valid in orderly during one working period, wherein when the Nth level clock signal line is the first clock signal, the N+2 clock signal line is the third clock signal and the N−1 clock signal line is the fourth clock signal.

[0020] The advantage of this application is by adding the leakage control module between the Nth level gate terminal signal and the eighth transistor and/or the Nth level pull-down signal and the fifth transistor into the GOA circuit and the liquid crystal display structure to achieving of leakage blocking. In the valid period of the Nth level scanning signal, the Nth level gate terminal signal through the leakage pathway from the eighth transistor and/or the leakage pathway through the Nth level pull-down signal through the fifth transistor is blocked and enhance the stability of the GOA circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The following detailed descriptions accompanying drawings and the embodiment of the present invention make the aspect of the present invention and the other beneficial effect more obvious.

[0022] FIG. **1** is a schematic view illustrating the GOA circuit structure according to the present invention;

[0023] FIG. **2** is a circuit diagram of the GOA circuit structure illustrated in FIG. **1** according to the first embodiment of the present invention;

[0024] FIG. **3** is a timing diagram of the GOA circuit structure illustrated in FIG. **1** according to the first embodiment of the present invention;

[0025] FIG. **4** is a circuit diagram of the GOA circuit structure illustrated in FIG. **1** according to the second embodiment of the present invention;

[0026] FIG. **5** is a schematic view illustrating the liquid crystal display structure according to the embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] The specific components or items are used in the specification and claims. Those skilled in the art can use other possible modifications and variations in the same components or items. The specification and claim will not distinguish the different terms to the items or components but by the functions. Following is the detail description illustrated by the figures and the embodiments.

[0028] FIG. **1** is a schematic view illustrating the GOA circuit structure according to the present invention. FIG. **1** illustrates a GOA circuit **10** includes a plurality of GOA unit **11** connected in series. The Nth level GOA unit **11** is used and controlled by the first clock signal CK**1**, a second clock signal CK**2**, a third clock signal CK**3**, a fourth clock signal CK**4** and the pull-down signal ST (N−1), output the scanning signal G (N) to charge the Nth level horizontal scanning line in the corresponding display zone. Wherein the first clock signal CK**1**, the second clock signal CK**2**, the third clock signal CK**3**, the fourth clock signal CK**4** are timely working accordingly in one valid period, in other words, the first clock signal CK**1**, the second clock signal CK**2**, the third clock signal CK**3**, the fourth clock signal CK**4** are in high electrical potential accordingly in one valid period. And the transistors in the GOA circuit are IGZO TFT.

[0029] FIG. **2** is a circuit diagram of the GOA circuit structure illustrated in FIG. **1** according to the first embodiment of the present invention. As illustrated in FIG. **2**, the Nth level COA unit **11** includes a pull-up control module **100**, a pull-down module **200**, a pull-up module **300**, pull-down holding module **400**, a leakage control module **500** and a pull-down module **600**.

[0030] The pull-up control module **100** includes a first transistor T**1**, the gate terminal of the first transistor T**1** is connected to the N−1th level pull-down signal. The drain terminal of the first transistor T**1** is connected to the first leakage control signal. The source terminal of the first transistor T**1** is connected to the Nth levelgate terminal signalQ (N). In this embodiment, the first leakage control signal is the N−1th levelgate terminal signalQ (N−1). Wherein in the valid period of the Nth level scanning signalG (N), the N−1th levelgate terminal signal is in high electric potential to make the drain terminal of the first transistor T**1** in high electric potential and the Vgs of the first transistor T**1** small than 0 to block the leakage pathway of the Nth levelgate terminal signalQ (N) through the first transistor T**1**.

[0031] The pull-down module **200** includes a second transistor T**2**. The gate terminal of the second transistor T**2** is connected to the Nth levelgate terminal signalQ (N), the drain terminal of the second transistor T**2** is connected to the Nth level clock signal line CKn, and the source terminal of the second transistor T**2** outputs the Nth level pull-down signal ST (N).

[0032] The pull-up module **300** includes a third transistor T**3**, the gate terminal of the third transistor T**3** is connected to the Nth levelgate terminal signalQ (N), the drain terminal of the third transistor T**3** is connected to the Nth level clock signal line CKn, and the source terminal of the third transistor T**3** output the Nth level scanning signal G (N).

[0033] The pull-down holding module **400** includes a fifth transistor T**5** and a eighth transistor T**8**. The gate terminal of the fifth transistor T**5** is connected to the Nth level common signalP (N), the drain terminal of the fifth transistor T**5** is connected to the Nth level pull-down signal ST (N), the source terminal of the fifth transistor T**5** is connected to a first low direct current voltage source (VGL**1**). The gate terminal of the eighth transistor T**8** is connected to the Nth level common signalP (N), the source terminal of the eighth transistor T**8** is connected to the first low direct current voltage source (VGL**1**) and the drain terminal of the eighth transistor T**8** is connected to the Nth levelgate terminal signalQ (N).

[0034] Wherein in the valid period of the Nth level scanning signal G (N), because of the Vgs of the fifth transistor T**5** is equal to 0, the Nth level pull-down signal ST (N) is leakage through the fifth transistor T**5**, and the Nth level pull-down signal ST (N) cannot reach the high electric level. In the meantime, because of the Vgs of the eighth transistor T**8** is equal to 0, the Nth levelgate terminal signalQ (N) is leakage through the eighth transistor T**8**, and the Nth levelgate terminal signalQ (N) cannot reach the high electric level.

[0035] In order to solve the problem mentioned above, the leakage control module **500** is connected in series between the pull-down holding circuits **400**, the Nth level pull-down signal ST (N) and the Nth level gate terminal signal Q (N). By the second leakage control signal to block the Nth level gate terminal signal Q (N) through the leakage pathway of the eighth transistor T**8** and the Nth level pull-down signal ST (N) through the leakage pathway of the fifth transistor T**5**.

[0036] To more specific, the leakage control module **500** includes a fourth transistor T**4**, a sixth transistor T**6** and a seventh transistor T**7**. The gate terminal of the fourth transistor T**4** is connected to the second leakage control signal, the drain terminal of the fourth transistor T**4** is connected to the direct current signaling source VGL, the source terminal of the fourth transistor T**4** is connected to the drain terminal of the eighth transistor T**8**, the sixth transistor T**6** is connected between the Nth level pull-down signal ST (N) and the drain terminal of the fifth transistor T**5**. The gate terminal of the sixth transistor T**6** is connected to the Nth level common signalP (N), the drain terminal of the sixth transistor T**6** is connected to the Nth level pull-down signal ST (N). The source terminal of the sixth transistor T**6** is connected to the drain terminal of the fifth transistor T**5** and the source terminal of the fourth transistor T**4**. The seventh transistor T**7** is connected between the Nth levelgate terminal signalQ (N) and the drain terminal of the eighth transistor T**8**. The gate terminal of the seventh transistor T**7** is connected to the Nth level common signalP (N), the drain terminal of the seventh transistor T**7** is connected to the Nth levelgate terminal signalQ (N) and the source terminal of the seventh transistor T**7** is connected to the drain terminal of the eighth transistor T**8**. In this embodiment, the second leakage control signal is a Nth level pull-down signal ST (N).

[0037] Wherein in the valid period of the Nth level scanning signal G (N), the Nth level clock signal line CKn is from low electric level to high electric level. The Nth level pull-down signal ST (N) and the Nth levelgate terminal signalQ (N) is output in a high electric level. The Nth level pull-down signal ST (N) and the Nth level gate terminal signal Q (N) is output in a high electric level. The drain terminals of the sixth transistor T**6** and the seventh transistor T**7** is effected by the fourth transistor T**4** to a high electric level and the Vgs of the sixth transistor T**6** and the seventh transistor T**7** is smaller than **0** to block the Nth levelgate terminal signalQ (N) of the leakage pathway through the eighth transistor T**8** and the Nth level pull-down signal ST (N) of the leakage pathway through the fifth transistor T**5**.

[0038] Those skilled in the art can understand, in the embodiment, the leakage control module **500** includes the fourth transistor T**4**, the sixth transistor T**6** and the seventh transistor T**7** to block the Nth levelgate terminal signalQ (N) of the leakage pathway through the eighth transistor T**8** and

the Nth level pull-down signal ST (N) of the leakage pathway through the fifth transistor T**5**. In other embodiment, the leakage control module **500** can only include the fourth transistor T**4** and the sixth transistor T**6** to block the Nth levelgate terminal signalQ (N) of the leakage pathway through the fifth transistor T**5**. Besides the leakage control module **500** can only include the fourth transistor T**4** and the seventh transistor T**7** to block the Nth levelgate terminal signalQ (N) of the leakage pathway through the eighth transistor T**8**.

[0039] The pull-down circuit **600** includes a ninth transistor T**9**, a tenth transistor T**10**, an eleventh transistor T**11**, a twelfth transistor T**12**, a thirteenth transistor T**13** and a fourteenth transistor T**14**. Wherein the gate terminal of the ninth transistor T**9** is connected to the Nth pull-down signal ST (N), the source terminal of the ninth transistor T**9** is connected to the a second low direct current voltage source (VGL**2**). The drain terminal of the ninth transistor T**9** is connected to the Nth level common signal P (N), the gate terminal of the tenth transistor T**10** is connected to the N−1th level pull-down signal ST (N−1), the source terminal of the tenth transistor T**10** is connected to the second low direct current voltage source (VGL**2**), the drain terminal of the tenth transistor T**10** is connected to the Nth level common signal P (N). The gate terminal of the eleventh transistor T**11** is connected to the N−1th level pull-down signal ST (N−1), the source terminal of the eleventh transistor T**11** is connected to the second low direct current voltage source (VGL**2**). The drain terminal of the eleventh transistor T**11** is connected to the source terminal of the twelfth transistor T**12**, the gate terminal of the twelfth transistor T**12** is connected to the N−1th level clock signal line CKn-**1**. The drain terminal of the twelfth transistor T**12** is connected to the gate terminal of the thirteenth transistor T**13** and the source terminal of the fourteenth transistor T**14**, the source terminal of the thirteenth transistor T**13** is connected to the Nth level common signal P (N), the drain terminals of the thirteenth transistor T**13** and the fourteenth transistor T**14** are connected to the direct current signaling source VGL, the gate terminal of the fourteenth transistor T**14** is connected to the N+2th level clock signal line CKn+**2**.

[0040] In this embodiment, the electric potential of the first low direct current voltage source (VGL**1**) is smaller than the electric potential of the second low direct current voltage source (VGL**2**). The lower electric potential of the N−1th level pull-down signal ST (N-**1**), the Nth level pull-down signal ST (N) are smaller than the electric potential of the of the second low direct current voltage source (VGL**2**) and makes the Nth level pull-down signal ST (N) in an invalid period and the Nth level common signal P (N) in the high electric potential period, the Vgs of the ninth transistor T**9**, the tenth transistor T**10**, the eleventh transistor T**11** are smaller than 0 to block the leakage pathway of the Nth common signal P (N) through the ninth transistor T**9**, the tenth transistor T**10**, the eleventh transistor T**11** to maintain the Nth common signal P (N) in a high electric potential.

[0041] In this embodiment, when the Nth level clock signal line CKn is in first clock signal CK**1**, the N+2th level clock signal line CKn+**2** is in third clock signal CK**3**, the N−1th level clock signal line CKn-**1** is in fourth clock signal CK**4**.

[0042] In one preferred embodiment, the Nth level GOA unit **11** further includes a filter capacitor C**1** and a bootstrap capacitor C**2**. One terminal of the filter capacitor C**1** is connected to the Nth level common signal P (N), another terminal of the filter capacitor C**1** is connected to the second low direct current voltage source (VGL**2**). One terminal of the bootstrap capacitor C**2** is connected to the Nth level gate terminal signal Q (N), another terminal of the bootstrap capacitor C**2** is connected to the Nth level pull-down signal ST (N).

[0043] Referring to FIG. **3**, it is a timing diagram of the GOA circuit structure. As illustrated in FIG. **3**, the valid period of the Nth level GOA includes:

[0044] In the T**1** stage, the N−1th level pull-down signal ST (N-**1**) and the N−1 gate terminal signal Q (N-**1**) is in high electric potential, the first transistor T**1**, the second transistor T**2** and the third transistor T**3** are open and make the Nth levelgate terminal signalQ (N) in high electric potential. The tenth transistor T**10**, the eleventh transistor T**11** and the twelfth transistor T**12** are open, and the thirteenth transistor T**13** is close to make the Nth level common signal P (N) in a low electric potential.

[0045] In the T**2** stage, the Nth level clock signal line CKn so as the first clock signal CK**1** is from a low electric potential to a high electric potential, the Nth level pull-down signal ST (N) output a high electric potential to drive the N+1 GOA unit, and the Nth levelgate terminal signalQ (N) output a high electric potential to charge the Nth level horizontal scanning line in the corresponding display zone. In the meantime, the drain terminal of the first transistor T**1** input the N−1 gate terminal signalQ (N-**1**) is in a high electric potential to make the Vgs of the first transistor T**1** smaller than 0 to block the Nth levelgate terminal signalQ (N) from the leakage pathway of the first transistor T**1**. The drain terminals of the sixth transistor T**6** and the seventh transistor T**7** are in a high electric potential to make the Vgs of the sixth transistor T**6** and the seventh transistor T**7** smaller than 0 to block the Nth levelgate terminal signalQ (N) from the leakage pathway of the eighth transistor T**8** and block the Nth level pull-down signal ST (N) from the leakage pathway of the fifth transistor T**5**.

[0046] In the T**3** stage, the Nth level clock signal line CKn so as the first clock signal CK**1** is from a high electric potential to a low electric potential. In the meantime, the Nth levelgate terminal signalQ (N) is in a high electric potential and the Nth level common P (N) in a low electric potential.

[0047] In the T**4** stage, the N+2th level clock signal line CKn+**2** so as the third clock signal CK**3** is in a high electric potential, the thirteenth transistor T**13** and the fourteenth transistor T**14** are open and make the Nth level common signal P (N) in high electric potential. The fifth transistor T**5**, the sixth transistor T**6**, the seventh transistor T**7** and the eighth transistor T**8** are open to make the Nth level pull-down signal ST (N) and the Nth level common signal Q (N) in a low electric potential. In the meantime, the electric potential of the first low direct current voltage source (VGL**1**) is smaller than the electric potential of the second low direct current voltage source (VGL**2**). The lower electric potential of the N−1th level pull-down signal ST (N-**1**), the Nth level pull-down signal ST (N) are smaller than the electric potential of the of the second low direct current voltage source (VGL**2**) and makes the Vgs of the ninth transistor T**9**, the tenth transistor T**10** and the eleventh transistor T**11** are smaller than 0 to block the leakage pathway of the Nth level common signal P (N) through the ninth transistor T**9**, the tenth transistor T**10** and the eleventh transistor T**11**.

[0048] FIG. **4** is a circuit diagram of the GOA circuit structure illustrated in FIG. **1** according to the second embodiment of the present invention. As the second embodiment illustrated in FIG. **4**, the difference between the first embodiments illustrated in FIG. **2** is as followed. The gate terminal of the fourth transistor T**4** illustrated in FIG. **4** is connected to the N−1th level gate terminal signal Q (N-**1**) and the gate terminal of the fourth transistor T**4** illustrated in FIG. **2** is connected to the Nth level pull-down signal ST (N).

[0049] Wherein in the T**1** stage illustrated in FIG. **3**, since the N−1th level gate terminal signal Q (N-**1**) connected to the gate terminal of the fourth transistor T**4** is in a high electric potential to make the Vgs of the seventh transistor T**7** smaller than 0 and the Nth levelgate terminal signalQ (N) becomes a high electric potential to block the leakage pathway through the Nth levelgate terminal signalQ (N) usually.

[0050] FIG. **5** is a schematic view illustrating the liquid crystal display structure according to the embodiment of the present invention. As illustrated in FIG. **5**, the liquid crystal display structure includes the GOA circuit **10** mentioned above.

[0051] The advantage of this application is by adding the leakage control module between the Nth level gate terminal signal and the eighth transistor T**8** and/or the Nth level pull-down signal and the fifth transistor T**5** into the GOA circuit and the liquid crystal display structure to achieving of leakage blocking. In the valid period of the Nth level scanning signal, the Nth level gate terminal signal through the leakage pathway from the eighth transistor T**8** and/or the leakage pathway through the Nth level pull-down signal through the fifth transistor T**5** is blocked and enhance the stability of the GOA circuit.

[0052] It will be apparent to those having ordinary skill in the art that various modifications and variations can be made to the devices in accordance with the present disclosure without departing from the scope or spirit of the disclosure. In view of the foregoing, it is intended that the present disclosure covers modifications and variations of this disclosure provided they fall within the scope of the following claims and their equivalents.

[0053] Although the drawings and the illustrations above are corresponding to the specific embodiments individually, the element, the practicing method, the designing principle, and the technical theory can be referred, exchanged, incorporated, collocated, coordinated except they are conflicted, incompatible, or hard to be put into practice together.

[0054] Although the present application has been explained above, it is not the limitation of the range, the sequence in practice, the material in practice, or the method in practice. Any modification or decoration for present application is not detached from the spirit and the range of such.

What is claimed is:

1. A GOA circuit for liquid crystal display, the GOA circuit comprising a plurality of GOA unit connected in series, wherein a Nth level GOA unit including a pull-up control module, a pull-down module, a pull-up module, a pull-down holding module and a leakage control module;

wherein the pull-up control module including a first transistor, a gate terminal of the first transistor is connected to a N−1th level pull-down signal, a drain terminal of the first transistor is connected to the first leakage control signal and the source terminal of the first transistor is connected to the Nth levelgate terminal signal;

wherein the pull-down module including a second transistor, the gate terminal of the second transistor is connected to the Nth levelgate terminal signal, the drain terminal of the second transistor is connected to the Nth level clock signal line, and the source terminal of the second transistor output the Nth level pull-down signal;

wherein the pull-up module including a third transistor, the gate terminal of the third transistor is connected to the Nth levelgate terminal signal, the drain terminal of the third transistor is connected to the Nth level clock signal line, and the source terminal of the third transistor output the Nth level scanning signal;

wherein the pull-down holding module including a fifth transistor and a eighth transistor, the gate terminal of the fifth transistor is connected to the Nth level common signal, the drain terminal of the fifth transistor is connected to the Nth level pull-down signal, the source terminal of the fifth transistor is connected to a first low direct current voltage source; and the gate terminal of the eighth transistor is connected to the Nth level common signal, the source terminal of the eighth transistor is connected to the first low direct current voltage source and the drain terminal of the eighth transistor is connected to the Nth levelgate terminal signal;

wherein the leakage control module is connected in series between the Nth level gate terminal signal and the eighth transistor and/or between the Nth level pull-down signal and the fifth transistor; in the valid period of the Nth level scanning signal, a second leakage control signal is to block the Nth level gate terminal signal through the leakage pathway of the eighth transistor and/or to block the Nth level pull-down signal through the leakage pathway of the fifth transistor;

wherein the leakage control module further including a fourth transistor and a seventh transistor, the gate terminal of the fourth transistor is connected to the second leakage control signal, the drain terminal of the fourth transistor is connected to the direct current signaling source, the source terminal of the fourth transistor is connected to the drain terminal of the eighth transistor; the seventh transistor is connected between the Nth levelgate terminal signal and the drain terminal of the eighth transistor, the gate terminal of the seventh transistor is connected to the Nth level common signal, the drain terminal of the seventh transistor is connected to the Nth levelgate terminal signal and the source terminal of the seventh transistor is connected to the drain terminal of the eighth transistor to block the Nth levelgate terminal signal through the leakage pathway of the eighth transistor in the valid period of the Nth level scanning signal;

wherein the first leakage control signal is the N−1th level gate terminal signal and to block the Nth levelgate terminal signal through the leakage pathway of the first transistor in the valid period of the Nth level scanning signal.

2. The GOA circuit according to claim **1**, wherein the second leakage control signal is the Nth level pull-down signal.

3. A GOA circuit for liquid crystal display, the GOA circuit comprising a plurality of GOA unit connected in series, wherein a Nth level GOA unit including a pull-up control module, a pull-down module, a pull-up module, a pull-down holding module and a leakage control module;

wherein the pull-up control module including a first transistor, a gate terminal of the first transistor is connected to a N−1th level pull-down signal, a drain terminal of the first transistor is connected to the first leakage control signal and the source terminal of the first transistor is connected to the Nth levelgate terminal signal;

wherein the pull-down module including a second transistor, the gate terminal of the second transistor is connected to the Nth levelgate terminal signal, the drain terminal of the second transistor is connected to the Nth level clock signal line, and the source terminal of the second transistor output the Nth level pull-down signal;

wherein the pull-up module including a third transistor, the gate terminal of the third transistor is connected to the Nth levelgate terminal signal, the drain terminal of the third transistor is connected to the Nth level clock signal line, and the source terminal of the third transistor output the Nth level scanning signal;

wherein the pull-down holding module including a fifth transistor and a eighth transistor, the gate terminal of the fifth transistor is connected to the Nth level common signal, the drain terminal of the fifth transistor is connected to the Nth level pull-down signal, the source terminal of the fifth transistor is connected to a first low direct current voltage source; and the gate terminal of the eighth transistor is connected to the Nth level common signal, the source terminal of the eighth transistor is connected to the first low direct current voltage source and the drain terminal of the eighth transistor is connected to the Nth levelgate terminal signal;

wherein the leakage control module is connected in series between the Nth level gate terminal signal and the eighth transistor and/or between the Nth level pull-down signal and the fifth transistor; in the valid period of the Nth level scanning signal, a second leakage control signal is to block the Nth level gate terminal signal through the leakage pathway of the eighth transistor and/or to block the Nth level pull-down signal through the leakage pathway of the fifth transistor.

4. The GOA circuit according to claim 3, wherein the leakage control module further including a fourth transistor and a seventh transistor, the gate terminal of the fourth transistor is connected to the second leakage control signal, the drain terminal of the fourth transistor is connected to the direct current signaling source, the source terminal of the fourth transistor is connected to the drain terminal of the eighth transistor; the seventh transistor is connected between the Nth levelgate terminal signal and the drain terminal of the eighth transistor, the gate terminal of the seventh transistor is connected to the Nth level common signal, the drain terminal of the seventh transistor is connected to the Nth levelgate terminal signal and the source terminal of the seventh transistor is connected to the drain terminal of the eighth transistor to block the Nth levelgate terminal signal through the leakage pathway of the eighth transistor in the valid period of the Nth level scanning signal.

5. The GOA circuit according to claim 4, wherein the second leakage control signal is the Nth level pull-down signal.

6. The GOA circuit according to claim 4, wherein the second leakage control signal is the N−1th level gate terminal signal.

7. The GOA circuit according to claim 4, wherein the leakage control module further comprising a sixth transistor, wherein the sixth transistor is connected between the Nth level pull-down signal and the drain terminal of the fifth transistor, the gate terminal of the sixth transistor is connected to the Nth level common signal, the drain terminal of the sixth transistor is connected to the Nth level pull-down signal, the source terminal of the sixth transistor is connected to the drain terminal of the fifth transistor and the source terminal of the fourth transistor to block the Nth level pull-down signal through the leakage pathway of the fifth transistor in the valid period of the Nth level scanning signal.

8. The GOA circuit according to claim 3, wherein the first leakage control signal is the N−1th level gate terminal signal to block the Nth levelgate terminal signal through the leakage pathway of the first transistor in the valid period of the Nth level scanning signal.

9. The GOA circuit according to claim 3, wherein the Nth level GOA unit further comprising a pull-down module, the pull-down module comprising a ninth transistor, a tenth transistor, an eleventh transistor, a twelfth transistor, a thirteenth transistor and a fourteenth transistor; wherein the gate terminal of the ninth transistor is connected to the Nth level pull-down signal, the source terminal of the ninth transistor is connected to the a second low direct current voltage source, the drain terminal of the ninth transistor is connected to the Nth level common signal, the gate terminal of the tenth transistor is connected to the N−1th level pull-down signal, the source terminal of the tenth transistor is connected to the second low direct current voltage source, the drain terminal of the tenth transistor is connected to the Nth level common signal, the gate terminal of the eleventh transistor is connected to the N−1th level pull-down signal, the source terminal of the eleventh transistor is connected to the second low direct current voltage source, the drain terminal of the eleventh transistor is connected to the source terminal of the twelfth transistor, the gate terminal of the twelfth transistor is connected to the N−1th level clock signal line, the drain terminal of the twelfth transistor is connected to the gate terminal of the thirteenth transistor and the source terminal of the fourteenth transistor, the source terminal of the thirteenth transistor is connected to the Nth level common signal, the drain terminals of the thirteenth transistor and the fourteenth transistor are connected to the direct current signaling source, the gate terminal of the fourteenth transistor is connected to the N+2th level clock signal line.

10. The GOA circuit according to claim 9, wherein the electric potential of the first low direct current voltage source is smaller than the electric potential of the second low direct current voltage source, the lower electric potential of the N−1th level pull-down signal, the Nth level pull-down signal are smaller than the electric potential of the of the second low direct current voltage source to block the leakage pathway of the Nth level common signal through the ninth transistor, the tenth transistor, the eleventh transistor in the invalid period of the Nth level scanning signal.

11. The GOA circuit according to claim 9, the Nth level GOA unit received a first clock signal, a second clock signal, a third clock signal, and a fourth clock signal, and the first clock signal, the second clock signal, the third clock signal, and the fourth clock signal CK4 are timely valid in orderly during one working period, wherein when the Nth level clock signal line is the first clock signal, the N+2 clock signal line is the third clock signal and the N−1 clock signal line is the fourth clock signal.

12. A liquid crystal display having a GOA circuit, the GOA circuit comprising a plurality of GOA unit connected in series, wherein a Nth level GOA unit including a pull-up control module, a pull-down module, a pull-up module, a pull-down holding module and a leakage control module;

wherein the pull-up control module including a first transistor, a gate terminal of the first transistor is connected to a N−1th level pull-down signal, a drain terminal of the first transistor is connected to the first leakage control signal and the source terminal of the first transistor is connected to the Nth levelgate terminal signal;

wherein the pull-down module including a second transistor, the gate terminal of the second transistor is connected to the Nth levelgate terminal signal, the drain terminal of the second transistor is connected to the Nth level clock signal line, and the source terminal of the second transistor output the Nth level pull-down signal;

wherein the pull-up module including a third transistor, the gate terminal of the third transistor is connected to the Nth levelgate terminal signal, the drain terminal of the third transistor is connected to the Nth level clock signal line, and the source terminal of the third transistor output the Nth level scanning signal;

wherein the pull-down holding module including a fifth transistor and a eighth transistor, the gate terminal of the fifth transistor is connected to the Nth level common signal, the drain terminal of the fifth transistor is connected to the Nth level pull-down signal, the source terminal of the fifth transistor is connected to a first low direct current voltage source; and the gate terminal of the eighth transistor is connected to the Nth level common signal, the source terminal of the eighth transistor is connected to the first low direct current voltage source and the drain terminal of the eighth transistor is connected to the Nth levelgate terminal signal;

wherein the leakage control module is connected in series between the Nth level gate terminal signal and the eighth transistor and/or between the Nth level pull-down signal and the fifth transistor; in the valid period of the Nth level scanning signal, a second leakage control signal is to block the Nth level gate terminal signal through the leakage pathway of the eighth transistor and/or to block the Nth level pull-down signal through the leakage pathway of the fifth transistor.

13. The liquid crystal display according to claim 12, wherein the leakage control module further including a fourth transistor and a seventh transistor, the gate terminal of the fourth transistor is connected to the second leakage control signal, the drain terminal of the fourth transistor is connected to the direct current signaling source, the source terminal of the fourth transistor is connected to the drain terminal of the eighth transistor; the seventh transistor is connected between the Nth levelgate terminal signal and the drain terminal of the eighth transistor, the gate terminal of the seventh transistor is connected to the Nth level common signal, the drain terminal of the seventh transistor is connected to the Nth levelgate terminal signal and the source terminal of the seventh transistor is connected to the drain terminal of the eighth transistor to block the Nth levelgate terminal signal through the leakage pathway of the eighth transistor in the valid period of the Nth level scanning signal.

14. The liquid crystal display according to claim 13, wherein the second leakage control signal is the Nth level pull-down signal.

15. The liquid crystal display according to claim 13, wherein the second leakage control signal is the N−1th level gate terminal signal.

16. The liquid crystal display according to claim 13, wherein the leakage control module further comprising a sixth transistor, wherein the sixth transistor is connected between the Nth level pull-down signal and the drain terminal of the fifth transistor, the gate terminal of the sixth transistor is connected to the Nth level common signal, the drain terminal of the sixth transistor is connected to the Nth level pull-down signal, the source terminal of the sixth transistor is connected to the drain terminal of the fifth transistor and the source terminal of the fourth transistor to block the Nth level pull-down signal through the leakage pathway of the fifth transistor in the valid period of the Nth level scanning signal.

17. The liquid crystal display according to claim 12, wherein the first leakage control signal is the N−1th level gate terminal signal to block the Nth levelgate terminal signal through the leakage pathway of the first transistor in the valid period of the Nth level scanning signal.

18. The liquid crystal display according to claim 12, wherein the Nth level GOA unit further comprising a pull-down module, the pull-down module comprising a ninth transistor, a tenth transistor, an eleventh transistor, a twelfth transistor, a thirteenth transistor and a fourteenth transistor; wherein the gate terminal of the ninth transistor is connected to the Nth level pull-down signal, the source terminal of the ninth transistor is connected to the a second low direct current voltage source, the drain terminal of the ninth transistor is connected to the Nth level common signal, the gate terminal of the tenth transistor is connected to the N−1th level pull-down signal, the source terminal of the tenth transistor is connected to the second low direct current voltage source, the drain terminal of the tenth transistor is connected to the Nth level common signal, the gate terminal of the eleventh transistor is connected to the N−1th level pull-down signal, the source terminal of the eleventh level transistor is connected to the second low direct current voltage source, the drain terminal of the eleventh transistor is connected to the source terminal of the twelfth transistor, the gate terminal of the twelfth transistor is connected to the N−1th level clock signal line, the drain terminal of the twelfth transistor is connected to the gate terminal of the thirteenth transistor and the source terminal of the fourteenth transistor, the source terminal of the thirteenth transistor is connected to the Nth level common signal, the drain terminals of the thirteenth transistor and the fourteenth transistor are connected to the direct current signaling source, the gate terminal of the fourteenth transistor is connected to the N+2th level clock signal line.

19. The liquid crystal display according to claim **18**, wherein the electric potential of the first low direct current voltage source is smaller than the electric potential of the second low direct current voltage source, the lower electric potential of the N−1th level pull-down signal, the Nth level pull-down signal are smaller than the electric potential of the of the second low direct current voltage source to block the leakage pathway of the Nth level common signal through the ninth transistor, the tenth transistor, the eleventh transistor in the invalid period of the Nth level scanning signal.

20. The liquid crystal display according to claim **18**, the Nth level GOA unit received a first clock signal, a second clock signal, a third clock signal, and a fourth clock signal, and the first clock signal, the second clock signal, the third clock signal, and the fourth clock signal CK**4** are timely valid in orderly during one working period, wherein when the Nth level clock signal line is the first clock signal, the N+2 clock signal line is the third clock signal and the N−1 clock signal line is the fourth clock signal.

* * * * *

专利名称(译)	GOA电路和液晶显示器		
公开(公告)号	US20170162151A1	公开(公告)日	2017-06-08
申请号	US14/786088	申请日	2015-09-23
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IPC分类号	G09G3/36		
CPC分类号	G09G3/3677 G09G3/3696 G09G2310/0213 G09G2310/08 G09G2300/0426 G09G2300/0809 G09G2300/0408 G09G2310/0289		
优先权	201510594063.9 2015-09-17 CN		
其他公开文献	US9721520		
外部链接	Espacenet USPTO		

摘要(译)

该申请公开了一种GOA电路和一种液晶显示器。 GOA电路包括串联连接的多个GOA单元，其中第N级GOA单元包括第五晶体管，第八晶体管和泄漏控制模块。其中，泄漏控制模块串联连接在第N级栅极端子信号和第八晶体管的漏极端子之间和/或第N级下拉信号和第五晶体管的漏极端子之间;在第N级扫描信号的有效期内，可以通过第八晶体管的漏电通路阻断第N级栅极端子信号和/或通过第五晶体管的漏电通路阻断第N级栅极下拉信号，以实现稳定GOA电路。