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(19) **United States**(12) **Patent Application Publication**
TAE et al.(10) **Pub. No.: US 2019/0196257 A1**(43) **Pub. Date: Jun. 27, 2019**(54) **DISPLAY DEVICE HAVING A
NON-RECTILINEAR DISPLAY AREA****G02F 1/1362** (2006.01)**G02F 1/1343** (2006.01)(71) Applicant: **Samsung Display Co., Ltd.**, Yongin-Si
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2001/134345 (2013.01); **G02F 2001/133357**
(2013.01); **G02F 2201/123** (2013.01)(72) Inventors: **Changil TAE**, Seoul (KR); **Seungjun**
YU, Cheonan-si (KR); **Youngeoo**
SONG, Asan-si (KR)(21) Appl. No.: **16/286,306**(22) Filed: **Feb. 26, 2019**

(57)

ABSTRACT**Related U.S. Application Data**(62) Division of application No. 15/411,639, filed on Jan.
20, 2017, now Pat. No. 10,254,580.**Foreign Application Priority Data**

May 4, 2016 (KR) 10-2016-0055317

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A display device includes a first substrate; a second substrate covering the first substrate; a liquid crystal layer between the first substrate and the second substrate; a plurality of pixels on the first substrate; and a light blocking member disposed on at least one of the first substrate and the second substrate, the light blocking member disposed in a curved area and defining a display area and a non-display area. The plurality of pixels includes a first pixel outside the curved area; and a second pixel in the curved area, and a pixel electrode of the first pixel has a different shape from a shape of a pixel electrode of the second pixel.

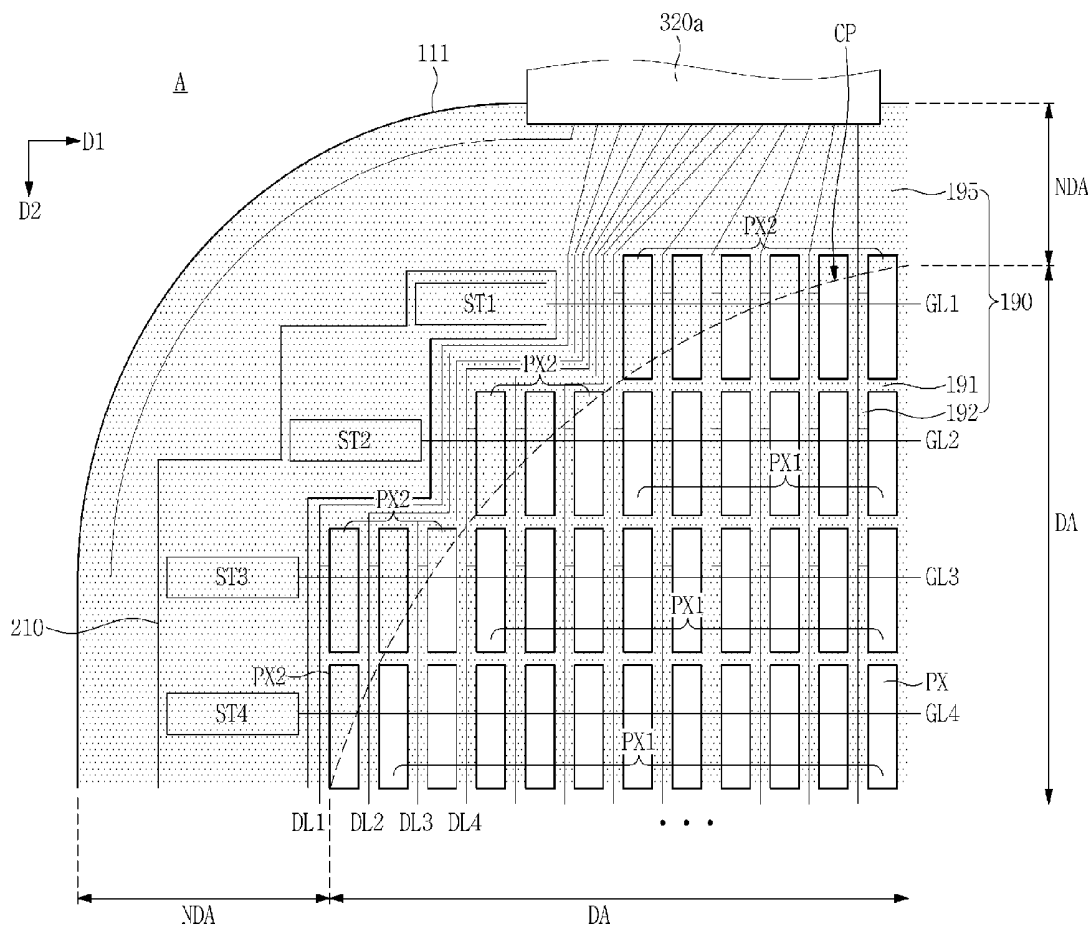


FIG. 1

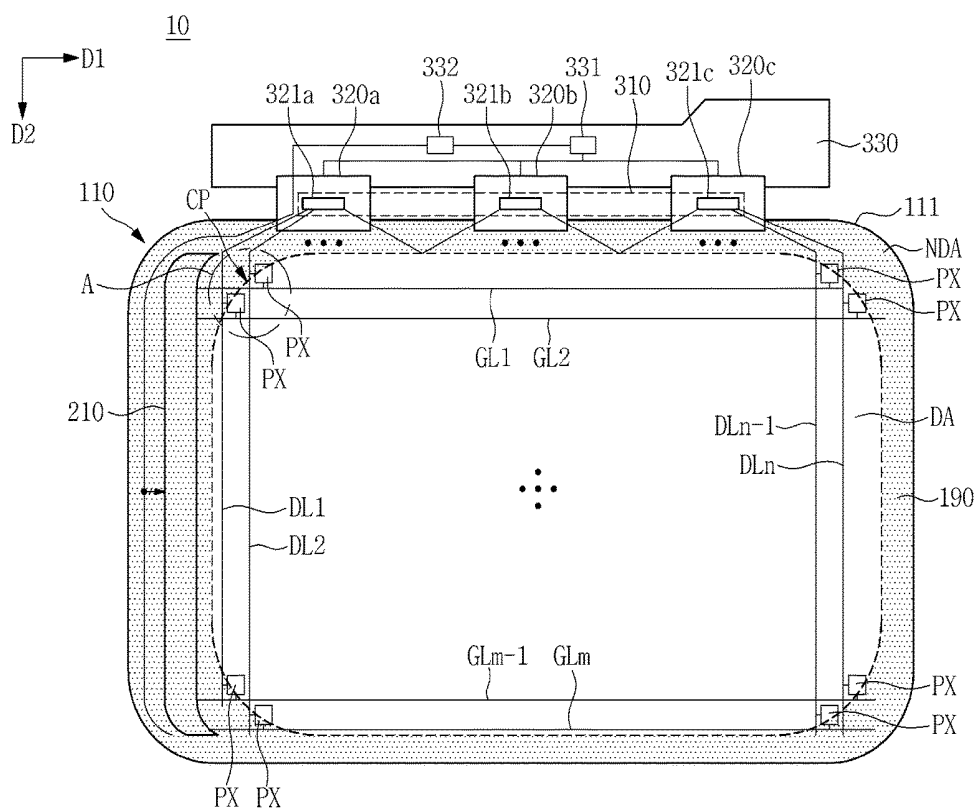


FIG. 2

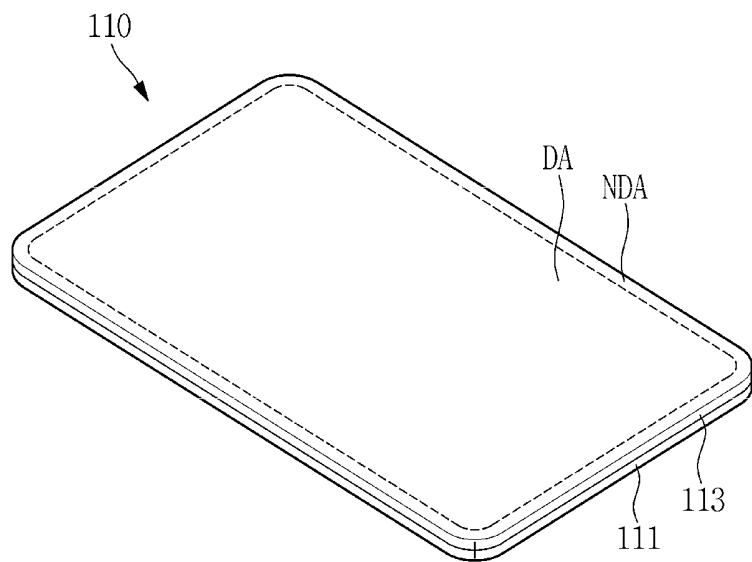


FIG. 3

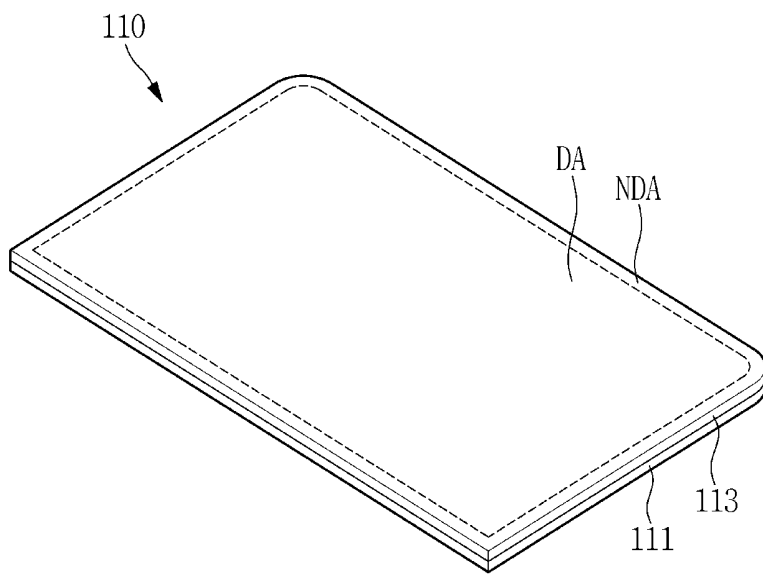


FIG. 4

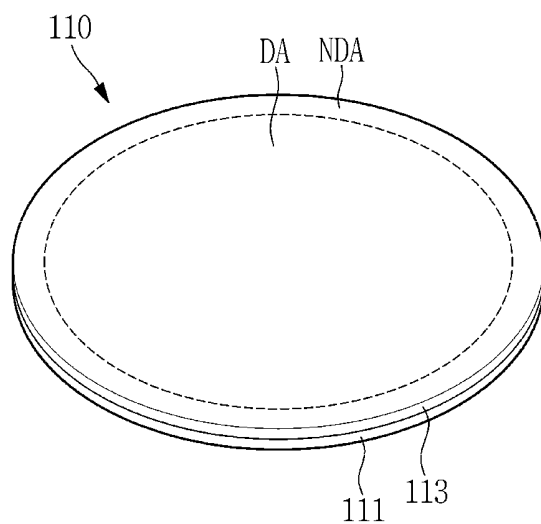


FIG. 5

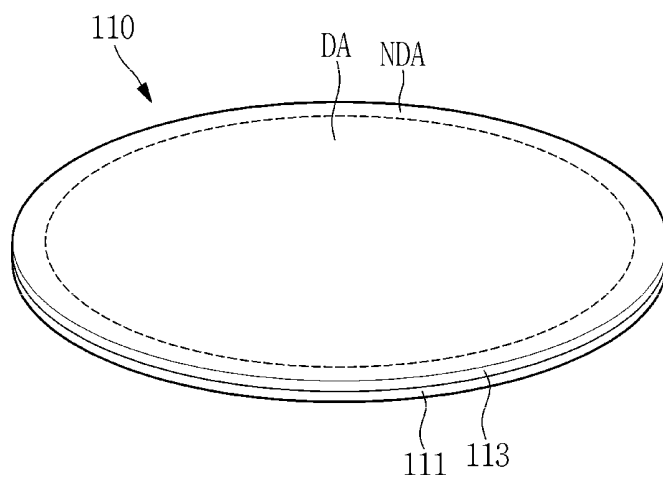


FIG. 6

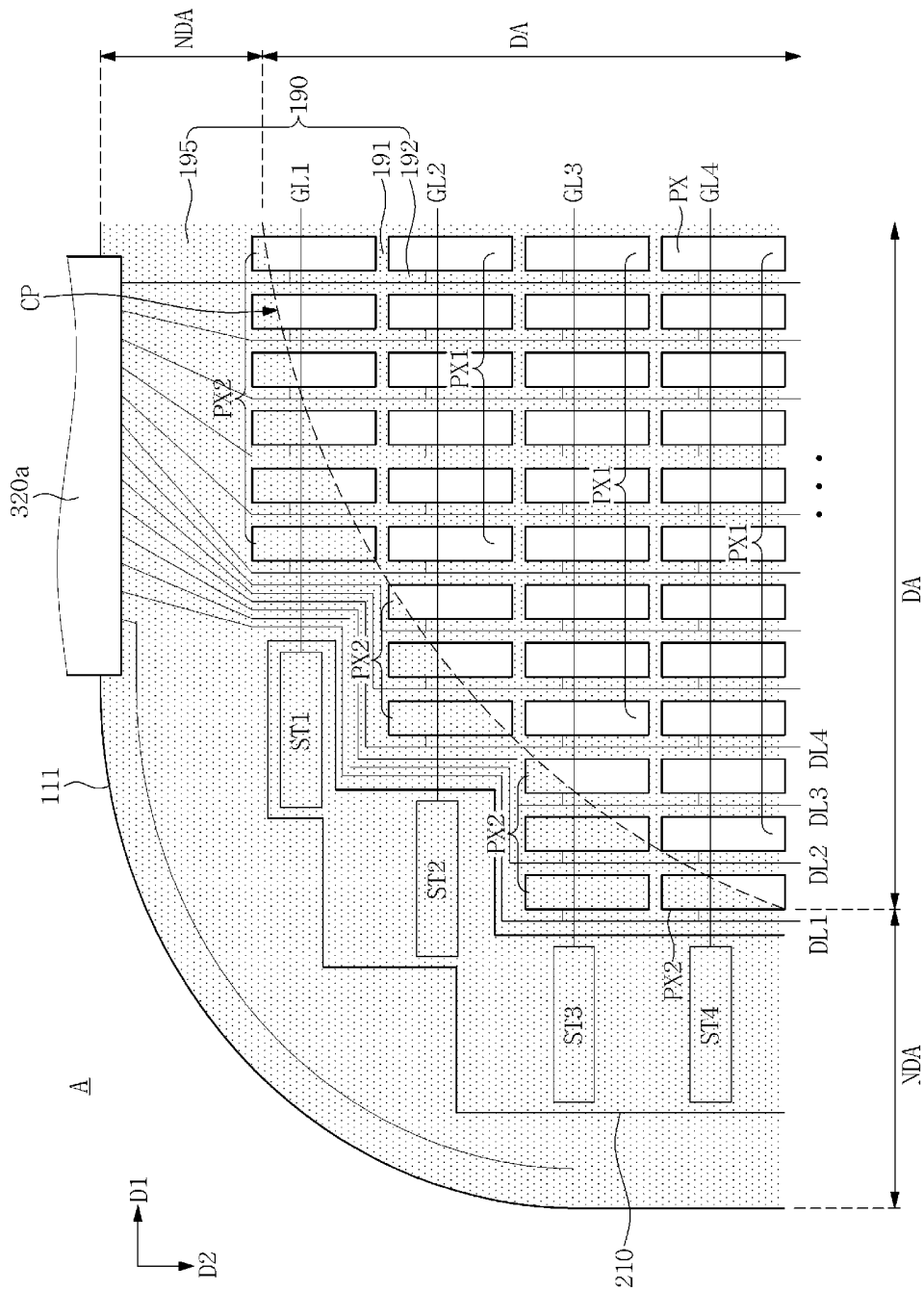


FIG. 7

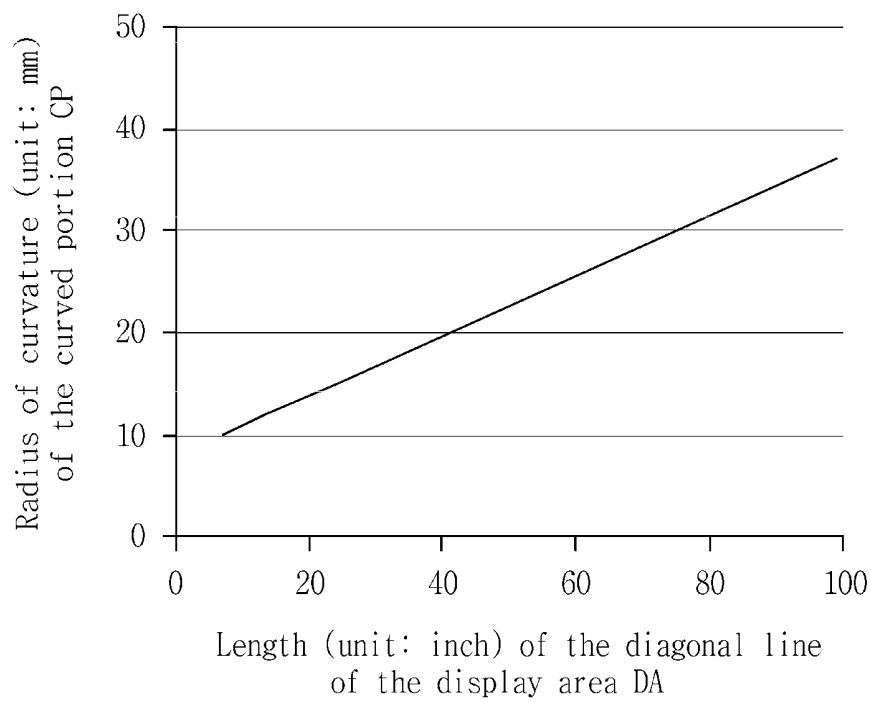


FIG. 9

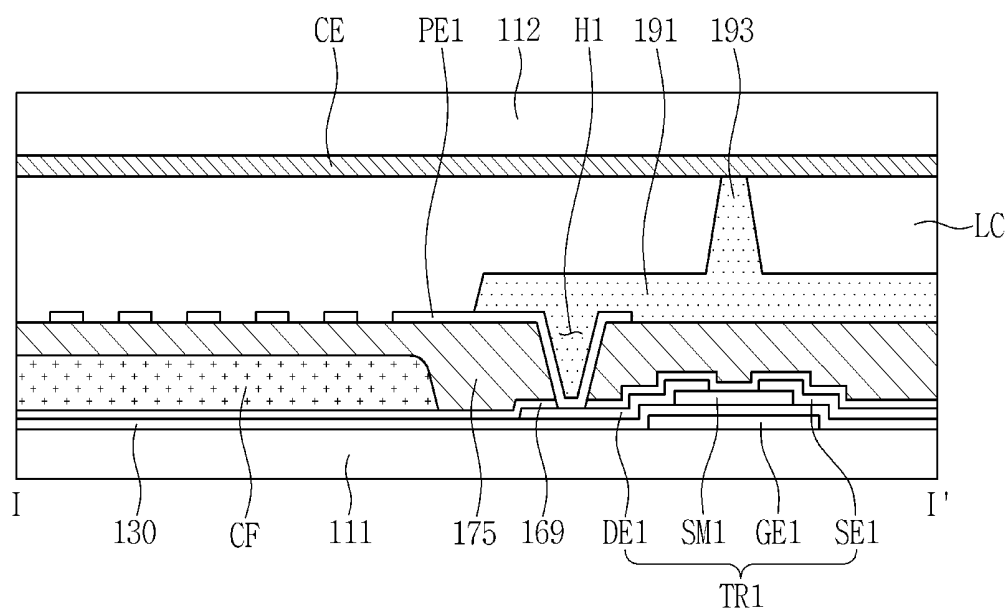


FIG. 10

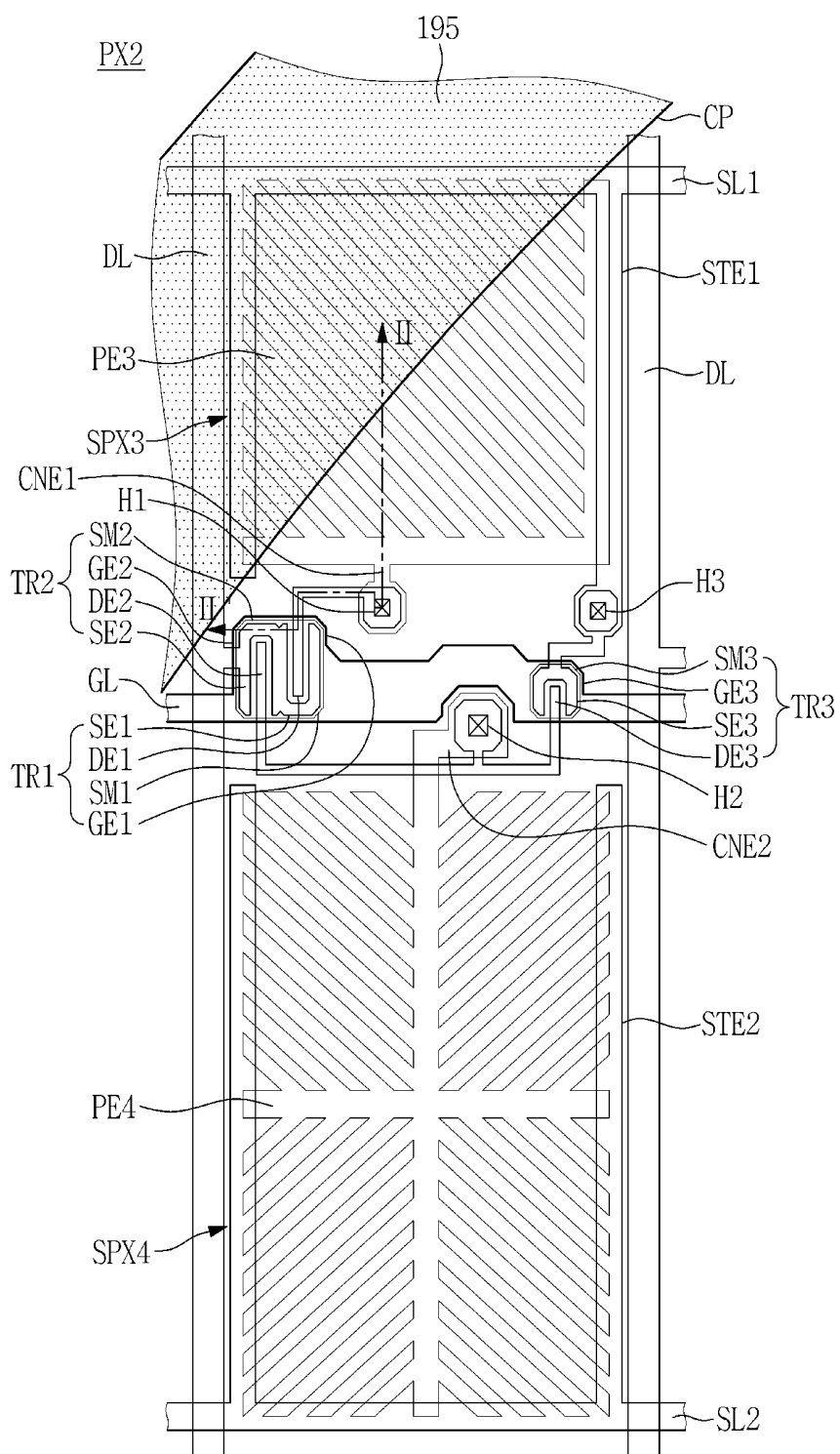


FIG. 11

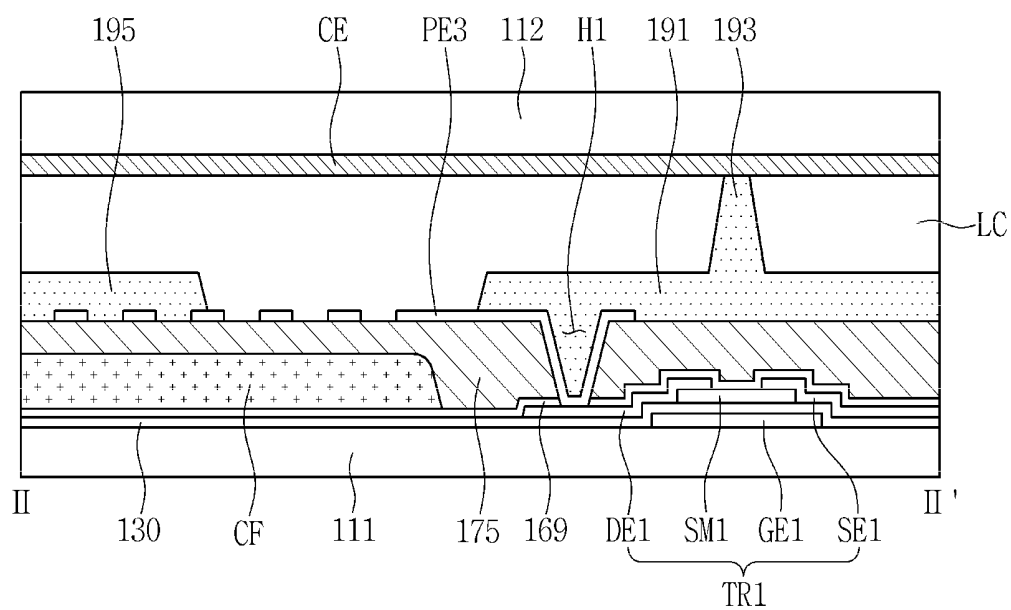


FIG. 13

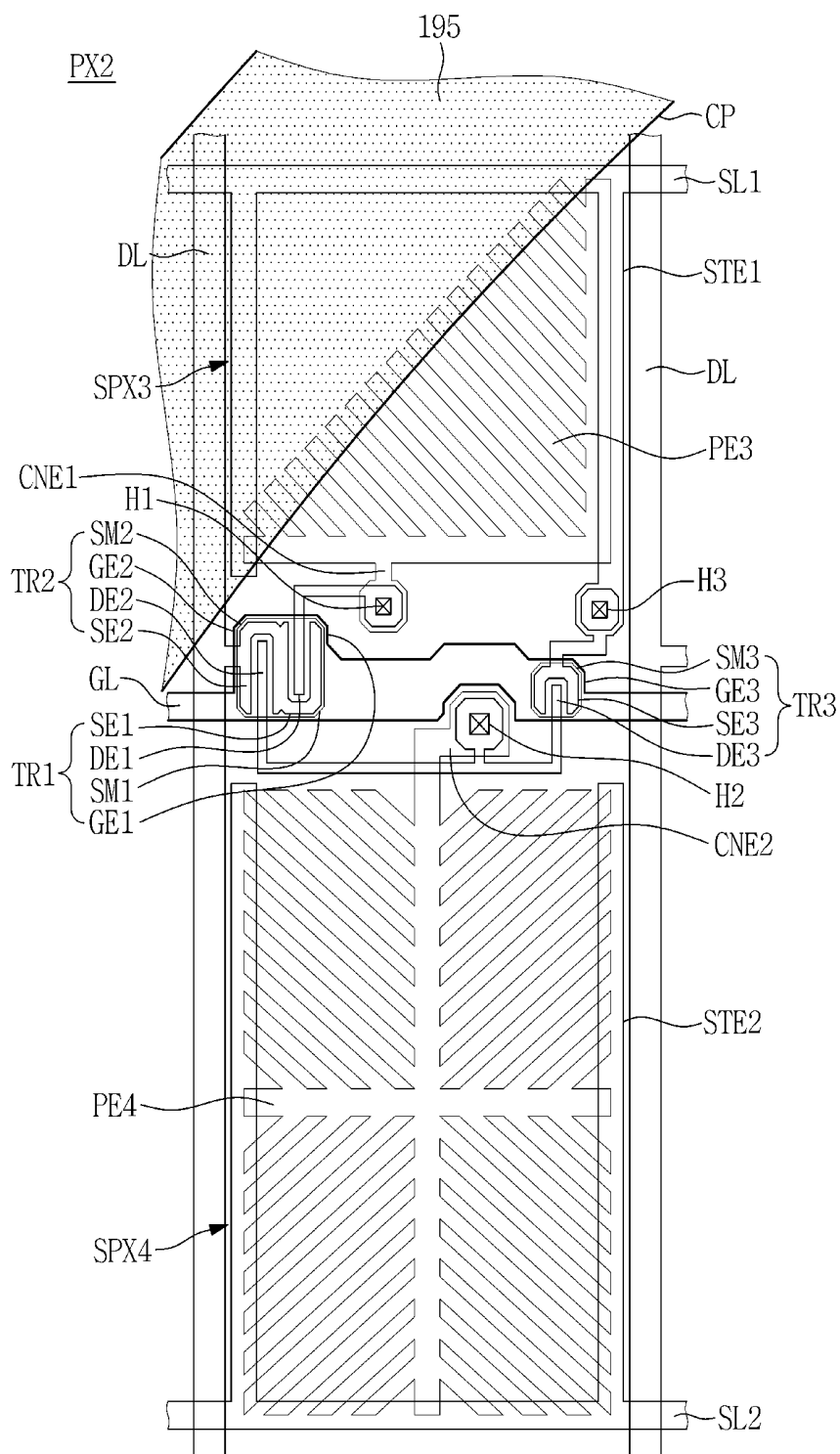


FIG. 14

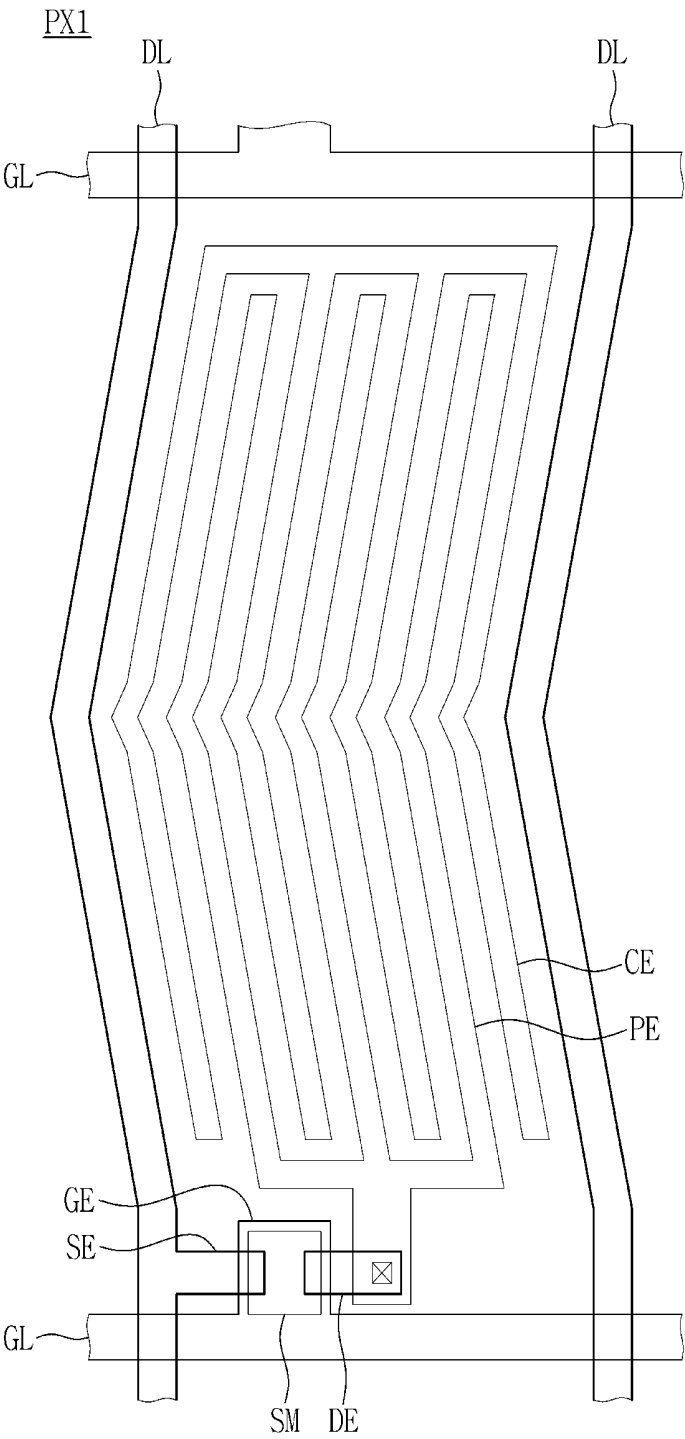


FIG. 15

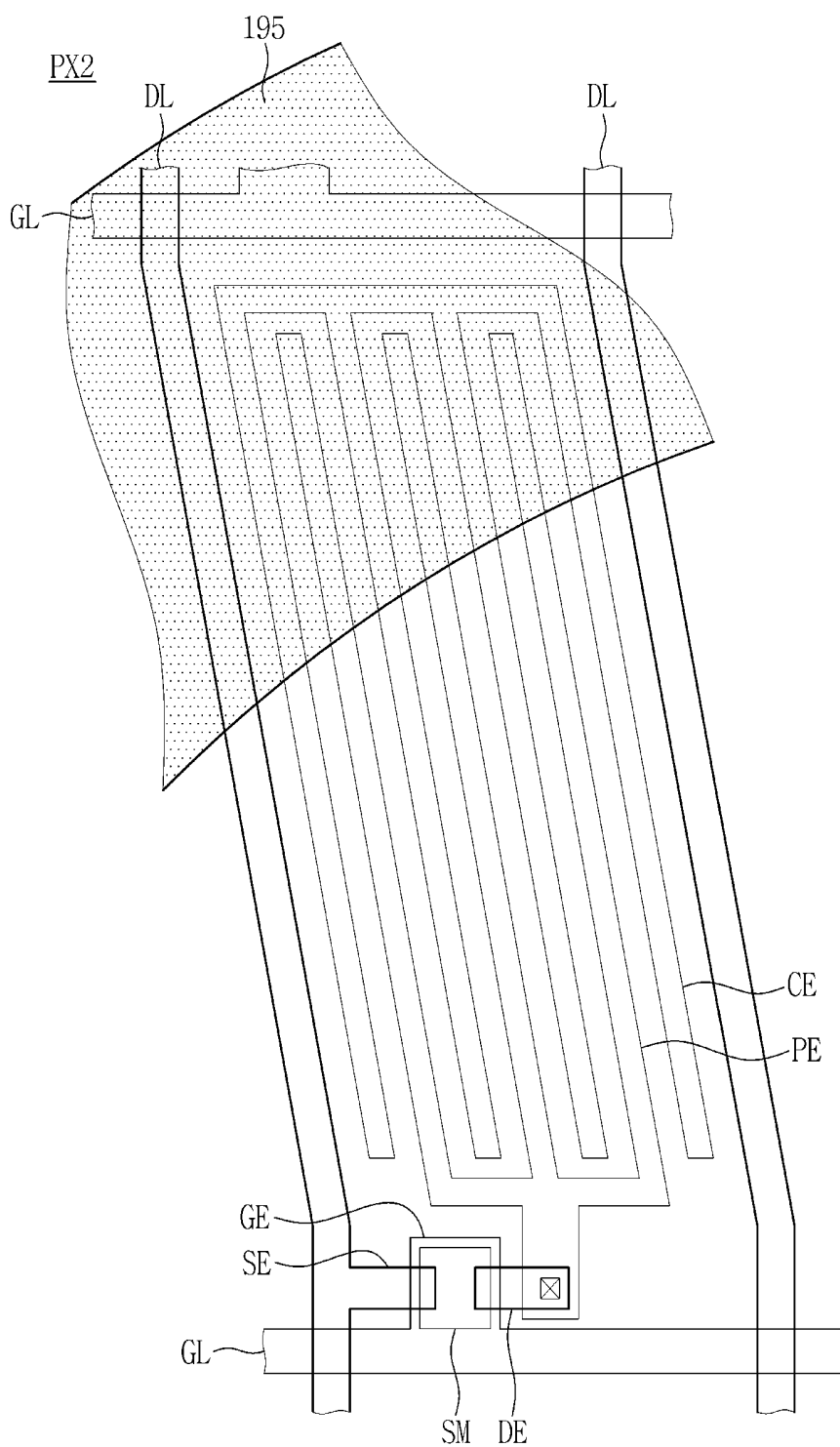


FIG. 16

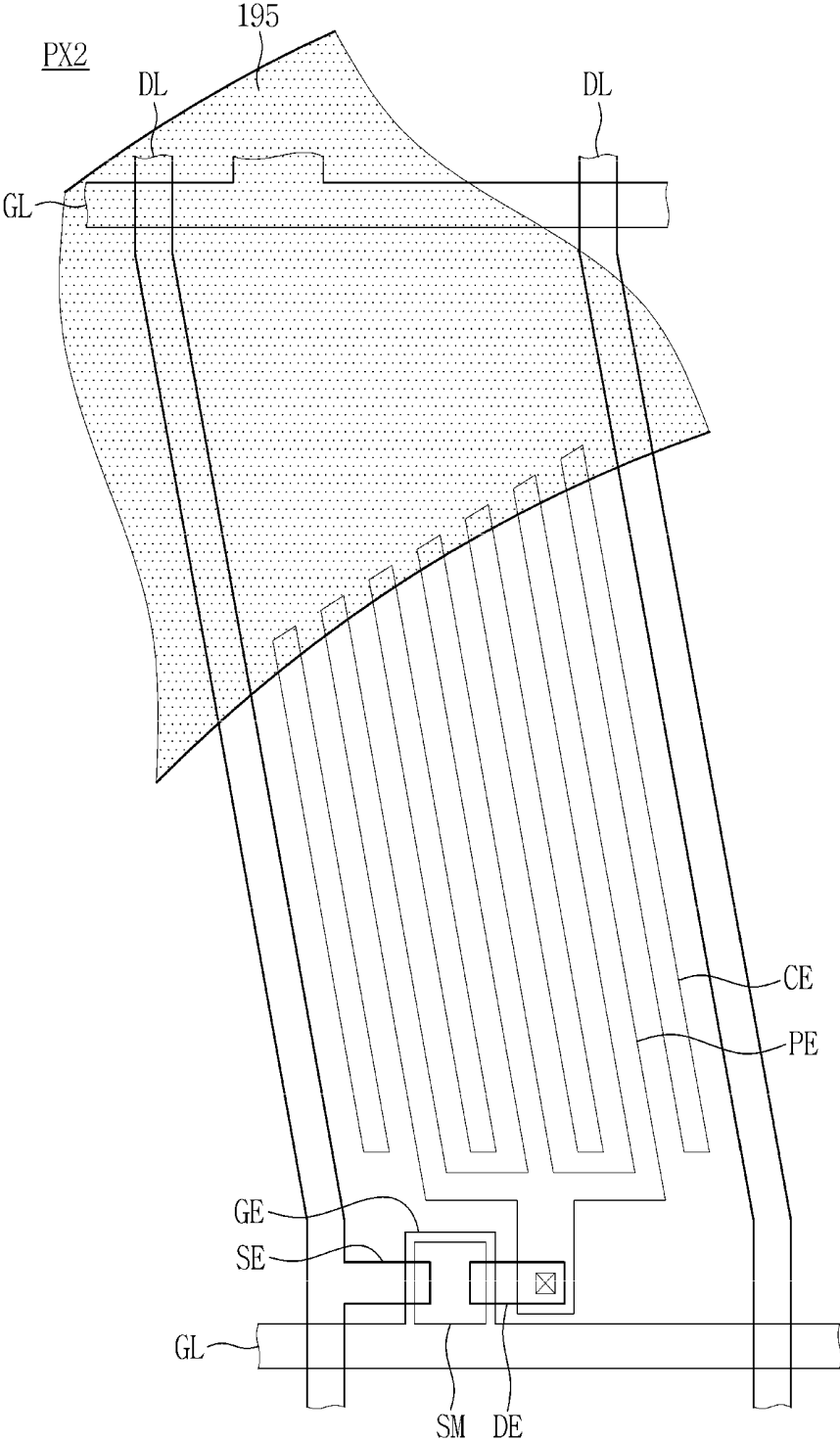


FIG. 17

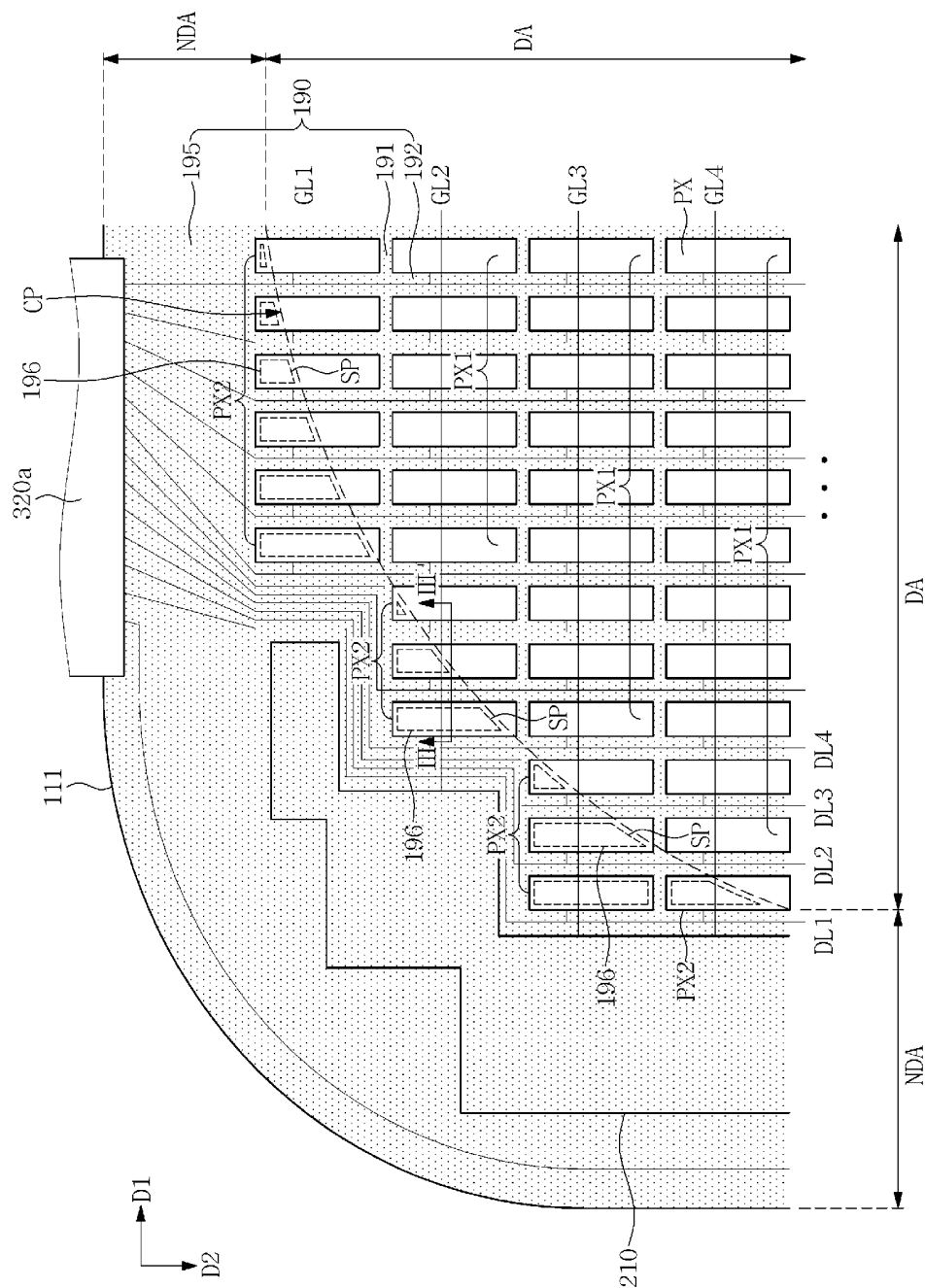


FIG. 18

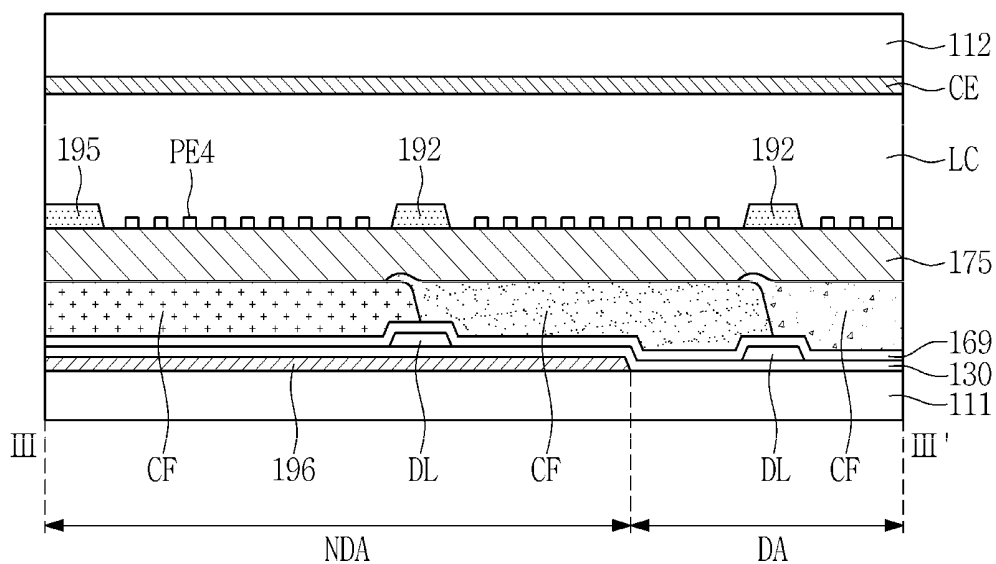


FIG. 19

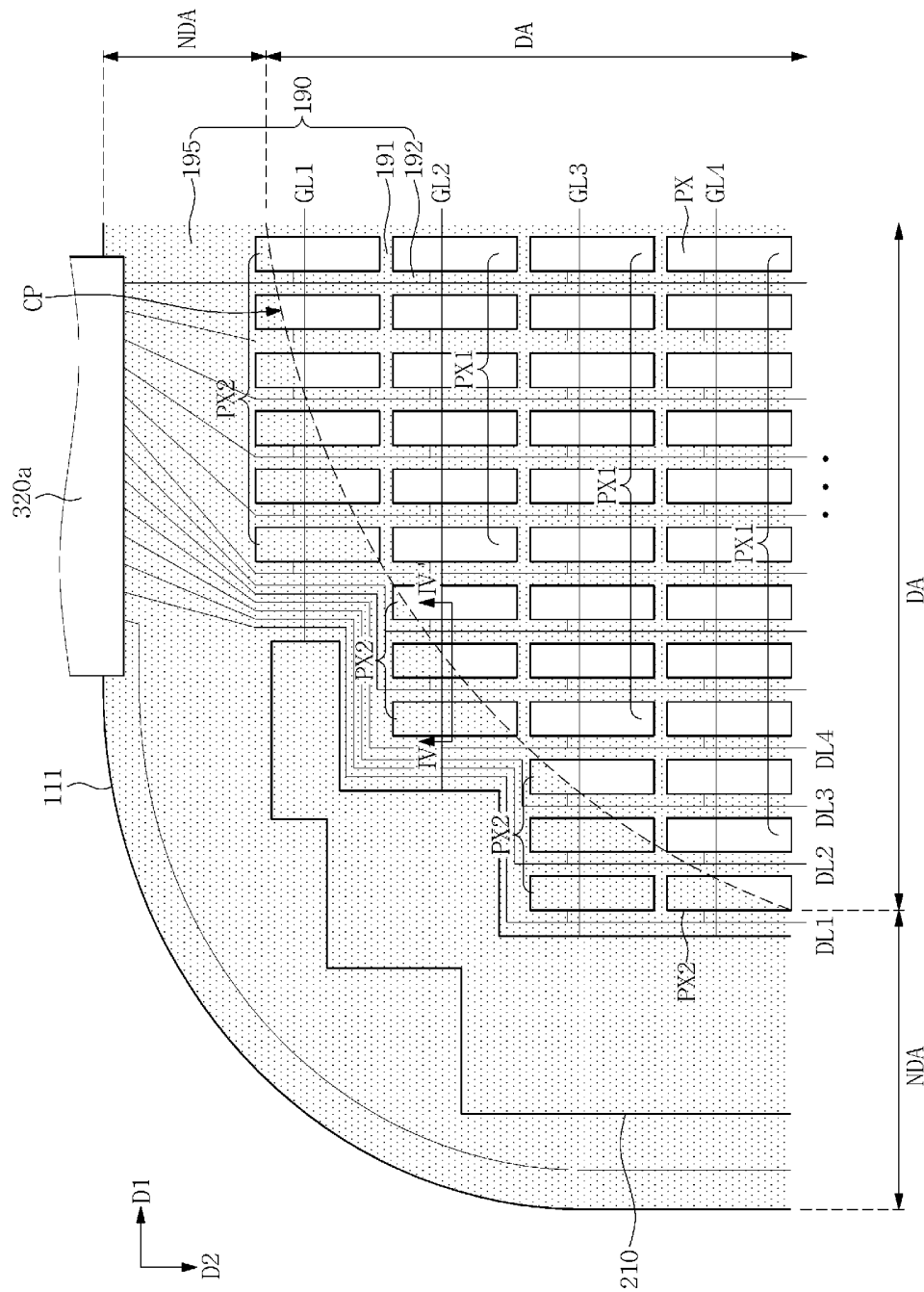


FIG. 20

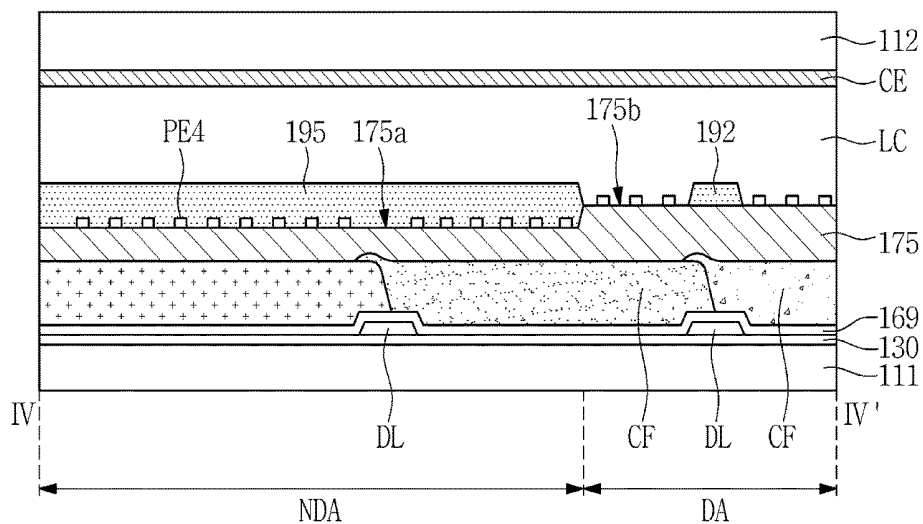
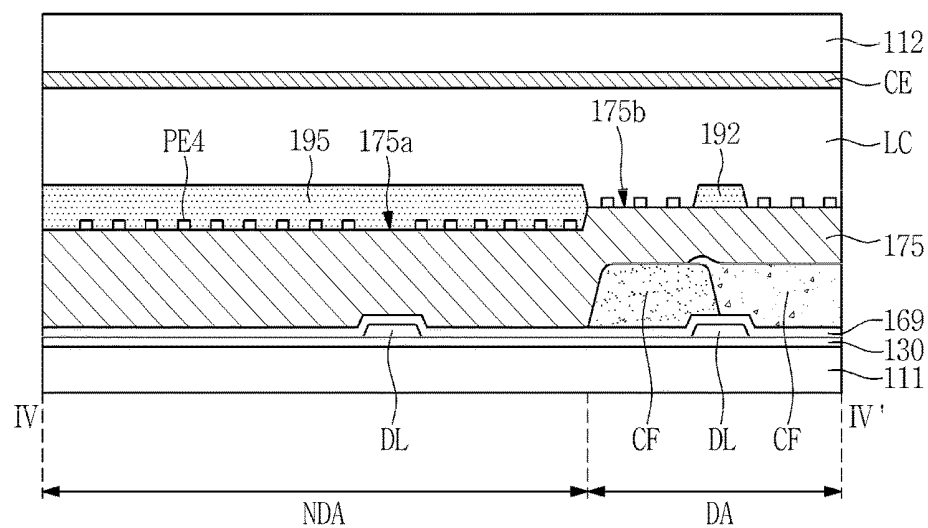


FIG. 21



DISPLAY DEVICE HAVING A NON-RECTILINEAR DISPLAY AREA

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional application of U.S. patent application Ser. No. 15/411,639 filed on Jan. 20, 2017, which claims priority under 35 USC § 119 to Korean Patent Application No. 10-2016-0055317 filed on May 4, 2016, in the Korean Intellectual Property Office, the disclosures of which are incorporated herein in their entirety by reference.

BACKGROUND

1. Field

[0002] Exemplary embodiments of the invention relate to a display device, and more particularly, to a display device that has a non-rectangular display area.

2. Description of the Related Art

[0003] Display devices can be classified as a liquid crystal display ("LCD") device, an organic light emitting diode ("OLED") display device, a plasma display panel ("PDP") device, an electrophoretic display ("EPD") device, and the like, based on a light emitting scheme thereof.

[0004] Among the different types of display devices, LCD devices include a display substrate and a cover substrate, each including an electrode formed thereon, and a liquid crystal layer interposed therebetween. In recent times, a color filter on array (COA) structure is employed, in which a color filter is disposed on the display substrate to enhance transmittance.

[0005] In addition, in order to prevent misalignment from occurring during the process of coupling the display substrate with a color filter and the cover substrate with a light blocking member, a black matrix on array (BOA) structure is employed, in which both of the color filter and the light blocking member are disposed on the display substrate.

[0006] As wearable devices, e.g., a smart watch and a head mount display, are currently being used in various fields, a demand on an LCD device including a display area having a curvature is growing.

[0007] The display area having a curvature may be realized using pixels arranged in a staircase shape and a light blocking member having a predetermined curvature. However, in such a case, the light blocking member is disposed on the pixels arranged in staircase shape to cause a step difference of the light blocking member such that liquid crystals may not be aligned in a desired direction. This incorrect alignment of liquid crystals may cause a smear to appear.

[0008] It is to be understood that this background of the technology section is intended to provide useful background for understanding the technology and as such disclosed herein, the technology background section may include ideas, concepts or recognitions that were not part of what was known or appreciated by those skilled in the pertinent art prior to a corresponding effective filing date of subject matter disclosed herein.

SUMMARY

[0009] Exemplary embodiments are directed to a display device, including a display area having a curvature, which is significantly reduced in a smear appearing at a curved portion.

[0010] In accordance with one or more embodiments, a display device includes a first substrate; a second substrate covering the first substrate; a liquid crystal layer between the first substrate and the second substrate; a plurality of pixels on the first substrate; and a light blocking member disposed on at least one of the first substrate and the second substrate, the light blocking member disposed in a curved area and defining a display area and a non-display area. The plurality of pixels includes a first pixel outside the curved area; and a second pixel in the curved area, and a pixel electrode of the first pixel has a different shape from a shape of a pixel electrode of the second pixel.

[0011] The second pixel may be arranged to have an outline of a staircase.

[0012] The first pixel may include a greater number of liquid crystal domains than the number of liquid crystal domains of the second pixel.

[0013] The light blocking member covers less than all of the pixel electrode of the second pixel.

[0014] The pixel electrode of the first pixel may include a first sub-pixel electrode and a second sub-pixel electrode, each of the first sub-pixel electrode and the second sub-pixel electrode including a cross-shaped stem portion and a plurality of branch portions each diagonally extending in different directions, respectively, from the cross-shaped stem portion.

[0015] The pixel electrode of the second pixel may include a third sub-pixel electrode including a stem portion and a plurality of branch portions diagonally extending in no more than one direction from the stem portion; and a fourth sub-pixel electrode including a cross-shaped stem portion and a plurality of branch portions each diagonally extending in different directions, respectively, from the cross-shaped stem portion.

[0016] The branch portion of the third sub-pixel electrode may be substantially perpendicular to the curved portion.

[0017] The branch portion of the third sub-pixel electrode may be substantially parallel to the curved portion.

[0018] The light blocking member may include a first edge light blocking member that is positioned in the curved area outside an area on the second pixel and a second edge light blocking member on the second pixel.

[0019] The second edge light blocking member may be formed on less than all of the second pixel.

[0020] The plurality of pixels may include a gate line disposed on the first substrate and extending in a first direction; a data line disposed on the first substrate to be insulated from the gate line and extending in a second direction which intersects the first direction; and a color filter disposed on at least one of the first substrate and the second substrate and insulated from the gate line and the data line.

[0021] The second edge light blocking member may be disposed on a same layer as a layer on which the gate line is disposed.

[0022] The second edge light blocking member may include substantially a same material as that included in the gate line.

[0023] The second edge light blocking member may be disposed on a same layer as a layer on which the data line is disposed.

[0024] The second edge light blocking member may include substantially a same material as that included in the data line.

[0025] The second edge light blocking member may be disposed on a same layer as a layer on which the color filter is disposed.

[0026] The second edge light blocking member may include at least one color filter.

[0027] In accordance with one or more embodiments, a display device includes a first substrate; a plurality of pixels on the first substrate; and a light blocking member disposed on at least one of the first substrate and the second substrate and including a curved inner edge. The plurality of pixels include: a gate line and a data line disposed on the first substrate and extending in non-parallel directions; a color filter disposed on the first substrate and insulated from the gate line and the data line; and a passivation layer on the color filter. The passivation layer includes a first passivation layer overlapping the light blocking member; and a second passivation layer not overlapping the first edge light blocking member. A height of the first passivation layer is lower than a height of the second passivation layer.

[0028] The color filter may be absent below the first passivation layer.

[0029] The light blocking member may be disposed on a same layer as a layer on which the color filter is disposed.

[0030] The light blocking member may include at least one color filter.

[0031] In another aspect, the inventive concept pertains to a display device that includes a substrate having a curved outer edge and a curved area adjacent to the curved outer edge. A plurality of first pixels are disposed on the substrate in rows and columns, wherein the number of first pixels in the rows varies. A plurality of second pixels including a second pixel is positioned at an end of each row wherein the end is in the curved area, wherein each second pixel has a pixel electrode that is shaped differently from a pixel electrode of the first pixel. A light blocking member is disposed on only the second pixels out of the first and second pixels.

[0032] The foregoing is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The above and other features and aspects of the present disclosure of invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0034] FIG. 1 is a plan view illustrating an exemplary embodiment of a liquid crystal display (LCD) device;

[0035] FIG. 2 is a perspective view illustrating an exemplary embodiment of an LCD device;

[0036] FIGS. 3, 4, and 5 are perspective views illustrating alternative exemplary embodiments of an LCD device;

[0037] FIG. 6 is a partial enlarged view illustrating an area "A" of FIG. 1;

[0038] FIG. 7 is a graph illustrating a relationship between a size of a display area and a radius of curvature of a curved portion in an exemplary embodiment of an LCD device;

[0039] FIG. 8 is a plan view illustrating an exemplary embodiment of a first pixel;

[0040] FIG. 9 is a cross-sectional view taken along line I-I' of FIG. 8;

[0041] FIG. 10 is a plan view illustrating an exemplary embodiment of a second pixel;

[0042] FIG. 11 is a cross-sectional view taken along line II-II' of FIG. 10;

[0043] FIGS. 12 and 13 are plan views illustrating alternative exemplary embodiments of a second pixel;

[0044] FIG. 14 is a plan view illustrating an alternative exemplary embodiment of a first pixel;

[0045] FIGS. 15 and 16 are plan views illustrating another alternative exemplary embodiments of a second pixel;

[0046] FIG. 17 is a plan view illustrating an alternative exemplary embodiment of an LCD device;

[0047] FIG. 18 is a cross-sectional view taken along line III-III' of FIG. 17;

[0048] FIG. 19 is a plan view illustrating another alternative exemplary embodiment of an LCD device;

[0049] FIG. 20 is a cross-sectional view illustrating an exemplary embodiment taken along line IV-IV' of FIG. 19;

[0050] FIG. 21 is a cross-sectional view illustrating an alternative exemplary embodiment taken along line IV-IV' of FIG. 19; and

[0051] FIG. 22 is a partial enlarged view illustrating still another alternative exemplary embodiment of an LCD device.

DETAILED DESCRIPTION

[0052] Exemplary embodiments will now be described more fully hereinafter with reference to the accompanying drawings. Although the invention can be modified in various manners and have several embodiments, exemplary embodiments are illustrated in the accompanying drawings and will be mainly described in the specification. However, the scope of the invention is not limited to the exemplary embodiments and should be construed as including all the changes, equivalents, and substitutions included in the spirit and scope of the invention.

[0053] In the drawings, thicknesses of a plurality of layers and areas are illustrated in an enlarged manner for clarity and ease of description thereof. When a layer, area, or plate is referred to as being "on" another layer, area, or plate, it may be directly on the other layer, area, or plate, or intervening layers, areas, or plates may be present therebetween. Conversely, when a layer, area, or plate is referred to as being "directly on" another layer, area, or plate, intervening layers, areas, or plates may be absent therebetween. Further when a layer, area, or plate is referred to as being "below" another layer, area, or plate, it may be directly below the other layer, area, or plate, or intervening layers, areas, or plates may be present therebetween. Conversely, when a layer, area, or plate is referred to as being "directly below" another layer, area, or plate, intervening layers, areas, or plates may be absent therebetween.

[0054] The spatially relative terms "below", "beneath", "less", "above", "upper", and the like, may be used herein for ease of description to describe the relations between one element or component and another element or component as illustrated in the drawings. It will be understood that the

spatially relative terms are intended to encompass different orientations of the device in use or operation, in addition to the orientation depicted in the drawings. For example, in the case where a device shown in the drawing is turned over, the device positioned “below” or “beneath” another device may be placed “above” another device. Accordingly, the illustrative term “below” may include both the lower and upper positions. The device may also be oriented in the other direction, and thus the spatially relative terms may be interpreted differently depending on the orientations.

[0055] Throughout the specification, when an element is referred to as being “connected” to another element, the element is “directly connected” to the other element, or “electrically connected” to the other element with one or more intervening elements interposed therebetween. It will be further understood that the terms “comprises,” “comprising,” “includes” and/or “including,” when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0056] It will be understood that, although the terms “first,” “second,” “third,” and the like may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, “a first element” discussed below could be termed “a second element” or “a third element,” and “a second element” and “a third element” can be termed likewise without departing from the teachings herein.

[0057] Unless otherwise defined, all terms used herein (including technical and scientific terms) have the same meaning as commonly understood by those skilled in the art to which this invention pertains. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an ideal or excessively formal sense unless clearly defined in the present specification.

[0058] Some of the parts which are not associated with the description may not be provided in order to specifically describe embodiments of the present invention, and like reference numerals refer to like elements throughout the specification.

[0059] Hereinafter, an exemplary embodiment of a display device will be described under the assumption that it is a liquid crystal display (“LCD”) device. However, exemplary embodiments are not limited thereto, and the present invention may be applied to an organic light emitting diode (“OLED”) display device.

[0060] FIG. 1 is a plan view illustrating an exemplary embodiment of an LCD device, FIG. 2 is a perspective view illustrating an exemplary embodiment of an LCD device, and FIGS. 3, 4, and 5 are perspective views illustrating alternative exemplary embodiments of an LCD device.

[0061] Referring to FIG. 1, an exemplary embodiment of an LCD device 10 includes an LCD panel 110 which displays an image, a gate driver 210 which outputs a gate voltage to the LCD panel 110, and a data driver 310 which outputs a data voltage to the LCD panel 110.

[0062] Referring to FIG. 2, the LCD panel 110 includes a first substrate 111, a second substrate (not illustrated) cov-

ering the first substrate 111, and a liquid crystal layer (not illustrated) between the first substrate 111 and the second substrate.

[0063] The LCD panel 110 may have a substantially quadrangular shape with a corner portion having a predetermined curvature on a plane of the LCD panel 110. However, exemplary embodiments are not limited thereto, and the LCD panel 110 may have a quadrangular shape with right-angled corners.

[0064] The LCD panel 110 may include a display area DA in which an image is displayed and a non-display area NDA around the display area DA, and the display area DA may have substantially the same shape as that of the LCD panel 110 on a plane.

[0065] Referring to FIG. 3, the LCD panel 110 may have a substantially quadrangular shape, and may include at least one curved outer edge having a predetermined curvature.

[0066] For example, the LCD panel 110 may include two corner portions having a predetermined curvature in an upper portion or a lower portion thereof. In addition, the LCD panel 110 may include two curved outer edges having a predetermined curvature, e.g. in a left portion and a right portion.

[0067] In addition, referring to FIG. 4, the LCD panel 110 may have a substantially circular shape, and referring to FIG. 5, the LCD panel 110 may have a substantially elliptical shape.

[0068] Referring back to FIG. 1, the LCD panel 110 includes a plurality of gate lines GL1 to GLm (or GL) on the first substrate 111, a plurality of data lines DL1 to DLn (or DL) insulated from and intersecting the plurality of gate lines GL1 to GL, and a plurality of pixels PX which are connected to the plurality of gate lines GL1 to GLm and the plurality of data lines DL1 to DLn, respectively, to display an image.

[0069] The gate driver 210 is disposed adjacent to one end portion of the plurality of gate lines GL1 to GLm. The gate driver 210 is electrically connected to the one end portion of the plurality of gate lines GL1 to GLm and sequentially applies the gate voltage to the plurality of gate lines GL1 to GLm. In FIG. 1, the gate driver 210 is depicted as being disposed on one side (e.g., a left side) of the first substrate 111, but exemplary embodiments are not limited thereto. In an exemplary embodiment, the gate driver 210 may be disposed on another side (e.g., a right side) of the first substrate 111 or may be disposed on both sides of the first substrate 111.

[0070] The data driver 310 is disposed adjacent to one end portion of the plurality of data lines DL1 to DLn. The data driver 310 includes a plurality of driving circuit boards 320a, 320b, and 320c. For example, the plurality of driving circuit boards 320a, 320b, and 320c may be a tape carrier package (TCP) or a chip on film (COF). A plurality of data driving integrated circuits (ICs) 321a, 321b, and 321c are mounted on the plurality of driving circuit boards 320a, 320b, and 320c, respectively. The plurality of data driving ICs 321a, 321b, and 321c are electrically connected to the one end portion of the plurality of data lines DL1 to DLn to output the data voltage to the plurality of data lines DL1 to DLn.

[0071] The LCD device 10 further includes a control printed circuit board (PCB) 330 to control operations of the gate driver 210 and the plurality of data driving ICs 321a, 321b, and 321c. The control PCB 330 outputs a data control

signal and an image data to control the operation of the plurality of data driving ICs **321a**, **321b**, and **321c**, and outputs a gate control signal to control the operation of the gate driver **210**.

[0072] The control PCB **330** includes a timing controller **331** which externally receives an image data and generates the data control signal and the gate control signal, and a gate control circuit **332** which generates the gate control signal. However, exemplary embodiments are not limited thereto, and the control PCB **330** may be a data PCB which receives a control signal from another PCB including a timing controller and thereby generates and outputs the data control signal.

[0073] The timing controller **331** controls operations of the plurality of data driving ICs **321a**, **321b**, and **321c** and the gate driver **210**. The gate control circuit **332** generates a clock signal to drive the gate driver **210** and a start signal to notice the start of the gate signal.

[0074] The control PCB **330** applies the data control signal and the image data to the plurality of data driving ICs **321a**, **321b**, and **321c** through the plurality of driving circuit boards **320a**, **320b**, and **320c**. In addition, the control PCB **330** applies the gate control signal to the gate driver **210** through the driving circuit board **320a** that is adjacent to the gate driver **210**.

[0075] However, exemplary embodiments are not limited thereto, and the plurality of data driving ICs **321a**, **321b**, and **321c** may be directly disposed (e.g., embedded) in the LCD panel **110**, disposed (e.g., embedded) on a flexible printed circuit film (not illustrated) to be attached to the LCD panel **110**, or disposed (e.g., embedded) on a separate PCB (not illustrated). In an alternative exemplary embodiment, the plurality of data driving ICs **321a**, **321b**, and **321c**, along with the gate lines GL1 to GLm and a thin film transistor ("TFT") (not illustrated), may be disposed (e.g., embedded) in the LCD panel **110**. In an alternative exemplary embodiment, the plurality of data driving ICs **321a**, **321b**, and **321c**, the timing controller **331**, and the gate control circuit **332** may be integrated into a single chip.

[0076] FIG. 6 is a partial enlarged view illustrating an area "A" of FIG. 1, and FIG. 7 is a graph illustrating a relationship between a size of a display area and a radius of curvature of a curved portion in an exemplary embodiment of an LCD device.

[0077] Referring to FIGS. 1 and 6, the LCD panel **110** further includes a light blocking member **190** on the first substrate **111**. An exemplary embodiment of the LCD panel **110** is described under the assumption that the light blocking member **190** is disposed on the first substrate **111**, but exemplary embodiments are not limited thereto. In an exemplary embodiment, the light blocking member **190** may be disposed on the second substrate (not illustrated). The light blocking member **190** is indicated with dotted shading in the figures.

[0078] The light blocking member **190** includes a first light blocking member **191** extending in a first direction D1, a second light blocking member **192** extending in a second direction D2 which intersects the first direction D1, and a first edge light blocking member **195** that has a curved inner edge CP. The area between the curved outer edge of the substrate **111** and the curved inner edge CP is herein referred to as the "curved area." The second light blocking member **192** may be omitted based on disposition of color filters, which will be described further below. While FIG. 6 shows

the first light blocking member **191** as being disposed only between rows of pixels, this is done to clearly illustrate the pixel arrangement and in fact, there may be first light blocking member **191** disposed in select portions of the pixels. For example, as will be shown below in FIG. 11, the first light blocking member **191** may be disposed on the first transistor TR1 of the second pixel PX2 between two sub-pixel electrodes of a pixel.

[0079] The light blocking member **190** may use a black pigment or a black resin, and may use a combination of a red color filter and a blue color filter, for example. For example, a red color filter and a blue color filter may be stacked.

[0080] The first edge light blocking member **195** includes at least one curved inner edge CP having a predetermined curvature. A display area DA in which an image is displayed and a non-display area NDA in which an image is not displayed are defined by the first edge light blocking member **195**.

[0081] Where a length of a diagonal line of the display area DA is "D" mm and a radius of curvature of the curved inner edge CP is "R" mm, "D" and "R" may satisfy, for example, the following Formula 1.

$$0.01 \times D + 5 \leq R \leq 0.01 \times D + 15 \quad \text{[Formula 1]}$$

[0082] In addition, where a length of a diagonal line of the display area DA is "d" inches and a radius of curvature of the curved inner edge CP is "R" mm, "d" and "R" may satisfy, for example, the following Formula 2.

$$0.25 \times d + 5 \leq R \leq 0.25 \times d + 15 \quad \text{[Formula 2]}$$

[0083] A relationship between the length (unit: inch) of the diagonal line of the display area DA and the radius of curvature (unit: mm) of the curved inner edge CP may be represented by the graph illustrated in FIG. 7.

[0084] Referring to FIGS. 1 and 6, the plurality of pixels PX include a first pixel PX1 not overlapping the curved inner edge CP of the first edge light blocking member **195** and a second pixel PX2 overlapping at least a portion of the curved inner edge CP of the first edge light blocking member **195**. As shown, the first pixels are disposed in rows and columns, and the number of first pixels in a row varies according to the inner curved edge CP, to generally produce a similar outline as the curved inner edge CP. At least one second pixel is positioned at the end of each row that extends into the curved area.

[0085] An exemplary embodiment of the second pixel PX2 is depicted as being arranged in a staircase shape on a plane, but exemplary embodiments are not limited thereto. In another exemplary embodiment, the second pixel PX2 may be arranged in a matrix form.

[0086] As an exemplary embodiment of the second pixel PX2 is arranged in a staircase shape on a plane, the gate driver **210** and the data lines DL1 to DLn connected to the second pixel PX2 may be arranged in a staircase shape.

[0087] For example, the gate driver **210** includes a plurality of stages ST1, ST2, ST3, and ST4 connected to respective gate lines GL1 to GLm, and a stage connected to the second pixel PX2 may protrude toward the second pixel PX2. As such, as the plurality of stages are arranged in a staircase shape, an area of the non-display area NDA may be significantly reduced (e.g., minimized).

[0088] In addition, the data lines DL1 to DLn connected to the second pixel PX2 may extend to be bent into a staircase shape, but exemplary embodiments are not limited thereto.

In another exemplary embodiment, the data lines DL1 to DLn may extend to be bent into a diagonal line or a curved shape.

[0089] A pixel electrode of the first pixel PX1 has a different shape from a shape of a pixel electrode of the second pixel PX2.

[0090] FIG. 8 is a plan view illustrating an exemplary embodiment of a first pixel PX1, and FIG. 9 is a cross-sectional view taken along line I-I' of FIG. 8.

[0091] Referring to FIG. 8, an exemplary embodiment of the first pixel PX1 includes a first sub-pixel SPX1 and a second sub-pixel SPX2.

[0092] The first sub-pixel SPX1 includes a first TFT TR1, a first sub-pixel electrode PE1, and a first storage electrode STE1. The second sub-pixel SPX2 includes a second TFT TR2, a second sub-pixel electrode PE2, a second storage electrode STE2, and a third TFT TR3.

[0093] The first sub-pixel SPX1 may also be referred to as a high pixel, and the second sub-pixel SPX2 may also be referred to as a low pixel.

[0094] The first TFT TR1 of the first sub-pixel SPX1 includes a first gate electrode GE1 branching off from the gate line GL, a first semiconductor layer SM1 disposed to overlap the first gate electrode GE1, a first source electrode SE1 branching off from the data line DL and overlapping the first semiconductor layer SM1, and a first drain electrode DE1 spaced apart from the first source electrode SE1 and overlapping the first semiconductor layer SM1. The first drain electrode DE1 is connected to the first sub-pixel electrode PE1. For example, the first drain electrode DE1 extends toward the first sub-pixel electrode PE1 and is electrically connected, through the first contact hole H1, to a first connecting electrode CNE1 which branches off from the first sub-pixel electrode PE1.

[0095] The first storage electrode STE1 is connected to a first storage line SL1. The first sub-pixel electrode PE1 overlaps portions of the first storage line SL1 and the first storage electrode STE1 to define a first storage capacitor. The first storage electrode STE1 receives a storage voltage.

[0096] The second TFT TR2 of the second sub-pixel SPX2 includes a second gate electrode GE2 branching off from the gate line GL, a second semiconductor layer SM2 overlapping the second gate electrode GE2, a second source electrode SE2 branching off from the data line DL and overlapping the second semiconductor layer SM2, and a second drain electrode DE2 spaced apart from the second source electrode SE2 and overlapping the second semiconductor layer SM2. The second drain electrode DE2 is connected to the second sub-pixel electrode PE2. For example, the second drain electrode DE2 extends toward the second sub-pixel electrode PE2 and is electrically connected, through a second contact hole H2, to a second connecting electrode CNE2 which branches off from the second sub-pixel electrode PE2.

[0097] The third TFT TR3 of the second sub-pixel SPX2 includes a third gate electrode GE3 branching off from the gate line GL, a third source electrode SE3 electrically connected to the first storage electrode STE1 through a third contact hole H3, a third drain electrode DE3 extending from the second drain electrode DE2, and a third semiconductor layer SM3. The third source electrode SE3 and the first storage electrode STE1 are electrically connected to each other through the third contact hole H3. In addition, the third drain electrode DE3 is electrically connected to the second sub-pixel electrode PE2 through the second contact hole H2.

[0098] The second storage electrode STE2 is connected to a second storage line SL2. The second sub-pixel electrode PE2 overlaps portions of the second storage line SL2 and the second storage electrode STE2 to define a second storage capacitor. The second storage electrode STE2 receives the storage voltage.

[0099] Referring to FIGS. 8 and 9, the gate line GL, the first, second, and third gate electrodes GE1, GE2, and GE3 branching off from the gate line GL, the first storage line SL1, the first storage electrode STE1, the second storage line SL2, and the second storage electrode STE2 are disposed on the first substrate 111.

[0100] The gate insulating layer 130 is disposed on the first substrate 111 to cover the gate line GL, the first, second, and third gate electrodes GE1, GE2, and GE3, the first and second storage lines SL1 and SL2, and the first and second storage electrodes STE1 and STE2.

[0101] The first, second, and third semiconductor layers SM1, SM2, and SM3 are disposed on the gate insulating layer 130. The first, second, and third semiconductor layers SM1, SM2, and SM3 may include or be formed of amorphous silicon or an oxide semiconductor including at least one selected from the group consisting of: gallium (Ga), indium (In), tin (Sn), and zinc (Zn). For example, the oxide semiconductor includes at least one selected from the group consisting of: zinc oxide (ZnO), zinc-tin oxide (ZTO), zinc indium oxide (ZIO), indium oxide (InO), titanium oxide (TiO), indium-gallium-zinc oxide (IGZO), and indium-zinc-tin oxide (IZTO). Although not illustrated, an ohmic contact layer may be disposed on the first, second, and third semiconductor layers SM1, SM2, and SM3.

[0102] The data line DL extends in a longitudinal direction to be disposed on the gate insulating layer 130. The first, second, and third source electrodes SE1, SE2, and SE3 are disposed to overlap the first, second, and third semiconductor layers SM1, SM2, and SM3, respectively, and the first, second, and third drain electrodes DE1, DE2, and DE3 are disposed to overlap the first, second, and third semiconductor layers SM1, SM2, and SM3, respectively, and thus the first, second, and third TFTs TR1, TR2, and TR3 are formed.

[0103] The third source electrode SE3 of the third TFT TR3 is electrically connected to the first storage electrode STE1 through the third contact hole H3 which is defined through the gate insulating layer 130.

[0104] The insulating interlayer 169 is disposed to cover the data line DL and the first, second, and third TFTs TR1, TR2, and TR3. The insulating interlayer 169 covers upper portions of the first, second, and third semiconductor layers SM1, SM2, and SM3. The insulating interlayer 169 may have a monolayer or multilayer structure including silicon oxide, silicon nitride, a photosensitive organic material, and/or a silicon-based low dielectric constant insulating material, for example.

[0105] A color filter CF is disposed on the insulating interlayer 169.

[0106] The color filter CF is disposed to overlap the first and second sub-pixel electrodes PE1 and PE2 and imparts color to light that is transmitted through the pixel. The color filter CF may be one of a red color filter, a green color filter, and a blue color filter. In an alternative exemplary embodiment, the color filter CF may be a white color filter.

[0107] The color filter CF may be disposed on the first and second sub-pixel electrodes PE1 and PE2, or may extend along the second direction D2.

[0108] In addition, different colors of color filters CF may be disposed along the first direction D1, and in such an exemplary embodiment, the color filters CF disposed along the first direction D1 may overlap or may not overlap one another. In a case where the color filters CF disposed along the first direction D1 overlap one another, the aforementioned second light blocking member 192 (refer to FIG. 6) may be omitted.

[0109] The passivation layer 175 is disposed on the insulating interlayer 169 and the color filter CF. The passivation layer 175 may have a monolayer or multilayer structure including silicon oxide, silicon nitride, a photosensitive organic material, and/or a silicon-based low dielectric constant insulating material, for example.

[0110] The passivation layer 175 may planarize upper portions of the first, second, and third TFTs TR1, TR2, and TR3, and the color filter CF. Thus, the passivation layer 175 may also be referred to as a planarization layer.

[0111] Portions of the insulating interlayer 169 and the passivation layer 175 are removed such that the first contact hole H1 exposing a portion of the first drain electrode DE1 and the second contact hole H2 exposing a portion of the second drain electrode DE2 are defined.

[0112] The first sub-pixel electrode PE1 and the second sub-pixel electrode PE2 are disposed on the passivation layer 175. The first sub-pixel electrode PE1 is electrically connected to the first drain electrode DE1 through the first contact hole H1. The second sub-pixel electrode PE2 is electrically connected to the second drain electrode DE2 through the second contact hole H2.

[0113] Referring to FIG. 8, each of the first and second sub-pixel electrodes PE1 and PE2 includes a stem portion having a cross shape and a plurality of branch portions extending from the cross-shaped stem portion. The first and second sub-pixel electrodes PE1 and PE2 may include or be formed of a transparent conductive material. For example, the first and second sub-pixel electrodes PE1 and PE2 may include a transparent conductive material such as indium tin oxide (ITO), indium zinc oxide (IZO), indium tin zinc oxide (ITZO), aluminum zinc oxide (AZO), and the like.

[0114] Referring to FIG. 9, the first light blocking member 191 extending in the first direction D1 is disposed on the passivation layer 175. In addition, the column spacer 193 may further be disposed on the first light blocking member 191.

[0115] According to an exemplary embodiment, the light blocking member 190 and the column spacer 193 are simultaneously formed in a same process. The light blocking member 190 and the column spacer 193 are collectively referred to as a black column spacer BCS. In addition, a structure in which the light blocking member 190 and the first, second, and third TFTs TR1, TR2, and TR3 are disposed on a same substrate may be referred to as a black matrix on array (BOA) structure.

[0116] Although not illustrated, a lower alignment layer may be disposed on the first and second sub-pixel electrodes PE1 and PE2 and the light blocking member 190. The lower alignment layer may be a homeotropic alignment layer, and may include a photosensitive material.

[0117] The second substrate 112 is an insulating substrate including a transparent material such as glass or plastic.

[0118] The common electrode CE is disposed on the second substrate 112. The common electrode CE may include or be formed of a transparent conductive oxide

(TCO) such as indium tin oxide (ITO), indium zinc oxide (IZO), and aluminum zinc oxide (AZO), for example.

[0119] Although not illustrated, an upper alignment layer may be disposed on the common electrode CE. The upper alignment layer may include a same material as that included in the aforementioned lower alignment layer.

[0120] When a surface of the first substrate 111 and a surface of the second substrate 112 that face each other are defined as upper surfaces of the corresponding substrates, respectively, and surfaces opposite to their respective upper surface are defined as the respective lower surface of their corresponding substrates, polarizers may be disposed on the lower surface of the first substrate 111 and the lower surface of the second substrate 112, respectively.

[0121] The liquid crystal layer LC is disposed in a space which is maintained by the column spacer 193 and between the first substrate 111 and the second substrate 112.

[0122] The liquid crystal layer LC may include liquid crystal molecules. The liquid crystal molecules of the liquid crystal layer LC may have a structure in which a major axis thereof is aligned parallel to one of the first substrate 111 and the second substrate 112, and the direction is spirally twisted about 90 degrees from a rubbing direction of the alignment layer of the first substrate 111 to the second substrate 112. Alternatively, the liquid crystal layer LC may include homeotropic liquid crystal molecules.

[0123] FIG. 10 is a plan view illustrating an exemplary embodiment of a second pixel PX2, and FIG. 11 is a cross-sectional view taken along line II-II of FIG. 10. FIGS. 12 and 13 are plan views illustrating alternative exemplary embodiments of the second pixel PX2. Hereinafter, repeated descriptions described hereinabove with respect to the first pixel PX1 will be omitted in descriptions with respect to the second pixel PX2.

[0124] Referring to FIG. 10, an exemplary embodiment of the second pixel PX2 includes a third sub-pixel SPX3 and a fourth sub-pixel SPX4.

[0125] The third sub-pixel SPX3 includes the first TFT TR1, a third sub-pixel electrode PE3, and the first storage electrode STE1. The fourth sub-pixel SPX4 includes the second TFT TR2, a fourth sub-pixel electrode PE4, the second storage electrode STE2, and the third TFT TR3.

[0126] An exemplary embodiment of the third sub-pixel electrode PE3 is described under the assumption that the curved inner edge CP of the first edge light blocking member 195 overlaps the third sub-pixel electrode PE3 but does not overlap the fourth sub-pixel electrode PE4.

[0127] The third sub-pixel electrode PE3 may include a stem portion and a plurality of branch portions diagonally extending from the stem portion in no more than one direction, as shown in FIGS. 10, 12, and 13 for example. The fourth sub-pixel electrode PE4 may include a stem portion having a cross shape and a plurality of branch portions diagonally extending in different directions from the cross-shaped stem portion.

[0128] In such an exemplary embodiment, the third sub-pixel electrode PE3 which overlaps the first edge light blocking member 195 includes a single domain, but exemplary embodiments are not limited thereto. In another exemplary embodiment, the fourth sub-pixel electrode PE4 overlaps the first edge light blocking member 195 and the fourth sub-pixel electrode PE4 may have a single domain.

[0129] Accordingly, all liquid crystal molecules on the third sub-pixel electrode PE3 may be initially aligned in a

same direction. As such, in an exemplary embodiment of the LCD device, although a step difference occurs due to the first edge light blocking member **195**, the second pixel **PX2** overlapping the first edge light blocking member **195** only has a single domain, such that occurrence of a smear may be prevented. The branch portion of the third sub-pixel electrode **PE3** may be substantially perpendicular to the first edge light blocking member **195** (refer to FIG. **10**) or may extend substantially parallel to the first edge light blocking member **195** (refer to FIG. **12**).

[0130] In addition, referring to FIGS. **8** and **13**, the third sub-pixel electrode **PE3** of the second pixel **PX2** may have less planar area than that of the first sub-pixel electrode **PE1** of the first pixel **PX1**.

[0131] FIG. **14** is a plan view illustrating an alternative exemplary embodiment of a first pixel **PX1**. Hereinafter, repeated descriptions described hereinabove with respect to an exemplary embodiment of the first pixel **PX1** will be omitted in descriptions with respect to an alternative exemplary embodiment of the first pixel **PX1**.

[0132] Referring to FIG. **14**, an alternative exemplary embodiment of the first pixel **PX1** may include a first substrate **111**, a gate line **GL**, a gate electrode **GE**, a semiconductor layer **SM**, a data line **DL**, a source electrode **SE**, a drain electrode **DE**, a pixel electrode **PE**, and a common electrode **CE**, for example.

[0133] The pixel electrode **PE** and the common electrode **CE** may be disposed on a same layer or different layers, respectively. The pixel electrode **PE** and the common electrode **CE** generate together a horizontal electric field.

[0134] The pixel electrode **PE** and the common electrode **CE** may respectively have linear shapes that are alternately disposed on a plane, and may have a shape that is bent at least once on a plane to form a multi-domain as illustrated in FIG. **14**. Based on the shape of the pixel electrode **PE** and the common electrode **CE** being bent, the data line **DL** may be bent into a similar shape as that of the pixel electrode **PE** and the common electrode **CE**.

[0135] As the pixel electrode **PE** and the common electrode **CE** have a multi-domain layout, a wide viewing angle may be achieved.

[0136] FIGS. **15** and **16** are plan views illustrating another alternative exemplary embodiments of a second pixel **PX2**. Hereinafter, repeated descriptions described hereinabove with respect to an alternative exemplary embodiment of the first pixel **PX1** will be omitted in descriptions with respect to another alternative exemplary embodiment of the second pixel **PX2**.

[0137] Referring to FIG. **15**, a pixel electrode **PE** and a common electrode **CE** of another alternative exemplary embodiment of the second pixel **PX2** may respectively have linear shapes that are alternately disposed on a plane.

[0138] That is, the second pixel **PX2** overlapping the first edge light blocking member **195** includes one domain, and all liquid crystal molecules on the second pixel **PX2** may be initially aligned in a same direction.

[0139] As such, in this alternative exemplary embodiment of the LCD device, although a step difference occurs due to the first edge light blocking member **195**, the second pixel **PX2** overlapping the first edge light blocking member **195** only has a single domain, such that occurrence of a smear may be prevented.

[0140] In addition, referring to FIG. **16**, the pixel electrode **PE** and the common electrode **CE** of the second pixel **PX2**

may have less planar area than the pixel electrode **PE** and the common electrode **CE** of the first pixel **PX1**.

[0141] FIG. **17** is a plan view illustrating an alternative exemplary embodiment of an LCD device, and FIG. **18** is a cross-sectional view taken along line III-III' of FIG. **17**. Hereinafter, repeated descriptions described hereinabove with respect to an exemplary embodiment of an LCD device will be omitted in descriptions with respect to an alternative exemplary embodiment of an LCD device.

[0142] Referring to FIGS. **17** and **18**, an alternative exemplary embodiment of an LCD panel **110** includes a plurality of gate lines **GL1** to **GLm** (or **GL**) on a first substrate **111**, a plurality of data lines **DL1** to **DLn** (or **DL**) insulated from and intersecting the plurality of gate lines **GL1** to **GL**, and a plurality of pixels **PX** which are connected to the plurality of gate lines **GL1** to **GLm** and the plurality of data lines **DL1** to **DLn**, respectively, to display an image.

[0143] A gate driver **210** is disposed adjacent to one end portion of the plurality of gate lines **GL1** to **GLm**, and sequentially applies a gate voltage to the plurality of gate lines **GL1** to **GLm**.

[0144] A data driver (not illustrated) is disposed adjacent to one end portion of the plurality of data lines **DL1** to **DLn**, and includes a plurality of driving circuit boards **320a**.

[0145] The LCD panel **110** further includes a light blocking member **190** on the first substrate **111**. The light blocking member **190** includes a first light blocking member **191** extending in a first direction **D1**, a second light blocking member **192** extending in a second direction **D2** which intersects the first direction **D1**, and a first edge light blocking member **195** disposed along an edge of the plurality of pixels **PX**.

[0146] According to an alternative exemplary embodiment, the first edge light blocking member **195** may be disposed in a staircase shape (not shown) along an edge of the plurality of pixels **PX**, but exemplary embodiments are not limited thereto.

[0147] The plurality of pixels **PX** may be classified as a first pixel **PX1** disposed in an area not including a corner portion, and a second pixel **PX2** disposed in the corner portion.

[0148] The plurality of pixels **PX** included in the second pixel **PX2** may include second edge light blocking members **196** which defines a display area **DA** and a non-display area **NDA**. The second edge light blocking members **196** will be described under the assumption that one second edge light blocking member **196** is provided for every two second pixels **PX2**, but exemplary embodiments are not limited thereto. In another exemplary embodiment, one second edge light blocking member **196** may be provided for every plurality of second pixels **PX2** that are adjacent to one another, even if this plurality constitutes more than two second pixels **PX2**. In addition, a second edge light blocking member **196** may extend to an edge of the first substrate **111** from a second pixel **PX2**.

[0149] At least some of the second edge light blocking members **196** in the second pixels **PX2** may have different planar areas from one another. In addition, each of the second edge light blocking members **196** may have an inclined portion **SP** for distinguishing the display area **DA** and the non-display area **NDA**, and when connecting each of the inclined portions **SP** of the second edge light blocking members **196**, a curved inner edge **CP** may be defined.

[0150] The second edge light blocking member **196** may be disposed on a same layer as a layer on which a gate wiring including the gate line and a gate electrode is disposed, and may be spaced apart from the gate wiring. In addition, the second edge light blocking member **196** and the gate wiring may include a same material, and may be simultaneously formed in a same process.

[0151] However, exemplary embodiments are not limited thereto, and the second edge light blocking member **196** may be disposed on a same layer as a layer on which a data wiring including the data line, a source electrode, and a drain electrode is disposed, and may be spaced apart from the data wiring. In addition, the second edge light blocking member **196** and the data wiring may include a same material, and may be simultaneously formed in a same process.

[0152] In addition, the second edge light blocking member **196** may be disposed on a same layer as a layer on which a color filter CF is disposed, and in such an exemplary embodiment, the second edge light blocking member **196** may include a red color filter and a blue color filter.

[0153] FIG. **19** is a plan view illustrating another alternative exemplary embodiment of an LCD device, and FIG. **20** is a cross-sectional view illustrating an exemplary embodiment taken along line IV-IV' of FIG. **19**. Hereinafter, repeated descriptions described hereinabove with respect to an exemplary embodiment of an LCD device will be omitted in descriptions with respect to another alternative exemplary embodiment of an LCD device.

[0154] Referring to FIGS. **19** and **20**, another alternative exemplary embodiment of an LCD panel **110** includes a plurality of gate lines GL1 to GLm (or GL) on a first substrate **111**, a plurality of data lines DL1 to DLn (or DL) insulated from and intersecting the plurality of gate lines GL1 to GL, and a plurality of pixels PX which are connected to the plurality of gate lines GL1 to GLm and the plurality of data lines DL1 to DLn, respectively, to display an image.

[0155] A gate driver **210** is disposed adjacent to one end portion of the plurality of gate lines GL1 to GLm, and sequentially applies a gate voltage to the plurality of gate lines GL1 to GLm.

[0156] A data driver (not illustrated) is disposed adjacent to one end portion of the plurality of data lines DL1 to DLn, and includes a plurality of driving circuit boards **320a**.

[0157] The LCD panel **110** may further include a light blocking member **190** on the first substrate **111**. The light blocking member **190** includes a first light blocking member **191** extending in a first direction D1, a second light blocking member **192** extending in a second direction D2 which intersects the first direction D1, and a first edge light blocking member **195**.

[0158] The first edge light blocking member **195** includes at least one curved inner edge CP having a predetermined curvature. A display area DA in which an image is displayed and a non-display area NDA in which an image is not displayed are defined by the first edge light blocking member **195**.

[0159] The plurality of pixels PX include a first pixel PX1 not overlapping the curved inner edge CP of the first edge light blocking member **195** and a second pixel PX2 overlapping at least a portion of the curved inner edge CP of the first edge light blocking member **195**.

[0160] A passivation layer **175** includes a first passivation layer **175a** overlapping the first edge light blocking member **195** and a second passivation layer **175b** not overlapping the

first edge light blocking member **195**. The first passivation layer **175a** may have a lower height than that of the second passivation layer **175b**.

[0161] Accordingly, a step difference that occurs due to the first edge light blocking member **195** may be reduced such that occurrence of a smear may be prevented.

[0162] FIG. **21** is a cross-sectional view illustrating an alternative exemplary embodiment taken along line IV-IV' of FIG. **19**.

[0163] Referring to FIG. **21**, according to an alternative exemplary embodiment, the passivation layer **175** includes a first passivation layer **175a** overlapping the first edge light blocking member **195** and a second passivation layer **175b** not overlapping the first edge light blocking member **195**. The first passivation layer **175a** may have a lower height than that of the second passivation layer **175b**.

[0164] In addition, a color filter CF below the first passivation layer **175a** may be omitted.

[0165] As such, in an alternative exemplary embodiment of the LCD device, a step difference that occurs due to the first edge light blocking member **195** may be prevented such that a smear that occurs due to the first edge light blocking member **195** may be prevented.

[0166] FIG. **22** is a partial enlarged view illustrating still another alternative exemplary embodiment of an LCD device. Hereinafter, repeated descriptions described hereinabove with respect to an exemplary embodiment of an LCD device will be omitted in descriptions with respect to still another alternative exemplary embodiment of an LCD device.

[0167] Referring to FIG. **22**, still another alternative exemplary embodiment of an LCD device includes a plurality of pixels PX that have a longer length in a first direction D1 than that in a second direction D2.

[0168] An LCD panel **110** includes a light blocking member **190** on a first substrate **111**. The light blocking member **190** includes a first light blocking member **191** extending in the first direction D1, a second light blocking member **192** extending in a second direction D2 which intersects the first direction D1, and a first edge light blocking member **195**.

[0169] The first edge light blocking member **195** includes at least one curved inner edge CP having a predetermined curvature. A display area DA in which an image is displayed and a non-display area NDA in which an image is not displayed are defined by the first edge light blocking member **195**.

[0170] The plurality of pixels PX include a first pixel PX1 not overlapping the curved inner edge CP of the first edge light blocking member **195** and a second pixel PX2 overlapping at least a portion of the curved inner edge CP of the first edge light blocking member **195**.

[0171] As the second pixel PX2 is arranged in a staircase shape on a plane, the gate driver **210** and the data lines DL1 to DLn connected to the second pixel PX2 may be arranged in a staircase shape.

[0172] For example, the gate driver **210** includes a plurality of stages ST1 to ST12 connected to respective ones of the gate lines GL1 to GLm, and a stage connected to the second pixel PX2 may protrude toward the second pixel PX2. As such, as the plurality of stages are arranged in a staircase shape, an area of the non-display area NDA may be significantly reduced (e.g., minimized).

[0173] In addition, the data lines DL1 to DLn connected to the second pixel PX2 may extend to be bent into a staircase

shape, but exemplary embodiments are not limited thereto. In an exemplary embodiment, the data lines DL1 to DLn may extend to be bent into a diagonal line or a curved shape.

[0174] A pixel electrode of the first pixel PX1 has a different shape from a shape of a pixel electrode of the second pixel PX2. For example, the second pixel PX2 may have a single domain. Accordingly, a smear that occurs due to a step difference of the first edge light blocking member 195 may be prevented.

[0175] Although a step difference occurs, in an exemplary embodiment of an LCD device, due to a first edge light blocking member, a pixel overlapping the first edge light blocking member only has a single domain, such that occurrence of a smear may be prevented.

[0176] In another alternative exemplary embodiment of an LCD device, a first edge light blocking member and a pixel disposed in a corner portion are prevented from overlapping each other, such that occurrence of a smear may be prevented and a display area having a curvature may be achieved using a second edge light blocking member.

[0177] In still another alternative exemplary embodiment of an LCD device, a step difference that occurs due to the first edge light blocking member is complemented using a passivation layer and a color filter, for example, such that occurrence of a smear may be prevented.

[0178] As set forth hereinabove, in one or more exemplary embodiments of a display device that includes a display area having a curvature, a smear appearing at a curved portion may be significantly reduced.

[0179] From the foregoing, it will be appreciated that various embodiments in accordance with the present disclosure have been described herein for purposes of illustration, and that various modifications may be made without departing from the scope and spirit of the present teachings.

Accordingly, the various embodiments disclosed herein are not intended to be limiting of the true scope and spirit of the present teachings. Various features of the above described and other embodiments can be mixed and matched in any manner, to produce further embodiments consistent with the invention.

1. A display device comprising:

a first substrate;
a plurality of pixels on the first substrate; and
a light blocking layer member disposed on at least one of the first substrate and the second substrate and comprising a curved inner edge,

wherein the plurality of pixels comprise:

a gate line and a data line disposed on the first substrate and extending in non-parallel directions;
a color filter disposed on the first substrate and insulated from the gate line and the data line; and
a passivation layer on the color filter,

wherein the passivation layer comprises:

a first passivation layer overlapping the light blocking layer; and

a second passivation layer disposed in an area around the light blocking layer,

wherein a height of the first passivation layer is lower than a height of the second passivation layer.

2. The display device as claimed in claim 1, wherein the color filter is absent below the first passivation layer.

3. The display device as claimed in claim 1, wherein the light blocking layer is disposed on a same layer as a layer on which the color filter is disposed.

4. The display device as claimed in claim 1, wherein the light blocking layer comprises at least one color filter.

* * * * *

专利名称(译)	具有非直线显示区域的显示装置		
公开(公告)号	US20190196257A1	公开(公告)日	2019-06-27
申请号	US16/286306	申请日	2019-02-26
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	TAE CHANGIL YU SEUNGJUN SONG YOUNGGOO		
发明人	TAE, CHANGIL YU, SEUNGJUN SONG, YOUNGGOO		
IPC分类号	G02F1/1335 G02F1/1333 G02F1/1362 G02F1/1343		
CPC分类号	G02F1/133512 G02F1/133345 G02F1/136286 G02F1/134309 G02F2201/123 G02F2001/136222 G02F2001/134345 G02F2001/133357 G02F2201/56 G02F1/133707 G02F1/13394 G02F1/134336 G02F1/136209		
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摘要(译)

一种显示装置，包括第一基板；覆盖第一基板的第二基板；第一基板和第二基板之间的液晶层；第一基板上的多个像素；光阻挡构件设置在第一基板和第二基板中的至少一个上，光阻挡构件设置在弯曲区域中并限定显示区域和非显示区域。多个像素包括弯曲区域外的第一像素；在弯曲区域中的第二像素，第一像素的像素电极具有与第二像素的像素电极的形状不同的形状。

