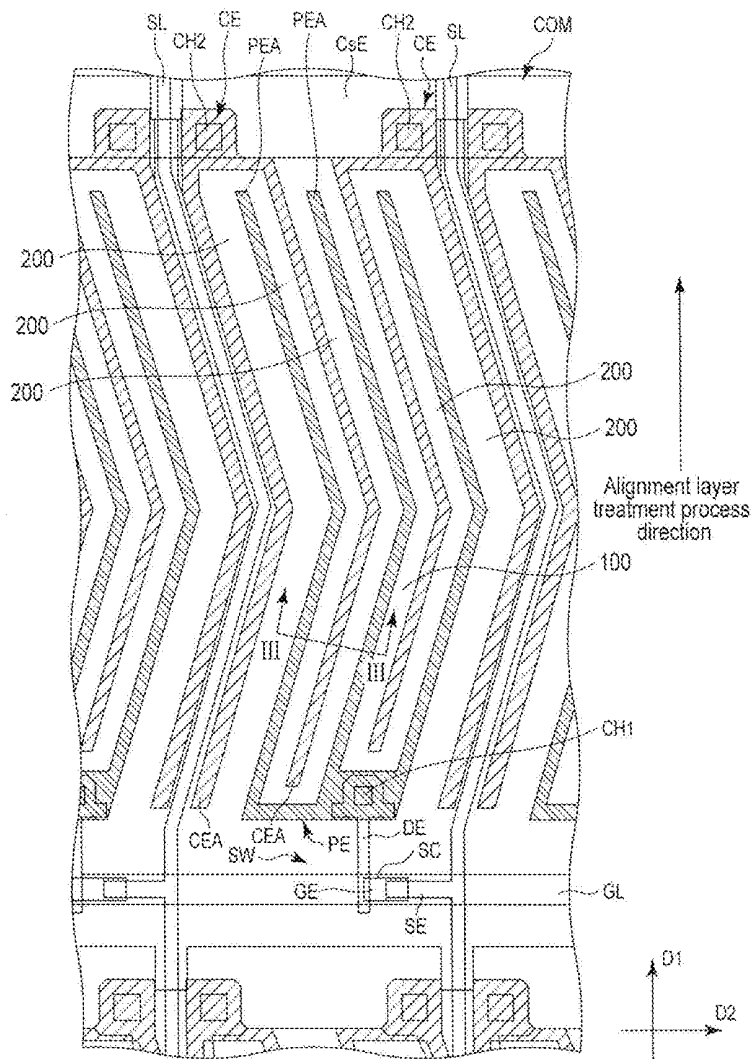


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<i>G02F 1/1333</i>	(2006.01)



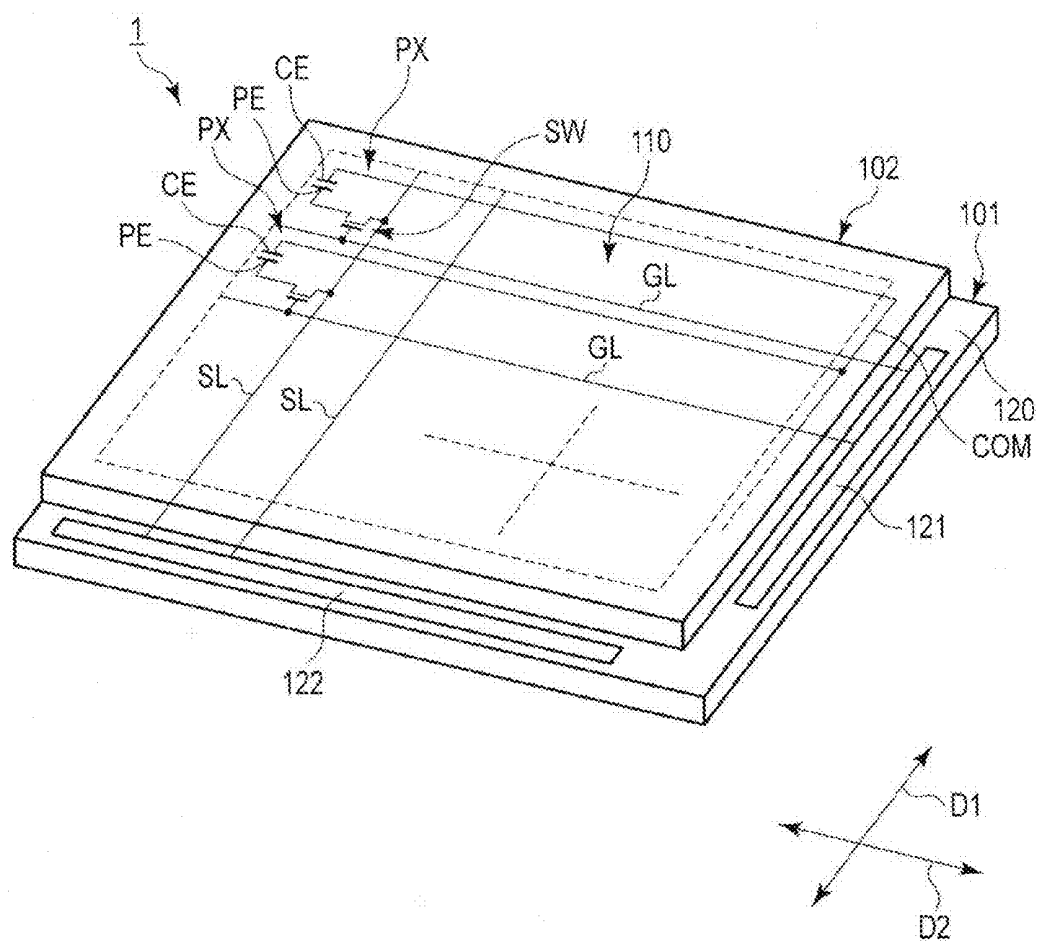


FIG. 1

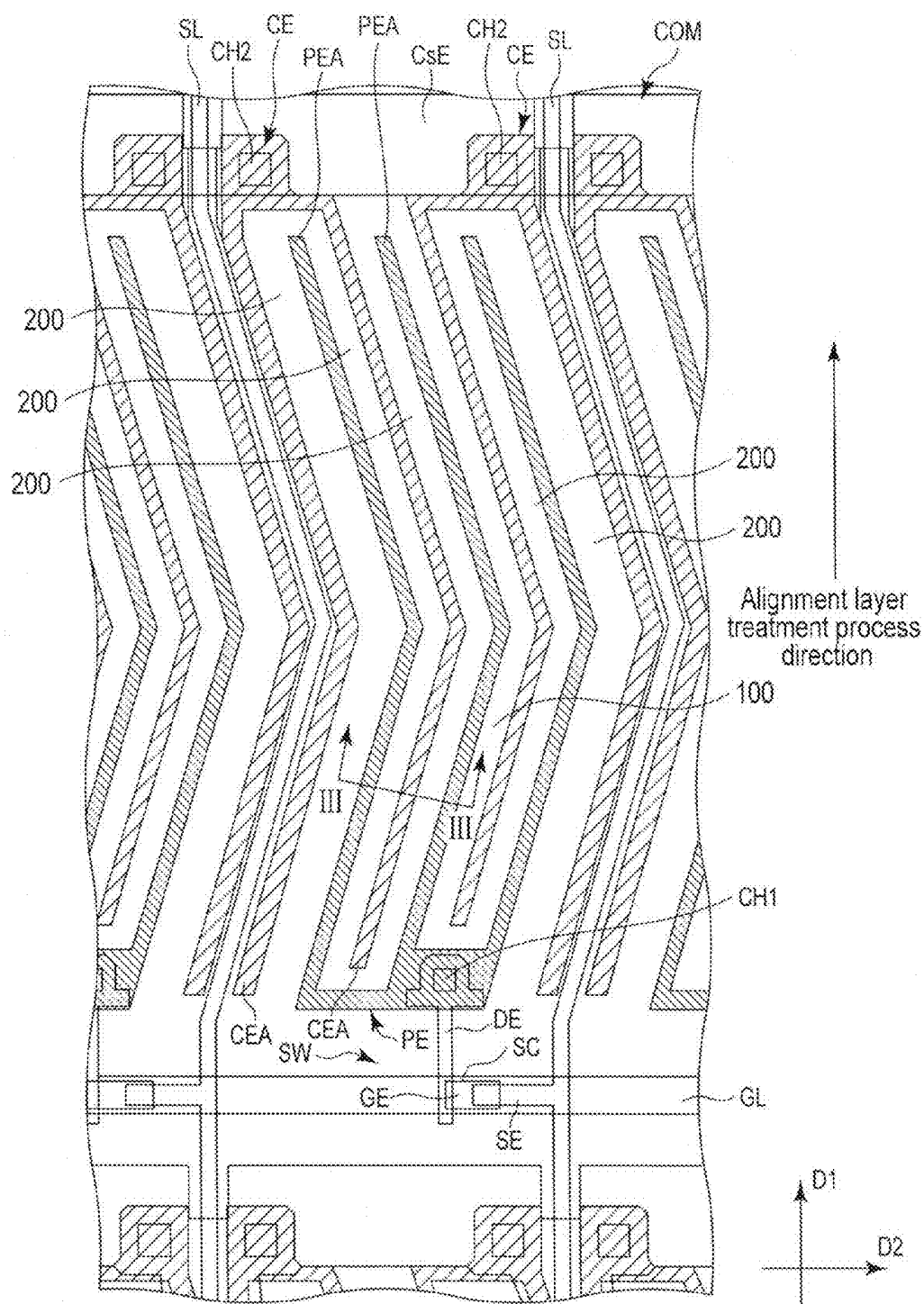


FIG. 2

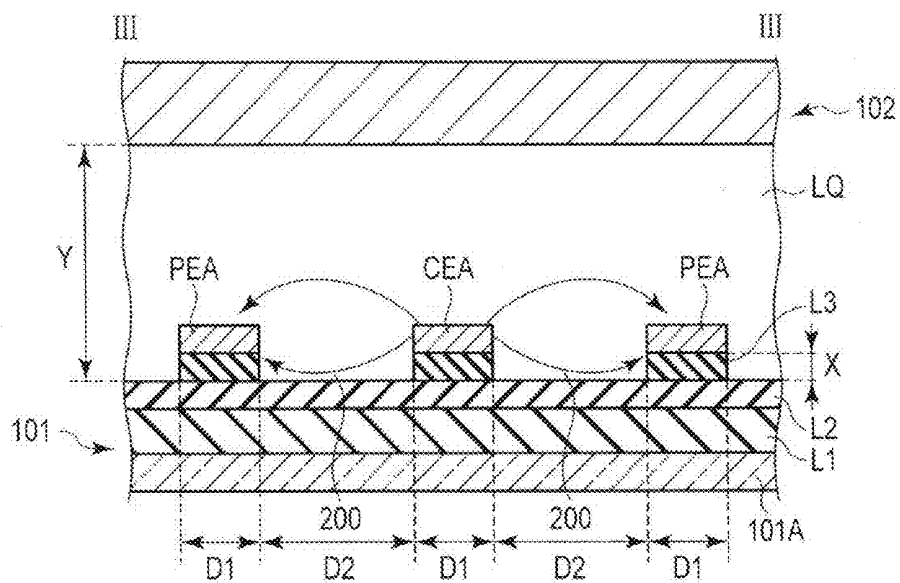


FIG. 3

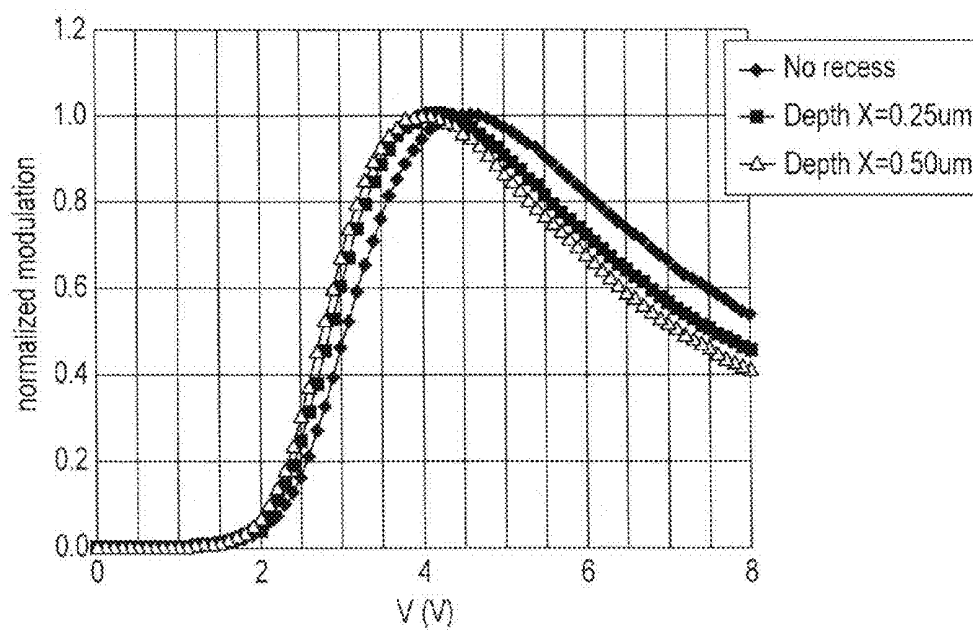


FIG. 4

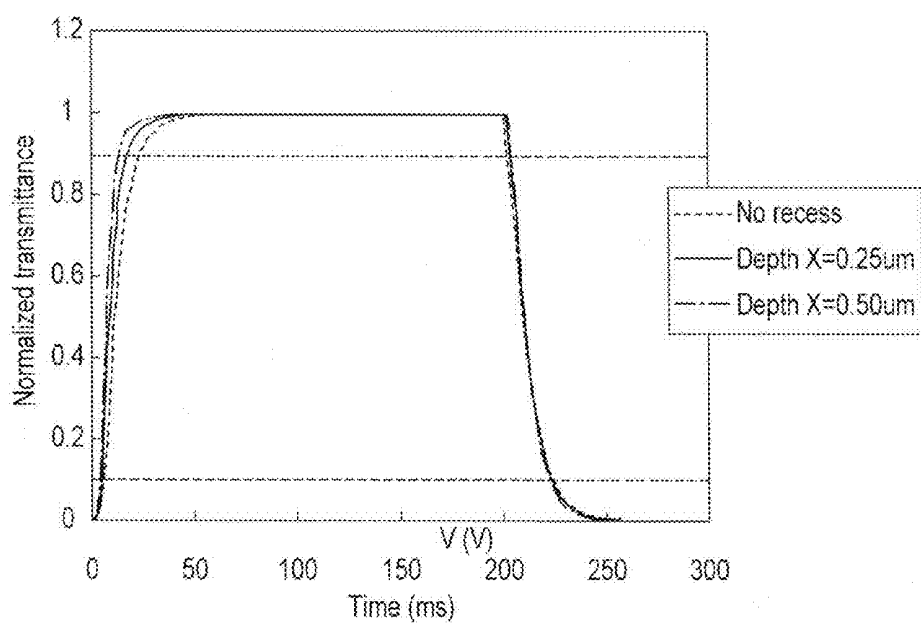


FIG. 5

	No recess	$X=0.25\mu\text{m}$	$X=0.50\mu\text{m}$
τ_{on}	18.9	13.2	8.9
τ_{off}	21.2	19.5	17.9
$\tau_{\text{on}} + \tau_{\text{off}}$	40.1	32.7	26.8

Response time unit : ms

FIG. 6

LIQUID CRYSTAL DISPLAY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2011-267686, filed Dec. 7, 2011, the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate generally to a liquid crystal display.

BACKGROUND

[0003] Recently, flat displays are extensively developed, and liquid crystal displays are particularly applied to various fields by making use of features such as light weight, flatness, and low power consumption. A liquid crystal display like this has a structure in which a liquid crystal layer is held between a pair of substrates, and controls the modulation factor to light passing through the liquid crystal layer by an electric field between a pixel electrode and common electrode, thereby displaying an image.

[0004] The liquid crystal displays are classified into plural types of displays. One is a display in which the alignment state of a liquid crystal is controlled by applying, to the liquid crystal layer, a longitudinal electric field almost perpendicular to the substrate surfaces of the pair of substrates. The other one is a display in which the alignment state of a liquid crystal is controlled by applying, to the liquid crystal layer, a transverse electric field (including a fringe electric field) almost parallel to the substrate surfaces of the pair of substrates.

[0005] The liquid crystal display using the transverse electric field is particularly attracting attention from the viewpoint of a wide viewing angle. The transverse electric field type liquid crystal display having an In-Plane Switching (IPS) mode or Fringe Field Switching (FFS) mode includes pixel electrodes and common electrodes formed on a first substrate.

[0006] In the IPS-mode liquid crystal display, the pixel electrodes and common electrodes are spaced apart and juxtaposed in a direction almost parallel to the substrate surfaces, and a transverse electric field generated between the pixels electrode and common electrode controls the alignment state of liquid crystal molecules.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 is a schematic view showing an arrangement example of a liquid crystal display of an embodiment;

[0008] FIG. 2 is a schematic view showing an arrangement example of a display pixel of the liquid crystal display shown in FIG. 1;

[0009] FIG. 3 is a view for explaining an arrangement example of an array substrate of the liquid crystal display of the embodiment;

[0010] FIG. 4 is a graph showing an example of the simulation result of a normalized modulation factor with respect to a potential difference [V] between a comb pixel electrode and comb common electrode;

[0011] FIG. 5 is a graph showing an example of the simulation result of the change in normalized transmittance with time; and

[0012] FIG. 6 is a table showing the simulation result shown in FIG. 5, i.e., showing the time required for the

transmittance to reach 0.9 from 0.1 when the voltage was ON, the time required for the transmittance to reach 0.1 from 0.9 when the voltage was OFF, and the sum of these times.

DETAILED DESCRIPTION

[0013] In general, according to one embodiment, a liquid crystal display comprises a first substrate comprising a pixel electrode including a plurality of comb pixel electrodes, a common electrode including a plurality of comb common electrodes arranged between the plurality of comb pixel electrodes such that predetermined spaces are formed between the plurality of comb pixel electrodes and the plurality of comb common electrodes, and a recess formed between and along the comb pixel electrode and the comb common electrode; a second substrate opposing the first substrate; and a liquid crystal layer held between the first substrate and the second substrate.

[0014] A liquid crystal display of an embodiment will be explained below with reference to the accompanying drawings.

[0015] FIG. 1 is a schematic view showing an arrangement example of a liquid crystal display 1 of this embodiment. The liquid crystal display 1 according to this embodiment is a normally-black, IPS-mode liquid crystal display, and includes a pair of opposing substrates, i.e., a first substrate 101 and second substrate 102, a liquid crystal layer (not shown) held between the first substrate 101 and second substrate 102, and a display unit 110 including display pixels PX arranged in a matrix. Each of the first substrate 101 and second substrate 102 includes a light-transmitting insulating substrate such as a glass substrate.

[0016] In the display unit 110, the first substrate 101 includes a plurality of scanning lines GL running along a row direction (second direction) D2 in which the display pixels PX are arranged, a plurality of signal lines SL running along a column direction (first direction) D1 in which the display pixels PX are arranged, pixel switches SW arranged near the intersections of the scanning lines GL and signal lines SL, a plurality of pixel electrodes PE formed in one-to-one correspondence with the display pixels PX, and common electrodes CE so arranged as to form transverse electric fields between the plurality of pixel electrodes PE and common electrodes CE.

[0017] On the first substrate 101, a gate driver 121 and source driver 122 are arranged in a region around the display unit 110. The plurality of scanning lines GL are extended to the region around the display unit 110, and connected to the gate driver 121. The plurality of signal lines SL are extended to the region around the display unit 110, and connected to the source driver 122.

[0018] The gate driver 121 sequentially drives the plurality of scanning lines GL, thereby electrically connecting the source and drain of each pixel switch SW connected to the scanning line GL. The source driver 122 supplies an image signal to the plurality of signal lines SL. This image signal supplied to each signal line SL is supplied to the pixel electrode PE via the corresponding pixel switch. A common voltage is applied to the common electrodes CE via a common line COM.

[0019] FIG. 2 is a plan view for explaining an arrangement example of the display pixel PX.

[0020] The pixel switch SW is a thin-film transistor including a semiconductor layer SC made of, e.g., amorphous silicon. Note that the pixel switch SW may also be a thin-film

transistor including a polysilicon semiconductor layer. A gate electrode GE of the pixel switch SW is electrically connected to (or integrated with) a corresponding scanning line GL. A source electrode SE of the pixel switch SW is electrically connected (or integrated with) a corresponding signal line SL. In the liquid crystal display 1 according to this embodiment, the pixel switch SW includes two source electrodes. A drain electrode DE of the pixel switch SW is connected to a corresponding pixel electrode PE via a contact hole CH1.

[0021] The pixel switch SW whose gate potential is controlled by the scanning line GL formed on one side along the first direction D1 switches the electrical connections of the pixel electrode PE to the signal line SL.

[0022] The pixel electrode PE is formed into the shape of a comb by using a transparent electrode material such as ITO (indium tin oxide) or IZO (indium zinc oxide), and includes a plurality of comb pixel electrodes PEA extending almost parallel to the first direction D1 in which the display pixels PX are arranged. Each of the plurality of comb pixel electrodes PEA bends in an almost central portion of the display pixel PX in the longitudinal direction (first direction D1), and extends into the shape of “>”.

[0023] The common electrode CE is formed into the shape of a comb by using a transparent electrode material such as ITO (indium tin oxide) or IZO (indium zinc oxide), and includes a plurality of comb common electrodes CEA extending almost parallel to the first direction D1 in which the display pixels PX are arranged. Each of the plurality of comb common electrodes CEA bends in an almost central portion of the display pixel PX in the longitudinal direction (first direction D1), and extends into the shape of “>”. The common electrode CE is electrically connected to the common line COM (to be described later) in a contact hole CH2.

[0024] Note that the signal lines SL are illustrated as straight lines in FIG. 1, but each signal line SL bends in an almost central portion of the display pixel PX in the longitudinal direction as shown in FIG. 2, like the shape of the comb pixel electrode PEA of the pixel electrode PE and the comb common electrode CEA of the common electrode CE.

[0025] In the same layer as that of the scanning line GL, the common line COM runs almost parallel to the direction (second direction D2) in which the scanning line GL runs. The common line COM is electrically connected to the common electrodes CE arranged for a plurality of pixel electrodes PX arranged in the second direction D2, and applies a common voltage to the common electrodes CE.

[0026] The comb pixel electrodes PEA of the pixel electrodes PE and the comb common electrodes CEA of the common electrodes CE are alternately arranged at predetermined spaces in the second direction D2 in which the display pixels PX are arranged.

[0027] In this embodiment, recesses 200 are formed between the comb pixel electrodes PEA and comb common electrodes CEA. The recesses 200 extend along the comb pixel electrodes PEA and comb common electrodes CEA.

[0028] In the display unit 110, the second substrate 102 includes light-shielding layers (not shown) arranged in the form of a lattice so as to oppose the signal lines SL and scanning lines GL, and a light-shielding layer (not shown) formed to surround the display unit 110. When the liquid crystal display is a color display type liquid crystal display, the second substrate 102 includes a color filter layer (not shown).

[0029] The color filter layer includes a red color filter (not shown) for transmitting light whose dominant wavelength is red, a green color filter (not shown) for transmitting light whose dominant wavelength is green, and a blue color filter (not shown) for transmitting light whose dominant wavelength is blue. Each of these color filters for the plurality of colors is so formed as to oppose one pixel electrode PE.

[0030] A pair of alignment films (not shown) opposing each other with the liquid crystal layer being held between them are formed on the first substrate 101 and second substrate 102. To regulate the initial alignment direction of liquid crystal molecules contained in the liquid crystal layer, an aligning process such as a rubbing process or optical aligning process is performed on the surfaces of these alignment films in a predetermined direction.

[0031] A transverse electric field generated by the potential difference between an image signal supplied to the comb pixel electrodes PEA and the common voltage applied to the comb common electrodes CEA controls the alignment state of the liquid crystal layer.

[0032] FIG. 3 is a view for explaining an arrangement example of the first substrate 101 along a line III-III. The first substrate 101 includes a transparent insulating substrate 101A such as glass, a semiconductor layer (not shown) formed on the transparent insulating substrate 101A, a gate insulating layer L1 formed on the semiconductor layer, the scanning lines GL formed on the gate insulating layer L1, an insulating layer L2 formed on the scanning lines GL, the signal lines SL formed on the insulating layer L2, an insulating layer L3 formed on the signal lines SL, and the comb pixel electrodes PEA and comb common electrodes CEA formed on the insulating layer L3. The insulating layers L1 to L3 are made of, e.g., silicon nitride or HRC.

[0033] The recesses 200 are formed by removing the insulating layer L3 between the comb pixel electrodes PEA and comb common electrodes CEA. When the recesses 200 are formed, the component on the side of the first substrate 101 of an electric field generated between the comb pixel electrode PEA and comb common electrode CEA can be used to control the alignment of a liquid crystal.

[0034] Note that the recesses 200 are formed by removing the insulating layer L3 in FIG. 3, but a plurality of insulating layers may also be removed in accordance with a depth X of the recesses 200. Also, at least one of the insulating layers L1 to L3 need only be removed in the recesses 200. Furthermore, it is also possible to form, on the insulating layer L3, another insulating layer as an underlayer of the comb pixel electrodes PEA and comb common electrodes CEA, and then form the recesses 200.

[0035] An example of the result of simulation performed on the modulation factor with respect to the potential difference [V] between the comb pixel electrode PEA and comb common electrode CEA and the response speed in the liquid crystal display in which the recesses 200 were formed as described above will be explained below.

[0036] In this simulation, the alignment film was rubbed in a direction at an angle of 7° to the direction in which the comb pixel electrodes PEA and comb common electrodes CEA run, dielectric anisotropy $\Delta\epsilon$ of the liquid crystal was set at 9.0, and refractive-index anisotropy Δn of the liquid crystal was set at 0.103 (550 [nm]).

[0037] Also, simulation was performed by changing the depth X of the recess 200 to 0, 0.25, and 0.50 [μm] in a liquid crystal display in which the electrode width D1 of the comb

pixel electrode PEA and comb common electrode CEA was 3.0 [μm], the distance D2 between the electrodes was 5.0 [μm], and a distance (cell gap) Y between the first substrate 101 and second substrate 102 was 3.4 [μm].

[0038] FIG. 4 is a graph showing an example of the simulation result of a normalized modulation factor with respect to the potential difference [V] between the comb pixel electrode PEA and comb common electrode CEA. According to this simulation result, the peak modulation factor when the depth X of the recess 200 was 0 [μm] (when no recess 200 was formed) was higher than those when the depth X of the recess 200 was 0.25 [μm] and 0.50 [μm].

[0039] On the other hand, a voltage at which the modulation factor was highest decreased as the depth X of the recess 200 increased, and the modulation factor when the recesses 200 were formed was higher than that when no recess 200 was formed until the potential difference [V] between the comb pixel electrode PEA and comb common electrode CEA reached 4 [V].

[0040] This is so presumably because when the recesses 200 were formed, an electric field on the side of the first substrate 101, among electric fields generated between the comb pixel electrode PEA and comb common electrode CEA, was used to modulate the liquid crystal, so the modulation factor was high at a low voltage. As described above, when the recesses 200 are formed, the same modulation factor can be obtained by driving at a voltage lower than that when no recess 200 is formed.

[0041] FIG. 5 is a graph showing an example of the simulation result of the change in normalized transmittance with time.

[0042] FIG. 6 is a table showing the simulation result shown in FIG. 5, i.e., showing a time τ_{on} required for the transmittance to reach 0.9 from 0.1 when the voltage was ON, a time τ_{off} required for the transmittance to reach 0.1 from 0.9 when the voltage was OFF, and the sum of these times.

[0043] According to this simulation result, as the depth X of the recess 200 increased, the time τ_{on} when the power supply was ON and the time τ_{off} when the power supply was OFF shortened, and the response of the liquid crystal increased.

[0044] The time τ_{on} shortened when the recesses 200 were formed probably because an electric field on the side of the first substrate 101, among electric fields generated between the comb pixel electrode PEA and comb common electrode CEA, was used to modulate the liquid crystal, so the electric field to be used to modulate the liquid crystal became intense even at the same voltage.

[0045] The time τ_{off} shortened when the recesses 200 were formed perhaps because the cell gap on the comb pixel electrode PEA and comb common electrode CEA decreased, and the anchoring effect occurred on the sidewalls of the recess 200.

[0046] Note that in the above simulation, the distance Y from the bottom surface of the recess 200 to the second substrate 102 was held constant, and the depth X of the recess 200 was changed. Simulation in which the distance from the surfaces of the comb pixel electrode PEA and comb common

electrode CEA to the second substrate 102 was held constant and the depth X of the recess 200 was increased will be explained below.

[0047] In this case, the larger the depth X of the recess 200, the larger the average value of the cell gaps. Therefore, the refractive-index anisotropy Δn is decreased when the retardation ($\Delta n \cdot d$) of the liquid crystal is held constant. Generally, the viscosity of a liquid crystal decreases as the refractive-index anisotropy Δn decreases, and the response time improves when the viscosity decreases.

[0048] That is, in the liquid crystal display of this embodiment, among electric fields generated between the comb pixel electrode PEA and comb common electrode CEA, an electric field on the side of the first substrate 101 contributes to modulation. This makes it possible to decrease the driving voltage, and increase the response speed of a liquid crystal. Accordingly, this embodiment can provide a liquid crystal display capable of reducing the driving voltage and improving the display quality.

[0049] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A liquid crystal display comprising:

a first substrate comprising a pixel electrode including a plurality of comb pixel electrodes, a common electrode including a plurality of comb common electrodes arranged between the plurality of comb pixel electrodes such that predetermined spaces are formed between the plurality of comb pixel electrodes and the plurality of comb common electrodes, and a recess formed between and along the comb pixel electrode and the comb common electrode;

a second substrate opposing the first substrate; and

a liquid crystal layer held between the first substrate and the second substrate.

2. The display according to claim 1, wherein

the first substrate comprises a plurality of insulating layers as underlayers of the comb pixel electrodes and the comb common electrodes, and

at least one of the plurality of insulating layers is removed in the recess.

3. The display according to claim 1, wherein a transverse electric field generated between the comb pixel electrode and the comb common electrode controls an alignment state of a liquid crystal.

4. The display according to claim 2, wherein a transverse electric field generated between the comb pixel electrode and the comb common electrode controls an alignment state of a liquid crystal.

* * * * *

专利名称(译)	液晶显示器		
公开(公告)号	US20130148068A1	公开(公告)日	2013-06-13
申请号	US13/705370	申请日	2012-12-05
[标]申请(专利权)人(译)	前田训久		
申请(专利权)人(译)	前田，训久		
当前申请(专利权)人(译)	日本展示CENTRAL INC.		
[标]发明人	MAEDA NORIHISA		
发明人	MAEDA, NORIHISA		
IPC分类号	G02F1/1343 G02F1/1333		
CPC分类号	G02F1/134309 G02F2001/134381 G02F1/134363 G02F1/133345		
优先权	2011267686 2011-12-07 JP		
外部链接	Espacenet USPTO		

摘要(译)

根据一个实施例，液晶显示器包括：第一基板，包括：像素电极，包括多个梳状像素电极;公共电极，包括布置在多个梳状像素电极之间的多个梳状公共电极，使得在它们之间形成预定空间。多个梳状像素电极和多个梳状公共电极，以及在梳状像素电极和梳状公共电极之间形成的凹槽，与第一基板相对的第二基板，以及保持在第一基板和第一基板之间的液晶层。第二个基板。

