



US 20130093740A1

(19) **United States**(12) **Patent Application Publication**
Wang(10) **Pub. No.: US 2013/0093740 A1**(43) **Pub. Date: Apr. 18, 2013**(54) **LIQUID CRYSTAL ARRAY AND LIQUID
CRYSTAL DISPLAY PANEL****Publication Classification**(75) Inventor: **Jin-jie Wang**, Shenzhen (CN)(51) **Int. Cl.****G09G 3/36** (2006.01)**G06F 3/038** (2006.01)(52) **U.S. Cl.**USPC **345/211; 345/87**(73) Assignee: **SHENZHEN CHINA STAR
OPTOELECTRONICS
TECHNOLOGY CO LTD.**, Shenzhen
(CN)

(57)

ABSTRACT

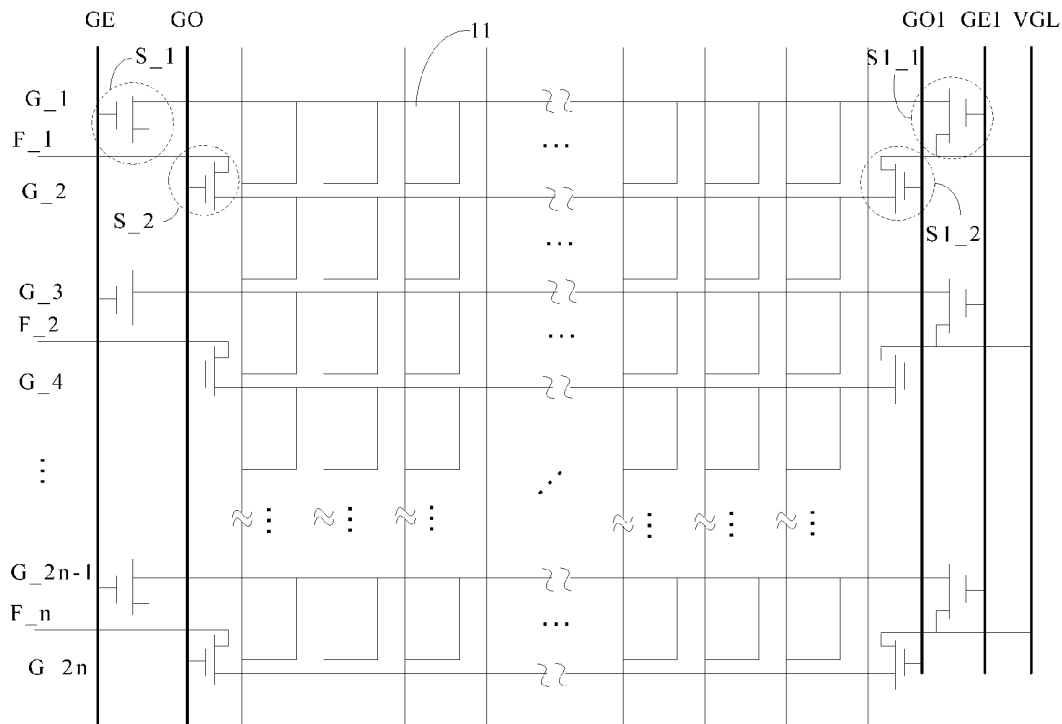
A liquid crystal array comprises a $(2N-1)^{th}$ and a $2N^{th}$ gate line, where N is a positive integer. An area between the $(2N-1)^{th}$ and the $2N^{th}$ gate lines comprises pixels arranged in a row direction. Said array further comprises a N^{th} wiring extension line, a $(2N-1)^{th}$ and a $2N^{th}$ switch elements; the $(2N-1)^{th}$ gate line is connected to the N^{th} wiring extension line via the $(2N-1)^{th}$ switch element, and the $2N^{th}$ gate line is connected to the N^{th} wiring extension line via the $2N^{th}$ switch element; said array further comprises a first and a second selection lines, the first selection line controls a voltage inputted to the $(2N-1)^{th}$ gate line by the $(2N-1)^{th}$ switch element, the second selection line controls a voltage inputted to the $2N^{th}$ gate line by the $2N^{th}$ switch element. The present invention can reduce the number of wiring extension lines, improve space utilization, and reduce cost.

(21) Appl. No.: **13/376,592**(22) PCT Filed: **Oct. 18, 2011**(86) PCT No.: **PCT/CN11/80876**

§ 371 (c)(1),

(2), (4) Date: **Dec. 7, 2011**(30) **Foreign Application Priority Data**

Oct. 14, 2011 (CN) 201110312934.5



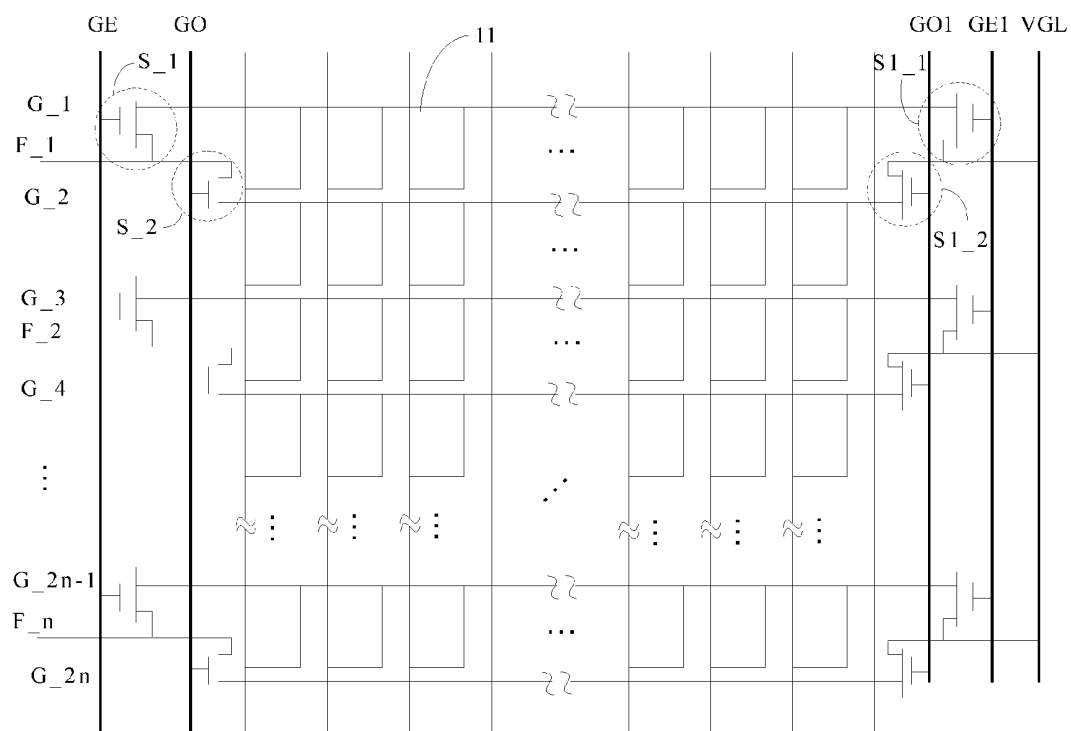


FIG. 1

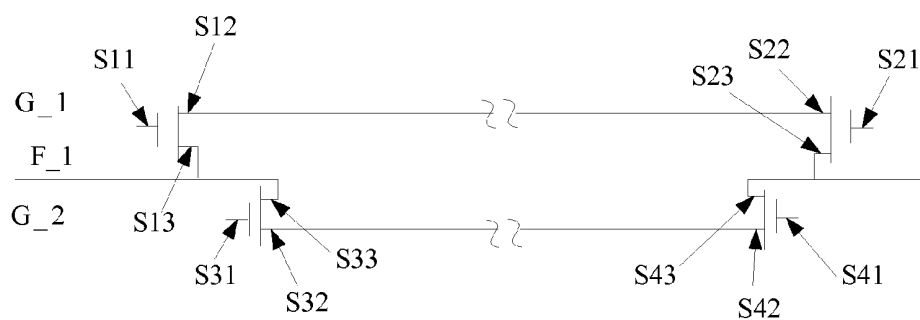


FIG. 2

	GE	GO	GEI	GOI	VGL	F_1	F_2	F_3	G_1	G_2	G_3	G_4	G_5	G_6
T1	H	L	L	H	L	H	L	L	H	L	L	L	L	L
T2	L	II	II	L	L	II	L	L	L	II	L	L	L	L
T3	H	L	L	H	L	L	H	L	L	L	H	L	L	L
T4	L	H	H	L	L	L	H	L	L	L	L	H	L	L
T5	H	L	L	H	L	L	L	H	L	L	L	L	H	L
T6	L	H	H	L	L	L	L	H	L	L	L	L	L	H

FIG. 3

LIQUID CRYSTAL ARRAY AND LIQUID CRYSTAL DISPLAY PANEL

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates to a technical field of a liquid crystal displaying technique, and more particularly, to a liquid crystal array and a liquid crystal display panel.

BACKGROUND OF THE INVENTION

[0002] As liquid crystal displays (LCD) are widely used, the performance of the liquid crystal displays required by users is higher and higher.

[0003] In conventional skills, taking a liquid crystal panel of a resolution $M \times N$ for example, the number of gate wiring extension lines and the number of source wiring extension lines of the liquid crystal panel are respectively N and $3M$ under a single gate driving mode. Assuming that the channel number of a gate driving IC and the channel number of a source driving IC are respectively a and b , the display product needs N/a pieces of gate driving ICs and $3M/b$ pieces of source driving ICs.

[0004] Also, the higher the resolution of the liquid crystal display panel, the greater the number of the wiring extension lines. This will make the space of the liquid crystal panel occupied by the wiring extension lines increased, and the number of the driving ICs is increased as well. It not merely reduces space utilization, but also wastes the resources.

[0005] How to reduce the number of wiring extension lines of the liquid crystal panel, improve space utilization, and reduce manufacturing cost is an important aspect in the liquid crystal displaying technical field.

SUMMARY OF THE INVENTION

[0006] An objective of the present invention is to provide a liquid crystal array for reducing the number of wiring extension lines in a liquid crystal panel, improving space utilization of the liquid crystal panel, and reducing manufacturing cost.

[0007] To achieve the above beneficial effects, the present invention provides a liquid crystal array, comprising a $(2N-1)^{th}$ gate line and a $2N^{th}$ gate line, where N is a positive integer, an area between the $(2N-1)^{th}$ gate line and the $2N^{th}$ gate line comprising a plurality of pixels arranged in a row direction.

[0008] said liquid crystal array further comprises a N^{th} wiring extension line, a $(2N-1)^{th}$ switch element, and a $2N^{th}$ switch element;

[0009] the $(2N-1)^{th}$ gate line is connected to the N^{th} wiring extension line via the $(2N-1)^{th}$ switch element, and the $2N^{th}$ gate line is connected to the N^{th} wiring extension line via the $2N^{th}$ switch element;

[0010] said liquid crystal array further comprises a first selection line and a second selection line, the first selection line comprises a first left selection line and a first right selection line, the second selection line comprises a second left selection line and a second right selection line, the first selection line controls a voltage inputted to the $(2N-1)^{th}$ gate line by utilizing the $(2N-1)^{th}$ switch element, the second selection line controls a voltage inputted to the $2N^{th}$ gate line by utilizing the $2N^{th}$ switch element;

[0011] when the first left selection line provides a first voltage level, the second left selection line provides a second voltage level, the first right selection line pro-

vides the second voltage level, and the second right selection line provides the first voltage level; or

[0012] when the first left selection line provides the second voltage level, the second left selection line provides the first voltage level, the first right selection line provides the first voltage level, and the second right selection line provides the second voltage level.

[0013] In the liquid crystal panel of the present invention, the first voltage level is higher than the second voltage level.

[0014] In the liquid crystal panel of the present invention, the $(2N-1)^{th}$ switch element comprises a $(2N-1)^{th}$ left switch element and a $(2N-1)^{th}$ right switch element, and the $2N^{th}$ switch element comprises a $2N^{th}$ left switch element and a $2N^{th}$ right switch element, wherein the $(2N-1)^{th}$ left switch element and the $2N^{th}$ left switch element are connected to the N^{th} wiring extension line, and the $(2N-1)^{th}$ right switch element and the $2N^{th}$ right switch element are connected to a gate voltage selection line of said liquid crystal array.

[0015] Another objective of the present invention is to provide a liquid crystal array for reducing the number of wiring extension lines in a liquid crystal panel, improving space utilization of the liquid crystal panel, and reducing manufacturing cost.

[0016] To achieve the above beneficial effects, the present invention provides a liquid crystal array, comprising a $(2N-1)^{th}$ gate line and a $2N^{th}$ gate line, where N is a positive integer, an area between the $(2N-1)^{th}$ gate line and the $2N^{th}$ gate line comprising a plurality of pixels arranged in a row direction.

[0017] said liquid crystal array further comprises a N^{th} wiring extension line, a $(2N-1)^{th}$ switch element, and a $2N^{th}$ switch element;

[0018] the $(2N-1)^{th}$ gate line is connected to the N^{th} wiring extension line via the $(2N-1)^{th}$ switch element, and the $2N^{th}$ gate line is connected to the N^{th} wiring extension line via the $2N^{th}$ switch element;

[0019] said liquid crystal array further comprises a first selection line and a second selection line, the first selection line controls a voltage inputted to the $(2N-1)^{th}$ gate line by utilizing the $(2N-1)^{th}$ switch element, the second selection line controls a voltage inputted to the $2N^{th}$ gate line by utilizing the $2N^{th}$ switch element.

[0020] In the liquid crystal panel of the present invention, the first selection line comprises a first left selection line and a first right selection line, the second selection line comprises a second left selection line and a second right selection line; the first left selection line, the first right selection line, the second left selection line, and the second right selection line provide a first voltage level or a second voltage level according to a predetermined time sequence, wherein the first voltage level is higher than the second voltage level.

[0021] In the liquid crystal panel of the present invention, when the first left selection line provides the first voltage level, the second left selection line provides the second voltage level, the first right selection line provides the second voltage level, and the second right selection line provides the first voltage level.

[0022] In the liquid crystal panel of the present invention, when the first left selection line provides the second voltage level, the second left selection line provides the first voltage level, the first right selection line provides the first voltage level, and the second right selection line provides the second voltage level.

[0023] In the liquid crystal panel of the present invention, the $(2N-1)^{th}$ switch element comprises a $(2N-1)^{th}$ left switch

element and a $(2N-1)^{th}$ right switch element, and the $2N^{th}$ switch element comprises a $2N^{th}$ left switch element and a $2N^{th}$ right switch element, wherein the $(2N-1)^{th}$ left switch element and the $2N^{th}$ left switch element are connected to the N^{th} wiring extension line, and the $(2N-1)^{th}$ right switch element and the $2N^{th}$ right switch element are connected to a gate voltage selection line of said liquid crystal array.

[0024] Still another objective of the present invention is to provide a liquid crystal display panel for reducing the number of wiring extension lines, improving space utilization, and reducing manufacturing cost.

[0025] To achieve the above beneficial effects, the present invention provides a liquid crystal display panel, comprising a liquid crystal array, said liquid crystal array comprising a $(2N-1)^{th}$ gate line and a $2N^{th}$ gate line, where N is a positive integer, an area between the $(2N-1)^{th}$ gate line and the $2N^{th}$ gate line comprising a plurality of pixels arranged in a row direction.

[0026] said liquid crystal array further comprises a N^{th} wiring extension line, a $(2N-1)^{th}$ switch element, and a $2N^{th}$ switch element;

[0027] the $(2N-1)^{th}$ gate line is connected to the N^{th} wiring extension line via the $(2N-1)^{th}$ switch element, and the $2N^{th}$ gate line is connected to the N^{th} wiring extension line via the $2N^{th}$ switch element;

[0028] said liquid crystal array further comprises a first selection line and a second selection line, the first selection line controls a voltage inputted to the $(2N-1)^{th}$ gate line by utilizing the $(2N-1)^{th}$ switch element, the second selection line controls a voltage inputted to the $2N^{th}$ gate line by utilizing the $2N^{th}$ switch element.

[0029] In the liquid crystal display panel of the present invention, the first selection line comprises a first left selection line and a first right selection line, the second selection line comprises a second left selection line and a second right selection line; the first left selection line, the first right selection line, the second left selection line, and the second right selection line provide a first voltage level or a second voltage level according to a predetermined time sequence, wherein the first voltage level is higher than the second voltage level.

[0030] In the liquid crystal display panel of the present invention, when the first left selection line provides the first voltage level, the second left selection line provides the second voltage level, the first right selection line provides the second voltage level, and the second right selection line provides the first voltage level.

[0031] In the liquid crystal display panel of the present invention, when the first left selection line provides the second voltage level, the second left selection line provides the first voltage level, the first right selection line provides the first voltage level, and the second right selection line provides the second voltage level.

[0032] In the liquid crystal display panel of the present invention, the $(2N-1)^{th}$ switch element comprises a $(2N-1)^{th}$ left switch element and a $(2N-1)^{th}$ right switch element, and the $2N^{th}$ switch element comprises a $2N^{th}$ left switch element and a $2N^{th}$ right switch element, wherein the $(2N-1)^{th}$ left switch element and the $2N^{th}$ left switch element are connected to the N^{th} wiring extension line, and the $(2N-1)^{th}$ right switch element and the $2N^{th}$ right switch element are connected to a gate voltage selection line of said liquid crystal array.

[0033] Compared to conventional skills, the present invention can reduce the number of wiring extension lines in the

liquid crystal panel, improve space utilization of the liquid crystal panel, and reduce manufacturing cost.

[0034] To make above content of the present invention more easily understood, it will be described in details by using preferred embodiments in conjunction with the appending drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] FIG. 1 is a structural diagram showing a liquid crystal array according to a preferred embodiment of the present invention.

[0036] FIG. 2 is a structural diagram showing switch elements in the present invention.

[0037] FIG. 3 is a schematic diagram showing a predetermined time sequence in the embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0038] The following descriptions for the respective embodiments are specific embodiments capable of being implemented for illustrations of the present invention with referring to appended figures.

[0039] FIG. 1 is a structural diagram showing a liquid crystal array according to a preferred embodiment of the present invention.

[0040] The liquid crystal array comprises a $(2N-1)^{th}$ gate line G_{2n-1} and a $2N^{th}$ gate line G_{2n} , where N is a positive integer. An area between the $(2N-1)^{th}$ gate line G_{2n-1} and the $2N^{th}$ gate line G_{2n} comprises a plurality of pixels 11 arranged in a row direction.

[0041] In the embodiment shown in FIG. 1, the liquid crystal array further comprises a N^{th} wiring extension line F_n , a $(2N-1)^{th}$ switch element, and a $2N^{th}$ switch element. In the present embodiment, the $(2N-1)^{th}$ switch element comprises a $(2N-1)^{th}$ left switch element S_{2n-1} and a $(2N-1)^{th}$ right switch element $S1_{2n-1}$; and the $2N^{th}$ switch element comprises a $2N^{th}$ left switch element S_{2n} and a $2N^{th}$ right switch element $S1_{2n}$.

[0042] Referring to FIG. 1, the liquid crystal array further comprises a first selection line and a second selection line. The first selection line comprises a first left selection line GE and a first right selection line $GE1$; the second selection line comprises a second left selection line GO and a second right selection line $GO1$.

[0043] Referring to FIG. 2, a first left switch element S_{2n-1} , a first right switch element $S1_{2n-1}$, a second left switch element S_{2n} , and a second right switch element $S1_{2n}$ are illustrated for example. The first left switch element S_{2n-1} comprises a first terminal $S11$, a second terminal $S12$, and a third terminal $S13$; the first right switch element $S1_{2n-1}$ comprises a first terminal $S21$, a second terminal $S22$, and a third terminal $S23$; the second left switch element S_{2n} comprises a first terminal $S31$, a second terminal $S32$, and a third terminal $S33$; the second right switch element $S1_{2n}$ comprises a first terminal $S41$, a second terminal $S42$, and a third terminal $S43$.

[0044] The $(2N-1)^{th}$ gate line G_{2n-1} is connected to the second terminal $S12$ of the $(2N-1)^{th}$ left switch element S_{2n-1} and the second terminal $S22$ of the $(2N-1)^{th}$ right switch element $S1_{2n-1}$; the $2N^{th}$ gate line G_{2n} is connected to the second terminal $S32$ of the $2N^{th}$ left switch element S_{2n} and the second terminal $S42$ of the $2N^{th}$ right switch element $S1_{2n}$.

[0045] The third terminal S13 of the $(2N-1)^{th}$ left switch element S_{2n-1} and the third terminal S33 of the $2N^{th}$ left switch element S_{2n} are connected to the N^{th} wiring extension line F_n; the third terminal S23 of the $(2N-1)^{th}$ right switch element S1_{2n-1} and the third terminal S43 of the $2N^{th}$ right switch element S1_{2n} are connected to a gate voltage selection line VGL.

[0046] The first terminal S11 of the $(2N-1)^{th}$ left switch element S_{2n-1} is connected to the first left selection line GE; the first terminal S31 of the $2N^{th}$ left switch element S_{2n} is connected to the second left selection line GO; the first terminal S21 of the $(2N-1)^{th}$ right switch element S1_{2n-1} is connected to the first right selection line GE1; the first terminal S41 of the $2N^{th}$ right switch element S1_{2n} is connected to the second right selection line GO1.

[0047] The first left selection line GE, the first right selection line GE1, the second left selection line GO, and the second right selection line GO1 provide a first voltage level H or a second voltage level L according to a predetermined time sequence, wherein the first voltage level H is higher than the second voltage level L.

[0048] In the present embodiment, the first left selection line GE and the first right selection line GE1 control a voltage inputted to the $(2N-1)^{th}$ gate line respectively by utilizing the $(2N-1)^{th}$ left switch element S_{2n-1} and the $(2N-1)^{th}$ right switch element S1_{2n-1}; the second left selection line GO and the second right selection line GO1 control a voltage inputted to the $2N^{th}$ gate line respectively by utilizing the $2N^{th}$ left switch element S_{2n} and the $2N^{th}$ right switch element S1_{2n}.

[0049] In the embodiment shown in FIG. 1, when the first left selection line GE provides the first voltage level, the second left selection line GO provides the second voltage level, the first right selection line GE1 provides the second voltage level, and the second right selection line GO1 provides the first voltage level.

[0050] In the embodiment shown in FIG. 1, when the first left selection line GE provides the second voltage level, the second left selection line GO provides the first voltage level, the first right selection line GE1 provides the first voltage level, and the second right selection line GO1 provides the second voltage level.

[0051] The more concrete working process of the preferred embodiment of the present invention is described below.

[0052] At the moment T1, the first left selection line GE is inputted with the first voltage level H, the second left selection line GO is inputted with the second voltage level L, a first wiring extension line F₁ is inputted with the first voltage level H, a second wiring extension line F₂ to the N^{th} wiring extension line F_n are inputted with the second voltage level L, the second right selection line GO1 is inputted with the first voltage level H, the first right selection line GE1 is inputted with the second voltage level L, and the gate voltage selection line VGL maintains at the second voltage level L.

[0053] Since the first left selection line GE is inputted with the first voltage level H, a signal on the first wiring extension line F₁ can be transmitted to the first gate line G₁ to turn on thin film transistors (TFTs) corresponding to the first gate line G₁. At this moment, the second voltage level L signal of the gate voltage selection line VGL will not enter the first gate line G₁ since the first right selection line GE1 is inputted with the second voltage level L.

[0054] At the same time, the first voltage level H signal of the first wiring selection line F₁ can not enter the second

gate line G₂ since the second left selection line GO is inputted with the second voltage level L. The second voltage level L signal of the gate voltage selection line VGL will enter the second gate line G₂ since the second right selection line GO1 is inputted with the first voltage level H.

[0055] At the same time, a second wiring extension line F₂ is inputted with the second voltage level L. Since the first left selection line GE is inputted with the first voltage level H, the second voltage level L signal of the second wiring extension line F₂ will enter the third gate line G₃. Also, the second voltage level L signal of the gate voltage selection line VGL will enter the fourth gate line G₄ since the second right selection line GO1 is inputted with the first voltage level H.

[0056] The working processes of a third wiring extension line F₃ to the N^{th} wiring extension line F_n are similar to above descriptions, and therefore the descriptions regarding this part are omitted herein.

[0057] At the moment T2, the first left selection line GE is inputted with the second voltage level L, the second left selection line GO is inputted with the first voltage level H, the first wiring extension line F₁ is inputted with the first voltage level H, the second wiring extension line F₂ to the N^{th} wiring extension line F_n are inputted with the second voltage level L, the second right selection line GO1 is inputted with the second voltage level L, the first right selection line GE1 is inputted with the first voltage level H, and the gate voltage selection line VGL maintains at the second voltage level L.

[0058] Since the second left selection line GO is inputted with the first voltage level H, a signal on the first wiring extension line F₁ will enter the second gate line G₂ to turn on TFTs corresponding to the second gate line G₂. At this moment, the second voltage level L signal of the gate voltage selection line VGL will not enter the second gate line G₂ since the second right selection line GO1 is inputted with the second voltage level L.

[0059] At the same time, the first voltage level H signal of the first wiring selection line F₁ can not enter the first gate line G₁ since the first left selection line GE is inputted with the second voltage level L. The second voltage level L signal of the gate voltage selection line VGL will enter the first gate line G₁ since the first right selection line GE1 is inputted with the first voltage level H.

[0060] At the same time, the second wiring extension line F₂ is inputted with the second voltage level L. Since the second left selection line GO is inputted with the first voltage level H, the second voltage level L signal of the second wiring extension line F₂ will enter the fourth gate line G₄. Also, the second voltage level L signal of the gate voltage selection line VGL will enter the third gate line G₃ since the first right selection line GE1 is inputted with the first voltage level H.

[0061] The working processes of a third wiring extension line F₃ to the N^{th} wiring extension line F_n are similar to above descriptions, and therefore the descriptions regarding this part are omitted herein.

[0062] Referring to FIG. 3, FIG. 3 is a schematic diagram showing a predetermined time sequence in the present invention. Obviously, the embodiments of the present invention can carry out "opening" and "closing" the gate lines in order by presetting the signal timing to control the first selection line and the second selection line. Also, compared to the design of one gate line corresponding to one wiring extension line in conventional skills, the number of wiring extension

lines of the embodiments of the present invention can be reduced by half and the number of driving chips are reduced as well since two gate lines correspond to one wiring extension line in the present invention. The present invention not merely makes the best use of the wiring space, but also reduces the cost.

[0063] The present invention further provides a liquid crystal display panel. Said liquid crystal display panel comprises the liquid crystal array provided in the embodiments of the present invention. Since the liquid crystal array is detailedly described above, the descriptions regarding this part are omitted herein.

[0064] While the preferred embodiments of the present invention have been illustrated and described in detail, various modifications and alterations can be made by persons skilled in this art. The embodiment of the present invention is therefore described in an illustrative but not restrictive sense. It is intended that the present invention should not be limited to the particular forms as illustrated, and that all modifications and alterations which maintain the spirit and realm of the present invention are within the scope as defined in the appended claims.

What is claimed is:

1. A liquid crystal array, comprising a $(2N-1)^{th}$ gate line and a $2N^{th}$ gate line, where N is a positive integer, an area between the $(2N-1)^{th}$ gate line and the $2N^{th}$ gate line comprising a plurality of pixels arranged in a row direction, characterized in that:

said liquid crystal array further comprises a N^{th} wiring extension line, a $(2N-1)^{th}$ switch element, and a $2N^{th}$ switch element;

the $(2N-1)^{th}$ gate line is connected to the N^{th} wiring extension line via the $(2N-1)^{th}$ switch element, and the $2N^{th}$ gate line is connected to the N^{th} wiring extension line via the $2N^{th}$ switch element;

said liquid crystal array further comprises a first selection line and a second selection line, the first selection line comprises a first left selection line and a first right selection line, the second selection line comprises a second left selection line and a second right selection line, the first selection line controls a voltage inputted to the $(2N-1)^{th}$ gate line by utilizing the $(2N-1)^{th}$ switch element, the second selection line controls a voltage inputted to the $2N^{th}$ gate line by utilizing the $2N^{th}$ switch element;

when the first left selection line provides a first voltage level, the second left selection line provides a second voltage level, the first right selection line provides the second voltage level, and the second right selection line provides the first voltage level; or

when the first left selection line provides the second voltage level, the second left selection line provides the first voltage level, the first right selection line provides the first voltage level, and the second right selection line provides the second voltage level.

2. The liquid crystal array according to claim 1, characterized in that the first voltage level is higher than the second voltage level.

3. The liquid crystal array according to claim 2, characterized in that the $(2N-1)^{th}$ switch element comprises a $(2N-1)^{th}$ left switch element and a $(2N-1)^{th}$ right switch element, and the $2N^{th}$ switch element comprises a $2N^{th}$ left switch element and a $2N^{th}$ right switch element, wherein the $(2N-1)^{th}$ left switch element and the $2N^{th}$ left switch element are connected

to the N^{th} wiring extension line, and the $(2N-1)^{th}$ right switch element and the $2N^{th}$ right switch element are connected to a gate voltage selection line of said liquid crystal array.

4. A liquid crystal array, comprising a $(2N-1)^{th}$ gate line and a $2N^{th}$ gate line, where N is a positive integer, an area between the $(2N-1)^{th}$ gate line and the $2N^{th}$ gate line comprising a plurality of pixels arranged in a row direction, characterized in that:

said liquid crystal array further comprises a N^{th} wiring extension line, a $(2N-1)^{th}$ switch element, and a $2N^{th}$ switch element;

the $(2N-1)^{th}$ gate line is connected to the N^{th} wiring extension line via the $(2N-1)^{th}$ switch element, and the $2N^{th}$ gate line is connected to the N^{th} wiring extension line via the $2N^{th}$ switch element;

said liquid crystal array further comprises a first selection line and a second selection line, the first selection line controls a voltage inputted to the $(2N-1)^{th}$ gate line by utilizing the $(2N-1)^{th}$ switch element, the second selection line controls a voltage inputted to the $2N^{th}$ gate line by utilizing the $2N^{th}$ switch element.

5. The liquid crystal array according to claim 4, characterized in that the first selection line comprises a first left selection line and a first right selection line, the second selection line comprises a second left selection line and a second right selection line;

the first left selection line, the first right selection line, the second left selection line, and the second right selection line provide a first voltage level or a second voltage level according to a predetermined time sequence, wherein the first voltage level is higher than the second voltage level.

6. The liquid crystal array according to claim 5, characterized in that when the first left selection line provides the first voltage level, the second left selection line provides the second voltage level, the first right selection line provides the second voltage level, and the second right selection line provides the first voltage level.

7. The liquid crystal array according to claim 5, characterized in that when the first left selection line provides the second voltage level, the second left selection line provides the first voltage level, the first right selection line provides the first voltage level, and the second right selection line provides the second voltage level.

8. The liquid crystal array according to claim 5, characterized in that the $(2N-1)^{th}$ switch element comprises a $(2N-1)^{th}$ left switch element and a $(2N-1)^{th}$ right switch element, and the $2N^{th}$ switch element comprises a $2N^{th}$ left switch element and a $2N^{th}$ right switch element, wherein the $(2N-1)^{th}$ left switch element and the $2N^{th}$ left switch element are connected to the N^{th} wiring extension line, and the $(2N-1)^{th}$ right switch element and the $2N^{th}$ right switch element are connected to a gate voltage selection line of said liquid crystal array.

9. A liquid crystal display panel, comprising a liquid crystal array, said liquid crystal array comprising a $(2N-1)^{th}$ gate line and a $2N^{th}$ gate line, where N is a positive integer, an area between the $(2N-1)^{th}$ gate line and the $2N^{th}$ gate line comprising a plurality of pixels arranged in a row direction, characterized in that:

said liquid crystal array further comprises a N^{th} wiring extension line, a $(2N-1)^{th}$ switch element, and a $2N^{th}$ switch element;

the $(2N-1)^{th}$ gate line is connected to the N^{th} wiring extension line via the $(2N-1)^{th}$ switch element, and the $2N^{th}$ gate line is connected to the N^{th} wiring extension line via the $2N^{th}$ switch element;

said liquid crystal array further comprises a first selection line and a second selection line, the first selection line controls a voltage inputted to the $(2N-1)^{th}$ gate line by utilizing the $(2N-1)^{th}$ switch element, the second selection line controls a voltage inputted to the $2N^{th}$ gate line by utilizing the $2N^{th}$ switch element.

10. The liquid crystal display panel according to claim **9**, characterized in that the first selection line comprises a first left selection line and a first right selection line, the second selection line comprises a second left selection line and a second right selection line;

the first left selection line, the first right selection line, the second left selection line, and the second right selection line provide a first voltage level or a second voltage level according to a predetermined time sequence, wherein the first voltage level is higher than the second voltage level.

11. The liquid crystal display panel according to claim **10**, characterized in that when the first left selection line provides the first voltage level, the second left selection line provides the second voltage level, the first right selection line provides the second voltage level, and the second right selection line provides the first voltage level.

12. The liquid crystal display panel according to claim **10**, characterized in that when the first left selection line provides the second voltage level, the second left selection line provides the first voltage level, the first right selection line provides the first voltage level, and the second right selection line provides the second voltage level.

13. The liquid crystal display panel according to claim **10**, characterized in that the $(2N-1)^{th}$ switch element comprises a $(2N-1)^{th}$ left switch element and a $(2N-1)^{th}$ right switch element, and the $2N^{th}$ switch element comprises a $2N^{th}$ left switch element and a $2N^{th}$ right switch element, wherein the $(2N-1)^{th}$ left switch element and the $2N^{th}$ left switch element are connected to the N^{th} wiring extension line, and the $(2N-1)^{th}$ right switch element and the $2N^{th}$ right switch element are connected to a gate voltage selection line of said liquid crystal array.

* * * * *

专利名称(译)	液晶阵列和液晶显示板		
公开(公告)号	US20130093740A1	公开(公告)日	2013-04-18
申请号	US13/376592	申请日	2011-10-18
[标]申请(专利权)人(译)	王金结		
申请(专利权)人(译)	王，金杰		
当前申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
[标]发明人	WANG JIN JIE		
发明人	WANG, JIN-JIE		
IPC分类号	G09G3/36 G06F3/038		
CPC分类号	G09G2300/0465 G09G3/3659		
优先权	201110312934.5 2011-10-14 CN		
外部链接	Espacenet USPTO		

摘要(译)

液晶阵列包括第 $(2N-1)$ 和第 $2N$ 栅极线，其中 N 是正整数。第 $(2N-1)$ 和第 $2N$ 栅极线之间的区域包括沿行方向排列的像素。所述阵列还包括第 N 布线延长线，第 $(2N-1)$ 和第 $2N$ 开关元件；第 $(2N-1)$ 栅极线通过第 $(2N-1)$ 开关元件连接到第 N 布线延长线，第 $2N$ 栅极线通过第 $2N$ 开关元件连接到第 N 布线延长线；所述阵列还包括第一和第二选择线，第一选择线控制由第 $(2N-1)$ 个开关元件输入到第 $(2N-1)$ 栅极线的电压，第二选择线控制输入的电压。第 $2N$ th 开关元件的第 $2N$ 栅极线。本发明可以减少布线延长线的数量，提高空间利用率并降低成本。

