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(54) **LIQUID CRYSTAL DISPLAY DEVICE AND RELATED ALIGNMENT METHOD**

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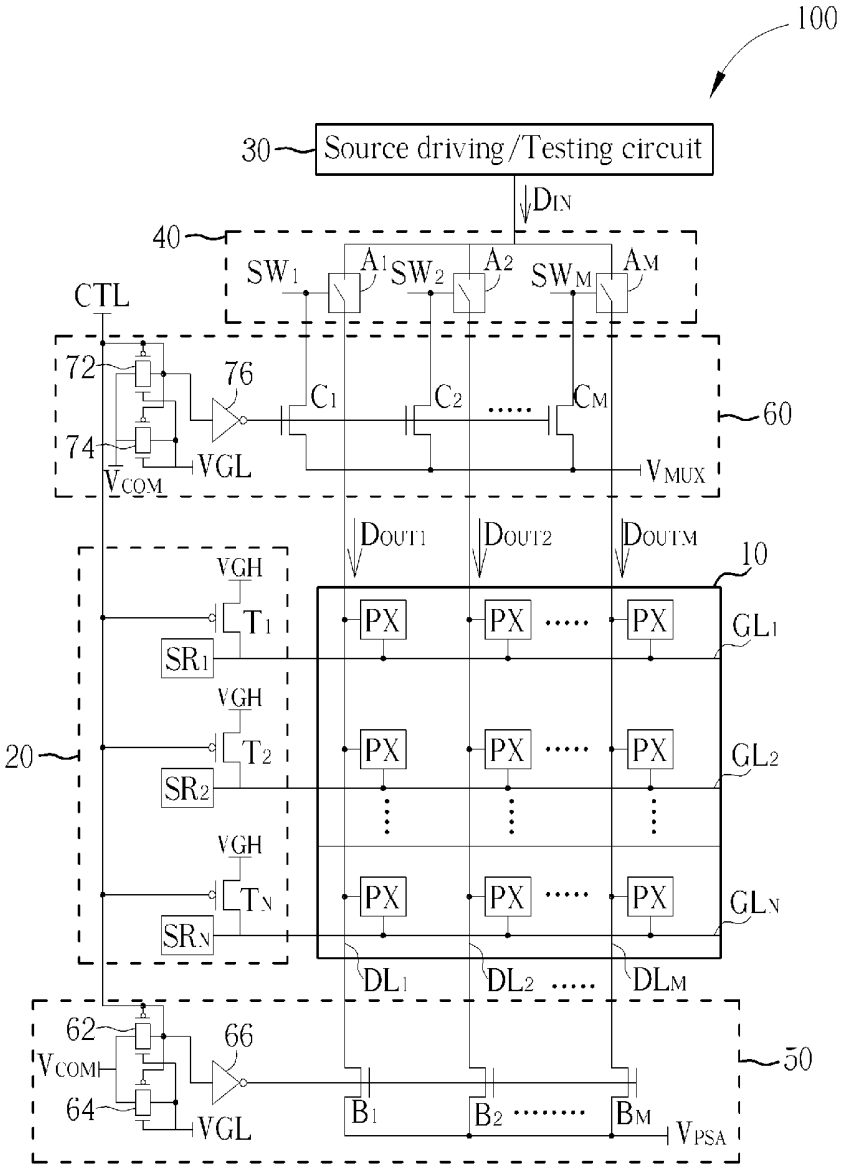
(57) **ABSTRACT**

A liquid crystal display device includes a display panel, a multiplexer, an alignment circuit and a short bar circuit. The multiplexer is configured to provide a plurality of output data signals according to a plurality of switch control signals and an input data signal. During the alignment period, the alignment circuit is configured to provide a curing voltage to the display panel, and the short bar circuit is configured to couple the multiplexer to a predetermined voltage.



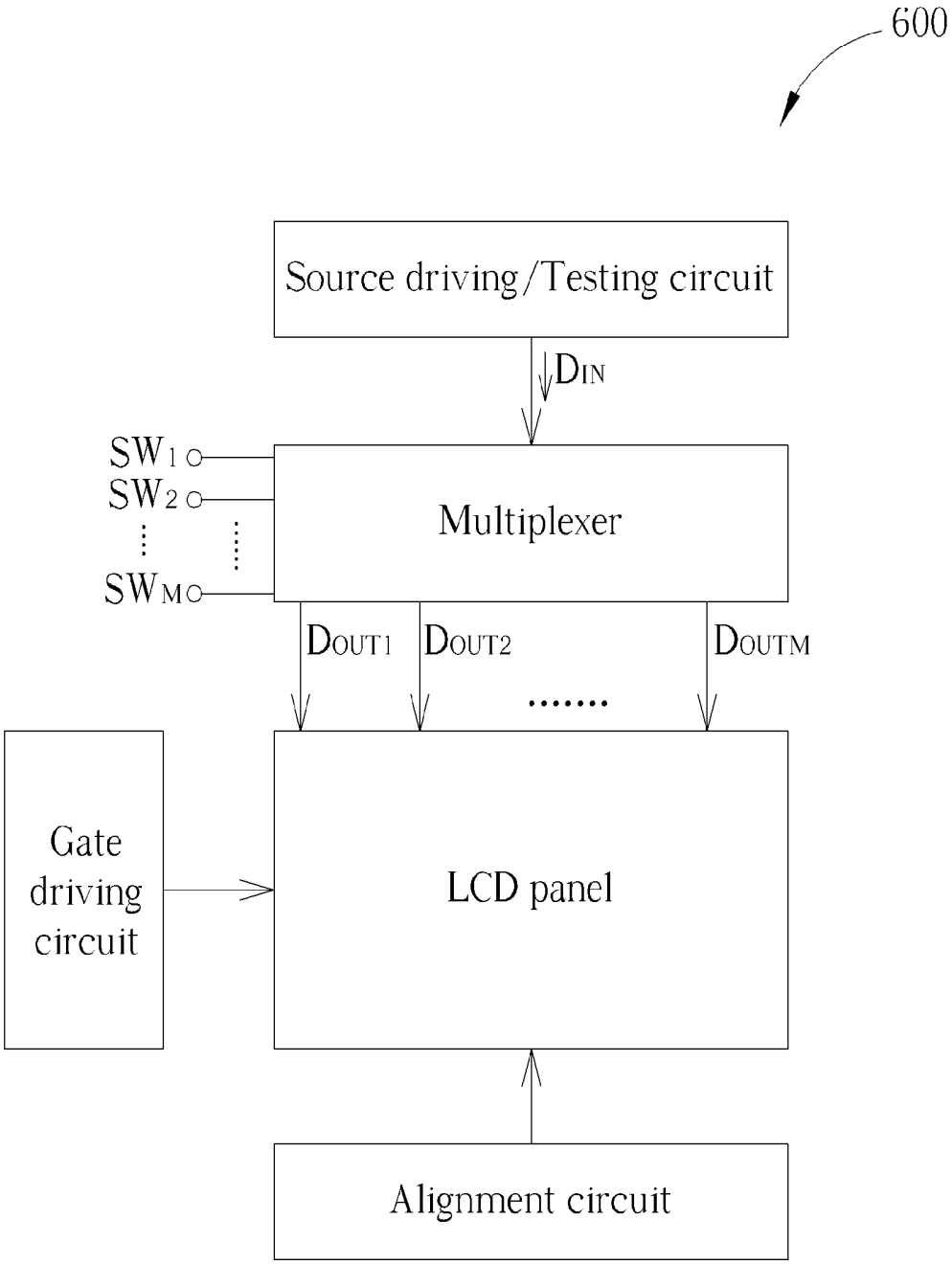


FIG. 1 PRIOR ART

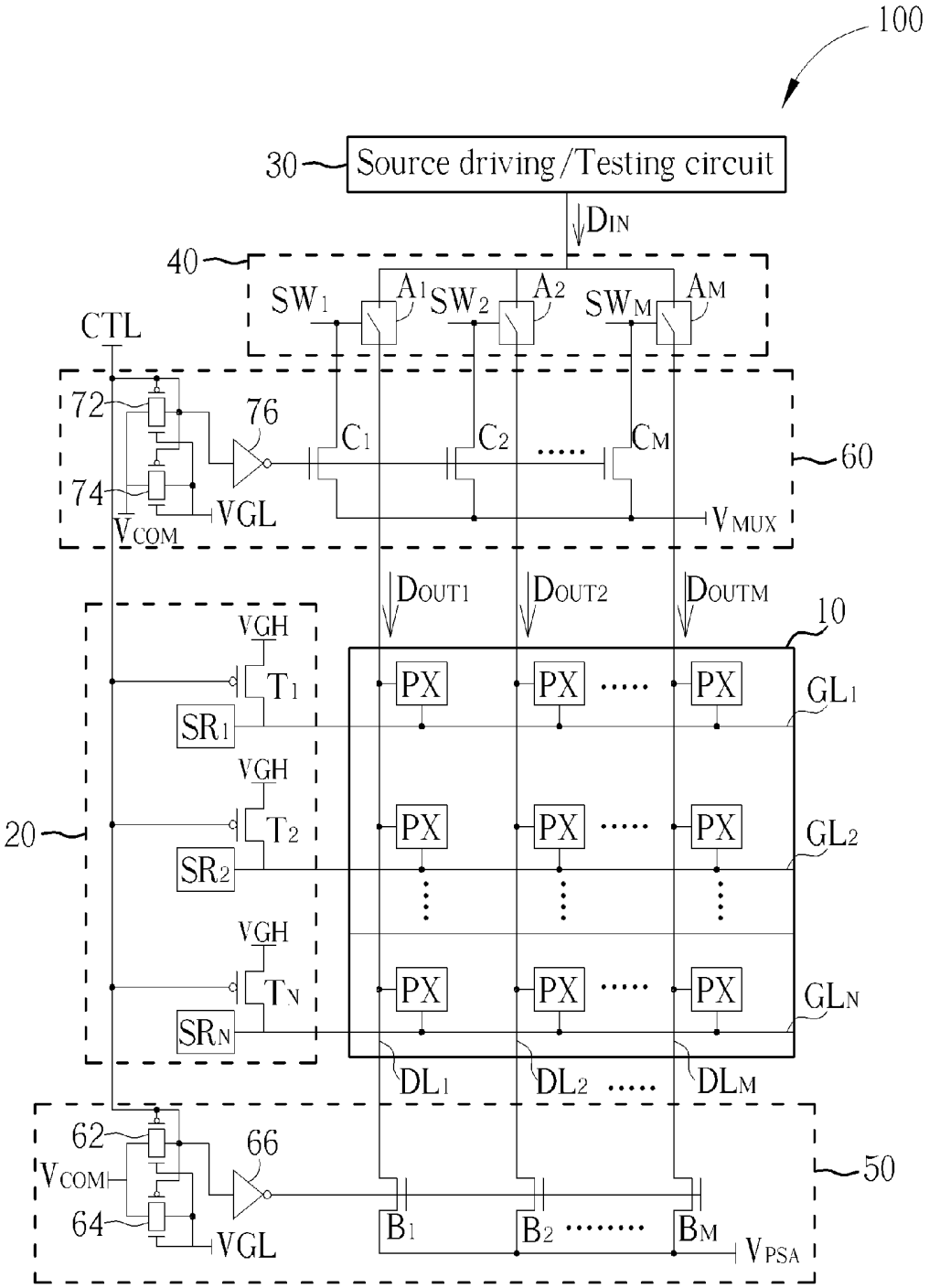

100
30
Source driving/Testing circuit
DIN
40
SW1
A1
SW2
A2
SWM
AM
CTL
72
76
74
VGL
VCOM
C1
C2
CM
60
VMUX
DOUT1
DOUT2
DOUTM
10
VGH
T1
SR1
T2
SR2
TN
SRN
20
PX
GL1
GL2
GLN
DL1
DL2
DLM
62
66
64
VGL
VCOM
50
B1
B2
BM
VPSA

FIG. 2

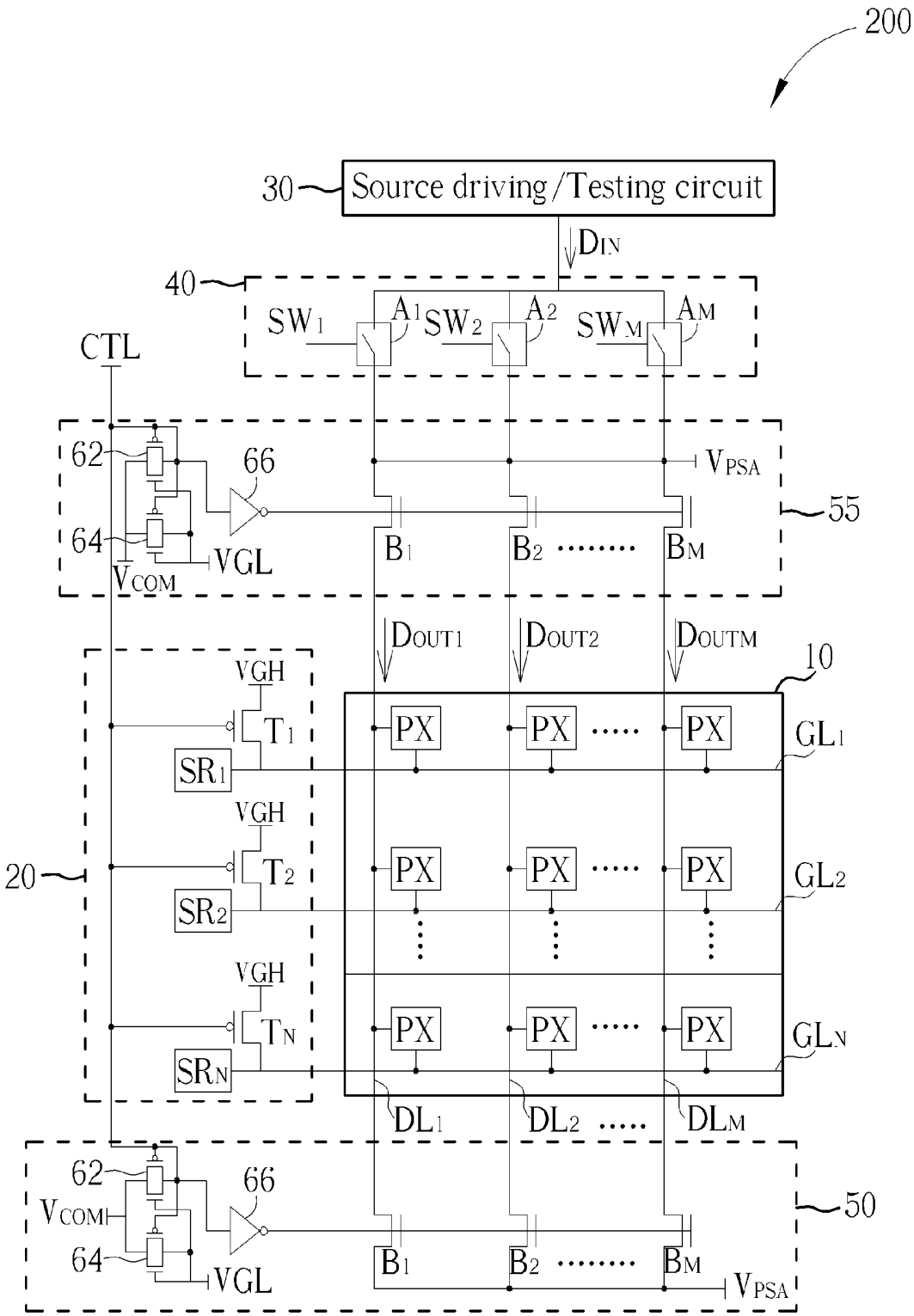
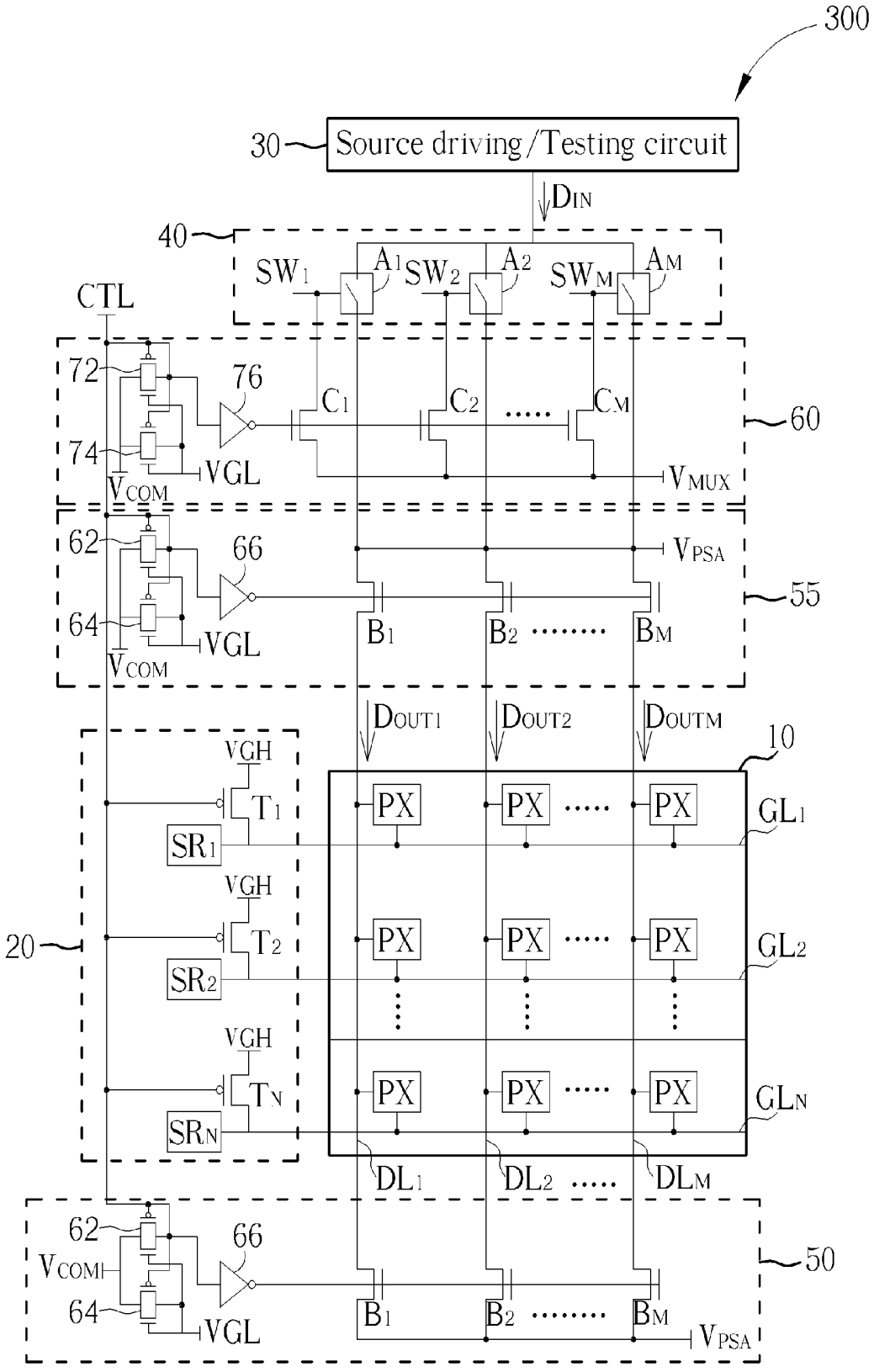

200
30
Source driving/Testing circuit
DIN
40
SW1
A1
SW2
A2
SWM
AM
CTL
62
66
VPSA
55
64
VCOM
VGL
B1
B2
BM
DOUT1
DOUT2
DOUTM
10
VGH
T1
PX
GL1
SR1
T2
GL2
SR2
20
TN
GLN
SRN
DL1
DL2
DLM
50

FIG. 3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30
Source driving/Testing circuit
DIN
40
SW1
A1
SW2
A2
SWM
AM
CTL
72
76
C1
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CM
60
74
VGL
VMUX
VCOM
62
66
VPSA
55
64
VGL
B1
B2
BM
VCOM
DOUT1
DOUT2
DOUTM
10
VGH
T1
PX
GL1
SR1
VGH
20
T2
GL2
SR2
VGH
TN
GLN
SRN
DL1
DL2
DLM
62
66
50
VCOM
64
VGL
B1
B2
BM
VPSA

FIG. 4

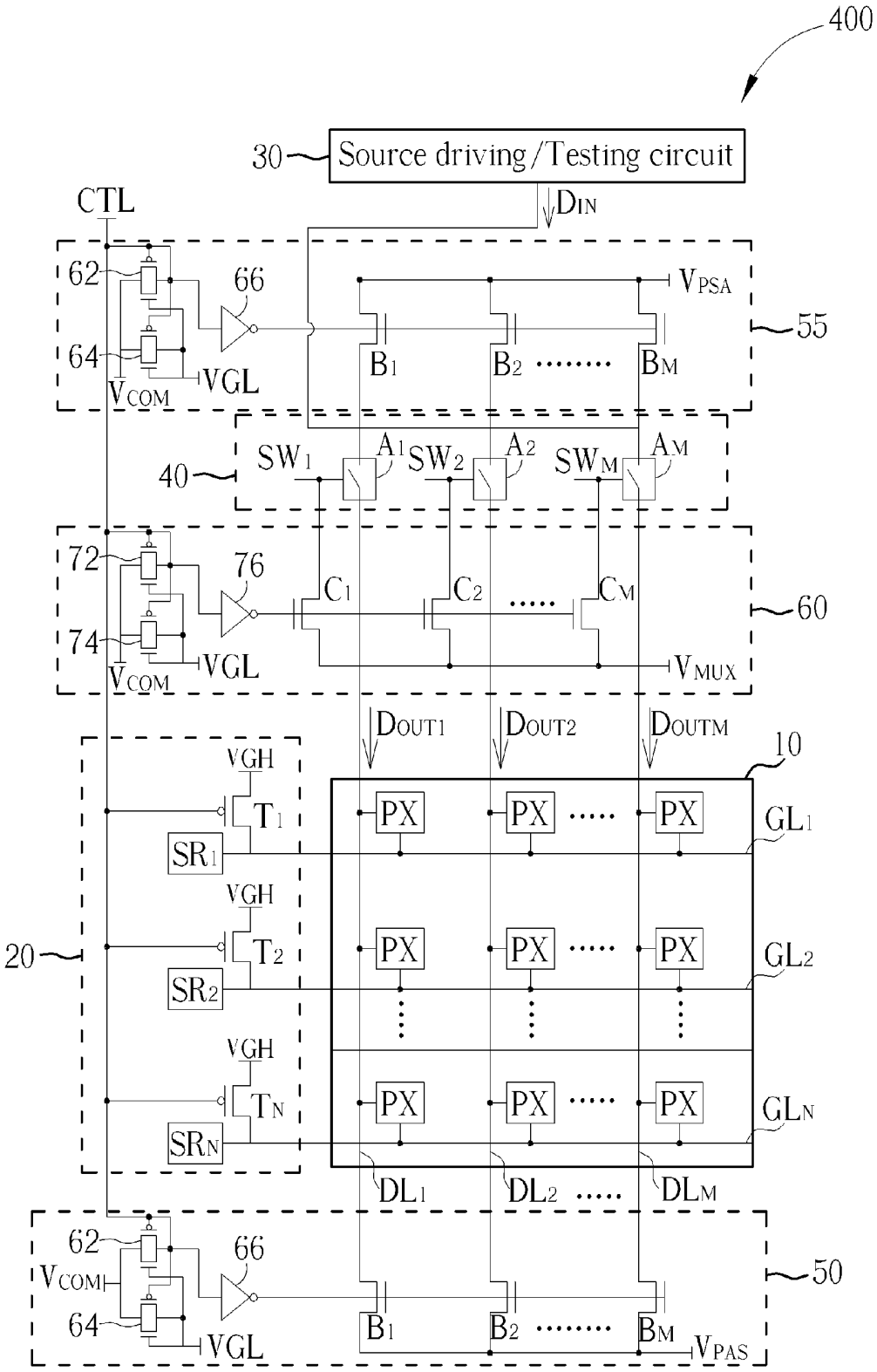
400
30
Source driving/Testing circuit
CTL
DIN
62
66
64
VCOM
VGL
VPSA
55
B1
B2
BM
40
SW1
A1
SW2
A2
SWM
AM
72
76
74
C1
C2
CM
60
VMUX
DOUT1
DOUT2
DOUTM
10
VGH
T1
SR1
T2
SR2
TN
SRN
20
PX
GL1
GL2
GLN
DL1
DL2
DLM
50
VPAS

FIG. 5

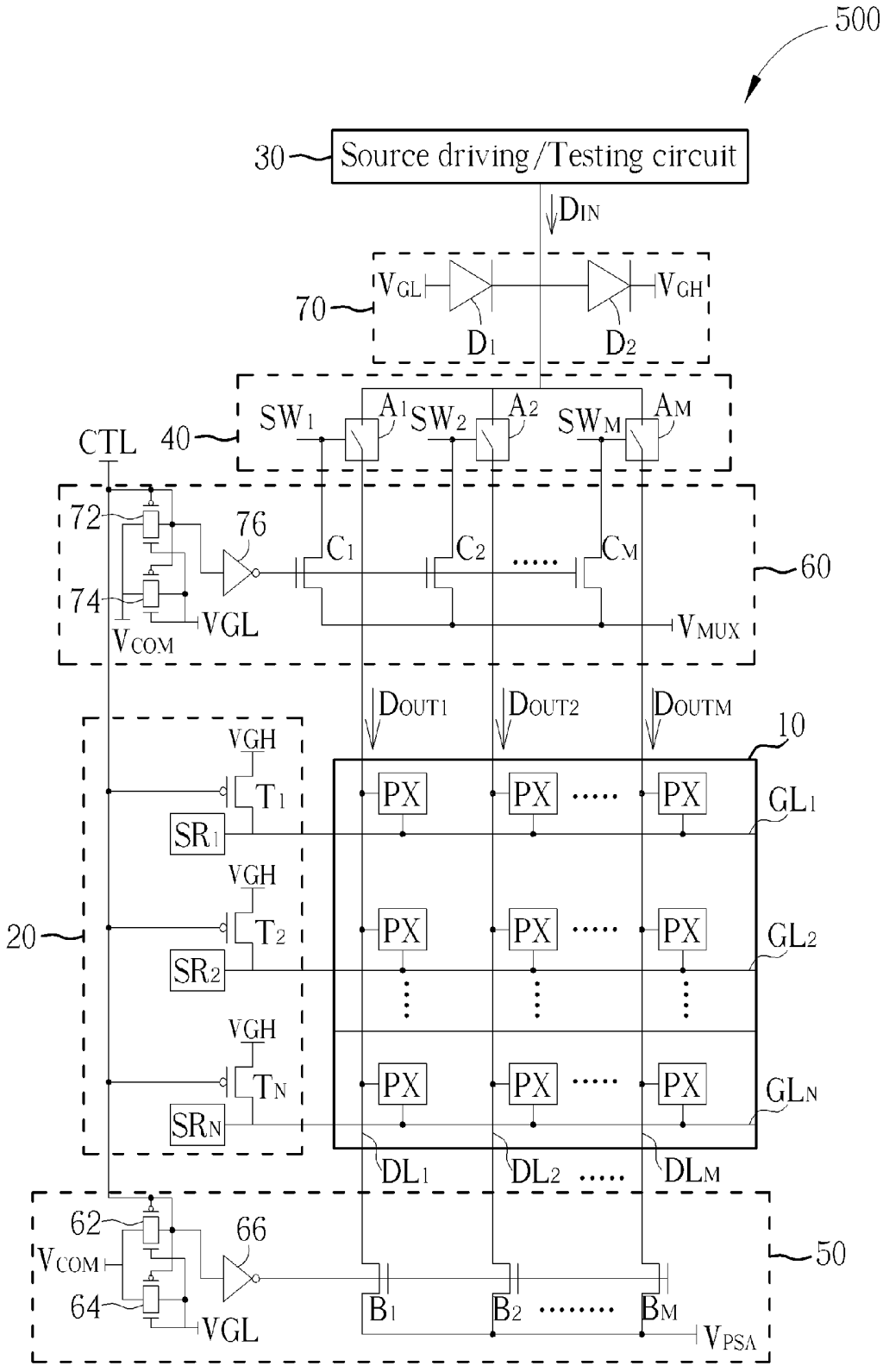
500
30
Source driving/Testing circuit
DIN
70
VGL
VGH
D1
D2
CTL
40
SW1
A1
SW2
A2
SWM
AM
72
76
74
VCOM
VGL
C1
C2
CM
60
VMUX
DOUT1
DOUT2
DOUTM
10
VGH
T1
SR1
PX
GL1
T2
SR2
GL2
20
TN
SRN
GLN
DL1
DL2
DLM
62
66
64
50
B1
B2
BM
VPSA

FIG. 6

LIQUID CRYSTAL DISPLAY DEVICE AND RELATED ALIGNMENT METHOD

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention is related to a liquid crystal display device and related alignment method, and more particularly, to a liquid crystal display device and related alignment method with ESD protection and reduced mura.

[0003] 2. Description of the Prior Art

[0004] With rapid development of large-size liquid crystal display (LCD) panels, the ability to provide multi-viewing angles have become a major feature. Because of the advantages of multi-viewing angles and low response time, multi-domain vertical alignment (MVA) LCD panels have become the mainstream products of the large-size display panels.

[0005] Conventional MVA LCD panels provide multi-viewing angle function by making the liquid crystal molecules in different areas slant in different directions using protrusions (bumps). However, in addition to complicating manufacturing processes, protrusions may also block part of light, thereby lowering the aperture ratio and the brightness performance.

[0006] Therefore, polymer stabilized alignment or phase separation alignment (PSA) technology has been developed in which polymers are used to replace the protrusions in MVA LCD panels. The core of PSA technology is to forma polymer-alignment layer over a conventionally coated polyimide by mixing a UV-curable monomer into the liquid crystal molecules. The monomer is then activated by UV radiation while applying a curing voltage. The monomer reacts with the polymer layer to form a surface that fixes the pre-tilt angle of the liquid crystal molecules.

[0007] FIG. **1** is a diagram illustrating a prior art LCD device **600**. The LCD device **600** includes an LCD panel, a gate driving circuit, a source driving/testing circuit, a multiplexer, and an alignment circuit. The LCD panel is manufactured using PSA technology in which a plurality of data lines, a plurality of gate lines, and a plurality of pixels (not shown) are disposed. The gate driving circuit may provide gate driving signals for turning on each column of pixels. The source driving/testing circuit may provide data signal D_{IN} for charging corresponding rows of pixel. According to the data signal D_{IN} and switch control signals SW_1~SW_M, the multiplexer may output data signal D_{OUT1}~D_{OUTM} to the LCD panel.

[0008] During the alignment period, the multiplexer in the prior art LCD device is floating. Unstable curing voltage or electrostatic discharge (ESD) may influence the alignment process and cause image mura which downgrades display quality.

SUMMARY OF THE INVENTION

[0009] An embodiment of the present invention provides an LCD device having a display panel, a multiplexer, an alignment circuit and a short bar circuit. The display panel includes a plurality of pixels; a plurality of data lines disposed along a first direction and respectively coupled to the plurality of pixels; and a plurality of gate lines disposed along a second direction and respectively coupled to the plurality of pixels. The multiplexer is disposed on a first side of the display panel and configured to provide a plurality of output data signals according to a plurality of switch control signals and an input data signal. The multiplexer includes an input end for receiving the input data signal; a plurality of output ends coupled to the plurality of data lines for respectively outputting the plurality of output data signals; and a plurality of switches configured to control transmission paths between the input end and the plurality of output ends according to the plurality of switch control signals. The alignment circuit is configured to provide a curing voltage to the plurality of data lines during an alignment period. The short bar circuit is configured to couple the multiplexer to a predetermined voltage during the alignment period.

[0010] An embodiment of the present invention further provides an alignment method for use in an LCD device. The alignment method includes providing the LCD device which includes a display panel having a plurality of pixels and a plurality of data lines; a multiplexer having an input end, a plurality of output ends coupled to the pixels, and a plurality of switches configured to control transmission paths between the input end and the plurality of output ends according to a plurality of switch control signals, respectively; providing a curing voltage to the plurality of data lines and a UV light to the display panel during an alignment period; and coupling the multiplexer to a predetermined voltage for maintaining the plurality of switch control signals at a same level during the alignment period.

[0011] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is a diagram illustrating a prior art LCD device.

[0013] FIGS. **2-6** are diagrams illustrating the structure and the operation of LCD devices according to embodiments of the present invention.

DETAILED DESCRIPTION

[0014] FIGS. **2-6** are diagrams illustrating the structure and the operation of LCD devices according to embodiments of the present invention. The LCD device **100** depicted in FIG. **2** includes an LCD panel **10**, a gate driving circuit **20**, a source driving/testing circuit **30**, a multiplexer **40**, a first alignment circuit **50**, and a short bar circuit **60**. The LCD device **200** depicted in FIG. **3** includes an LCD panel **10**, a gate driving circuit **20**, a source driving/testing circuit **30**, a multiplexer **40**, a first alignment circuit **50**, and a second alignment circuit **55**. The LCD device **300** depicted in FIG. **4** and the LCD device **400** depicted in FIG. **5** each include an LCD panel **10**, a gate driving circuit **20**, a source driving/testing circuit **30**, a multiplexer **40**, a first alignment circuit **50**, a second alignment circuit **55**, and a short bar circuit **60**. The LCD device **500** depicted in FIG. **6** includes an LCD panel **10**, a gate driving circuit **20**, a source driving/testing circuit **30**, a multiplexer **40**, a first alignment circuit **50**, a short bar circuit **60**, and an ESD protection circuit **70**.

[0015] In the embodiments of the present invention, the LCD panel **10** may be manufactured using PSA technology in which a plurality of data lines DL_1~DL_M (M is an integer larger than 1), a plurality of gate lines GL_1~GL_N (N is an integer larger than 1), and a plurality of pixels PX are disposed on the active area. The gate driving circuit **20** is configured to provide gate driving signals for turning on each row

of pixels. The source driving/testing circuit **30** and the multiplexer **40** are configured to provide data signals for charging each column of pixels.

[0016] Referring to FIG. **2** for a first embodiment of the present invention, the LCD device **100** performs alignment process using single-sided driving scheme and with ESD protection. During the alignment period, the first alignment circuit **50** is configured to provide a curing voltage V_{PSA} to the data lines DL_1~DL_M, and the short bar circuit **60** is configured to couple the multiplexer **40** to a predetermined voltage V_{MUX} for turning off the multiplexer **40**. The turned-off multiplexer **40** may prevent the ESD generated by the source driving/testing circuit **30** from reaching the data lines DL_1~DL_M, thereby improving image mura.

[0017] Referring to FIG. **3** for a second embodiment of the present invention, the LCD device **200** performs alignment process using dual-sided driving scheme and with ESD protection. The first alignment circuit **50** and the second alignment circuit **55** are respectively disposed on opposite sides of the LCD panel **10**. During the alignment period, the first alignment circuit **50** is configured to provide a curing voltage V_{PSA} to the first side of the data lines DL_1~DL_M, the second alignment circuit **55** is configured to provide a curing voltage V_{PSA} to the second side of the data lines DL_1~DL_M, and the multiplexer **40** is floating. The second alignment circuit **55** may share the ESD generated by the source driving/testing circuit **30**, thereby improving image mura.

[0018] Referring to FIG. **4** for a third embodiment of the present invention, the LCD device **300** performs alignment process using dual-sided driving scheme and with ESD protection. The first alignment circuit **50** and the second alignment circuit **55** are respectively disposed on opposite sides of the LCD panel **10**, wherein the first alignment circuit **50** is disposed between the LCD panel **10** and the multiplexer **40**. During the alignment period, the first alignment circuit **50** is configured to provide a curing voltage V_{PSA} to the first side of the data lines DL_1~DL_M, the second alignment circuit **55** is configured to provide a curing voltage V_{PSA} to the second side of the data lines DL_1~DL_M, and the short bar circuit **60** is configured to couple the multiplexer **40** to a predetermined voltage V_{MUX} for turning off the multiplexer **40**. The turned-off multiplexer **40** may prevent the ESD generated by the source driving/testing circuit **30** from reaching the data lines DL_1~DL_M, thereby improving image mura.

[0019] Referring to FIG. **5** for a fourth embodiment of the present invention, the LCD device **400** performs alignment process using dual-sided driving scheme and with ESD protection. The first alignment circuit **50** and the second alignment circuit **55** are respectively disposed on opposite sides of the LCD panel **10**, wherein the multiplexer **40** is disposed between the LCD panel **10** and the second alignment circuit **55**. During the alignment period, the short bar circuit **60** is configured to couple the multiplexer **40** to a predetermined voltage V_{MUX} for turning on the multiplexer **40**, the first alignment circuit **50** is configured to provide a curing voltage V_{PSA} to the first side of the data lines DL_1~DL_M, and the second alignment circuit **55** is configured to provide a curing voltage V_{PSA} to the second side of the data lines DL_1~DL_M via the turned-on multiplexer **40**. The second alignment circuit **55** may share the ESD present at the input end of the multiplexer **40**, thereby improving image mura.

[0020] Referring to FIG. **6** for a fifth embodiment of the present invention, the LCD device **500** performs alignment process using single-sided driving scheme and with ESD protection. During the alignment period, the first alignment circuit **50** is configured to provide a curing voltage V_{PSA} to the data lines DL_1~DL_M, and the short bar circuit **60** is configured to couple the multiplexer **40** to a predetermined voltage V_{MUX} for turning off the multiplexer **40**. The ESD protection circuit **70** is disposed between the source driving/testing circuit **30** and the input end of the multiplexer **40**. The ESD protection circuit **70** may share the ESD generated by the source driving/testing circuit **30**, and the turned-off multiplexer **40** may prevent the ESD generated by the source driving/testing circuit **30** from reaching the data lines DL_1~DL_M, thereby improving image mura.

[0021] In the embodiment illustrated in FIG. **6**, the ESD protection circuit **70** may include a first diode and a second diode. The anode of the first diode is coupled to a low level voltage V_{GL}, and the cathode of the first diode is coupled to the input end of the multiplexer **40**. The anode of the second diode is coupled to the input end of the multiplexer **40**, and the cathode of the second diode is coupled to a high level voltage V_{GH}. However, the embodiment of the ESD protection circuit **70** depicted in FIG. **6** is merely for illustrative purpose and does not limit the scope of the present invention.

[0022] In the embodiments of the present invention, the gate driving circuit **20** may include pull-up switches T_1~T_N and shift registers SR_1~SR_N. Each pull-up switch includes a first end for receiving a bias voltage VGH, a second end coupled to a corresponding gate line, and a control end for receiving a control signal CTL. During the alignment period, the control signal CTL is set to low level for turning on the pull-up switches T_1~T_N so that the bias voltage VGH may turn on the pixels PX for receiving the curing voltage V_{PSA}. During the display period, the control signal CTL is set to high level for turning off the pull-up switches T_1~T_N, thereby preventing the bias voltage VGH from reaching the gate lines GL_1~GL_N. At the same time, the control signal CTL is inverted to low level by a voltage buffer **66** for turning off the switches B_1~B_N, thereby preventing the pixels PX from receiving the curing voltage V_{PSA}.

[0023] In the embodiments of the present invention, the multiplexer **40** may adopt 1-to-M scheme and may include an input end, M output ends and M switches A_1~A_M. The input end of the multiplexer **40** is coupled to the source driving/testing circuit **30** for receiving an input signal D_{IN}. The switches A_1~A_m are configured to control the signal transmission paths between the input end and the output ends of the multiplexer **40** according to the control signals SW_1~SW_M, respectively. Therefore, the multiplexer **40** may output data signals D_{OUT1}~D_{OUTM} to the data lines DL_1~DL_M, respectively.

[0024] In the embodiments of the present invention, the alignment circuits **50** and **55** may each include M switches B_1~B_N, transmission logic gates **62** and **64**, and a voltage buffer **66**. The switches B_1~B_N include first ends respectively coupled to the data lines DL_1~DL_M, second ends for receiving a curing voltage V_{PSA}, and control ends coupled to the output end of the voltage buffer **66**. Each of the transmission logic gates **62** and **64** includes a first end coupled to the control ends of the pull-up switches T_1~T_N, a second control end for receiving a bias voltage VGL, and an input end for receiving a bias voltage V_{COM}. The output end of the transmission logic gate **62** is coupled to the input end of the voltage buffer **66**, and the output end of the transmission logic gate **64** is coupled to receive the bias voltage VGL. The bias voltage

VGH may be a high level voltage, the bias voltage VGL may be a low level voltage, and the bias voltage V_{COM} may be a common voltage.

[0025] In the embodiments of the present invention, the short bar circuit **60** may include M switches C_1~C_M, transmission logic gates **72** and **74**, and a voltage buffer **76**. The switches C_1~C_M include first ends respectively coupled to the control ends of the switches A_1~A_M, second ends for receiving a predetermined voltage $_{VMUX}$, and control ends coupled to the output end of the voltage buffer **76**. Each of the transmission logic gates **72** and **74** includes a first end coupled to the control ends of the pull-up switches T_1~T_N, a second control end for receiving a bias voltage VGL, and an input end for receiving a bias voltage V_{COM}. The output end of the transmission logic gate **72** is coupled to the input end of the voltage buffer **76**, and the output end of the transmission logic gate **74** is coupled to receive the bias voltage VGL. The bias voltage VGH may be a high level voltage, the bias voltage VGL may be a low level voltage, and the bias voltage V_{COM} may be a common voltage.

[0026] During the alignment period, the control signal CTL is set to turn on the switches B_1~B_M so that the data lines DL_1~DL_M may be coupled to the curing voltage V_{PSA}. Meanwhile, the control signal CTL is set to turn on the switches C_1~C_M so that the control ends of the switches A_1~A_M may be coupled to the predetermined voltage V_{MUX}.

[0027] In the LCD devices **100**, **200**, **300** and **500** according to embodiments of the present invention, the predetermined voltage V_{MUX} may be set to the turn-off voltage of the switches A_1~A_M or smaller than the turn-on voltage of the switches A_1~A_M so as to turn off the multiplexer **40** during the alignment period. The turned-off multiplexer **40** may prevent the ESD generated by the source driving/testing circuit **30** from reaching the data lines DL_1~DL_M, thereby improving image mura.

[0028] In the LCD device **400** according to embodiments of the present invention, the predetermined voltage V_{MUX} may be set to the turn-on voltage of the switches A_1~A_M or larger than the turn-on voltage of the switches A_1~A_M so as to turn on the multiplexer **40** during the alignment period. The second alignment circuit **55** may share the ESD present at the input end of the multiplexer **40**, thereby improving image mura.

[0029] During the alignment period, the multiplexer in the LCD device of the present invention is coupled to a predetermined voltage in order to prevent unstable curing voltage or ESD from influencing the curing process. The display quality can thus be improved by reducing image mura.

[0030] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A liquid crystal display device, comprising:

a display panel, comprising:

a plurality of pixels;

a plurality of data lines disposed along a first direction and respectively coupled to the plurality of pixels; and

a plurality of gate lines disposed along a second direction and respectively coupled to the plurality of pixels;

a multiplexer disposed on a first side of the display panel and configured to provide a plurality of output data signals according to a plurality of first switch control signals and an input data signal, the multiplexer comprising:

an input end for receiving the input data signal;

a plurality of output ends coupled to the plurality of data lines for respectively outputting the plurality of output data signals; and

a plurality of first switches configured to control transmission paths between the input end and the plurality of output ends according to the plurality of first switch control signals;

a first alignment circuit configured to provide a curing voltage to the plurality of data lines during an alignment period; and

a first short bar circuit configured to couple the multiplexer to a predetermined voltage during the alignment period.

2. The liquid crystal display device of claim **1**, wherein the first short bar circuit is further configured to provide the predetermined voltage for turning off the multiplexer during the alignment period.

3. The liquid crystal display device of claim **1**, further comprising:

a second short bar circuit coupled to the plurality of data lines and configured to provide the curing voltage to the plurality of data lines during the alignment period, wherein the first short bar circuit and the second short bar circuit are disposed on opposite sides of the display panel.

4. The liquid crystal display device of claim **3**, wherein:

the multiplexer is disposed between the display panel and the second short bar circuit;

the curing voltage is transmitted to the plurality of data lines via the multiplexer; and

the first short bar circuit is further configured to provide the predetermined voltage for turning on the multiplexer during the alignment period.

5. The liquid crystal display device of claim **4**, wherein the first short bar circuit is further configured to provide the predetermined voltage for turning off the multiplexer during the alignment period.

6. The liquid crystal display device of claim **1**, further comprising:

an electrostatic discharge circuit coupled to the input end of the multiplexer and comprising:

a first diode including an anode coupled to a low level voltage and a cathode coupled to the input end of the multiplexer; and

a second diode including an anode coupled to the input end of the multiplexer and a cathode coupled to a high level voltage.

7. The liquid crystal display device of claim **1**, wherein each gate line is coupled to a pull-up switch which includes:

a control end for receiving a second switch control signal;

a first end for receiving a high level voltage; and

a second end coupled to the gate line.

8. The liquid crystal display device of claim **7**, wherein the first alignment circuit comprises:

a plurality of second switches each including:

a control end;

a first end for receiving the curing voltage; and

a second end coupled to a corresponding data line;

a first transmission logic gate, comprising:
an input end for receiving a common voltage;
a first control end coupled to the control ends of the pull-up switches;
an output end coupled to the first control end of the first transmission logic gate; and
a second control end for receiving a low level voltage;
a second transmission logic gate, comprising:
an input end for receiving the common voltage;
a first control end coupled to the control ends of the pull-up switches;
an output end coupled to the second control end of the first transmission logic gate; and
a second control end coupled to the second control end of the first transmission logic gate; and
a voltage buffer, comprising:
an input end coupled to the output end of the first transmission logic gate; and
an output end coupled to the control end of the second switches.

9. The liquid crystal display device of claim **1**, wherein the first alignment circuit comprises:
a plurality of second switches each including:
a control end;
a first end for receiving the curing voltage; and
a second end coupled to a corresponding data line;
a first transmission logic gate, comprising:
an input end for receiving a common voltage;
a first control end coupled to the control ends of the pull-up switches;
an output end coupled to the first control end of the first transmission logic gate; and
a second control end for receiving a low level voltage;
a second transmission logic gate, comprising:
an input end for receiving the common voltage;
a first control end coupled to the control ends of the pull-up switches;
an output end coupled to the second control end of the first transmission logic gate; and
a second control end coupled to the second control end of the first transmission logic gate; and
a voltage buffer, comprising:
an input end coupled to the output end of the first transmission logic gate; and
an output end coupled to the control end of the second switches.

10. The liquid crystal display device of claim **1**, wherein each gate line is coupled to a pull-up switch which includes:
a control end for receiving a second switch control signal;
a first end for receiving a high level voltage; and
a second end coupled to the gate line.

11. The liquid crystal display device of claim **10**, wherein the first alignment circuit comprises a plurality of second switches each including:
a control end for receiving the second switch control signal;
a first end for receiving the predetermined voltage; and
a second end coupled to a corresponding output end of the multiplexer.

12. The liquid crystal display device of claim **1**, wherein the first alignment circuit comprises a plurality of second switches each including:
a control end for receiving the second switch control signal;
a first end for receiving the predetermined voltage; and
a second end coupled to a corresponding output end of the multiplexer.

13. An alignment method for use in an liquid crystal display device, comprising:
providing the liquid crystal display device which includes:
a display panel having a plurality of pixels and a plurality of data lines;
a multiplexer having an input end, a plurality of output ends coupled to the pixels, and a plurality of switches configured to control transmission paths between the input end and the plurality of output ends according to a plurality of switch control signals, respectively;
providing a curing voltage to the plurality of data lines and a UV light to the display panel during an alignment period; and
coupling the multiplexer to a predetermined voltage for maintaining the plurality of switch control signals at a same level during the alignment period.

14. The alignment method of claim **13**, further comprising:
coupling the multiplexer to the predetermined voltage for maintaining the plurality of switch control signals at the same level and for turning off the multiplexer using the predetermined voltage during the alignment period.

15. The alignment method of claim **13**, further comprising transmitting the curing voltage to a first side of the plurality of data lines during the alignment period.

16. The alignment method of claim **15**, further comprising transmitting the curing voltage to a second side of the plurality of data lines via the multiplexer during the alignment period.

17. The alignment method of claim **13**, further comprising coupling the multiplexer to the predetermined voltage for maintaining the plurality of switch control signals at the same level and for turning on the witches of the multiplexer using the predetermined voltage during the alignment period

18. The alignment method of claim **17**, further comprising transmitting the curing voltage to the plurality of data lines via the witches of the multiplexer during the alignment period.

* * * * *

专利名称(译)	液晶显示装置和相关的对准方法		
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申请(专利权)人(译)	友达光电.		
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摘要(译)

一种液晶显示装置，包括显示面板，多路复用器，对准电路和短路电路。多路复用器被配置为根据多个开关控制信号和输入数据信号提供多个输出数据信号。在对准时段期间，对准电路被配置为向显示面板提供固化电压，并且短条电路被配置为将多路复用器耦合到预定电压。