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(54) **LEVEL SHIFT CIRCUIT AND LEVEL SHIFT METHOD FOR GOA STRUCTURE LIQUID CRYSTAL PANEL**

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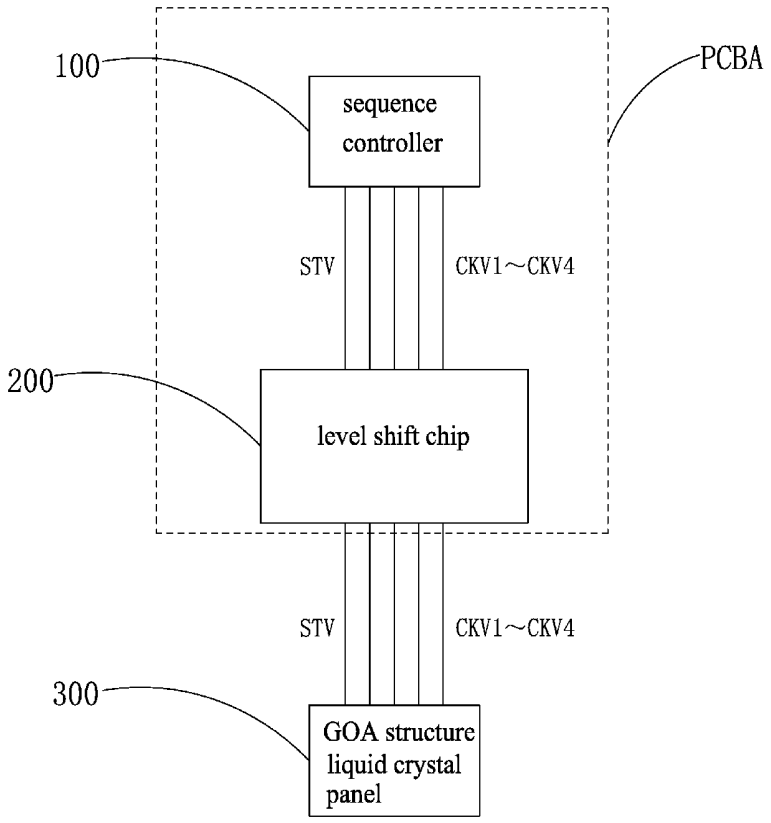
(57) **ABSTRACT**

The present invention provides a level shift circuit and a level shift method for a GOA structure liquid crystal panel. The level shift chip (**20**) comprises a time delay calculation register module (**201**) and a start signal line (**30**) and an Inter-Integrated Circuit bus (**40**) are employed to communicatively couple the sequence controller (**10**) and the level shift chip (**20**).The sequence controller (**10**) performs initialization assignment (T**1**-Tn) to the time delay calculation register module (**201**), and sends a start signal (STV) to the level shift chip (**20**) via the start signal line (**30**); the level shift chip (**20**) is triggered to output the at least four sets of sequence signals (CKV**1**-CKVn) on a basis of the start signal (STV) according to the initialization assignment (T**1**-Tn) of the time delay calculation register module, and raises voltages of the start signal (STV) and the at least four sets of sequence signals (CKV**1**-CKVn) for driving the GOA structure liquid crystal panel (**50**) and realizing the generation of more sequence signals with lower cost.



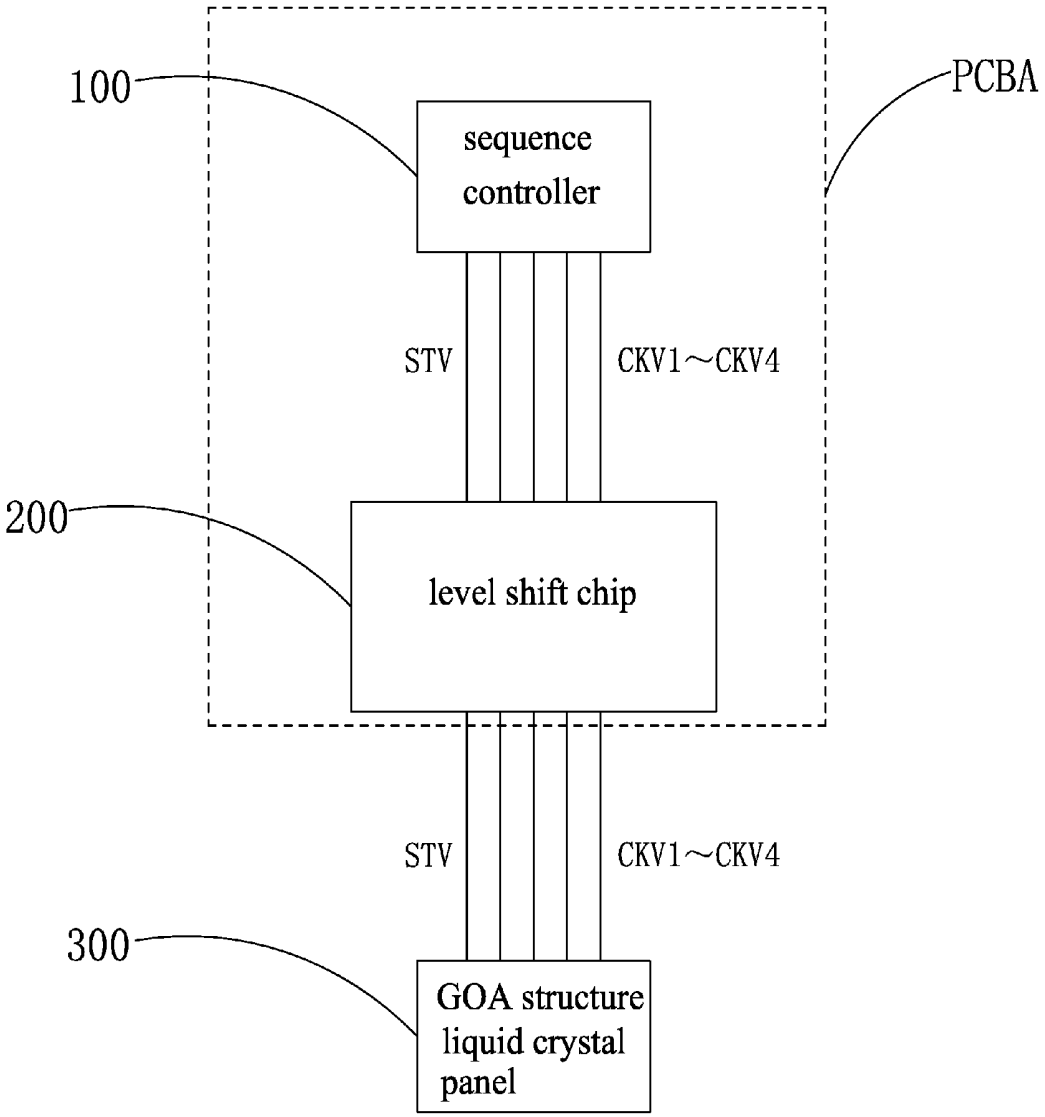

100
PCBA
sequence controller
STV
CKV1~CKV4
200
level shift chip
STV
CKV1~CKV4
300
GOA structure liquid crystal panel

Fig. 1

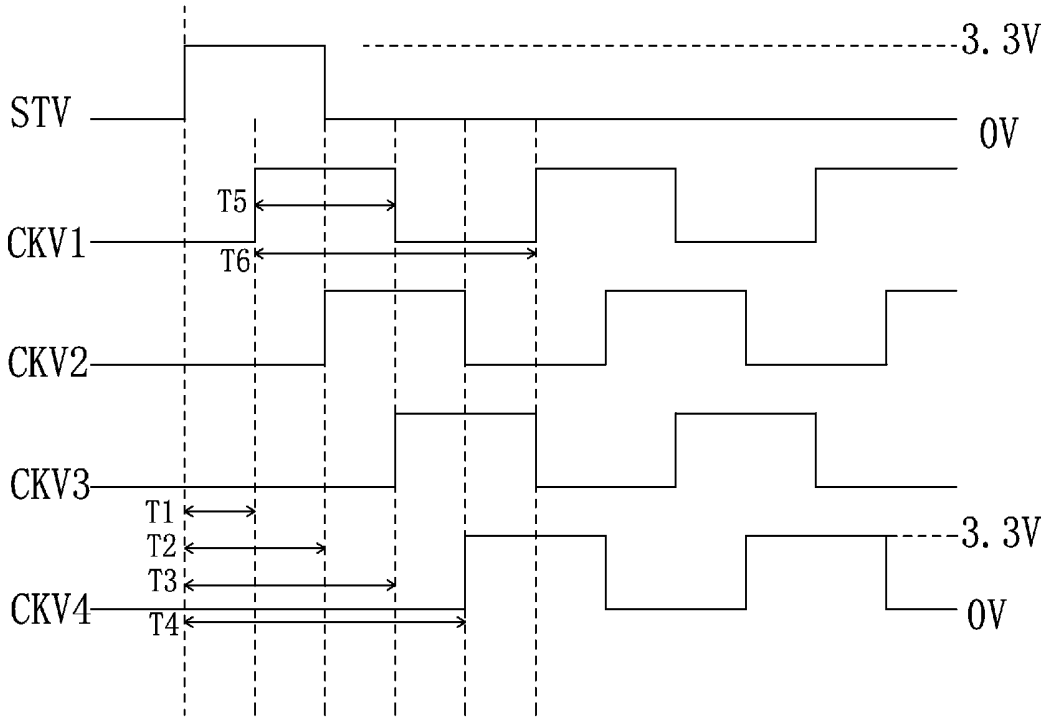


Fig. 2

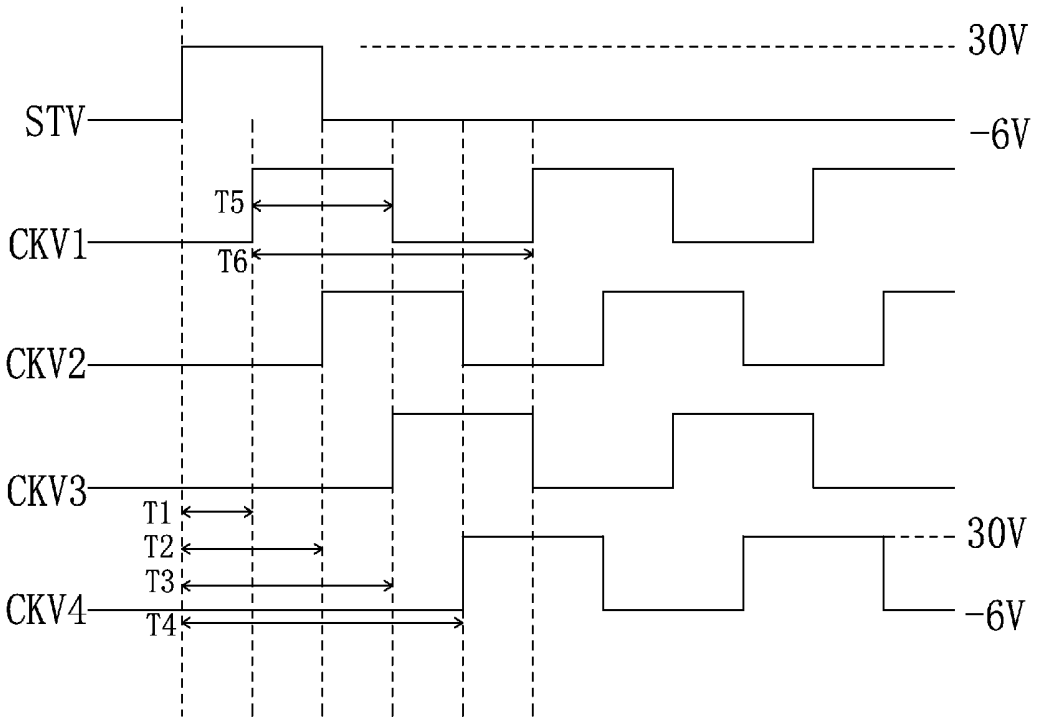


Fig. 3

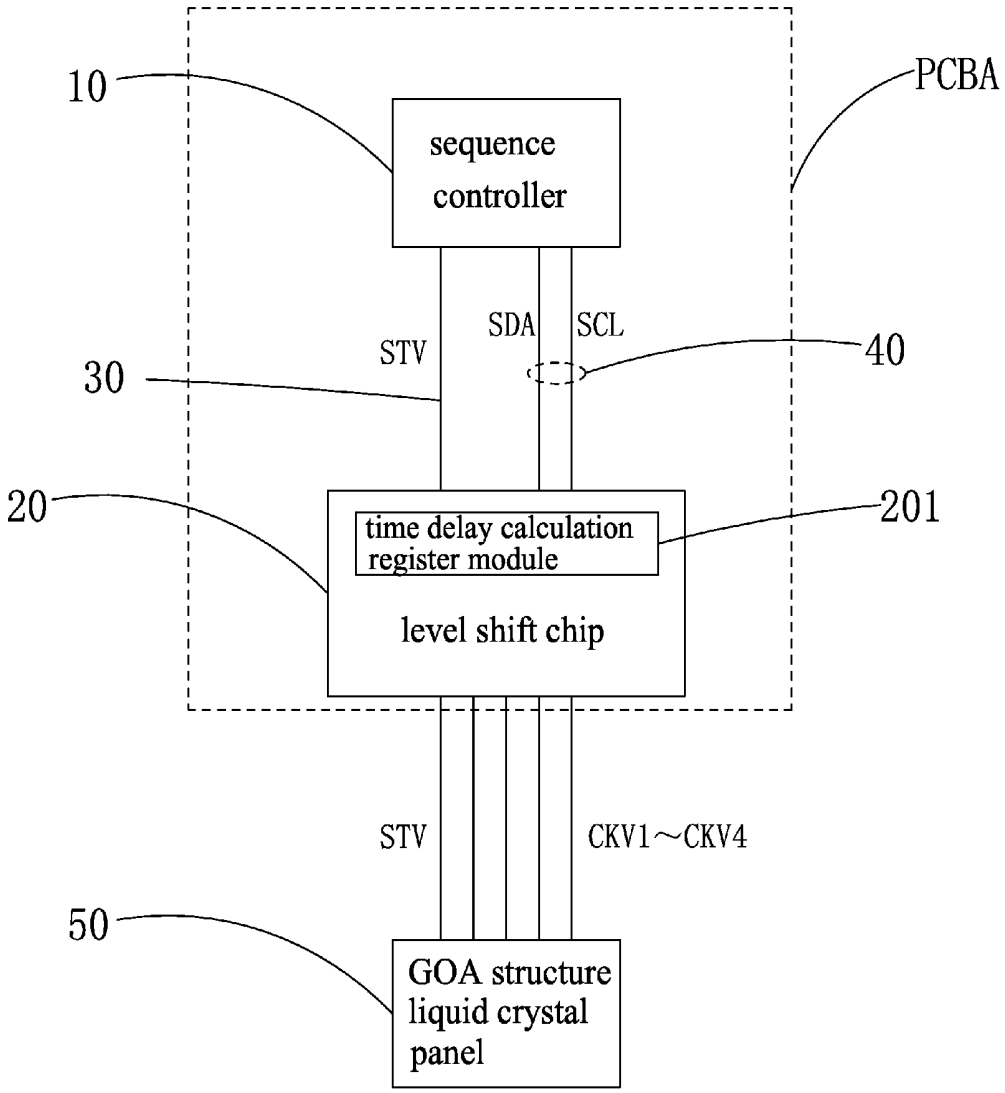

10
PCBA
sequence controller
SDA
SCL
STV
40
30
20
201
time delay calculation register module
level shift chip
STV
CKV1~CKV4
50
GOA structure liquid crystal panel

Fig. 4

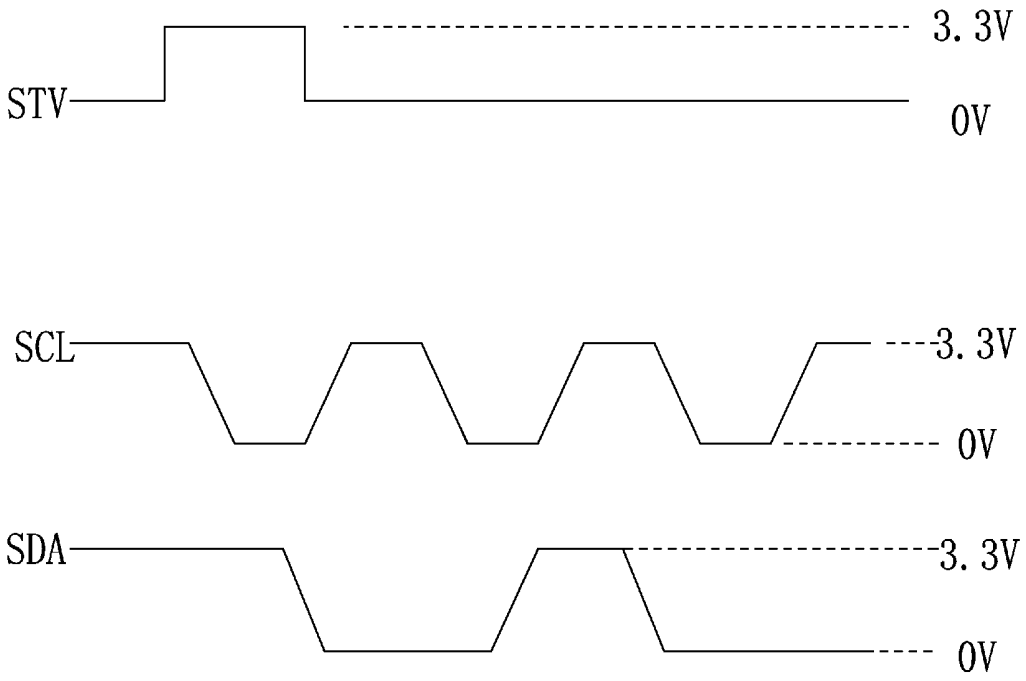


Fig. 5

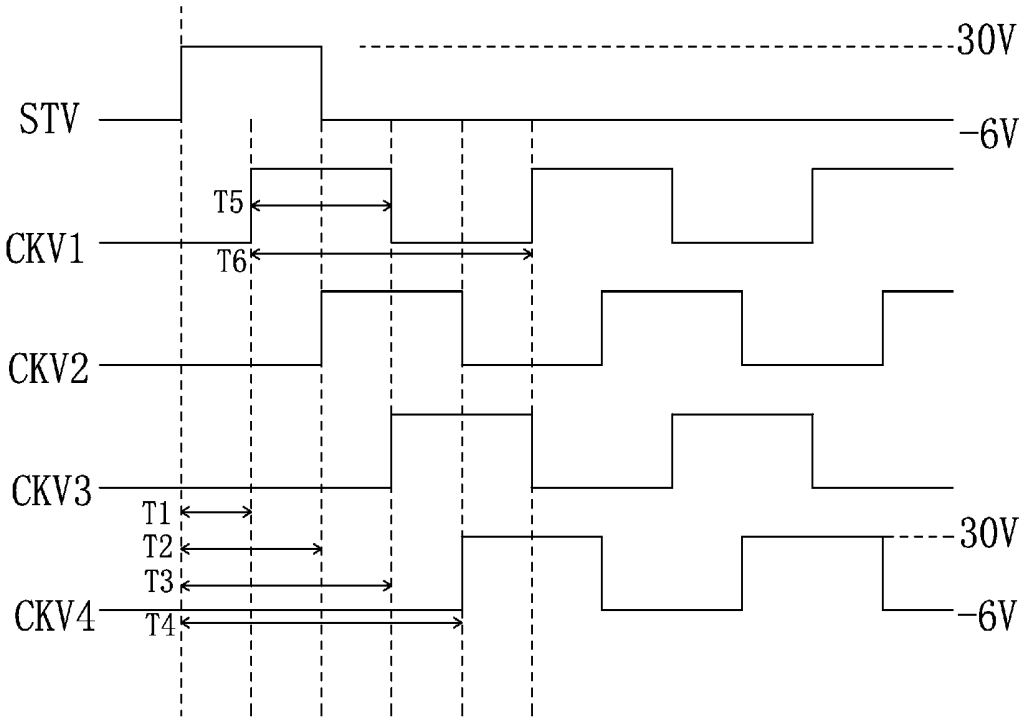


Fig. 6

LEVEL SHIFT CIRCUIT AND LEVEL SHIFT METHOD FOR GOA STRUCTURE LIQUID CRYSTAL PANEL

FIELD OF THE INVENTION

[0001] The present invention relates to a display technology field, and more particularly to a level shift circuit and a level shift method for a GOA structure liquid crystal panel.

BACKGROUND OF THE INVENTION

[0002] The Active Matrix Liquid Crystal Display (AMLCD) is the most common display device at present. The Active Matrix Liquid Crystal Display comprises a plurality of pixels, and each pixel comprises a Thin Film Transistor (TFT). The gate of the TFT is coupled to the scan line extending along the horizontal direction. The drain of the TFT is coupled to the data line extending along the vertical direction. The source of the TFT is coupled to the corresponding pixel electrode. When a sufficient positive voltage is applied to some scan line in the horizontal direction, all the TFT coupled to the scan line will be activated to write the data signal loaded in the data line into the pixel electrodes and thus to show images.

[0003] One type of Active Matrix Liquid Crystal Display utilizes GOA (Gate Drive On Array) structure, which integrates the gate driver (Gate Drive IC) on the thin film transistor array substrate to achieve the scan line by line for driving the liquid crystal panel. Compared with the drive method that the Integrated Circuit (IC) is manufactured outside the liquid crystal panel by the CMOS process, the GOA structure can diminish the manufacture processes and reduce the cost for raising the integration of the liquid crystal panel, which is beneficial for realizing the ultra narrow frame and the slimming of the panel. However, the GOA structure causes the circuit drive board (PCBA) to be with an extra level shift IC, which raises the low voltage drive signal to be the high voltage drive signal to drive the TFTs in the liquid crystal panel for functioning.

[0004] Please refer to FIG. **1**. The level shift circuit for the GOA structure liquid crystal panel according to prior art generally comprises: a sequence controller (TCON) **100** provided on the circuit drive board PCBA, and the sequence controller **100** is employed for generating and sending control signals, such as the start signal STV, the sequence signals CKVn, and n is a positive integer; a level shift chip **200** provided on the circuit drive board PCBA, and the level shift chip **200** is employed to raise the voltages of the start signal STV, the sequence signals CKVn transmitted from the sequence controller **100**. The start signal STV and the sequence signals CKVn after raising the voltages by the level shift chip **200** drives the TFTs in the GOA structure liquid crystal panel **300**.

[0005] For normally activating the TFTs in the GOA structure liquid crystal panel **300** line by line, four sets of sequence signals CKV**1**-CKV**4** or more sequence signals are required in general for realizing the display effect of scan line by line. Each control signal needs the corresponding leads of the sequence controller **100** and the level shift chip **200** for the communicative coupling. As shown in FIG. **1**, as there are four sets of sequence signals CKV**1**-CKV**4** and one start signal STV, five pairs of corresponding leads are required for the communicative coupling of the sequence controller **100** and the level shift chip **200** to raise the voltage of each control signal.

[0006] As shown in FIG. **2**, the sequence controller **100** generates the start signal STV, and sequentially generates the sequence signals CKV**1**, CKV**2**, CKV**3**, CKV**4** respectively with interval T**1**, T**2**, T**3**, T**4** on a basis of the rising edge of the start signal STV. The low voltage levels of the start signal STV and the sequence signals CKV**1**-CKV**4** are 0 V, and the high voltage levels are 3.3 V. The continue periods of high voltage levels are T**5** and the periodic times are T**6**. As shown in FIG. **3**, after the level shift chip **200** raises the voltage levels, all the low voltage levels of the start signal STV, and the sequence signals CKV**1**-CKV**4** are −6 V, and the high voltage levels are 30 V. The intervals, the continue periods, periodic times of high voltage levels of the sequence signals CKV**1**-CKV**4** relative to the rising edge of the start signal STV remain to be unchanged.

[0007] Although the aforesaid level shift circuit for the GOA structure can raise the voltage of each control signal to drive the TFTs in the liquid crystal panel, the leads required between the sequence controller **100** and the level shift chip **200** gets more and more as the required sequence signals CKVn become more and more. Every extra lead results in that the package size of the sequence controller **100** and the level shift chip **200** gets larger, and the dimension of the package size directly changes the cost of the IC. Meanwhile, more wirings make the dimension of the PCBA become larger and cost increase in advance. Therefore, as more sequence signals CKVn are required, the cost of the IC and the PCBA can be significantly increased and is disadvantageous to the purpose of lowering the cost with the GOA structure.

SUMMARY OF THE INVENTION

[0008] An objective of the present invention is to provide a level shift circuit for a GOA structure liquid crystal panel, capable of decreasing the lead count between the sequence controller and the level shift chip to reduce the package size of the sequence controller and the level shift chip and to decrease the total wiring amount between the sequence controller and the level shift chip for reducing the dimension of the circuit drive board and lowering the production cost.

[0009] Another objective of the present invention is to provide a level shift method for a GOA structure liquid crystal panel, capable of generating more sequence signals, and meanwhile, decreasing the lead count between the sequence controller and the level shift chip to reduce the package size of the sequence controller and the level shift chip and to decrease the total wiring amount between the sequence controller and the level shift chip for reducing the dimension of the circuit drive board and lowering the production cost.

[0010] For realizing the aforesaid objective, the present invention first provides a level shift circuit for a GOA structure liquid crystal panel, comprising a sequence controller and a level shift chip;

[0011] the level shift chip comprises a time delay calculation register module;

[0012] the sequence controller is communicatively coupled to the level shift chip via a start signal line and an Inter-Integrated Circuit bus;

[0013] the sequence controller performs initialization assignment to the time delay calculation register module

inside the level shift chip via the Inter-Integrated Circuit bus, and sends a start signal to the level shift chip via the start signal line;

[0014] the level shift chip is triggered to output at least four sets of sequence signals on a basis of the start signal according to the initialization assignment of the time delay calculation register module and raises voltages of the start signal and the at least four sets of sequence signals; the start signal and each set of sequence signal after raising the voltages are respectively transmitted to the GOA structure liquid crystal panel via one signal line.

[0015] The Inter-Integrated Circuit bus comprises a serial data signal line employed for transmitting serial data signals and a serial sequence signal line employed for transmitting serial sequence signals.

[0016] The level shift chip is triggered to output the at least four sets of sequence signals on a basis of a rising edge of the start signal according to the initialization assignment of the time delay calculation register module.

[0017] A generation point of the each set of sequence signal and the rising edge of the start signal are spaced with a corresponding initialization assignment.

[0018] Continue periods and periodic times of high voltage levels of the at least four sets of sequence signals are determined according to the initialization assignment of the time delay calculation register module.

[0019] The present invention relates to a display technology field, and more particularly to a level shift circuit and a level shift method for a GOA structure liquid crystal panel.

[0020] the level shift chip comprises a time delay calculation register module;

[0021] the sequence controller is communicatively coupled to the level shift chip via a start signal line and an Inter-Integrated Circuit bus;

[0022] the sequence controller performs initialization assignment to the time delay calculation register module inside the level shift chip via the Inter-Integrated Circuit bus, and sends a start signal to the level shift chip via the start signal line;

[0023] the level shift chip is triggered to output at least four sets of sequence signals on a basis of the start signal according to the initialization assignment of the time delay calculation register module and raises voltages of the start signal and the at least four sets of sequence signals; the start signal and each set of sequence signal after raising the voltages are respectively transmitted to the GOA structure liquid crystal panel via one signal line;

[0024] wherein the Inter-Integrated Circuit bus comprises a serial data signal line employed for transmitting serial data signals and a serial sequence signal line employed for transmitting serial sequence signals;

[0025] wherein the level shift chip is triggered to output the at least four sets of sequence signals on a basis of a rising edge of the start signal according to the initialization assignment of the time delay calculation register module.

[0026] The present invention further provides a level shift method for a GOA structure liquid crystal panel, comprising steps of:

[0027] step 1, providing the GOA structure liquid crystal panel and a level shift circuit for the GOA structure liquid crystal panel;

[0028] the level shift circuit for the GOA structure liquid crystal panel comprises a sequence controller and a level shift chip; the level shift chip comprises a time delay calculation register module; the sequence controller is communicatively coupled to the level shift chip via a start signal line and an Inter-Integrated Circuit bus;

[0029] step 2, performing initialization assignment to the time delay calculation register module inside the level shift chip via the Inter-Integrated Circuit bus by the sequence controller;

[0030] step 3, generating a start signal and sending the same to the level shift chip via the start signal line by the sequence controller;

[0031] step 4, triggering the level shift chip to output at least four sets of sequence signals on a basis of the start signal according to the initialization assignment of the time delay calculation register module and raising voltages of the start signal and the at least four sets of sequence signals; respectively transmitting the start signal and each set of sequence signal after raising the voltages to the GOA structure liquid crystal panel via one signal line.

[0032] The Inter-Integrated Circuit bus comprises a serial data signal line employed for transmitting serial data signals and a serial sequence signal line employed for transmitting serial sequence signals.

[0033] In the step 2, the initialization assignment of the time delay calculation register module is determined according to the serial data signals and the serial sequence signals.

[0034] In the step 4, the level shift chip is triggered to output the at least four sets of sequence signals on a basis of a rising edge of the start signal according to the initialization assignment of the time delay calculation register module; a generation point of the each set of sequence signal and the rising edge of the start signal are spaced with a corresponding initialization assignment.

[0035] In the step 4, continue periods and periodic times of high voltage levels of the at least four sets of sequence signals are determined according to the initialization assignment of the time delay calculation register module.

[0036] The benefits of the present invention are: the present invention provides a level shift circuit and a level shift method for a GOA structure liquid crystal panel. The time delay calculation register module is provided inside the level shift chip. The start signal line and the Inter-Integrated Circuit bus are employed to communicatively couple the sequence controller and the level shift chip. the sequence controller performs initialization assignment to the time delay calculation register module inside the level shift chip via the Inter-Integrated Circuit bus, and sends a start signal to the level shift chip via the start signal line; the level shift chip is triggered to output at least four sets of sequence signals on a basis of the start signal according to the initialization assignment of the time delay calculation register module and raises voltages of the start signal and the at least four sets of sequence signals to drive the GOA structure liquid crystal panel. It is capable of decreasing the lead count between the sequence controller and the level shift chip to reduce the package size of the sequence controller and the level shift chip and to decrease the total wiring amount between the sequence controller and the level shift chip for reducing the dimension of the circuit drive board, lowering the production cost and realizing the generation of more sequence signals with lower cost.

[0037] In order to better understand the characteristics and technical aspect of the invention, please refer to the following detailed description of the present invention is concerned with the diagrams, however, provide reference to the accom-

panying drawings and description only and is not intended to be limiting of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] The technical solution and the beneficial effects of the present invention are best understood from the following detailed description with reference to the accompanying figures and embodiments.

[0039] In drawings,

[0040] FIG. **1** is a diagram of a level shift circuit for a GOA structure liquid crystal panel according to prior art;

[0041] FIG. **2** is a sequence diagram of the circuit shown in FIG. **1** before raising the voltages;

[0042] FIG. **3** is a sequence diagram of the circuit shown in FIG. **1** after raising the voltages;

[0043] FIG. **4** is a diagram of a level shift circuit for a GOA structure liquid crystal panel according to the present invention;

[0044] FIG. **5** is a sequence diagram of the circuit shown in FIG. **4** before raising the voltages;

[0045] FIG. **6** is a sequence diagram of the circuit shown in FIG. **4** after raising the voltages.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0046] For better explaining the technical solution and the effect of the present invention, the present invention will be further described in detail with the accompanying drawings and the specific embodiments.

[0047] Please refer to FIG. **4**, FIG. **5** and FIG. **6**, together. The present invention provides a level shift circuit for a GOA structure liquid crystal panel. The level shift circuit for the GOA structure liquid crystal panel comprises: a sequence controller **10** and a level shift chip **20**. The sequence controller **10** and the level shift chip **20** are positioned on a circuit drive board PCBA.

[0048] The level shift chip **20** comprises a time delay calculation register module **201**.

[0049] The sequence controller **10** is communicatively coupled to the level shift chip **20** via a start signal line **30** and an Inter-Integrated Circuit bus **40**.

[0050] The Inter-Integrated Circuit bus **40**. comprises a serial data signal line employed for transmitting serial data signals SDA and a serial sequence signal line employed for transmitting serial sequence signals SCL.

[0051] The sequence controller is employed to perform initialization assignment T**1**-Tn to the time delay calculation register module **201** inside the level shift chip **20** via the Inter-Integrated Circuit bus **40**, where n is a positive integer, and sends a start signal STV to the level shift chip **20** via the start signal line **30**.

[0052] The level shift chip **20** is employed to be triggered to output at least four sets of sequence signals CKV**1**-CKVn on a basis of the start signal STV according to the initialization assignment T**1**-Tn of the time delay calculation register module **201** and raises voltages of the start signal STV and the at least four sets of sequence signals CKV**1**-CKVn; the start signal STV and each set of sequence signal after raising the voltages are respectively transmitted to the GOA structure liquid crystal panel **50** via one signal line.

[0053] Compared with a level shift circuit for a GOA structure liquid crystal panel according to prior art, the level shift circuit for the GOA structure liquid crystal panel according to the present invention can decrease the lead count between the sequence controller **10** and the level shift chip **20** to reduce the package size of the sequence controller **10** and the level shift chip **20** and to decrease the total wiring amount between the sequence controller **10** and the level shift chip **20** for reducing the dimension of the circuit drive board PCBA and lowering the production cost.

[0054] Furthermore, the level shift chip **20** is triggered to output the at least four sets of sequence signals CKV**1**-CKVn on a basis of a rising edge of the start signal STV according to the initialization assignment T**1**-Tn of the time delay calculation register module **201**.

[0055] A generation point of the each set of sequence signal CKVn and the rising edge of the start signal STV are spaced with a corresponding initialization assignment Tn.

[0056] Continue periods Tn+1 and periodic times Tn+2 of high voltage levels of the at least four sets of sequence signals CKV**1**-CKVn are also determined according to the initialization assignment of the time delay calculation register module **201**.

[0057] Specifically, that the level shift chip **20** outputs four sets of sequence signals CKV**1**-CKV**4** is illustrated with combination of FIG. **4**, FIG. **5**. The sequence controller **10** sends the serial data signals SDA and the serial sequence signals SCL to the time delay calculation register module **201** inside the level shift chip **20** respectively via the serial data signal line and the serial sequence signal line of the Inter-Integrated Circuit bus **40** for determining the initialization assignment T**1**-T**4** to the time delay calculation register module **201**, and sends the start signal STV to the level shift chip **20** via the start signal line **30**. All the low voltage levels of the start signal STV, the serial data signals SDA and the serial sequence signals SCL are 0 V, and the high voltage levels are 3.3 V.

[0058] In conjunction with FIG. **4**, FIG. **6**, the level shift chip **20** correctly identifies the rising edge of the start signal STV, and outputs four sets of sequence signals CKV**1**-CKV**4** on a basis of the rising edge of the start signal STV, and raises voltages of the start signal STV and the four sets of sequence signals CKV**1**-CKV**4**.A generation point of the first set of sequence signal CKV**1** and the rising edge of the start signal STV are spaced with a corresponding period of the initialization assignment T**1**. A generation point of the second set of sequence signal CKV**2** and the rising edge of the start signal STV are spaced with a corresponding period of the initialization assignment T**2**. A generation point of the third set of sequence signal CKV**3** and the rising edge of the start signal STV are spaced with a corresponding period of the initialization assignment T**3**. A generation point of the fourth set of sequence signal CKV**4** and the rising edge of the start signal STV are spaced with a corresponding period of the initialization assignment T**4**. Besides, the continue periods T**5** and the periodic times T**6** of high voltage levels of the four sets of sequence signals CKV**1**-CKV**4** are also determined according to the initialization assignment of the time delay calculation register module **201**. For the liquid crystal panels of different resolutions, the continue periods T**5** and the periodic times T**6** of high voltage levels can be set according to different initialization assignments. After the level shift chip **20** raises the voltage levels, all the low voltage levels of the start signal STV, and the first, the second, the third, the fourth sets of sequence signals CKV**1**, CKV**2**, CKV**3**, CKV**4** are −6 V, and the high voltage levels are 30 V, which can employed for driving the TFTs in the

GOA structure liquid crystal panel **50** and realizing the scan line by line. In this embodiment, only four sets of sequence signals are illustrated for explanation. However, the present invention is not limited thereby and applicable for the condition of more sets of sequence signals. As more sequence signals are required for the GOA structure liquid crystal panel **50**, the present invention can decrease the lead count between the sequence controller **10** and the level shift chip **20** to reduce the package size of the sequence controller **10** and the level shift chip **20** and to decrease the total wiring amount between the sequence controller **10** and the level shift chip **20** for reducing the dimension of the circuit drive board PCBA. The result of lowering the production cost can be more effective.

[0059] Please refer to FIG. **4**, FIG. **5** and FIG. **6**, together. The present invention further provides a level shift method for a GOA structure liquid crystal panel, comprising steps of:

[0060] step 1, providing the GOA structure liquid crystal panel **50** and a level shift circuit for the GOA structure liquid crystal panel.

[0061] The level shift circuit for the GOA structure liquid crystal panel comprises: a sequence controller **10** and a level shift chip **20**. The sequence controller **10** and the level shift chip **20** are positioned on a circuit drive board PCBA. The level shift chip **20** comprises a time delay calculation register module **201**. The sequence controller **10** is communicatively coupled to the level shift chip **20** via a start signal line **30** and an Inter-Integrated Circuit bus **40**.

[0062] The Inter-Integrated Circuit bus **40**. comprises a serial data signal line employed for transmitting serial data signals SDA and a serial sequence signal line employed for transmitting serial sequence signals SCL.

[0063] step 2, performing initialization assignment T**1**-Tn to the time delay calculation register module **201** inside the level shift chip **20** via the Inter-Integrated Circuit bus **40** by the sequence controller **10**. n is a positive integer.

[0064] Specifically, in the step **2**, the initialization assignment T**1**-Tn of the time delay calculation register module **201** is determined according to the serial data signals SDA and the serial sequence signals SCL.

[0065] step 3, generating a start signal STV and sending the same to the level shift chip **20** via the start signal line **30** by the sequence controller **10**.

[0066] Specifically, with combination of FIG. **4**, FIG. **5**, all the low voltage levels of the start signal STV, the serial data signals SDA and the serial sequence signals SCL are 0 V, and the high voltage levels are 3.3 V.

[0067] step 4, triggering the level shift chip **20** to output at least four sets of sequence signals CKV**1**-CKVn on a basis of the start signal STV, of which the basis can be preferably to be the rising edge of the start signal STV according to the initialization assignment T**1**-Tn of the time delay calculation register module **201** and raising voltages of the start signal STV and the at least four sets of sequence signals CKV**1**-CKVn; respectively transmitting the start signal STV and each set of sequence signal after raising the voltages to the GOA structure liquid crystal panel **50** via one signal line.

[0068] Furthermore, in the step 4, a generation point of the each set of sequence signal CKVn and the rising edge of the start signal STV are spaced with a corresponding initialization assignment Tn. Continue periods Tn+1 and periodic times Tn+2 of high voltage levels of the at least four sets of sequence signals CKV**1**-CKVn are also determined according to the initialization assignment of the time delay calculation register module **201**.

[0069] Specifically, that the level shift chip **20** outputs four sets of sequence signals CKV**1**-CKV**4** is illustrated with combination of FIG. **4**, FIG. **6**. The level shift chip **20** correctly identifies the rising edge of the start signal STV, and outputs four sets of sequence signals CKV**1**-CKV**4** on a basis of the rising edge of the start signal STV, and raises voltages of the start signal STV and the four sets of sequence signals CKV**1**-CKV**4**. A generation point of the first set of sequence signal CKV**1** and the rising edge of the start signal STV are spaced with a corresponding period of the initialization assignment T**1**. A generation point of the second set of sequence signal CKV**2** and the rising edge of the start signal STV are spaced with a corresponding period of the initialization assignment T**2**. A generation point of the third set of sequence signal CKV**3** and the rising edge of the start signal STV are spaced with a corresponding period of the initialization assignment T**3**. A generation point of the fourth set of sequence signal CKV**4** and the rising edge of the start signal STV are spaced with a corresponding period of the initialization assignment T**4**. Besides, the continue periods T**5** and the periodic times T**6** of high voltage levels of the four sets of sequence signals CKV**1**-CKV**4** are also determined according to the initialization assignment of the time delay calculation register module **201**. For the liquid crystal panels of different resolutions, the continue periods T**5** and the periodic times T**6** of high voltage levels can be set according to different initialization assignments. After the level shift chip **20** raises the voltage levels, all the low voltage levels of the start signal STV, and the first, the second, the third, the fourth set of sequence signals CKV**1**, CKV**2**, CKV**3**, CKV**4** are −6 V, and the high voltage levels are 30 V, which can employed for driving the TFTs in the GOA structure liquid crystal panel **50** and realizing the scan line by line. In this embodiment, only four sets of sequence signals are illustrated for explanation. However, the present invention is not limited thereby and applicable for the condition of more sets of sequence signals. As more sequence signals are required for the GOA structure liquid crystal panel **50**, the present invention can decrease the lead count between the sequence controller **10** and the level shift chip **20** to reduce the package size of the sequence controller **10** and the level shift chip **20** and to decrease the total wiring amount between the sequence controller **10** and the level shift chip **20** for reducing the dimension of the circuit drive board PCBA. The result of lowering the production cost can be more effective.

[0070] In conclusion, in the level shift circuit and the level shift method for the GOA structure liquid crystal panel according to the present invention, the time delay calculation register module is provided inside the level shift chip. The start signal line and the Inter-Integrated Circuit bus are employed to communicatively couple the sequence controller and the level shift chip. the sequence controller performs initialization assignment to the time delay calculation register module inside the level shift chip via the Inter-Integrated Circuit bus, and sends a start signal to the level shift chip via the start signal line; the level shift chip is triggered to output at least four sets of sequence signals on a basis of the start signal according to the initialization assignment of the time delay calculation register module and raises voltages of the start signal and the at least four sets of sequence

signals to drive the GOA structure liquid crystal panel. It is capable of decreasing the lead count between the sequence controller and the level shift chip to reduce the package size of the sequence controller and the level shift chip and to decrease the total wiring amount between the sequence controller and the level shift chip for reducing the dimension of the circuit drive board PCBA, lowering the production cost and realizing the generation of more sequence signals with lower cost.

[0071] Above are only specific embodiments of the present invention, the scope of the present invention is not limited to this, and to any persons who are skilled in the art, change or replacement which is easily derived should be covered by the protected scope of the invention. Thus, the protected scope of the invention should go by the subject claims.

What is claimed is:

1. A level shift circuit for a GOA structure liquid crystal panel, comprising a sequence controller and a level shift chip;

the level shift chip comprises a time delay calculation register module;

the sequence controller is communicatively coupled to the level shift chip via a start signal line and an Inter-Integrated Circuit bus;

the sequence controller performs initialization assignment to the time delay calculation register module inside the level shift chip via the Inter-Integrated Circuit bus, and sends a start signal to the level shift chip via the start signal line;

the level shift chip is triggered to output at least four sets of sequence signals on a basis of the start signal according to the initialization assignment of the time delay calculation register module and raises voltages of the start signal and the at least four sets of sequence signals; the start signal and each set of sequence signal after raising the voltages are respectively transmitted to the GOA structure liquid crystal panel via one signal line.

2. The level shift circuit for the GOA structure liquid crystal panel according to claim **1**, wherein the Inter-Integrated Circuit bus comprises a serial data signal line employed for transmitting serial data signals and a serial sequence signal line employed for transmitting serial sequence signals.

3. The level shift circuit for the GOA structure liquid crystal panel according to claim **1**, wherein the level shift chip is triggered to output at least four sets of sequence signals on a basis of a rising edge of the start signal according to the initialization assignment of the time delay calculation register module.

4. The level shift circuit for the GOA structure liquid crystal panel according to claim **3**, wherein a generation point of the each set of sequence signal and the rising edge of the start signal are spaced with a corresponding initialization assignment.

5. The level shift circuit for the GOA structure liquid crystal panel according to claim **4**, wherein continue periods and periodic times of high voltage levels of the at least four sets of sequence signals are determined according to the initialization assignment of the time delay calculation register module.

6. A level shift circuit for a GOA structure liquid crystal panel, comprising a sequence controller and a level shift chip;

the level shift chip comprises a time delay calculation register module;

the sequence controller is communicatively coupled to the level shift chip via a start signal line and an Inter-Integrated Circuit bus;

the sequence controller performs initialization assignment to the time delay calculation register module inside the level shift chip via the Inter-Integrated Circuit bus, and sends a start signal to the level shift chip via the start signal line;

the level shift chip is triggered to output at least four sets of sequence signals on a basis of the start signal according to the initialization assignment of the time delay calculation register module and raises voltages of the start signal and the at least four sets of sequence signals; the start signal and each set of sequence signal after raising the voltages are respectively transmitted to the GOA structure liquid crystal panel via one signal line;

wherein the Inter-Integrated Circuit bus comprises a serial data signal line employed for transmitting serial data signals and a serial sequence signal line employed for transmitting serial sequence signals;

wherein the level shift chip is triggered to output the at least four sets of sequence signals on a basis of a rising edge of the start signal according to the initialization assignment of the time delay calculation register module.

7. The level shift circuit for the GOA structure liquid crystal panel according to claim **6**, wherein a generation point of the each set of sequence signal and the rising edge of the start signal are spaced with a corresponding initialization assignment.

8. The level shift circuit for the GOA structure liquid crystal panel according to claim **7**, wherein continue periods and periodic times of high voltage levels of the at least four sets of sequence signals are determined according to the initialization assignment of the time delay calculation register module.

9. A level shift method for a GOA structure liquid crystal panel, comprising steps of:

step 1, providing the GOA structure liquid crystal panel and a level shift circuit for the GOA structure liquid crystal panel;

the level shift circuit for the GOA structure liquid crystal panel comprises a sequence controller and a level shift chip; the level shift chip comprises a time delay calculation register module; the sequence controller is communicatively coupled to the level shift chip via a start signal line and an Inter-Integrated Circuit bus;

step 2, performing initialization assignment to the time delay calculation register module inside the level shift chip via the Inter-Integrated Circuit bus by the sequence controller;

step 3, generating a start signal and sending the same to the level shift chip via the start signal line by the sequence controller;

step 4, triggering the level shift chip to output at least four sets of sequence signals on a basis of the start signal according to the initialization assignment of the time delay calculation register module and raising voltages

of the start signal and the at least four sets of sequence signals; respectively transmitting the start signal and each set of sequence signal after raising the voltages to the GOA structure liquid crystal panel via one signal line.

10. The level shift method for the GOA structure liquid crystal panel according to claim **9**, wherein the Inter-Integrated Circuit bus comprises a serial data signal line employed for transmitting serial data signals and a serial sequence signal line employed for transmitting serial sequence signals.

11. The level shift method for the GOA structure liquid crystal panel according to claim **10**, wherein in the step 2, determining the initialization assignment of the time delay calculation register module according to the serial data signals and the serial sequence signals.

12. The level shift method for the GOA structure liquid crystal panel according to claim **9**, wherein in the step 4, the level shift chip is triggered to output the at least four sets of sequence signals on a basis of a rising edge of the start signal according to the initialization assignment of the time delay calculation register module; a generation point of the each set of sequence signal and the rising edge of the start signal are spaced with a corresponding initialization assignment.

13. The level shift method for the GOA structure liquid crystal panel according to claim **12**, wherein in the step 4, continue periods and periodic times of high voltage levels of the at least four sets of sequence signals are determined according to the initialization assignment of the time delay calculation register module.

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摘要(译)

本发明提供一种用于GOA结构液晶面板的电平移位电路和电平移位方法。电平转换芯片（ 20 ）包括一个时间延迟计算寄存器模块（ 201 ）和一个启动信号线（ 30 ）和一个Inter-集成电路总线（ 40 ）用于通信耦合序列控制器（ 10 ）和电平转换芯片（ 20 ）。序列控制器（ 10 ）对时间延迟计算寄存器模块（ 201 ）执行初始化分配（T 1 -Tn），并发送启动信号（ STV ）通过起始信号线（ 30 ）到电平移位芯片（ 20 ）;触发电平移位芯片（ 20 ）以基于起始信号（STV）输出至少四组序列信号（CKV -CKVn）。到时间延迟计算寄存器模块的初始化分配（T 1 -Tn），并且升高启动信号（STV）和至少四组序列信号（CKV 1）的电压 -CKVn）用于驱动GOA结构液晶面板（ 50 ）并实现更低成本的更多序列信号的产生。